에이디반도체 TSM12S

12-CH Auto Sensitivity Calibration Capacitive Touch Sensor

SPECIFICATION

VER. 1.2

Revision History

Rev.	Description of change	Date	Originator
1.0	First Creation	18.02.28	CH LEE
1.1	Typing Mistake Modification	18.06.07	CH LEE
1.2	Single/Multi. Register added	18.07.03	CH LEE

General

The TSM12S is 12-Channel capacitive sensor with auto sensitivity calibration. And the supply voltage range is from 1.8 to 5.0V.

The TSM12S has the SLEEP mode to save the consumption. And the current consumption is 8 uA.

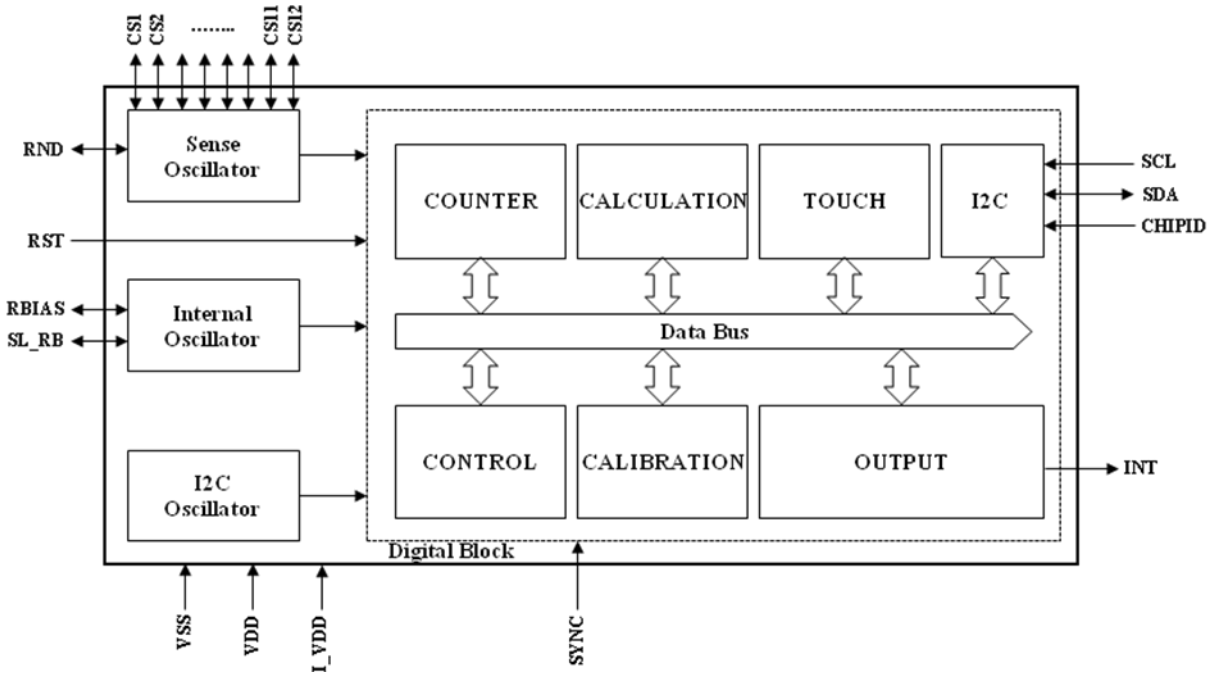
The TSM12S offers fast touch detection with fast response operation.

The result of touch sensing can be checked by the I^2C serial interface. And touch intensity can be detectable within 3 steps (Low, Middle and High).

Feature

■ 12-Channel capacitive sensor with auto sensitivity calibration
■ Selectable output operation (single mode / multi-mode)
■ Independently adjustable in 8 step sensitivity
■ Adjustable internal frequency with external resister
■ Adjustable response time and interrupt level by the control registers
■ I2C serial interface
■ Embedded high frequency noise elimination circuit
■ Typical current consumption xxx 45 uA (@3.0V)
■ Sleep mode current consumption 8 uA (@3.0V)
■ RoHS compliant 24QFN package

Block Diagram



Application

■ Mobile application (mobile phone / PDA / PMP etc)
■ Membrane switch replacement
■ Sealed control panels, keypads
■ Door key-lock matrix application
■ Touch screen replacement application

Ordering Information

Part No.	Package
TSM12S	24 QFN

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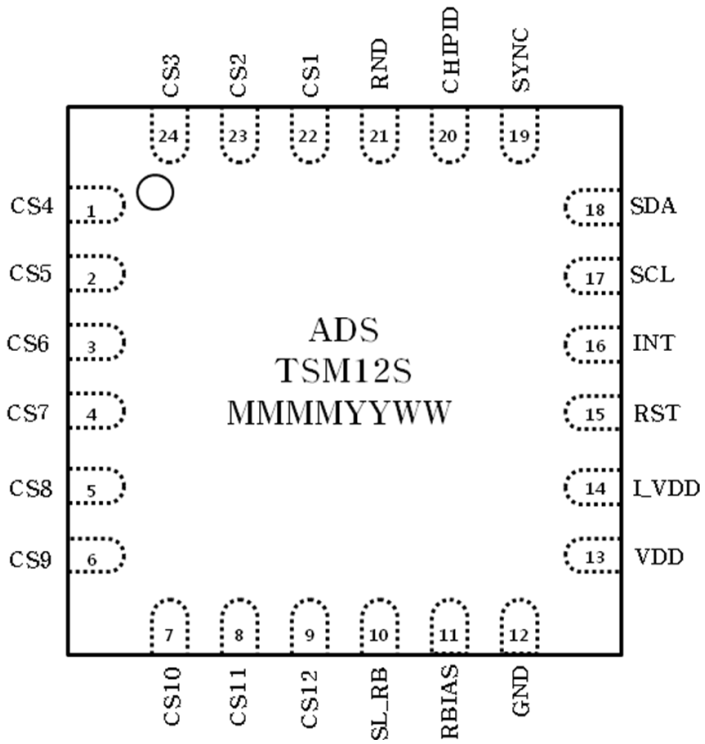
1 Pin Configuration



TSM12S (24 QFN)

2 Pin Description

VDD, VSS
Supply voltage and ground pin.

I_VDD
Supply voltage pin for IO pads.

RND
Reference channel capacitive sensor input pin.

CS1 ~ CS12
Capacitive sensor input pins.

SCL, SDA
SCL is I^2C clock input pin and SDA is I^2C data input-output pin.

INT
Touch sensing interrupt output pin.

RBIAS
Internal bias adjust input.

SL_RB
Internal bias adjust input for the SLEEP mode.

RST
System reset input.

CHIPID
I2C address selection input.

SYNC
The output mode selection input and sync pulse input/output for the sync operation.

2.1 Pin Map (24 QFN package)

Pin Number	Name	I/O	Description	Protection
PIN No.	**Name**	**I/O**	**Description**	**Protection**
1	CS4	Analog Input	CH4 capacitive sensor input	VDD/GND
2	CS5	Analog Input	CH5 capacitive sensor input	VDD/GND
3	CS6	Analog Input	CH6 capacitive sensor input	VDD/GND
4	CS7	Analog Input	CH7 capacitive sensor input	VDD/GND
5	CS8	Analog Input	CH8 capacitive sensor input	VDD/GND
6	CS9	Analog Input	CH9 capacitive sensor input	VDD/GND
7	CS10	Analog Input	CH10 capacitive sensor input	VDD/GND
8	CS11	Analog Input	CH11 capacitive sensor input	VDD/GND
9	CS12	Analog Input	CH12 capacitive sensor input	VDD/GND
10	SL_RB	Analog Input	SLEEP Mode Internal bias adjust input	VDD/GND
11	RBIAS	Analog Input	Internal bias adjust input	VDD/GND
12	GND	Ground	Supply ground	VDD
13	VDD	Power	Power (2.5V~5.0V)	GND
14	I_VDD	Power	IO PAD Power (2.5V~5.0V)	GND
15	RST	Digital Input	System reset (High reset)	VDD/GND
16	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
17	SCL	Digital Input	I2C clock input	VDD/GND
18	SDA	Digital Input/Output	I2C data (Open drain)	VDD/GND
19	SYNC	Digital Input/Output	Sync pulse input /output	VDD/GND
20	CHIPID	Digital Input	I2C address selection	VDD/GND
21	RND	Analog Input	Ref. Ch capacitive sensor input	VDD/GND
22	CS1	Analog Input	CH1 capacitive sensor input	VDD/GND
23	CS2	Analog Input	CH2 capacitive sensor input	VDD/GND
24	CS3	Analog Input	CH3 capacitive sensor input	VDD/GND

Note 1 : Refer to 6.3 SYNC implementation

3 Absolute Maximum Rating

Maximum supply voltage	5.5V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	-50 ~ 150℃
Operating Temperature	-40 ~ 85℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	8000V	VDD
		8000V	VSS
		8000V	P to P
M.M	Pos / Neg	400V	VDD
		400V	VSS
		400V	P to P
C.D.M	Pos / Neg	800V	DIRECT
		800V	

4.2 Latch-up Characteristics

Mode	Polarity	Max	Test Step
I Test	Positive	200mA	25mA
	Negative	-200mA	
V supply over 5.0V	Positive	8.25V	1.0V

5 Electrical Characteristics

▪ V_{DD}=3.3V, Rb=510k, Sync Mode (Rsync = 2MΩ) (Unless otherwise noted), T_A = 25℃

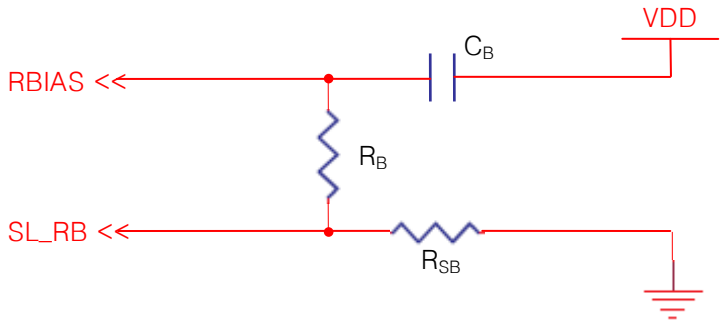
Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Power supply requirement and current consumption						
Operating supply voltage	V_{DD}		1.8	3.3	5.0	V
Current consumption	I_{DD}	V_{DD}= 3.3V R_B=510k R_SB=0	-	25	-	µA
		V_{DD}= 5.0V R_B=510k R_SB=0	-	46	-	
		V_{DD}= 3.3V R_B=510k R_SB=2M	-	8	-	
		V_{DD}= 5.0V R_B=510k R_SB=2M	-	18	-	
Touch sensing performance						
Minimum detective capacitance difference	ΔC	Cs = 10pF, C_{DEG} = 200pF (I2C default sensitivity select)	0.2	-	-	pF
Sense input capacitance range (**Note1**)	C_S		-	10	100	pF
Sense input resistance range	R_S		-	200	1000	Ω
Output impedance (open drain)	Zo	ΔC > 0.2pF, Cs = 10pF, (I2C default sensitivity select)	-	12	-	Ω
		ΔC < 0.2pF, Cs = 10pF, (I2C default sensitivity select)	-	30M	-	
		V_{DD} = 5.0V R_B = 510k	-	80	-	
System performance						
External reset high pulse width	V_{DD_RST}	T_A = 25℃	10	-	-	ms
Self calibration time after system reset	T_{CAL}	V_{DD} = 3.3V R_B = 510k	-	100	-	ms
		V_{DD} = 5.0V R_B = 510k	-	80	-	
Output maximum sink current	I_{OUT}	T_A = 25℃	-	-	4.0	mA
Recommended bias resistance range (**Note2**)	R_B	V_{DD} = 3.3V	200	510	820	kΩ
		V_{DD} = 5.0V	330	620	1200	
Maximum bias capacitance	C_{B_MAX}		-	820	1000	pF
Recommended sync resistance range	R_{SYNC}		1	2	20	MΩ
Max. I^2C SCL clock speed	f_{SCL_MAX}	Maximum internal I^2C clock	-	-	2	MHz

Note 1 : The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern.

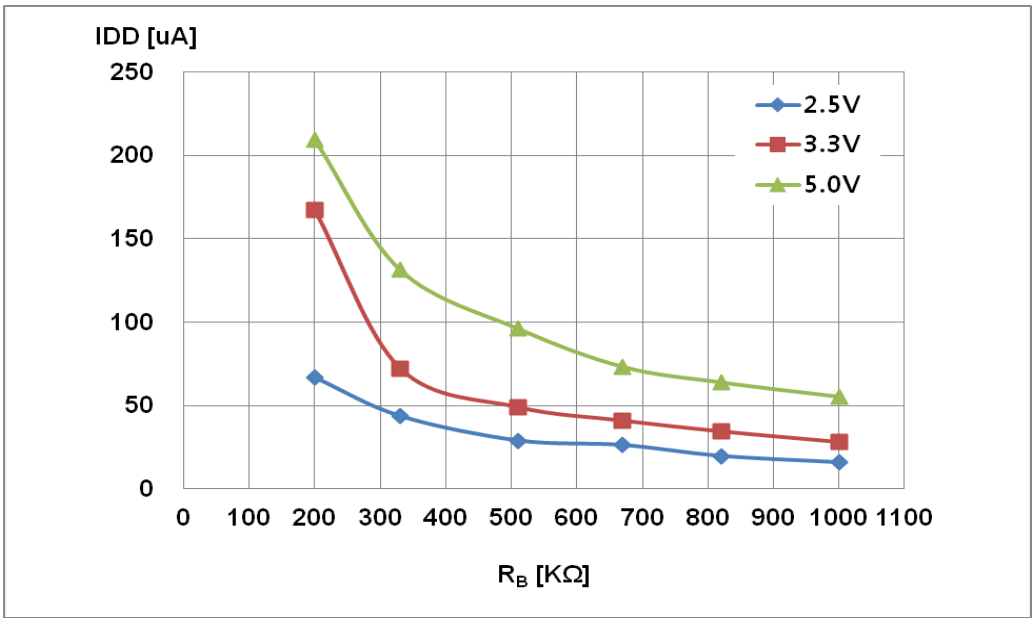
Note 2 : The lower R_B is recommended in noisy condition.

6 TSM12S Implementation

6.1 RBIAS & SL_RB implementation



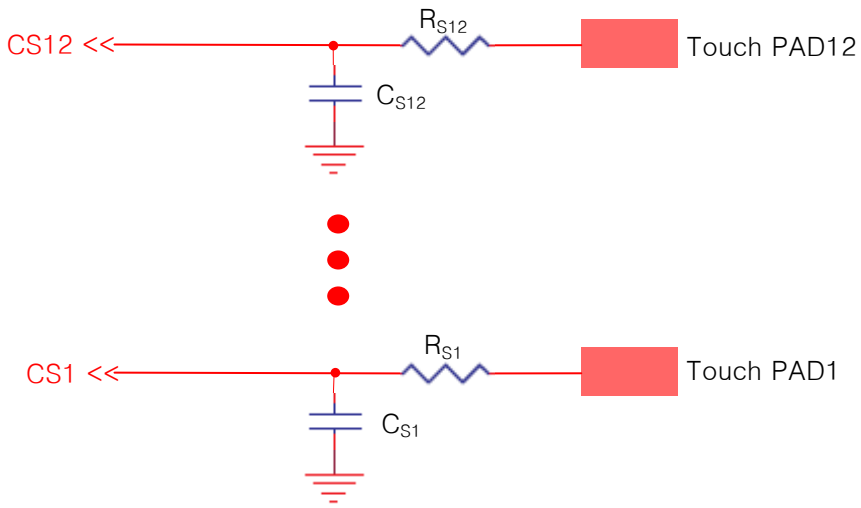
The RBIAS is connecting to the resistor to decide the oscillator and internal bias current. The sensing frequency, internal clock frequency and current consumption are therefore able to be adjusted with R_B. A voltage ripple on RBIAS can make critical internal error, so C_B is connected to the VDD (not GND) is recommended. (The typical value of C_B is 820pF and the maximum Value is 1nF.)
The R_{SB} should be connected as above figure when the TSM12S operates in SLEEP Mode to save the current consumption. In this case, the consumption depends on the sum of the serial resistors and the response time might be longer.



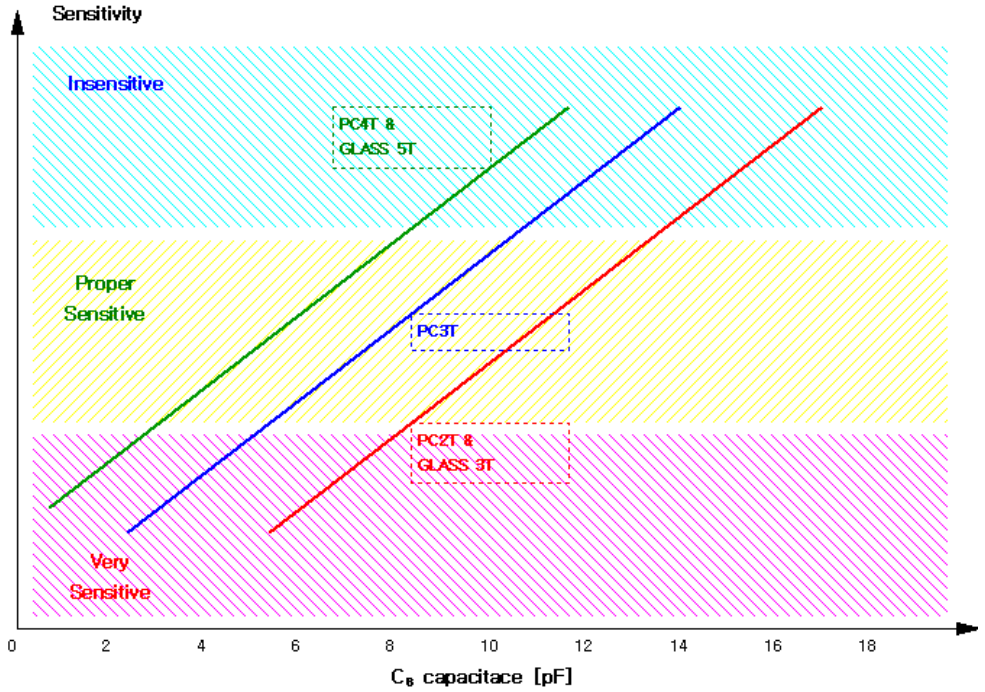
Normal operation current consumption curve

The current consumption curve of TSM12S is represented in accordance with R_B value as above. The lower R_B requires more current consumption but it is recommended in noisy application. For example, refrigerator, air conditioner and so on.

6.2 CS implementation



The TSM12S has basically eight steps sensitivity, which is available to control with internal register by I2C interface. The parallel capacitor C_{S1} is added to CS1 and C_{S12} to CS12 to adjust sensitivity. The sensitivity will be increased when smaller value of C_S is used. (Refer to the below Sensitivity Example Figure) It could be useful in case detail sensitivity mediation is required. The internal touch decision process of each channel is separated from each other. The twelve channel touch key board application can therefore be designed by using only one TSM12S without coupling problem. The R_S is serial connection resistor to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS1 ~ CS12 to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line. The unused CS pin must be connected with the ground to prevent the unpredictable mal-function that occurred in the floating CS pin.

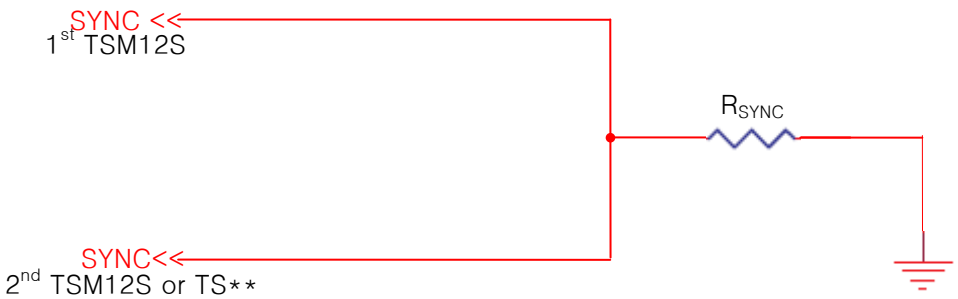


Sensitivity example figure with default sensitivity selection

6.3 SYNC implementation

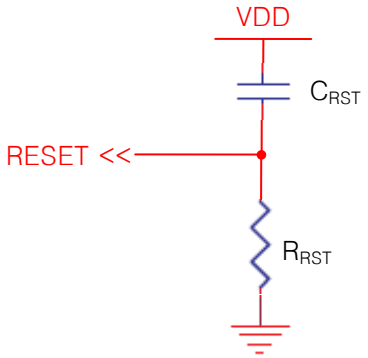
6.3.1 Multi Chip Application

Over two TSM12S can work on the one application at the same time thanks to SYNC function with this pin. The SYNC pulse prevents over two sensing signal from interfering with each other. R_{SYNC} is pull-down resistor of SYNC pin. Too big value of R_{SYNC} makes the SYNC pulse falling delay, and too small value of R_{SYNC} makes rising delay. Typical value of R_{SYNC} is 2MΩ.The Sync pin should be implemented as below. The TSM12S can also be used with the other TSxx series by employing this SYNC function. The TSM12S could only operate on multi output mode in this configuration.



6.4 RESET implementation

TSM12S has internal data latches, so initial state of these latches must be reset by external reset pulse before normal operation starts. The reset pulse can be controlled by host MCU directly or other reset device. If not, the circuit should be composed as below figure. The reset pulse must have high pulse duration about a few msec to cover power VDD rising time. The recommended value of R_{RST} and C_{RST} are 330KΩ and 100nF.

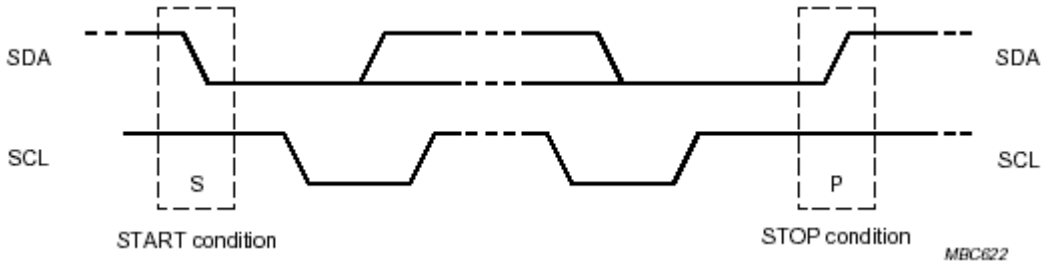


Recommended reset circuits 1

7 I²C Interface

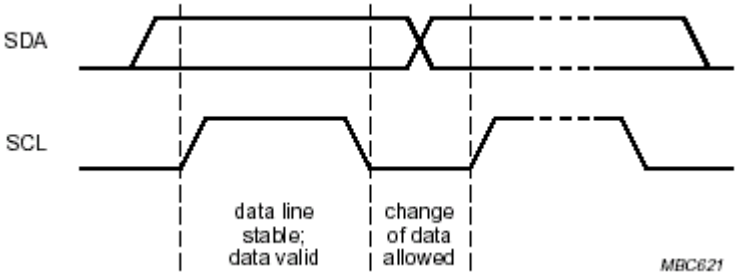
7.1 Start & Stop Condition

- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)



7.2 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

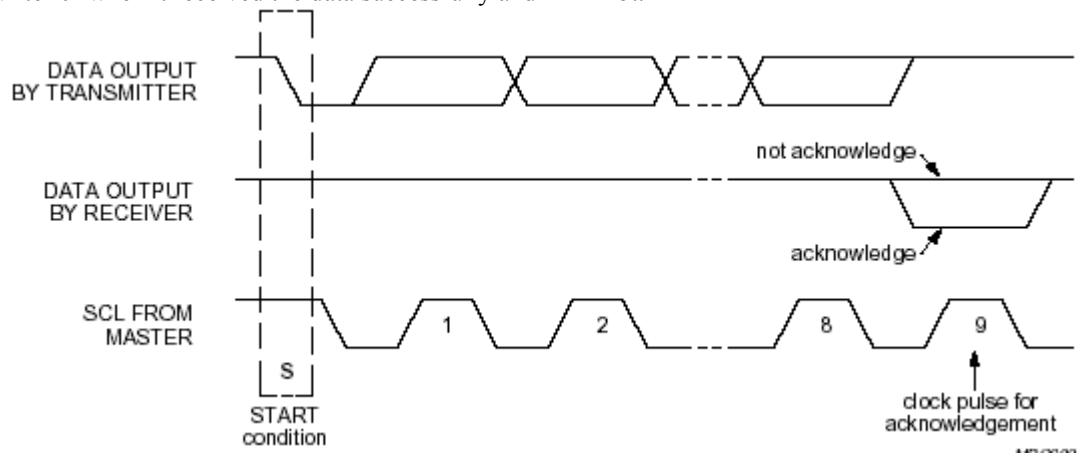


7.3 Byte Format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.4 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write '0' when it received the data successfully and '1' if not.



7.5 First Byte

7.5.1 Slave Address

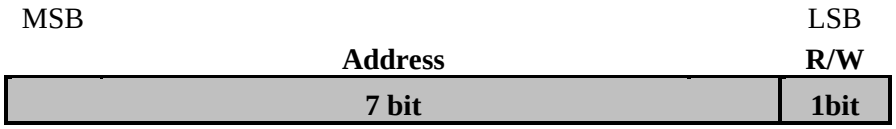
It is the first byte from the start condition. It is used to access the slave device.

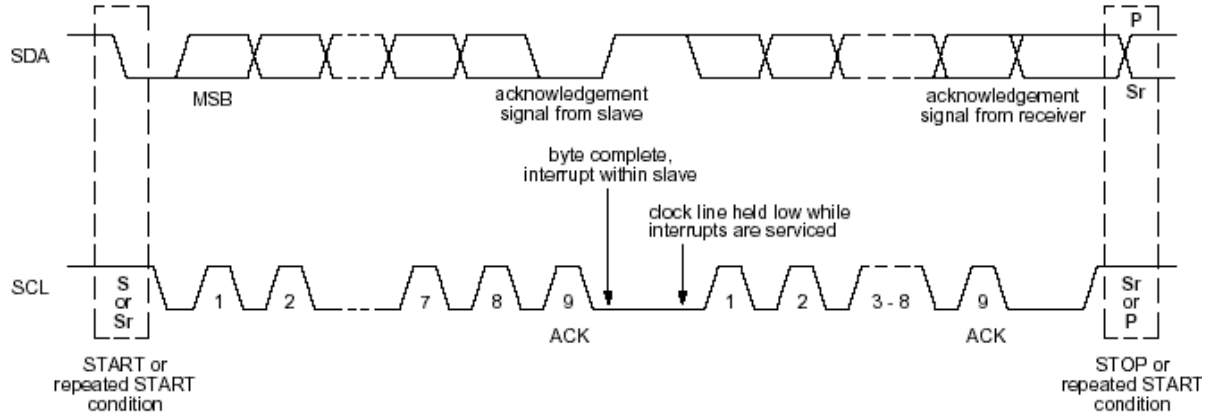
TSM12S Chip Address : 7bit

CHIPID	Address
GND	0xD0
VDD	0xF0

7.5.2 R/W

The direction of data is decided by the bit and it follows the address data.



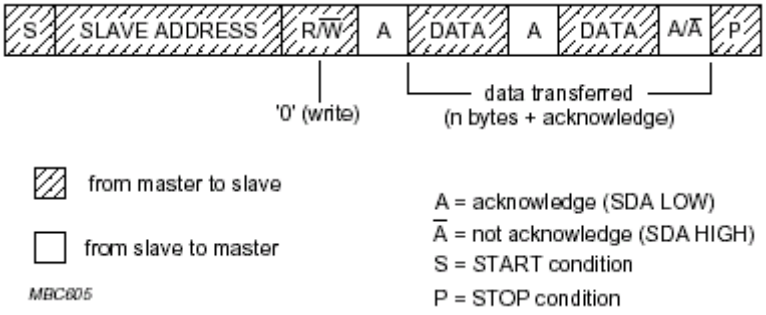


7.6 Transferring Data

7.6.1 Write Operation

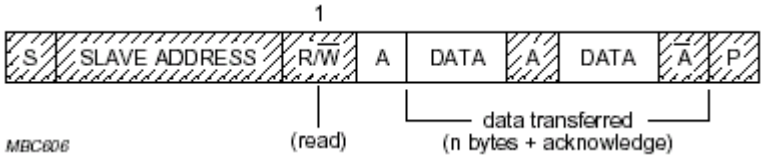
The byte sequence is as follows:

■ the first byte gives the device address plus the direction bit (R/W = 0).
■ the second byte contains the internal address of the first register to be accessed.
■ the next byte is written in the internal register. Following bytes are written in successive internal registers.
■ the transfer lasts until stop conditions are encountered.
■ the TSM12S acknowledges every byte transfer.

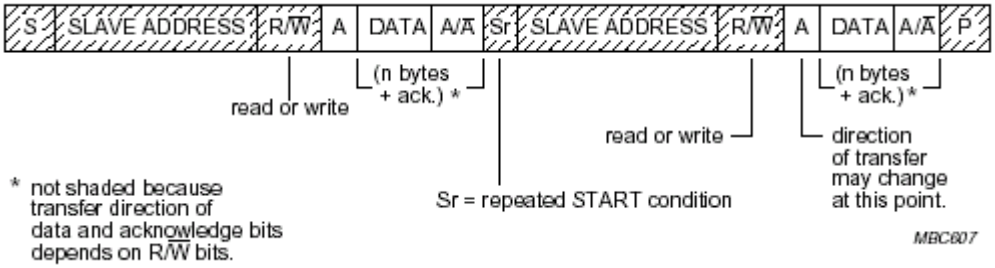


7.6.2 Read Operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.6.3 Read/Write Operation



7.7 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0xD0	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

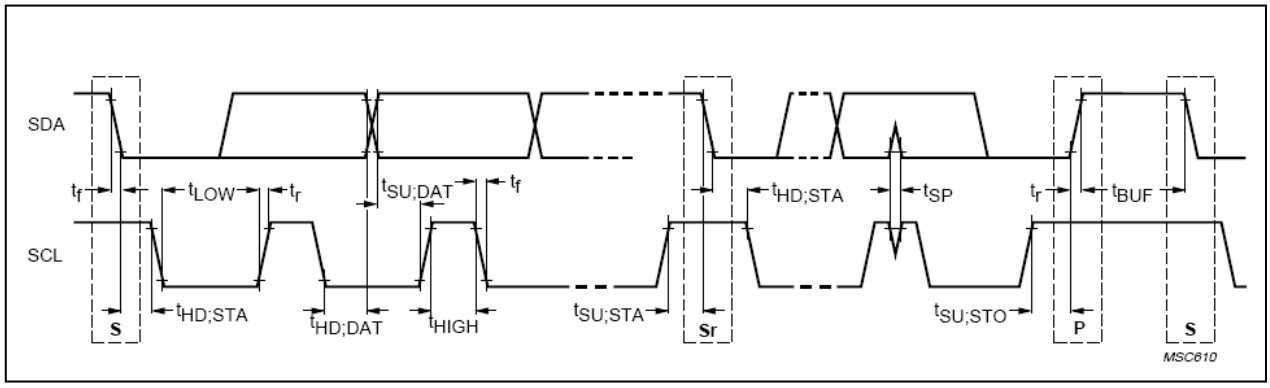
Read register 0x00 and 0x01

Start	Device Address 0xD0	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0xD1	ACK	Data Read AA	ACK	Data Read BB	$\overline{\text{ACK}}$	Stop

From Master to Slave From Slave to Master

7.8 I²C timing diagram



PARAMETER	SYMBOL	100kbps		400kbps		UNIT
		MIN.	MAX.	MIN.	MAX.	
Hold time (repeated)START condition.	tHD;STA	4.0	-	0.6	-	us
LOW period of the SCL clock	tLOW	4.7	-	1.3	-	us
HIGH period of the SCL clock	tHIGH	4.0	-	0.6	-	us
Set-up time for a repeated START condition	tSU;STA	4.7	-	0.6	-	us
Data hold time	tHD;DAT	1.0	-	-	-	us
Data set-up time	tSU;DAT	250	-	100	-	ns
Rise time of both SDA and SCL signals	tr	-	1000	20	300	ns
Fall time of both SDA and SCL signals	tf	-	300	20	300	ns
Set-up time for STOP condition	tSU;STO	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	tBUF	4.7	-	1.3	-	us
Noise margin at the LOW level for each connected device	VnL	0.1VDD	-	0.1VDD	-	V
Noise margin at the HIGH level for each connected device	VnH	0.2VDD	-	0.2VDD	-	V
Input Low level				0	V_{DD}*0.2	V
Input High level				V_{DD}*0.8	V_{DD}	V

8 TSM12S control register

- Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.
- Note: The bit0 and bit1 of CTRL2 register must be written by 0b11 after power on during an initialize phase. (Refer to the chapter 9. initialize flow)
- Note: HS (High Sensitivity) / MS (Middle Sensitivity) / LS (Low Sensitivity)
- Note: Low Output (light touch) / Middle Output (middle touch) / High Output (hard touch)

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sensitivity1	02h	1011 1011	Ch2HL	Ch2M			Ch1HL	Ch1M		
Sensitivity2	03h	1011 1011	Ch4HL	Ch4M			Ch3HL	Ch3M		
Sensitivity3	06h	1011 1011	Ch6HL	Ch6M			Ch5HL	Ch5M		
Sensitivity4	07h	1011 1011	Ch8HL	Ch8M			Ch7HL	Ch7M		
Sensitivity5	22h	1011 1011	Ch10HL	Ch10M			Ch9HL	Ch9M		
Sensitivity6	23h	1011 1011	Ch12HL	Ch12M			Ch11HL	Ch11M		
CTRL1	08h	0010 0010	MS	FTC		ILC		RTC		
CTRL2	09h	0000 0001	0	0	MULTI	IMP_SEL	SRST	SLEEP	Bits	
Ref_rst1	0Ah	1111 1110	1	1	1	1	Ch4	Ch3	Ch2	Ch1
Ref_rst2	0Bh	1111 1111	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5
Ch_hold1	0Ch	1111 1110	1	1	1	1	Ch4	Ch3	Ch2	Ch1
Ch_hold2	0Dh	1111 1111	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5
Cal_hold1	0Eh	0000 0000	0	0	0	0	Ch4	Ch3	Ch2	Ch1
Cal_hold2	0Fh	0000 0000	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5
Output1	10h	0000 0000	OUT4		OUT3		OUT2		OUT1	
Output2	12h	0000 0000	OUT8		OUT 7		OUT6		OUT5	
Output3	13h	0000 0000	OUT12		OUT11		OUT10		OUT9	
Lock_mask	3Bh	0000 0000	LOCK_MASK							
Force_en	41h	0001 0100	FEN	0	0	1	0	1	0	0

8.2 Details

8.2.1 Sensitivity Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	**Sensitivity1**	Ch2HL	Ch2M			Ch1HL	Ch1M		
03h	**Sensitivity2**	Ch4HL	Ch4M			Ch3HL	Ch3M		
06h	**Sensitivity3**	Ch6HL	Ch6M			Ch5HL	Ch5M		
07h	**Sensitivity4**	Ch8HL	Ch8M			Ch7HL	Ch7M		
22h	**Sensitivity5**	Ch10HL	Ch10M			Ch9HL	Ch9M		
23h	**Sensitivity6**	Ch12HL	Ch12M			Ch11HL	Ch11M		

Description

The sensitivity of channel 1 and 2 are adjustable by Sensitivity_1 register. ChxM[2:0] allows various middle sensitivity and also the high and low sensitivities are decided with ChxHL.

Bit name	Reset	Function	
ChxM[2:0]	011	Middle sensitivity T (= thickness of PC) @Cs = 0pF 000 : 0.50% 001 : 0.70% 010 : 0.90% 011 : 1.20% 100 : 1.50% 101 : 2.05% 110 : 2.55% 111 : 3.55%	
ChxHL	1	High and Low sensitivity selection for channel x	
		0	1
		Low Sensitivity 000 : 0.40% 001 : 0.55% 010 : 0.70 % 011 : 0.95% 100 : 1.20% 101 : 1.60% 110 : 2.05% 111 : 2.85%	High Sensitivity 000 : 0.6% 001 : 0.85% 010 : 1.10% 011 : 1.45% 100 : 1.85% 101 : 2.45% 110 : 3.05% 111 : 4.30%

8.2.2 General Control Register1

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
08h	CTRL1	MS	FTC[1:0]		ILC[1:0]		RTC[2:0]		

Description

The calibration speed just after power on reset is very high during the time which is defined by FTC[1:0] to have a good adoption against unstable external environment.

Bit name	Reset value	Function
MS	0	Mode Selection 0: auto alternate (fast/slow) mode 1: fast mode
FTC[1:0]	01	First Touch Control 00 : 19 * 16[1] * 1-Period (ms) 01 : 37 * 16 * 1-Period (ms) 10 : 56 * 16 * 1-Period (ms) 11 : 74 * 16 * 1-Period (ms)
ILC[1:0]	00	Interrupt Level Control 00: Interrupt is on middle or high output. 01: Interrupt is on low or middle or high output. 10: Interrupt is on middle or high output. 11: Interrupt is on high output.
RTC[2:0]	011	Response Time Control Response period = RTC[2:0] + 2

8.2.3 General Control Register2

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
09h	CTRL2	0	0	MULTI	IMP_SEL	SRST	SLEEP	0	1

Description

Single/Multi output mode is selected according to MULTI bit. For impedance, IMP_SEL bit is used. All the digital blocks except analog and I2C block are reset when SRST is set. The SLEEP function allows getting very low current consumption when it is set. But the response time will be longer than normal operation. The bit0 and bit1 must be written with 0b'11 by host MCU.

Bit name	Reset	Function
MULTI	0	Single/Multiple Output Select 0: Multiple Output 1: Single Output
IMP_SEL	0	Impedance Select 0: High Impedance 1: Low Impedance
SRST	0	Software Reset 0: Disable Software Reset 1: Enable Software Reset
SLEEP	0	Sleep Mode Enable 0: Disable Sleep Mode

[1] The number, 16 is the time control constant value

		1: Enable Sleep Mode
Bit[1:0]	01	These bits must be written by 2b'11 during a system initialize phase. (refer to the chapter 9 "initialize flow example")

8.2.4 Channel Reference Reset Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	**Ref_rst1**	1	1	1	1	Ch4	Ch3	Ch2	Ch1
0Bh	**Ref_rst2**	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5

Description

The reference value of each channel will be renewing when Chx is set.

Bit name	Reset	Function
Chx	1	0: Disable reference reset 1: Enable reference reset
Ch1	0	0: Disable reference reset 1: Enable reference reset

8.2.5 Channel Sensing Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	**Ch_hold1**	1	1	1	1	Ch4	Ch3	Ch2	Ch1
0D	**Ch_hold2**	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5

Description

The operation of each channel is independently available to control. A channel doesn't be worked and the calibration is paused when it is set.

Bit name	Reset	Function
Chx	1	0: Enable operation (sensing + calibration) 1: Hold operation (No sensing + Stop calibration)
Ch1	0	0: Enable operation (sensing + calibration) 1: Hold operation (No sensing + Stop calibration)

8.2.6 Channel Calibration Control Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	**Cal_hold1**	0	0	0	0	Ch4	Ch3	Ch2	Ch1
0Fh	**Cal_hold2**	Ch12	Ch11	Ch10	Ch9	Ch8	Ch7	Ch6	Ch5

Description

The calibration of each channel is independently available to control. Each channel is working even if a bit is set.

Bit name	Reset	Function
Chx	0	0: Enable reference calibration (sensing + calibration) 1: Disable reference calibration (sensing + No calibration)

8.2.7 Output Register

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	**output1**	OUT4[1:0]		OUT3[1:0]		OUT2[1:0]		OUT1[1:0]	
12h	**output2**	OUT8[1:0]		OUT7[1:0]		OUT6[1:0]		OUT5[1:0]	
13h	**output3**	OUT12[1:0]		OUT11[1:0]		OUT10[1:0]		OUT9[1:0]	

Description

The each channel output of TSM12S is compressed with 2 bits. It has 3 level output information that is low, middle and high.

Bit name	Reset value	Function
OUT1[1:0] ~ OUT12[1:0]	00	Output of channels 00: No output 01: low output 10: middle output 11: high output

8.2.8 Lock Mask Register

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Bh	**Lock_mask**	LOCK_MASK							

Description

Lock mask bits prevent the specific bits in TSM12S from changing in noise environments.

Bit name	Reset value	Function
LOCK_MASK	0000 0000	For applying MULTI bit(0x09[5]), Lock mask bits should be 8'h10100101

8.2.9 Touch Mode Register

Type: R/W

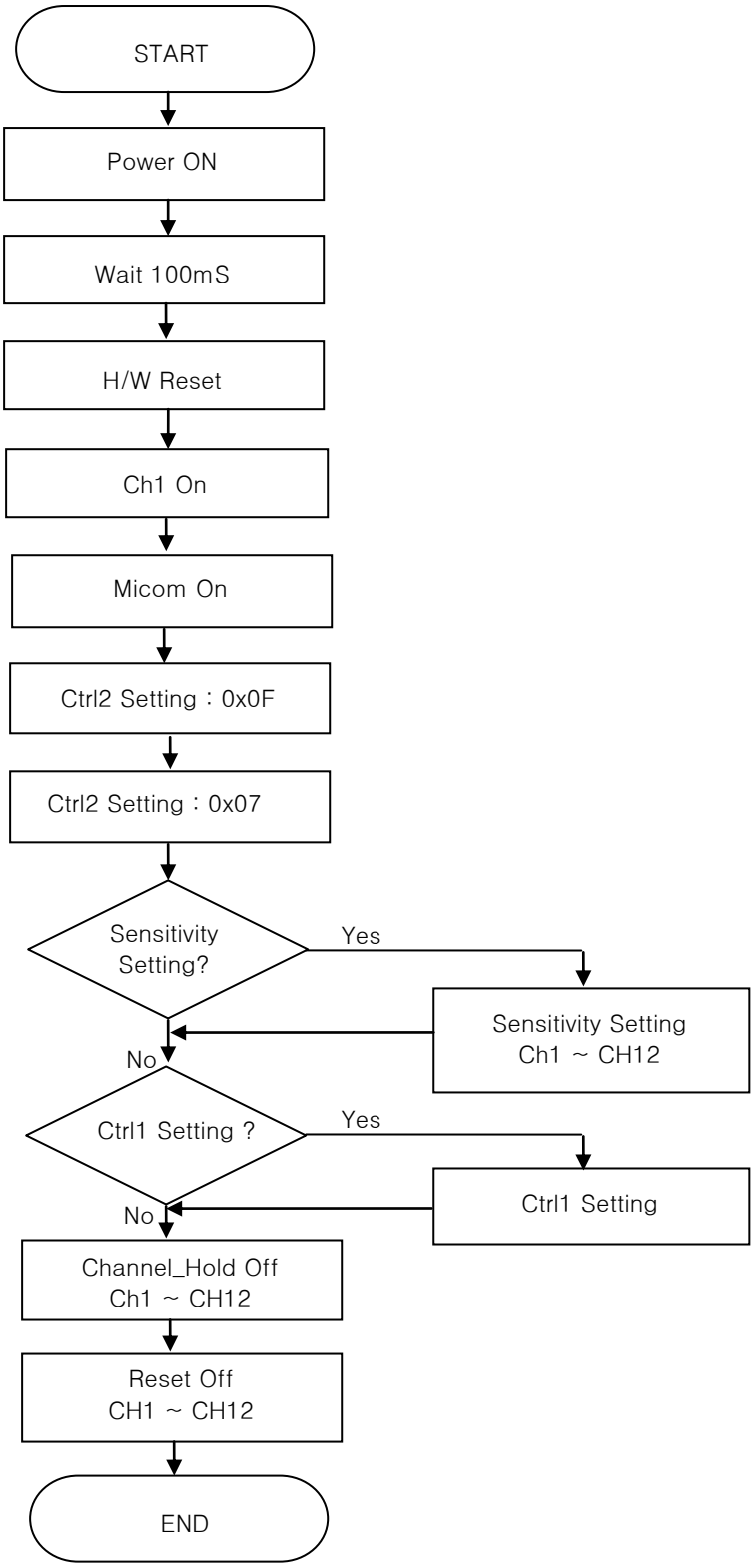
Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
41h	**Force_en**	FEN	0	0	1	0	1	0	0

Description

FEN bit selects the single and multi touch detection mode.

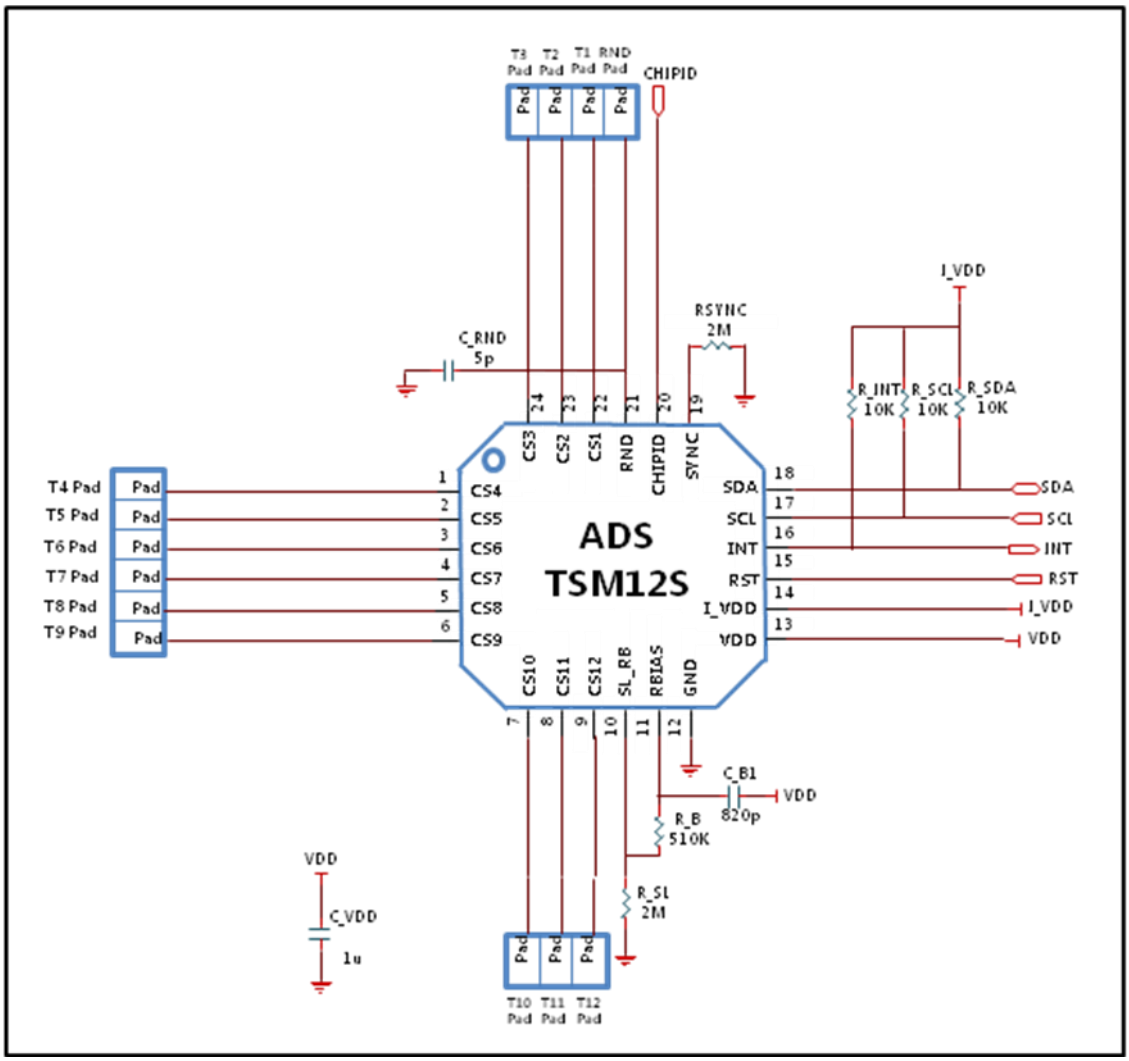
Bit name	Reset value	Function
FEN	0001 0100	For applying MULTI bit(0x09[5]), Lock mask bits should be 8'h10100101 and FEN bit should be 1'b1

9 Recommended TSM12S Initialize Flow (Example)



10 Recommended Circuit Diagram

10.1 Application Example in clean power environment



TSM12S Application Example Circuit (Clean power environment)

- ✓ In PCB layout, R_B should not be placed on touch pattern. If not, C_B has to be connected. The R_B pattern should be routed as short as possible.
- ✓ The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm.
- ✓ The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TSM12S.
- ✓ The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- ✓ The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- ✓ The TSM12S is reset if RST Pin is high. (See 6.5 Reset implementation chapter)
- ✓ The TSM12S is working with single output mode if the SYNC/OPT pin is high and it will be in multi output mode when it's low. The resistor which is connected with GND should be connected with SYNC pin when the application is required over two TSM12S devices (Multi output mode).

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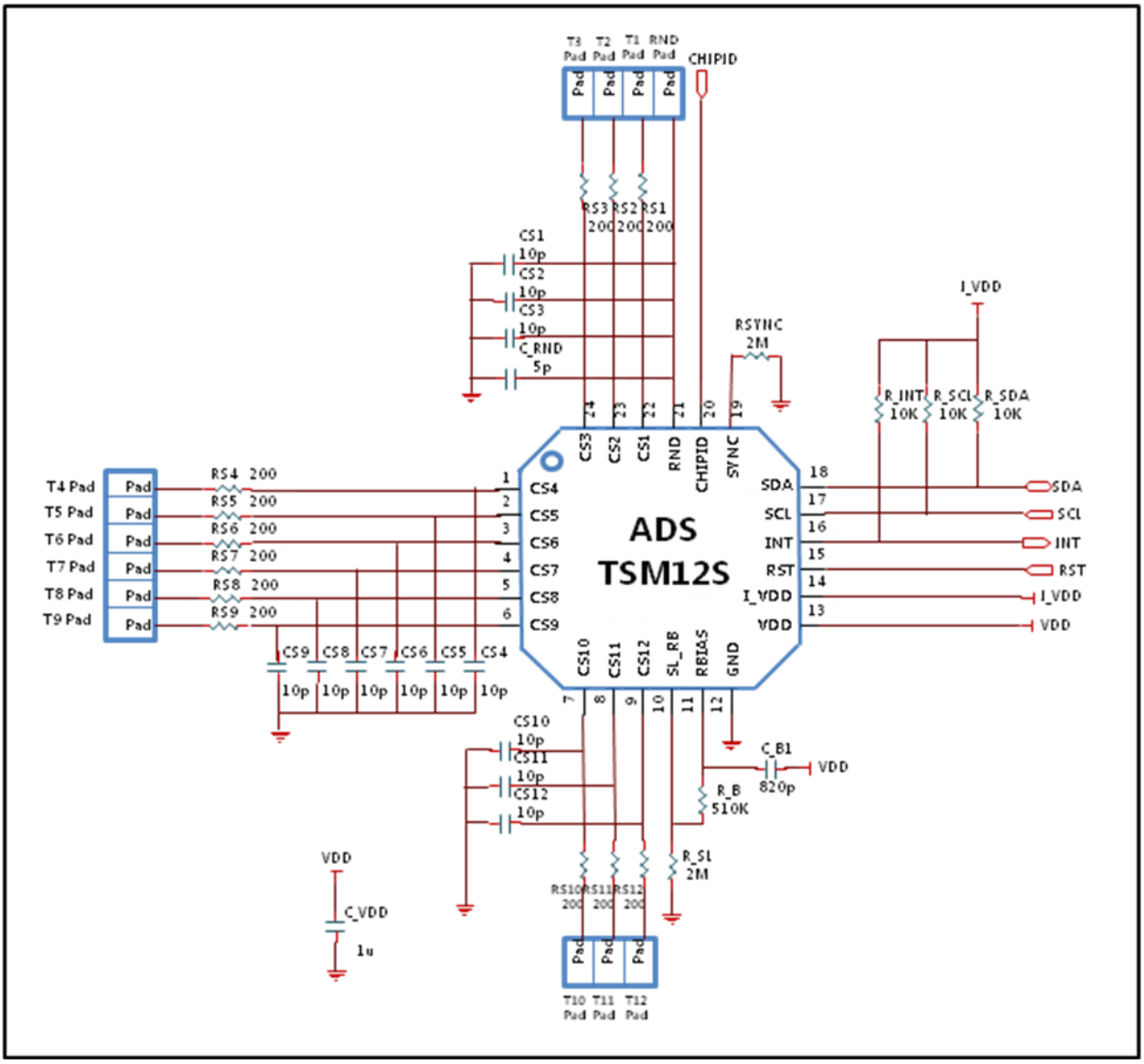
10.2 Application Example in noisy environment

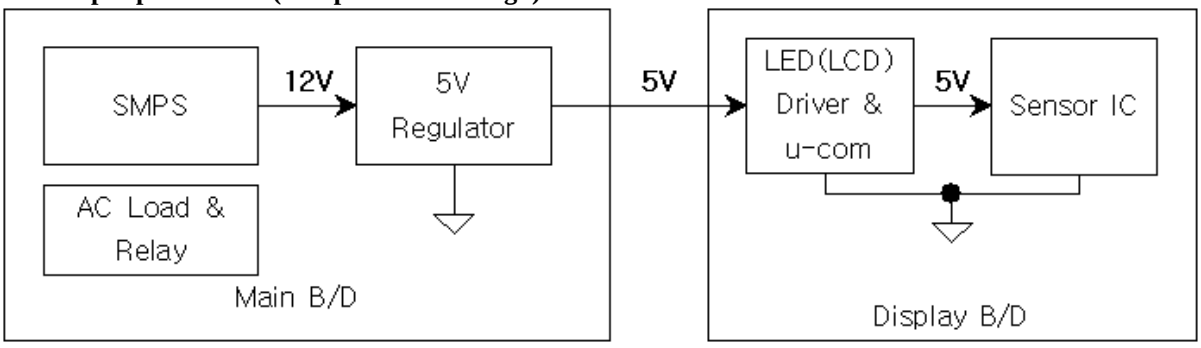


TSM12S Application Example Circuit (Noisy environment)

- ✓ The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- ✓ The smaller R_B is recommended in noisy environments.
- ✓

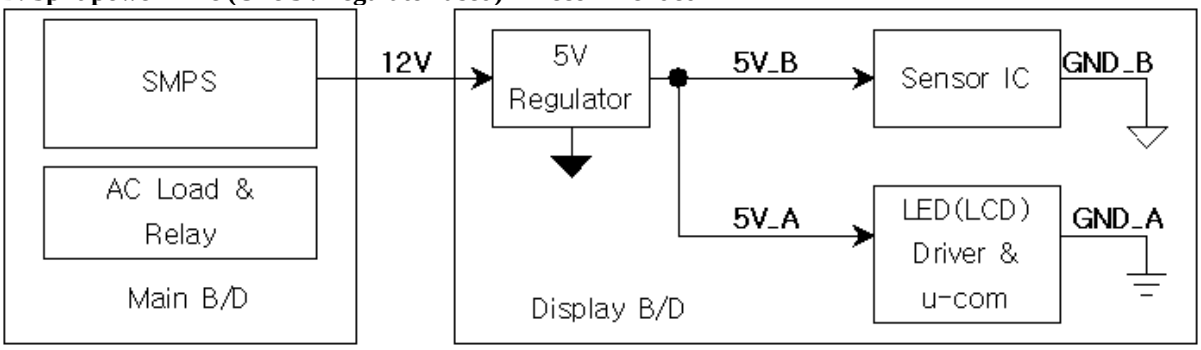
10.3 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

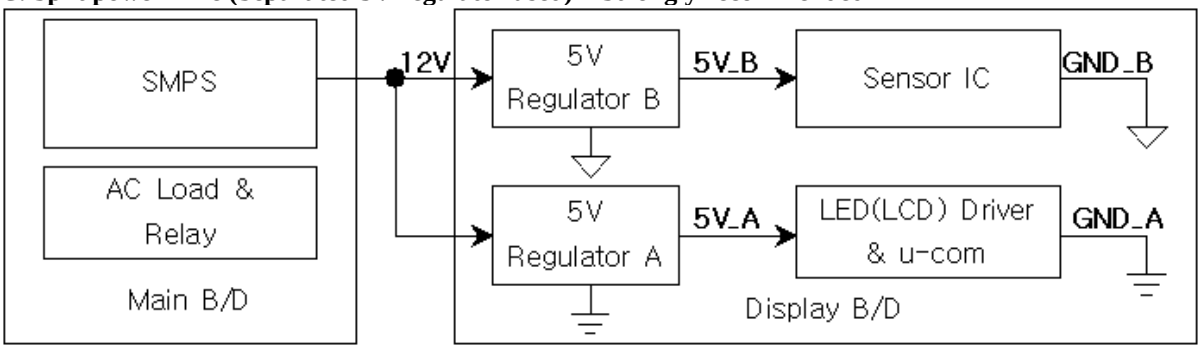


- ✓ The noise that is generated by AC load or relay can be loaded at 5V power line.
- ✓ A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power Line (One 5V regulator used) – Recommended

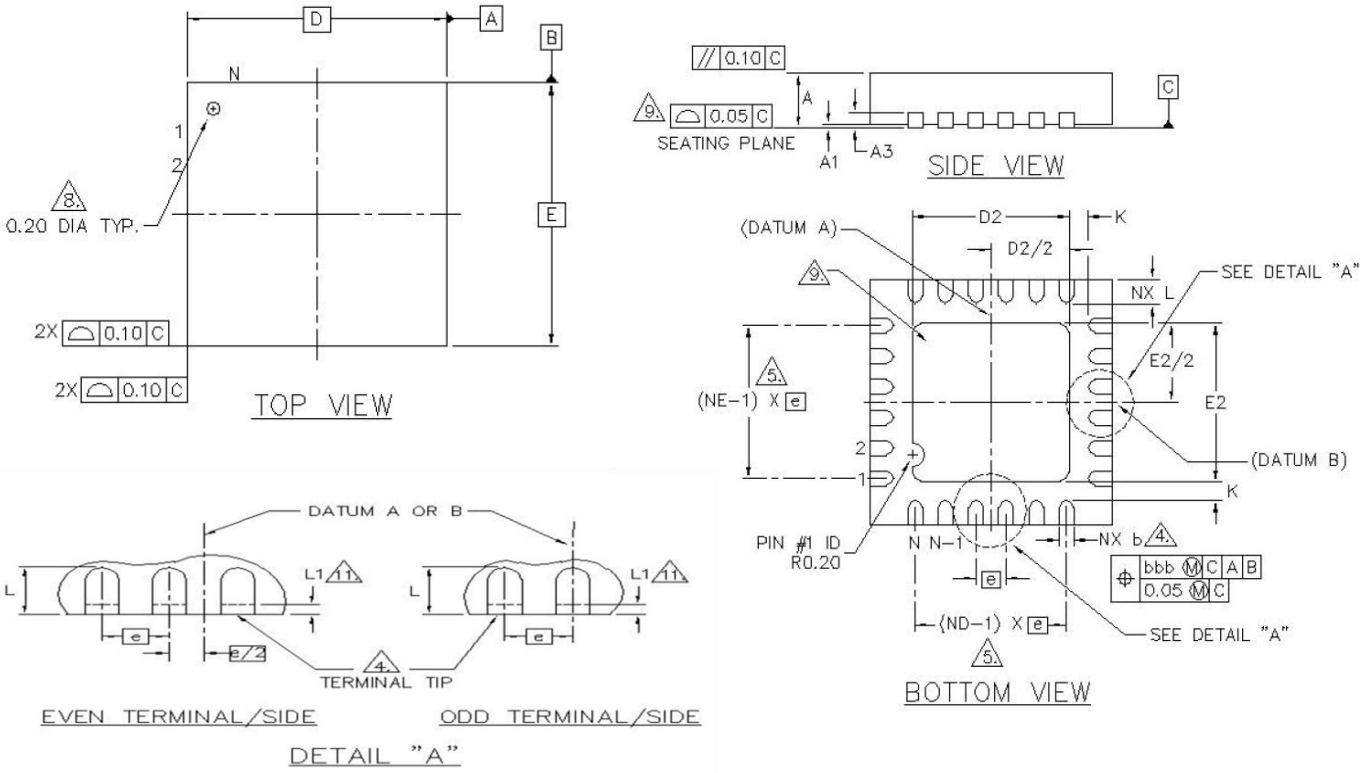


C. Split power Line (Separated 5V regulator used) – Strongly recommended



11 MECHANICAL DRAWING

11.1 AMKOR Mechanical Drawing of TSM12S (24 QFN)



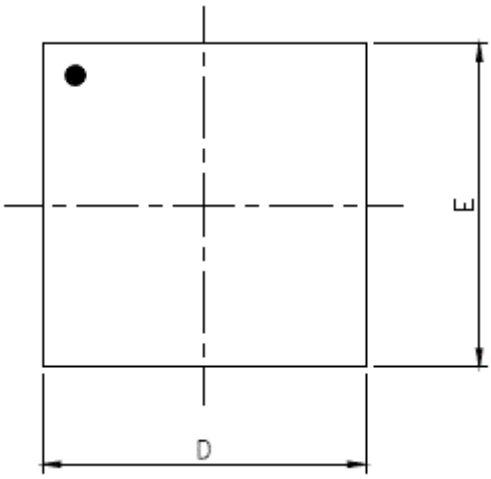
SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	0.80	0.85	0.90	
A1	0.00	0.02	0.05	
A3		0.20 REF.		
θ	0	—	12	2
K		0.20 MIN.		
D		4.0 BSC		
E		4.0 BSC		
L1		0.15 mm MAX		11

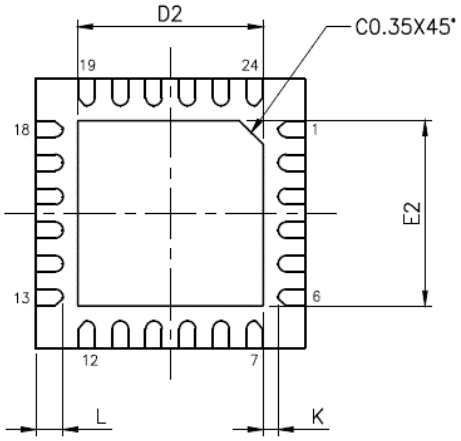
NOTES :

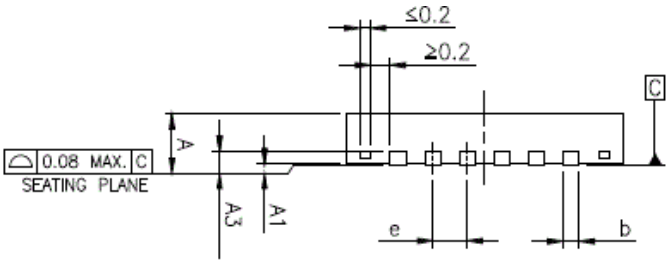
1. DIMENSIONING AND TOLERANCING CONFORME TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS, θ IS IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
5. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
6. MAX. PACKAGE WARPAGE IS 0.05 mm.
7. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
8. PIN #1 ID ON TOP WILL BE LASER MARKED.
9. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
10. THIS DRAWING CONFORMES TO JEDEC REGISTERED OUTLINE MO-220
11. DEPENDING ON THE METHOD OF LEAD TERMINATION AT THE EDGE OF THE PACKAGE, PULLBACK (L1) MAYBE PRESENT
12. PULLBACK DESIGN OPTION IS FOR 0.50mm NOMINAL LANDLENGTH ONLY.

SYMBOL	0.50mm LEAD PITCH																		NOTE
	VARIATION A			VARIATION B *			VARIATION C *			VARIATION D *			VARIATION E			VARIATION F			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
e	0.50 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			0.50 BSC.			
N	20			20			20			20			24			24			3
ND	5			5			5			5			6			6			12
NE	5			5			5			5			6			6			12
L	0.35	0.40	0.45	0.45	0.50	0.55	0.45	0.50	0.55	0.55	0.60	0.65	0.35	0.40	0.45	0.35	0.40	0.45	11
b	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	0.18	0.25	0.30	4
D2	2.50	2.60	2.70	2.30	2.40	2.50	2.00	2.10	2.30	2.00	2.10	2.30	2.50	2.60	2.70	2.40	2.50	2.60	
E2	2.50	2.60	2.70	2.30	2.40	2.50	2.00	2.10	2.30	2.00	2.10	2.30	2.50	2.60	2.70	2.40	2.50	2.60	

11.2 GREATEK Mechanical Drawing of TSM12S (24 QFN)







PAD SIZE : 110X11* MIL / 112X11* MIL
PAD SIZE : 113X11* MIL / 114X11* MIL
PAD SIZE : 115X11* MIL / B114X11* MIL

	PACKAGE TYPE					
JEDEC OUTLINE	MO-220			MO-220		
PKG CODE	WQFN(X424)			VQFN(Y424)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
D	4.00 BSC			4.00 BSC		
E	4.00 BSC			4.00 BSC		
e	0.50 BSC			0.50 BSC		
K	0.20	—	—	0.20	—	—

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

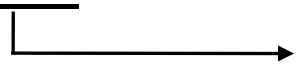
PAD SIZE	b			D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
110X11* MIL	0.18	0.25	0.30	1.95	2.00	2.05	1.95	2.00	2.05	0.30	0.40	0.50	V	V	W(V)GGD-2
112X11* MIL	0.18	0.25	0.30	2.20	2.25	2.30	2.20	2.25	2.30	0.35	0.40	0.45	V	X	W(V)GGD-8
113X11* MIL	0.18	0.25	0.30	2.55	2.60	2.65	2.55	2.60	2.65	0.35	0.40	0.45	X	V	W(V)GGD-6
114X11* MIL	0.18	0.25	0.30	2.65	2.70	2.75	2.65	2.70	2.75	0.35	0.40	0.45	V	X	W(V)GGD-6
115X11* MIL	0.18	0.25	0.30	2.45	2.50	2.55	2.45	2.50	2.55	0.35	0.40	0.45	V	X	W(V)GGD-8
120X12* MIL	0.18	0.25	0.30	2.55	2.60	2.65	2.55	2.60	2.65	0.275	0.325	0.375	V	X	W(V)GGD-8
A114X114 MIL	0.18	0.25	0.30	2.65	2.70	2.75	2.65	2.70	2.75	0.35	0.40	0.45	V	X	W(V)GGD-6
B114X11* MIL	0.18	0.25	0.30	2.65	2.70	2.75	2.65	2.70	2.75	0.35	0.40	0.45	V	X	W(V)GGD-6
⚠4 C114X11* MIL	0.19	0.24	0.29	2.40	2.45	2.50	2.40	2.45	2.50	0.35	0.40	0.45	V	X	W(V)GGD-8

＊PAD SIZE：113X113、120X120為某家客戶之CLOSE TOOL.
"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

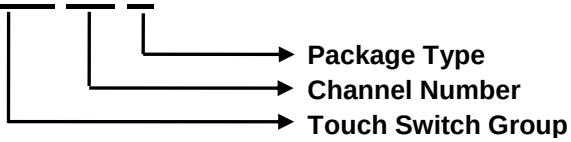
12 MARKING DESCRIPTION

12.1 Marking Description of TSM12S (24 QFN)

Company Code : **ADS**



Device Code : **TSM 12 S**



Year / Week Code : **MMMM AA WW**

Year Code	BH	BK	BM	CA	CB	CC	CD	CE	CF	CG
Production Year	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026

NOTES:

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