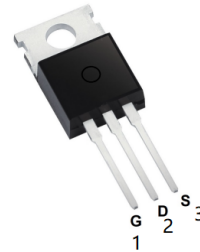


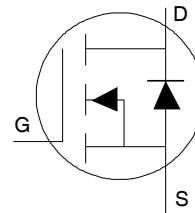
Applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters



Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free
- $V_{DS}(V) = 40V$
- $I_D = 100A$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 2.5m\Omega$ ($V_{GS} = 10V$)



Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	172 ^①	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	122 ^①	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Wire Bond Limited)	120	
I_{DM}	Pulsed Drain Current ^②	772	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	143	W
	Linear Derating Factor	0.95	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)		
	Mounting torque, 6-32 or M3 screw	10lbf·in (1.1N·m)	
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^③	161	mJ
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ^④	387	
I_{AR}	Avalanche Current ^⑤	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ^⑥		mJ
$R_{\theta JC}$	Junction-to-Case ^⑦	1.05	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	
$R_{\theta JA}$	Junction-to-Ambient	62	

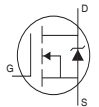
Static @ T = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.035		V/°C	Reference to 25°C, $I_D = 5.0mA$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance		2.0	2.5	mΩ	$V_{GS} = 10V, I_D = 100A$ ③
			3.0		mΩ	$V_{GS} = 6.0V, I_D = 50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
I_{DSS}	Drain-to-Source Leakage Current			1.0	μA	$V_{DS} = 40V, V_{GS} = 0V$
				150		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ C$
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage			-100		$V_{GS} = -20V$
R_G	Internal Gate Resistance		2.6		Ω	

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by T_{Jmax} , starting $T_J = 25^\circ C$, $L = 0.032mH$, $R_G = 50\Omega$, $I_{AS} = 100A$, $V_{GS} = 10V$.
- ④ $I_{SD} \leq 100A$, $di/dt \leq 1330A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175^\circ C$.
- ⑤ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑥ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ R_θ is measured at T_J approximately 90°C.
- ⑨ Limited by T_{Jmax} , starting $T_J = 25^\circ C$, $L = 1mH$, $R_G = 50\Omega$, $I_{AS} = 28A$, $V_{GS} = 10V$.

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	88			S	$V_{DS} = 10\text{V}$, $I_D = 100\text{A}$
Q_g	Total Gate Charge		90	135	nC	$I_D = 100\text{A}$ $V_{DS} = 20\text{V}$ $V_{GS} = 10\text{V}$ ⑤
Q_{gs}	Gate-to-Source Charge		23			
Q_{gd}	Gate-to-Drain ("Miller") Charge		32			
Q_{sync}	Total Gate Charge Sync. ($Q_g - Q_{gd}$)		58			
$t_{d(on)}$	Turn-On Delay Time		24		ns	$V_{DD} = 20\text{V}$ $I_D = 30\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ⑤
t_r	Rise Time		68			
$t_{d(off)}$	Turn-Off Delay Time		115			
t_f	Fall Time		68			
C_{iss}	Input Capacitance		4730		pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{ MHz}$ $V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 32V ⑦ $V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V}$ to 32V ⑧
C_{oss}	Output Capacitance		680			
C_{rss}	Reverse Transfer Capacitance		460			
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)		845			
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)		980			
I_S	Continuous Source Current (Body Diode)			172	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑨			772	A	
V_{SD}	Diode Forward Voltage		0.9	1.3	V	$T_J = 25^\circ\text{C}$, $I_S = 100\text{A}$, $V_{GS} = 0\text{V}$ ⑩
dv/dt	Peak Diode Recovery ⑪		6.8		V/ns	$T_J = 175^\circ\text{C}$, $I_S = 100\text{A}$, $V_{DS} = 40\text{V}$
t_{rr}	Reverse Recovery Time		24		ns	$T_I = 25^\circ\text{C}$ $V_R = 34\text{V}$, $T_J = 125^\circ\text{C}$ $I_F = 100\text{A}$
			28			
Q_{rr}	Reverse Recovery Charge		17		nC	$T_I = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ⑫ $T_J = 125^\circ\text{C}$
			20			
I_{RRM}	Reverse Recovery Current		1.3		A	$T_J = 25^\circ\text{C}$

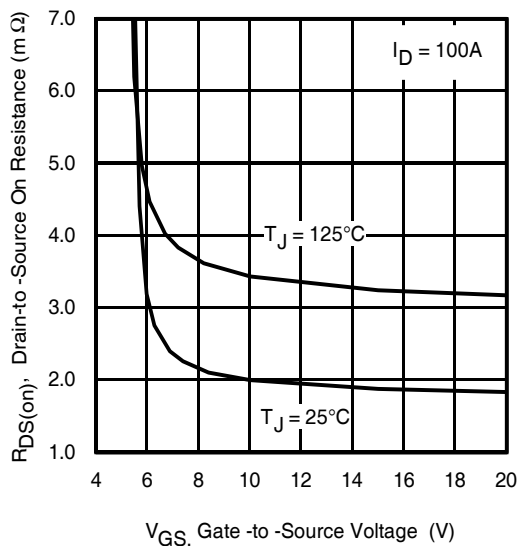


Fig 1. Typical On-Resistance vs. Gate Voltage

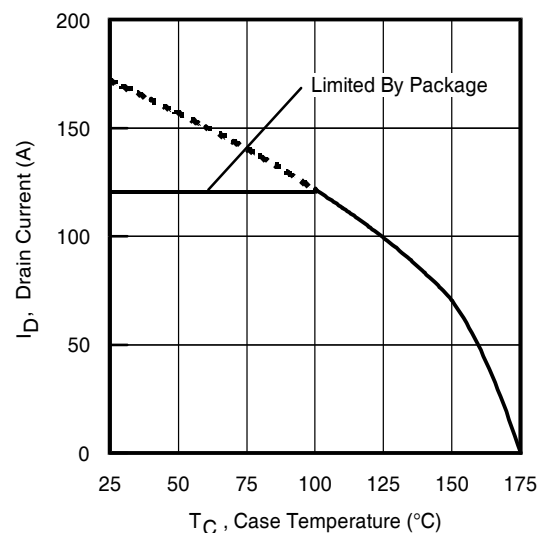


Fig 2. Maximum Drain Current vs. Case Temperature

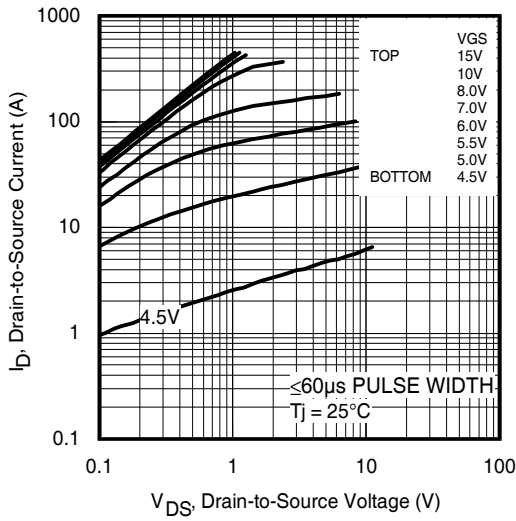


Fig 3. Typical Output Characteristics

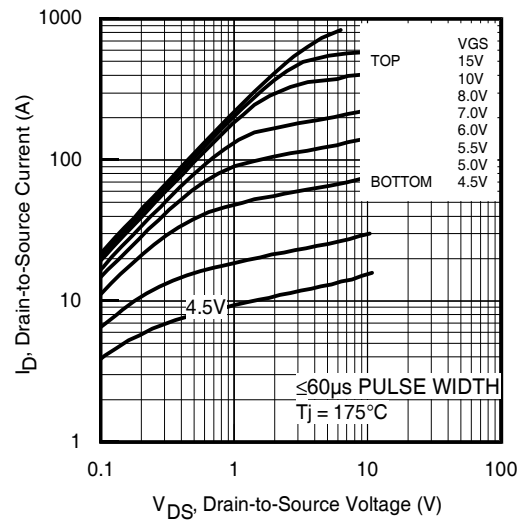


Fig 4. Typical Output Characteristics

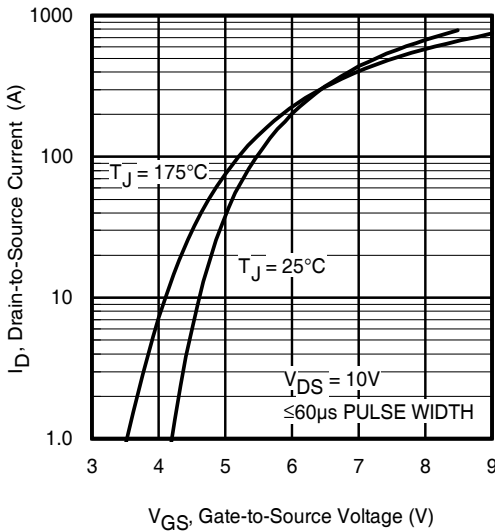


Fig 5. Typical Transfer Characteristics

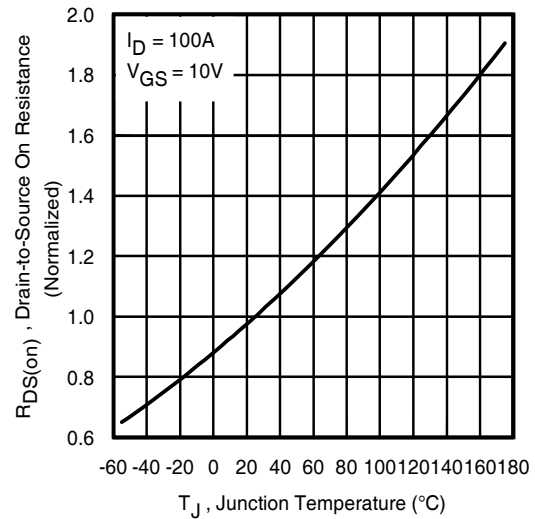


Fig 6. Normalized On-Resistance vs. Temperature

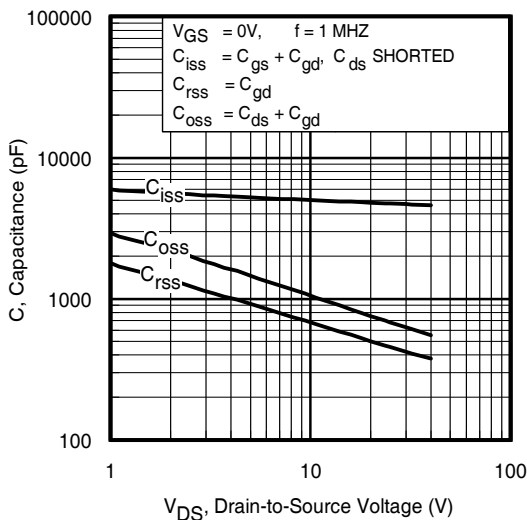


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

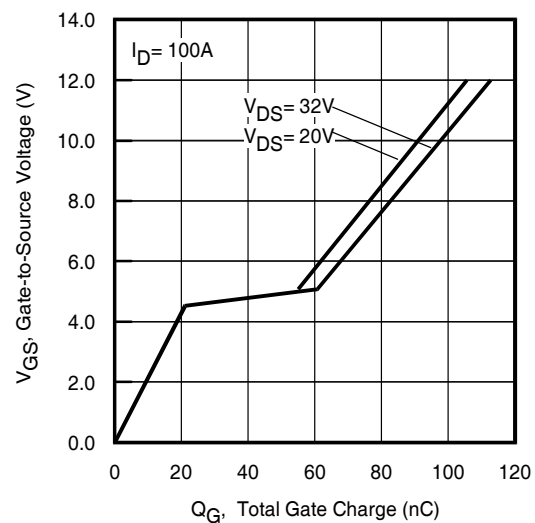


Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage

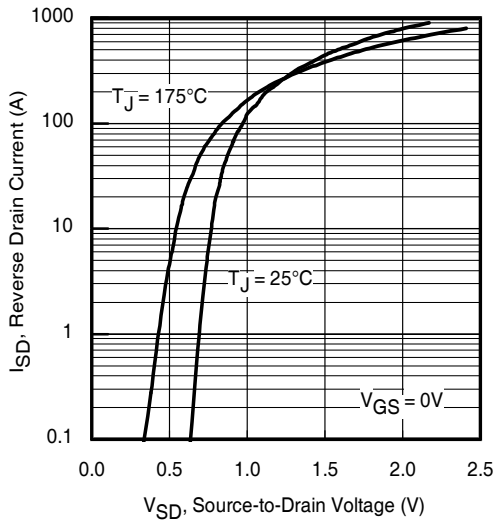


Fig 9. Typical Source-Drain Diode Forward Voltage

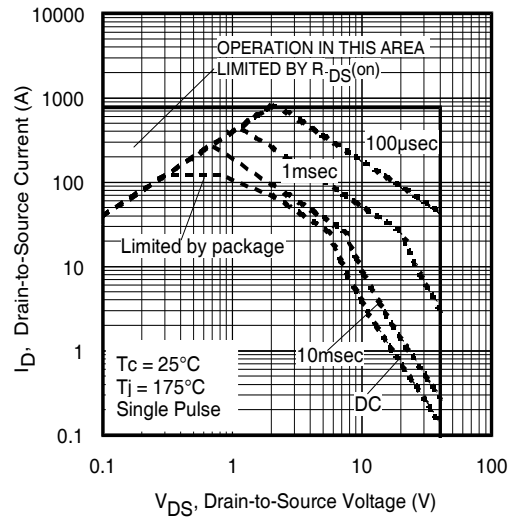


Fig 10. Maximum Safe Operating Area

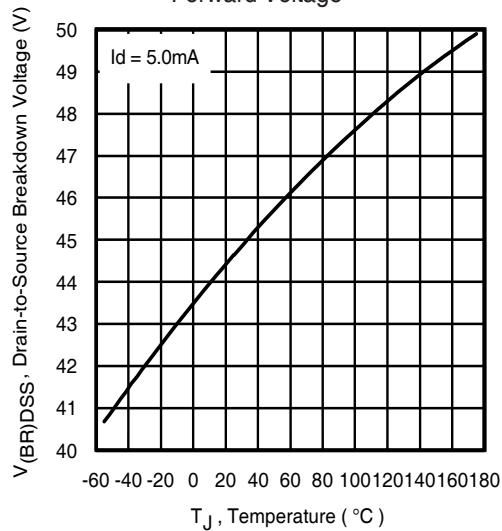


Fig 11. Drain-to-Source Breakdown Voltage

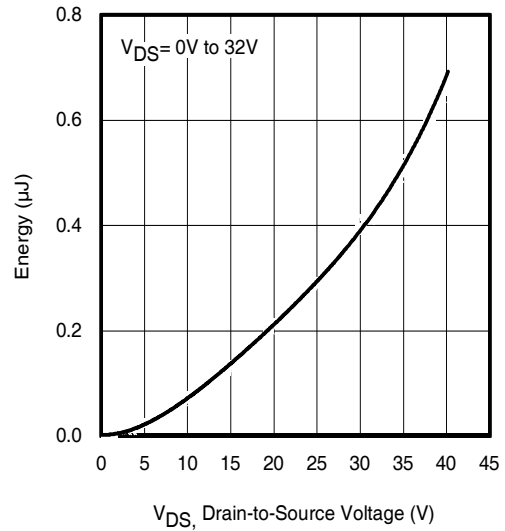


Fig 12. Typical C_{OSS} Stored Energy

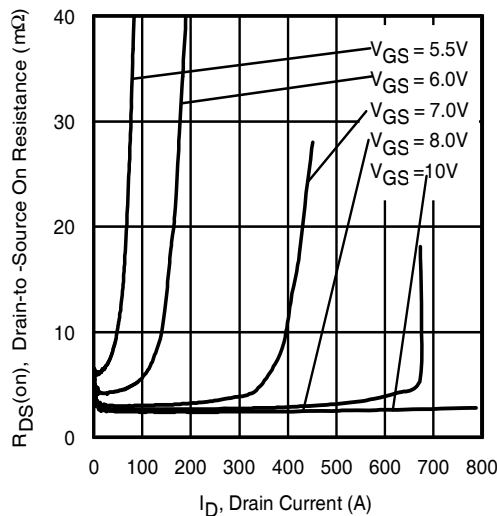


Fig 13. Typical On-Resistance vs. Drain Current

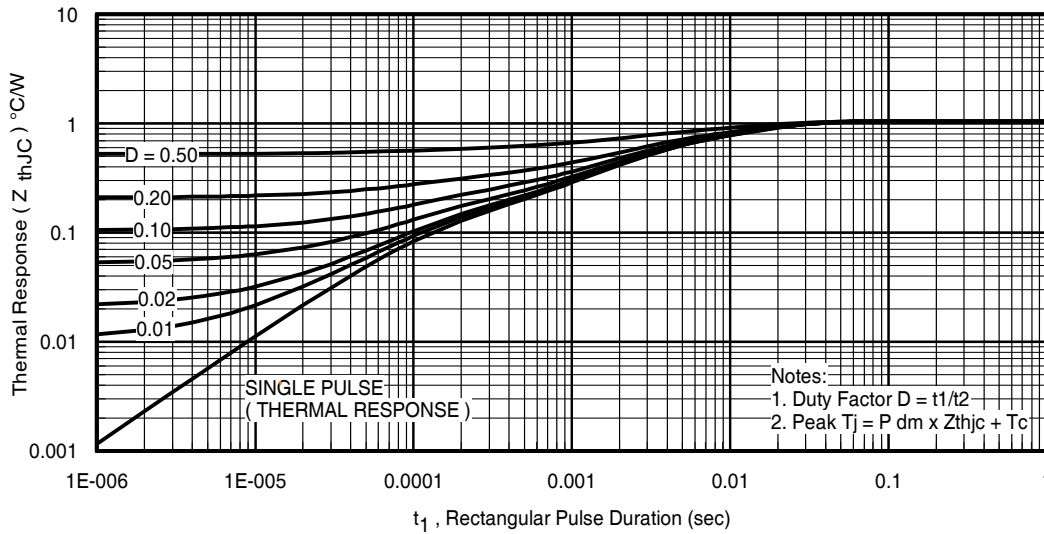


Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case

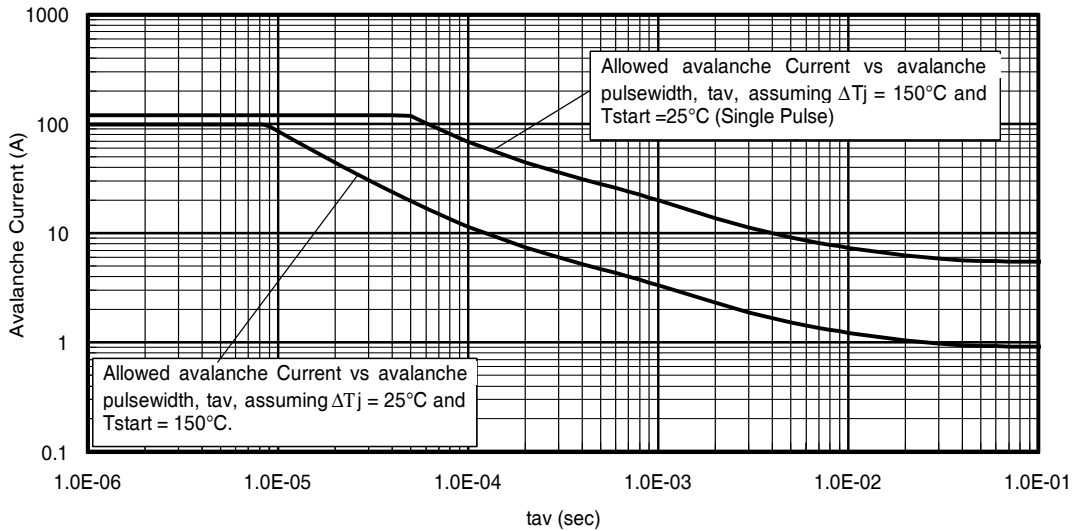


Fig 15. Typical Avalanche Current vs. Pulsewidth

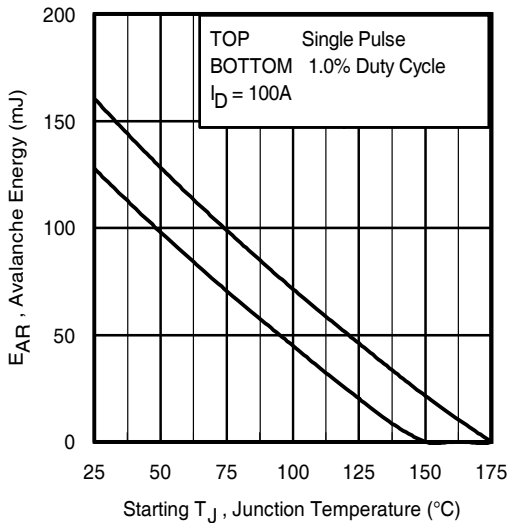


Fig 16. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves, Figures 14, 15:

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

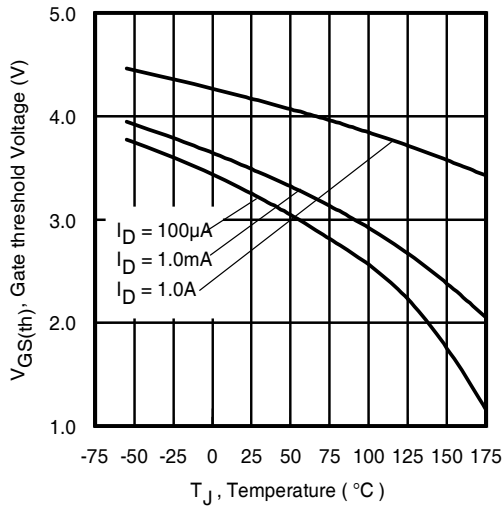


Fig 17. Threshold Voltage vs. Temperature

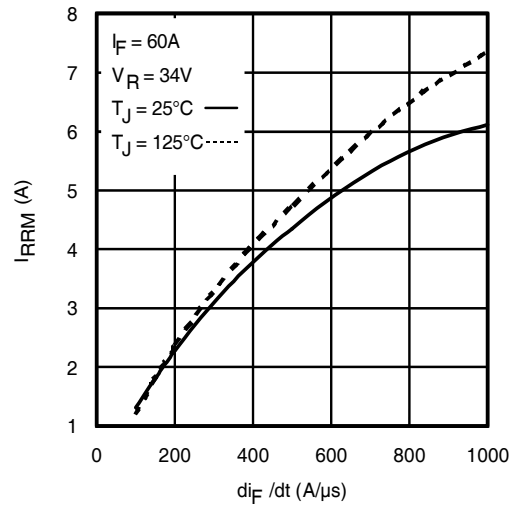


Fig 18. - Typical Recovery Current vs. di_F/dt

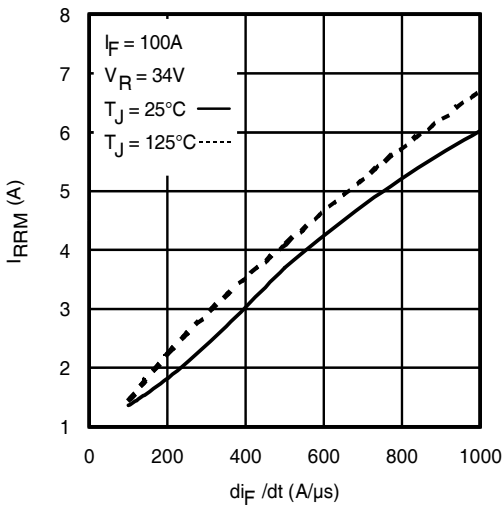


Fig 19. - Typical Recovery Current vs. di_F/dt

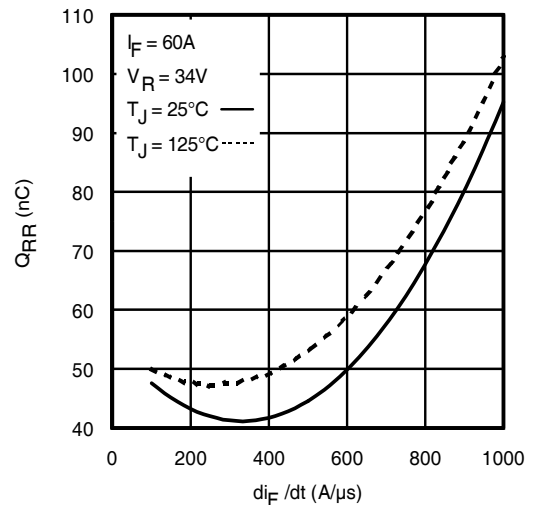


Fig 20. - Typical Stored Charge vs. di_F/dt

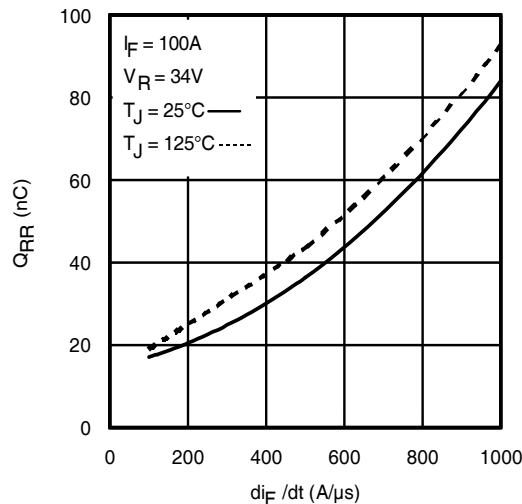
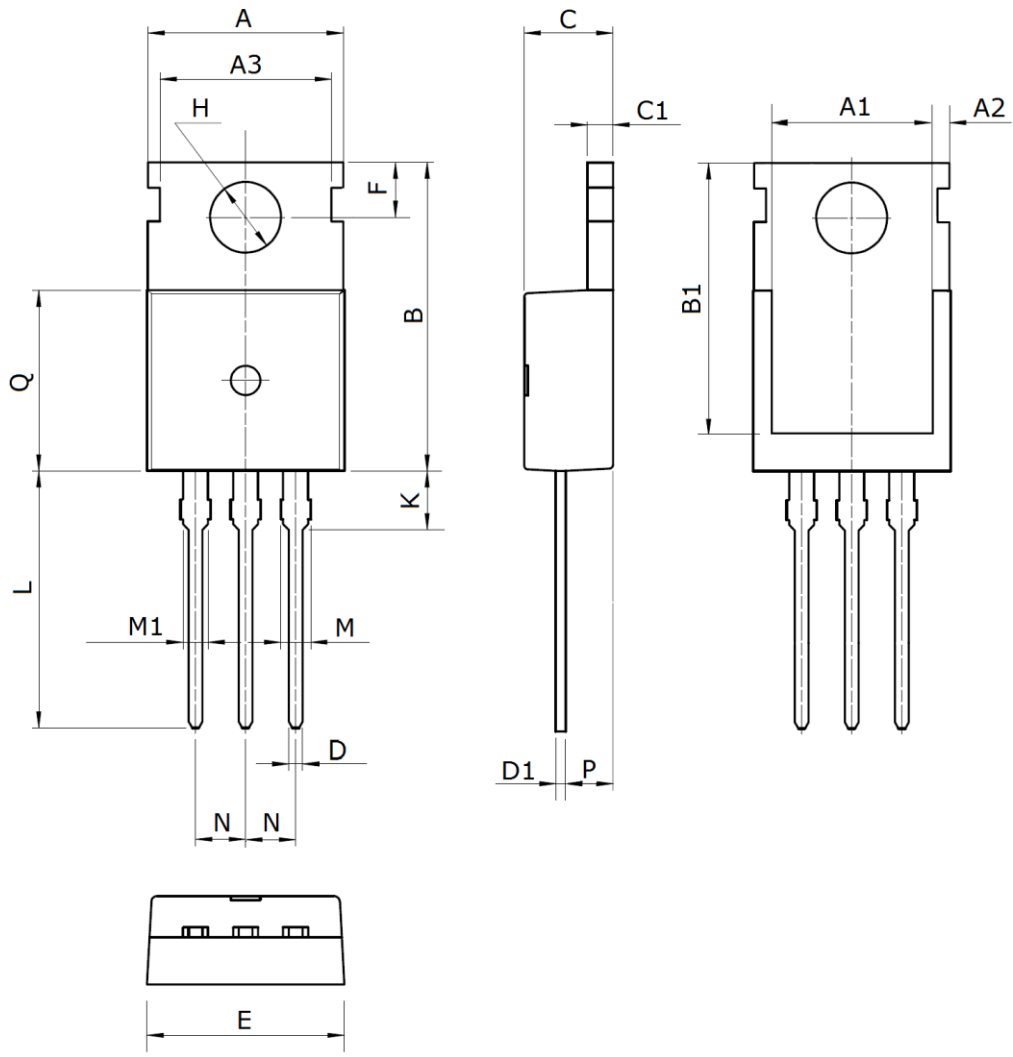


Fig 21. - Typical Stored Charge vs. di_F/dt

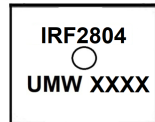
Package Dimensions

TO 220



Symbol	Dimensions (mm)	Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A	10.0±0.3	C1	1.3±0.2	L	13.2±0.4
A1	8.0±0.2	D	0.8±0.2	M	1.38±0.1
A2	0.94±0.1	D1	0.5±0.1	M1	1.28±0.1
A3	8.7±0.1	E	10.0±0.3	N	2.54(typ)
B	15.6±0.4	F	2.8±0.1	P	2.4±0.3
B1	13.2±0.2	H	3.6±0.1	Q	9.15±0.25
C	4.5±0.2	K	3.1±0.2		

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRFB7440PBF	TO-220	1000	Tube and box