



## 1. 特性

- 低偏置电压:  $\pm 100 \mu\text{V}$  (max)
- 低偏置电压温漂:  $0.6 \mu\text{V}/^\circ\text{C}$  (typ)
- 低噪声:  $17\text{nV}/\sqrt{\text{Hz}}$
- 共模抑制比: 146dB (Typ)
- 支持轨到轨输入/输出
- 单位增益稳定
- 输入电压范围支持负电源轨
- 增益带宽: 2.5MHz
- 低静态电流:  $550 \mu\text{A}$
- 滤波输入集成 RFI
- 支持 1 通道或者 2 通道

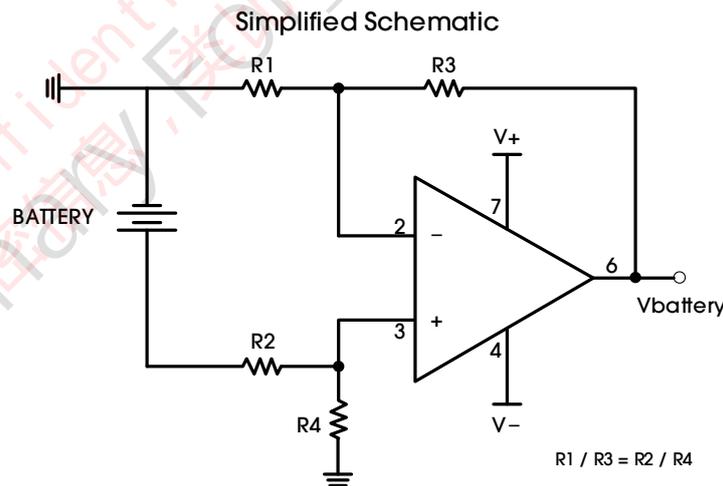
## 2. 应用

- 电池测试设备
- 商用电源
- 换能放大器
- 温度测试设备
- 功率模块跟随器
- 应变计

## 3. 说明

OPA305 是一款 36V 高性能支持轨到轨输入输出的运算放大器, 其具有常温下  $100\mu\text{V}$ (max) 的极低输入失调电压和 146dB 的高 CMRR。在配置为差分放大器时可提供出色的初始精度和轨到轨输出。该产品适用于单电源供电的便携式设备等应用中。

OPA305 具备 2.5MHz 的带宽, 配合出色的直流性能, 使得 OPA305 非常适用于有源滤波器电路。此外, OPA305 具备很好的稳定性, 在 Gain = 1 时, 最大可以驱动  $600\text{pF}$  的容性负载。OPA305 适用于多样化的电路, 并提供小外形封装以减少 PCB 使用面积, 降低设计成本。OPA305 封装类型包括: SOT23-5, MSOP-8 和 SOIC-8, 其中 OPA3052 为 2 通道版本, 封装为 SOIC-8, MSOP-8 和 TSSOP-8。所有版本的额定温度范围为  $-40^\circ\text{C}$  至  $+125^\circ\text{C}$ 。有关订购信息, 请参见表 1。



# OPA305/OPA3052

36V 高性能通用运算放大器

**Table 1. Order Information**

ORDER NUMBER (See Note 1)	PART NUMBER	CH (#)	PACKAGE	MARKING INFO. (See Note 2 and Note 3)	I <sub>Q</sub> PER CH (TYP) ( $\mu$ A)	GBW (MHz)	SLEW RATE (TYP) (V/ $\mu$ s)	OPERATING TEMP ( $^{\circ}$ C)	PACKAGE OPTION
OPA305ASOIC8	OPA305	1	SOIC-8	OPA305	550	2.5	1.6	-40-125	TBD
OPA305ASOT235	OPA305	1	SOT23-5	OPA305				-40-125	TBD
OPA305AMSOP8	OPA305	1	MSOP-8	OPA305				-40-125	TBD
OPA3052ASOIC8	OPA3052	2	SOIC-8	OPA3052				-40-125	TBD
OPA3052AMSOP8	OPA3052	2	MSOP-8	OPA3052				-40-125	TBD
OPA3052ATSSOP8	OPA3052	2	TSSOP-8	OPA3052				-40-125	TBD



## 4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration of the 1 CH devices.

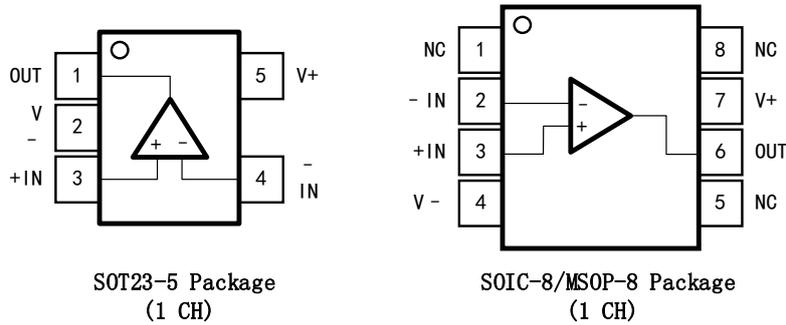


Figure 1. Pin Configuration (1 CH Devices)

Table 2 lists the pin functions of the 1 CH devices.

Table 2. Pin Functions (1 CH Devices)

PIN	POSITION		TYPE	DESCRIPTION
	SOT23-5	SOIC-8		
OUT	1	6	O	Output
V-	2	4	PWR	Negative (lowest) power supply
+IN	3	3	I	Positive (non-inverting) input
-IN	4	2	I	Negative (inverting) input
V+	5	7	PWR	Positive (highest) power supply
NC	—	1, 5, 8	I/O	No internal connection (can be left floating)

Figure 2 illustrates the pin configuration of the 2 CH devices.

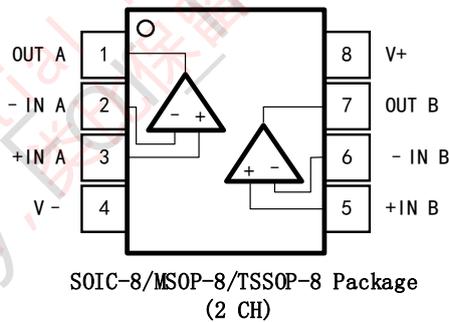


Figure 2. Pin Configuration (2 CH Devices)

Table 3 lists the pin functions of the 2 CH devices.

Table 3. Pin Functions (2 CH Devices)

PIN	POSITION	TYPE	DESCRIPTION
OUT A	1	O	Output, channel A
-IN A	2	I	Inverting input, channel A
+IN A	3	I	Non-inverting input, channel A
V-	4	PWR	Negative (lowest) power supply
+IN B	5	I	Non-inverting input, channel B
-IN B	6	I	Inverting input, channel B
OUT B	7	O	Output, channel B
V+	8	PWR	Positive (highest) power supply

## 5. SPECIFICATIONS

### 5.1 ABSOLUTE MAXIMUM RATINGS

Table 5 lists the absolute maximum ratings of the OPA305 family. Over operating free-air temperature range, unless otherwise noted (see Note 1 under Table 5).

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION		MIN	MAX	UNITS
Voltage	Supply	Split supply	±0	±20	V
		Single supply	0	40	
	Signal input pins	Common-mode	(V-) - 0.5	(V+) + 0.5	
		Differential		±6	
Current	Signal input pins			±10	mA
	Output short-circuit (see Note 2 under Table 5)		Continuous		
Temperature	Operating, T <sub>A</sub>		-40	125	°C
	Junction, T <sub>J</sub>			150	
	Storage, T <sub>stg</sub>		-65	150	

Note 1: Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 7. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: Short-circuit to ground, one amplifier per package.

### 5.2 ESD RATINGS

Table 6 lists the ESD ratings of the OPA305 family.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (see Note 1 under Table 6)	TBD	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (see Note 2 under Table 6)	TBD	

Note 1: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 RECOMMENDED OPERATING CONDITIONS

Table 7 lists the recommended operating conditions for the OPA305 family. Over operating free-air temperature range, unless otherwise noted.

Table 6. Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNITS
Operating Voltage Range	Split supply	±1.35		±18	V
	Single supply	2.7		36	V
Specified Temperature Range		-40		125	°C

## 5.4 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of the OPA305.  $T_A=25^{\circ}\text{C}$ ,  $V_S=36\text{V}$ ,  $V_{\text{CM}}=V_{\text{OUT}}=V_S/2$ , and  $R_{\text{LOAD}} = 10\text{k}\Omega$  connected to  $V_S / 2$ , unless otherwise noted.

Table 7. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>OFFSET VOLTAGE</b>						
Input Offset Voltage	$V_{\text{OS}}$	$V_S = 36\text{V}$ , $T_A = 25^{\circ}\text{C}$		$\pm 5$	$\pm 100$	$\mu\text{V}$
Offset Voltage Drift		$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		$\pm 0.6$	$\pm 4$	$\mu\text{V}/^{\circ}\text{C}$
$V_S$ Power Supply	PSRR	$V_S = 5\text{V}$ to $36\text{V}$ , $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$		0.15	$\pm 4.3$	$\mu\text{V}/\text{V}$
<b>INPUT BIAS CURRENT</b>						
Input Bias Current	$I_b$			5		pA
Over Temperature		$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$				nA
Input Offset Current	$I_{\text{OS}}$			20		pA
Over Temperature		$T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$				nA
<b>NOISE</b>						
Input Voltage Noise		$f = 0.1\text{Hz}$ to $10\text{Hz}$		4.5		$\mu\text{VPP}$
Input Voltage Noise Density	$e_n$	$f = 100\text{Hz}$		27.4		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{kHz}$		17		$\text{nV}/\sqrt{\text{Hz}}$
<b>INPUT VOLTAGE</b>						
Common-Mode Voltage Range (See Note under Table 8)	$V_{\text{CM}}$		(V-)		(V+)	V
Common-Mode Rejection Ratio	CMRR	$V_S = \pm 18\text{V}$ , $(V-) \text{ V} < V_{\text{CM}} < (V+) - 2.5\text{V}$ , $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	108	146		dB
<b>INPUT IMPEDANCE</b>						
Differential				100    3		$\text{M}\Omega$    pF
Common-Mode				6    3		$10^{12}\Omega$    pF
<b>OPEN-LOOP GAIN</b>						
Open-Loop Voltage Gain	$A_{\text{OL}}$	$(V-) < V_O < (V+)$ , $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	129	130		dB
<b>FREQUENCY RESPONSE</b>						
Gain Bandwidth Product	GBP			2.5		MHz
Slew Rate	SR	$G = 1$		1.6		$\text{V}/\mu\text{s}$
Settling Time	$t_s$	To 0.1%, $V_S = \pm 18\text{V}$ , $G = 1$ , 10V step		7		$\mu\text{s}$
		To 0.01% (12bit), $V_S = \pm 18\text{V}$ , $G = 1$ , 10V step		13		$\mu\text{s}$
Overload Recovery Time		$V_{\text{IN}} \times \text{gain} > V_S$		1		$\mu\text{s}$
<b>OUTPUT</b>						
Voltage Output Swing from Rail	$V_O$	$V_S = 36\text{V}$ , $R_L = 10\text{k}\Omega$		50		mV
Over Temperature		$R_L = 10\text{k}\Omega$ , $A_{\text{OL}} \geq 110\text{dB}$ , $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	TBD		TBD	V
Short-Circuit Current	$I_{\text{SC}}$			$\pm 25$		mA
Capacitive Load Drive	$C_{\text{LOAD}}$			600		pF

# OPA305/OPA3052

## 36V 高性能通用运算放大器

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Open-Loop Output Resistance	$R_o$	$f = 1\text{MHz}, I_o = 0\text{A}$		150		$\Omega$

### POWER SUPPLY

Specified Voltage Range	$V_s$		2.7		36	V
Quiescent Current per Amplifier	$I_q$	$I_o = 0\text{A}$		550	650	$\mu\text{A}$
Over Temperature		$I_o = 0\text{A}, T_A = -40^\circ\text{C to } +125^\circ\text{C}$			700	$\mu\text{A}$

### TEMPERATURE

Operating Range			-40		125	$^\circ\text{C}$
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Note: The input range can be extended beyond  $(V+) - 2\text{V}$  up to  $V+$ .

## 6. PACKAGE INFORMATION

The OPA305 family is available in the SOT23-5, SOIC-8, and TSSOP-14 packages.

### 6.1 SOT23-5 PACKAGE

Figure 4 shows the SOT23-5 package view.

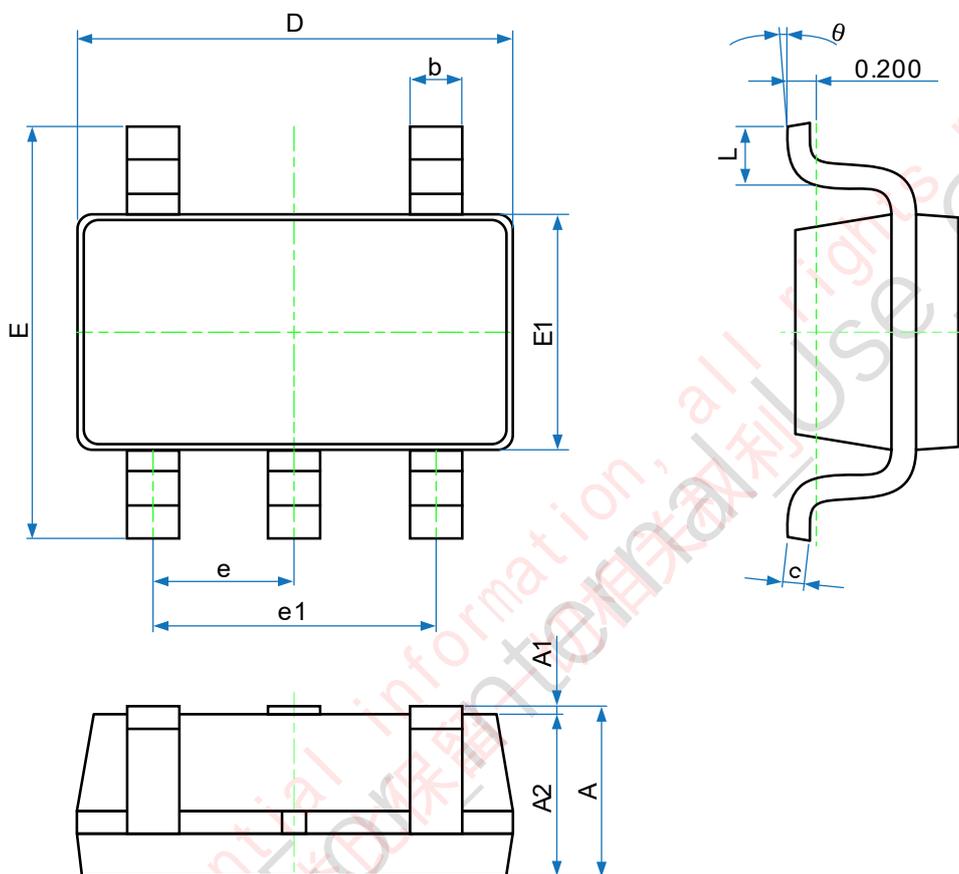


Figure 3. SOT23-5 Package View

Table 9 provides detailed information about the dimensions of the SOT23-5 package.

Table 8. Dimensions of the SOT23-5 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	2.650	2.950	0.104	0.116
E1	1.500	1.700	0.059	0.067
e	0.950 (BSC)		0.037 (BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
$\theta$	0°	8°	0°	8°

### 6.2 SOIC-8 PACKAGE

Figure 5 shows the SOIC-8 package view.

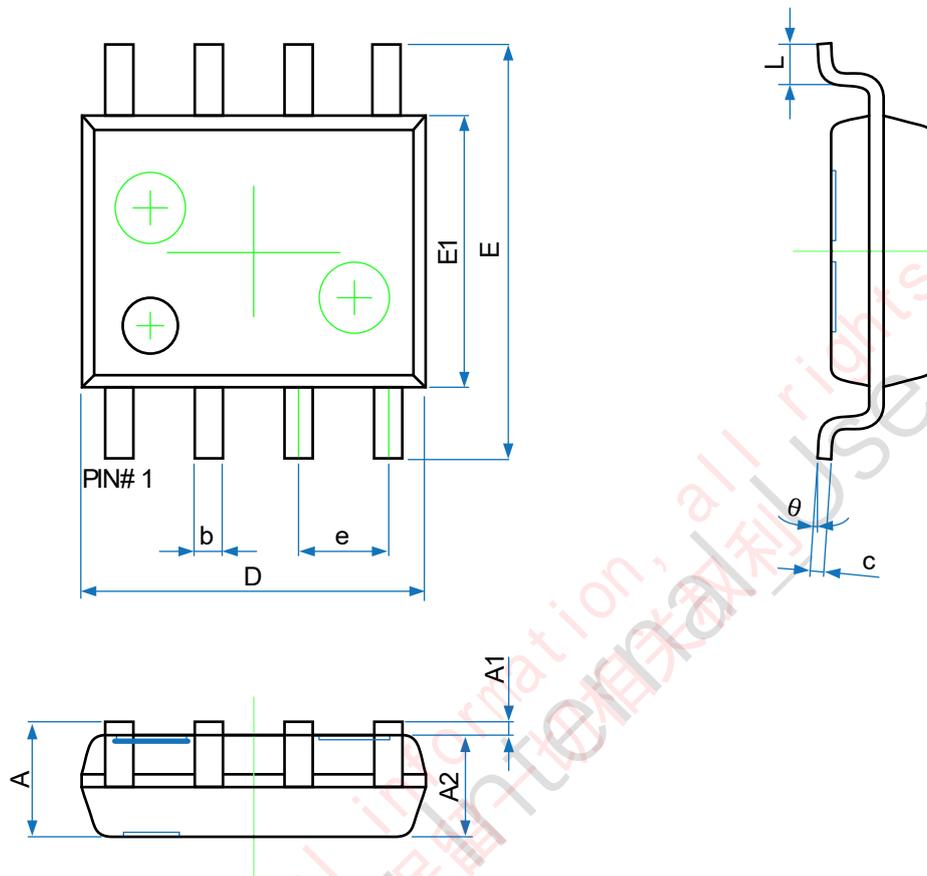


Figure 4. SOIC-8 Package View

Table 10 provides detailed information about the dimensions of the SOIC-8 package.

Table 9. Dimensions of the SOIC-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

### 6.3 MSOP-8 PACKAGE

Figure 6 shows the MSOP-8 package view.

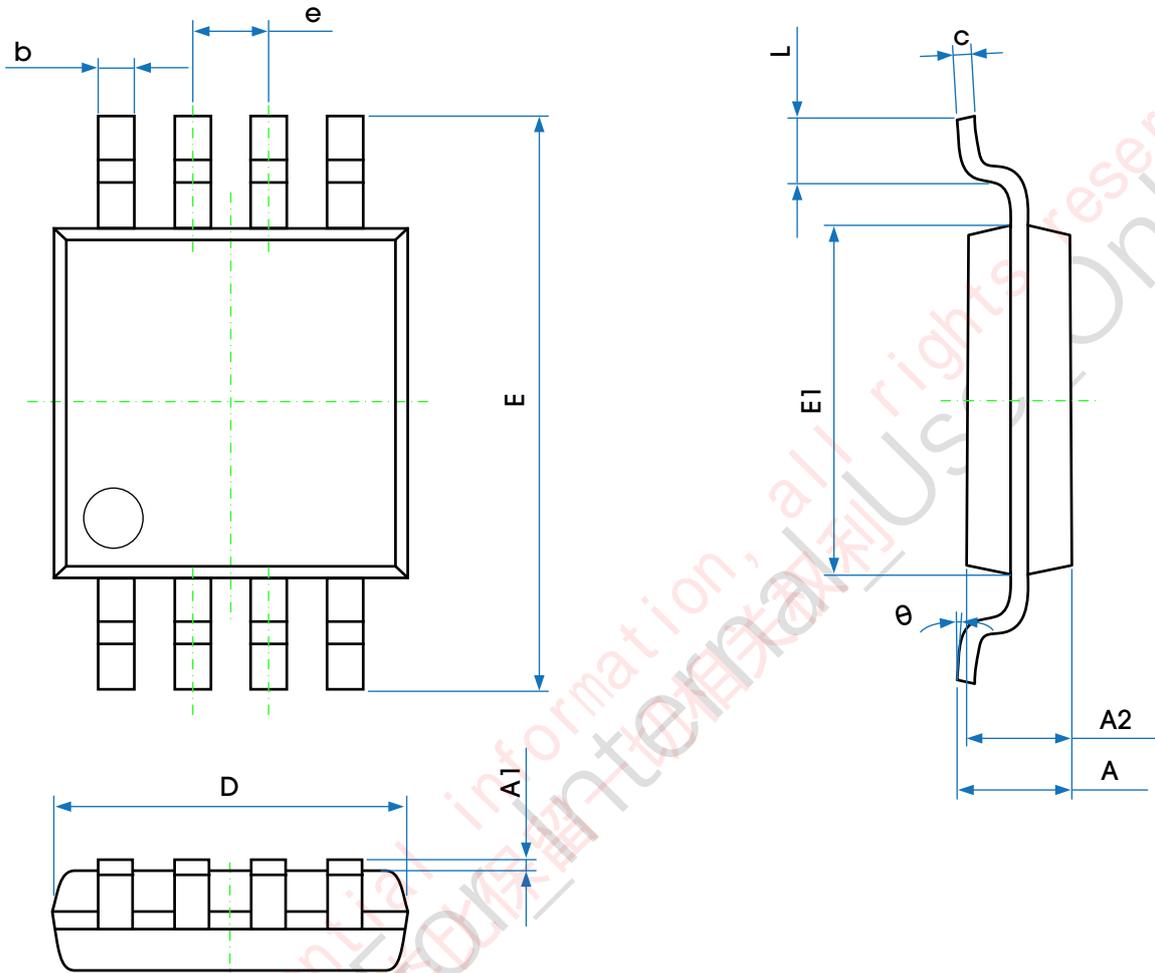


Figure 5. MSOP-8 Package View

Table 11 provides detailed information about the dimensions of the MSOP-8 package.

Table 10. Dimensions of the MSOP-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	---	1.100	---	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650 (BSC)		0.026 (BSC)	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

### 6.4 TSSOP-8 PACKAGE

Figure 30 shows the TSSOP-8 package view.

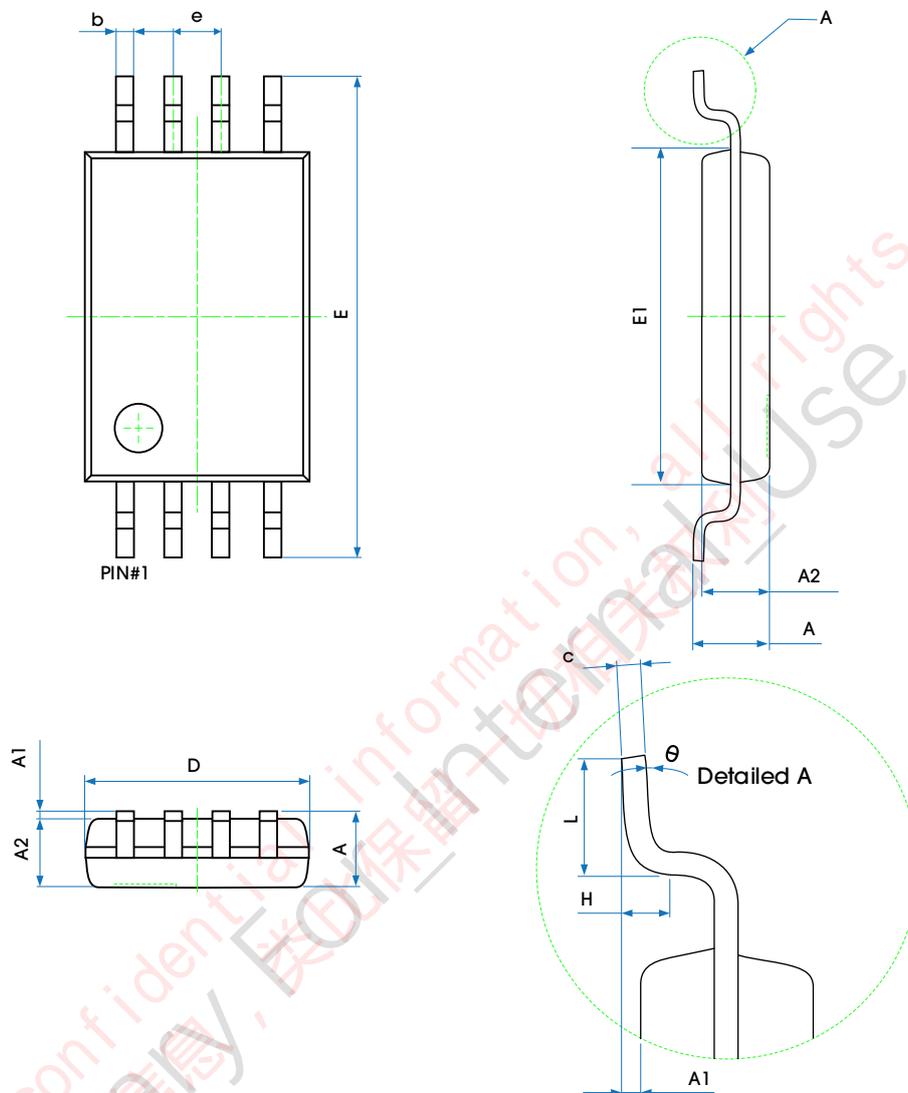


Figure 6. TSSOP-8 Package View

Table 9 provides detailed information about the dimensions of the TSSOP-8 package.

Table 11. Dimensions of the TSSOP-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	---	1.200	---	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	2.900	3.100	0.114	0.122
E	6.250	6.550	0.246	0.258
E1	4.300	4.500	0.169	0.177

e	0.650 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.250 (TYP)		0.010 (TYP)	
$\theta$	1°	7°	1°	7°

## 7. TAPE AND REEL INFORMATION

TBD

### REVISION HISTORY

REVISION	DATE	DESCRIPTION
V0.1	15 January 2021	Initial release.
V0.5	18 Oct 2022	Updated spec with sim results
V0.8	2 Feb 2023	Updated Spec with testing results
V0.8.1	24 Feb 2023	Updated Vcm range spec
V1.0	6 May 2023	Updated table 5.4 based on test data.