WS742133

Capless 2Vrms to 3Vrms Line Driver with Adjustable Gain

Http//:www.willsemi.com

Descriptions

The WS742133 is an integrated solution for Set-top box and high definition player, and designed to optimize the audio driver circuit performance while reducing the BOM cost by eliminating the peripheral discrete components for noise reduction. WS742133 features a 3Vrms stereo audio driver that designed to allow for the removal of output AC-coupling capacitors. Featuring differential input mode, gain range of ±1V/V to ±10V/V can be achieved via external gain resistor setting. The WS742133 is able to offer 3Vrms output at 600Ω load with 5V supply. Meanwhile, the WS742133 offers built-in shut-down control circuitry for optimal pop-free performance. Under under-voltage condition, WS742133 is able to detect it and mutes the output. WS742128 satisfies MSL3 level requirements.

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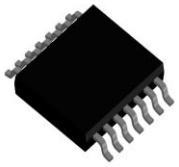
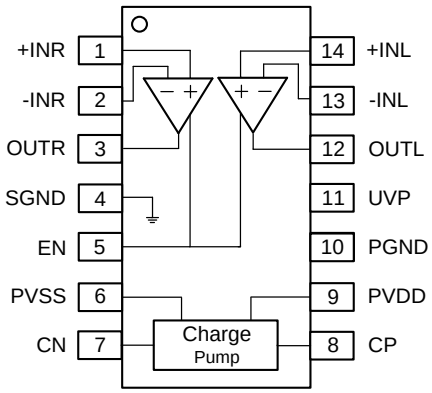


TSSOP-14L



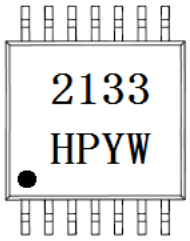
Pin configuration (Top view)

Applications

- Set-Top Boxes
- High Definition DVD Players
- Car Entertainment System
- Medical

Features

- Single Supply Voltage : 3.0V~5.5V
- THD+N : >100dB
- SNR : >112dB
- -40°C to 85°C Operation Range
- Voltage Output at 600Ω Load
  2Vrms with 3.3V supply voltage
  3Vrms with 5.0V supply voltage
- No Pop/Clicks Noise when Power ON/OFF
- No Need Output DC-Blocking Capacitors
- Optimized Frequency Response between 20Hz~20kHz
- Accepting Differential Input
- Featuring external under voltage mute
- Available in TSSOP-14L package
- Ultra Low noise and THD



Marking

2133 = Device code
HP = Special code
Y = Year code
W = Week code

Order Information

Device	Package	Shipping
WS742133H-14/TR	TSSOP-14L	4000/Reel &Tape

Pin Descriptions

Pin Number	Symbol	Descriptions
1	+INR	Right-channel positive input
2	-INR	Right-channel negative input
3	OUTR	Right-channel output
4	SGND	Signal ground
5	EN	Enable input, active-high
6	PVSS	Supply voltage
7	CN	Charge-pump flying capacitor negative
8	CP	Charge-pump flying capacitor positive
9	PVDD	Positive supply
10	PGND	Power ground
11	UVP	Under voltage protection input
12	OUTL	Left-channel output
13	-INL	Left-channel negative input
14	+INL	Left-channel positive input

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD} (2)	6	V
Input Differential Voltage	V_{IDR} (3)	±6	V
Input Common Mode Voltage Range	V_{ICR}	(V^-)-0.2 to (V^+)+0.2	V
Output Short-Circuit Duration	t_{SO}	Unlimited	/
Operating Fee-Air Temperature Range	T_A	-40 to 85	°C
Storage Temperature Range	T_{STG}	-65 to 150	°C
Junction Temperature Range	T_J	150	°C
Lead Temperature Range	T_L	260	°C
TSSOP-14LΘ_{JA}		115	°C/W

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values, except differential voltage are with respect to network terminal.
3. Differential voltages are at IN+ with respect to IN–.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8 JEDEC-EIA/JESD22-A114A	4	kV
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	200	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

Electronics Characteristics

The ***** denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, R_L = 25kΩ

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		*	3	5	5.5	V
V_{IH}	EN High level input voltage			1.1			V
V_{IL}	EN Low level input voltage					0.4	V
T_A	Operating Temperature Range		*	-40		85	°C
V_{os}	Output Offset Voltage	V_{DD}=3V to 5V, input grounded, unity gain.	*	-3.5	0.6	3.5	mV
OVP	V_{DD} Over Voltage Protection	V_{DD}>5.5V then device shutdown.			5.75		V
PSRR	Power Supply Rejection Ratio				90		dB
V_{OH}	High Level Output Voltage	V_{DD}=5V R_L=2.5KΩ			4.92		V
		V_{DD}=3.3V R_L=2.5KΩ		3.15			V
V_{OL}	Low Level Output Voltage	V_{DD}=5V R_L=2.5KΩ			-4.65		V
		V_{DD}=3.3V R_L=2.5KΩ				-3	V
I_{IH}	EN High level input current	V_{DD}=5V V_i=V_{DD}	*			1	μA
I_{IL}	EN Low level input current	V_{DD}=5V V_i=0	*			1	μA
I_{DD}	Quiescent Current	V_{DD}=3.3V V_i=V_{DD}			10.6		mA
		V_{DD}=5V V_i=V_{DD}			12.6		
		Shut down mode V_{DD} = 3-5V				0.15	
V_o	Output Voltage	THD=1%, V_{DD}=3.3V f=1kHz		2.05			V_{rms}
THD+N	Total Harmonic Distortion and Noise	V_o=2V_{rms} f=1kHz R_L=600Ω, V_{DD}=3.3V			0.001		%
X_{TALK}	Channel cross talk	V_o=2V_{rms} f=1kHz, V_{DD}=3.3V			100		dB
I_O	Maximum output current	V_{DD}=3.3V			30		mA
SNR	Signal noise ratio	V_o=2V_{rms} BW=22kHz A-weighted and V_{DD}=3.3V			110		dB
SR	Slew Rate				12		V/μs
V_N	Noise output voltage	BW=20Hz to 22kHz, V_{DD}=3.3V			5.1		μV_{rms}
G_{BW}	Gain-Bandwidth Product	V_{DD}=3.3V			5		MHz
A_{VO}	Open Loop Large Signal Gain	V_{DD}=3.3V			100		dB
V_{UVP}	External under-voltage detection	V_{DD}=3.3V		1.14	1.21	1.31	V
I_{HYS}	External under-voltage detection hysteresis current	V_{DD}=3.3V			4.7		μA
f_{CP}	Charge pump frequency	V_{DD}=3.3V			400		kHz

Electronics Characteristics (continued)

The *****denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 5V, R_L = 25kΩ

Attenuation@mute	Input-to-output attenuation in shutdown	EN=0V, V_{DD}=3.3V			90		dB
V_o	Output Voltage	THD=1%, V_{DD}=5V f=1kHz		3.05			V_{rms}
THD+N	Total Harmonic Distortion and Noise	V_o=2V_{rms} f=1kHz R_L=600Ω, V_{DD}=5V			0.001		%
X_{TALK}	Channel cross talk	V_o=2V_{rms} f=1kHz, V_{DD}=5V			95		dB
I_O	Maximum output current	V_{DD}=5V			60		mA
SNR	Signal noise ratio	V_o=2V_{rms} BW=22kHz A-weighted V_{DD}=5V			112		dB
SR	Slew Rate				12		V/μs
V_N	Noise output voltage	BW=20Hz to 22kHz, V_{DD}=5V			4.5		μV_{rms}
G_{BW}	Gain-Bandwidth Product	V_{DD}=5V			7		MHz
A_{VO}	Open Loop Large Signal Gain	V_{DD}=5V			110		dB
V_{UVP}	External under-voltage detection	V_{DD}=5V		1.14	1.21	1.31	V
I_{HYS}	External under-voltage detection hysteresis current	V_{DD}=5V			4.7		μA
f_{CP}	Charge pump frequency	V_{DD}=5V			410		kHz
Attenuation@mute	Input-to-output attenuation in shutdown	EN=0V, V_{DD}=5V			90		dB

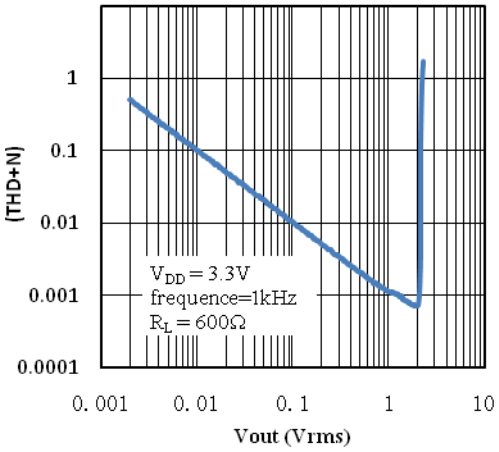
Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
2. A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.
3. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

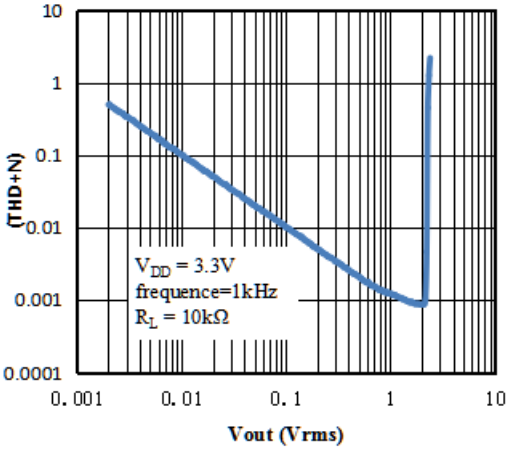
Typical Characteristics

T_A=25℃, V_{DD}=3.3V, unless otherwise noted

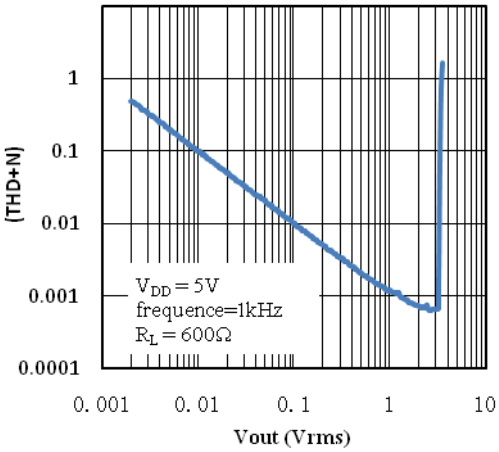
THD+N vs. Output Voltage



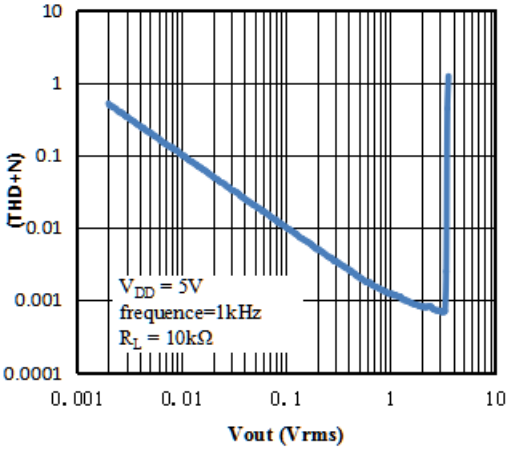
THD+N vs. Output Voltage



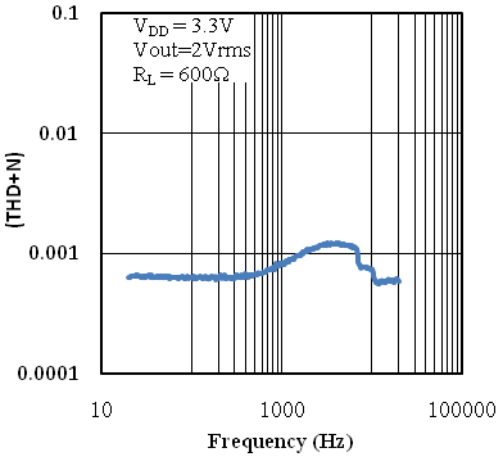
THD+N vs. Output Voltage



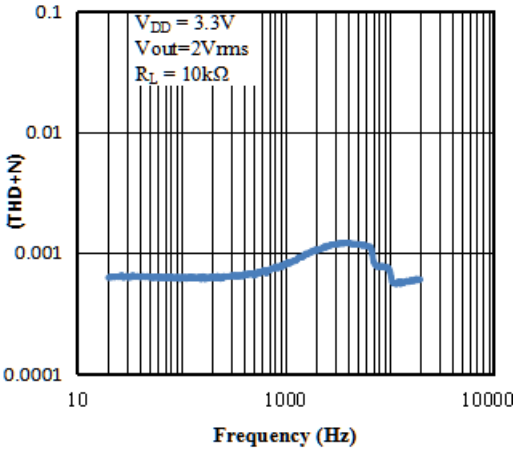
THD+N vs. Output Voltage



THD+N vs. Frequency



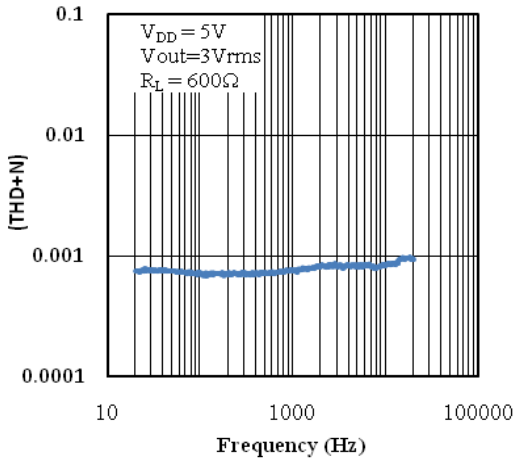
THD+N vs. Frequency



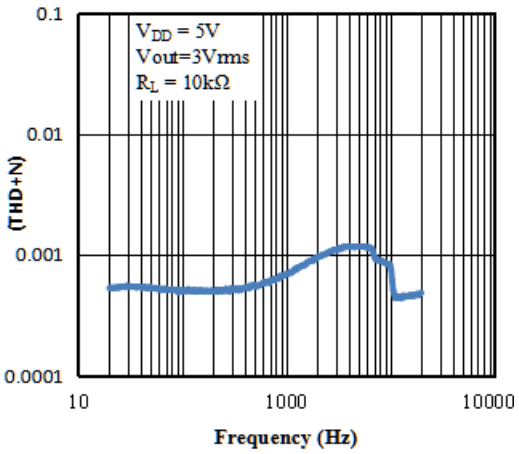
Typical Characteristics (continued)

T_A=25℃, V_{DD}=3.3V, unless otherwise noted

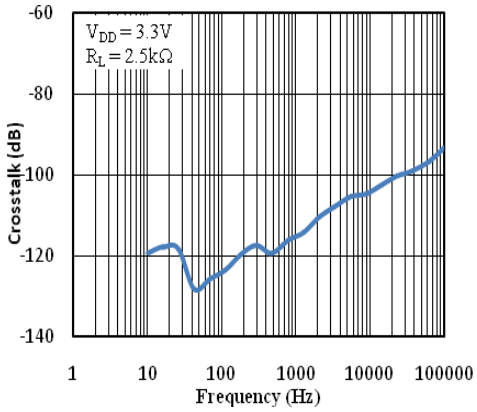
THD+N vs. Frequency



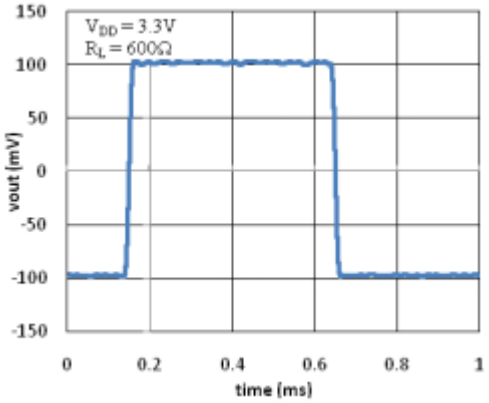
THD+N vs. Frequency



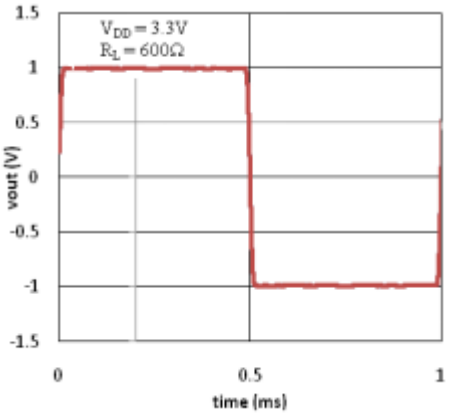
Crosstalk vs. Frequency



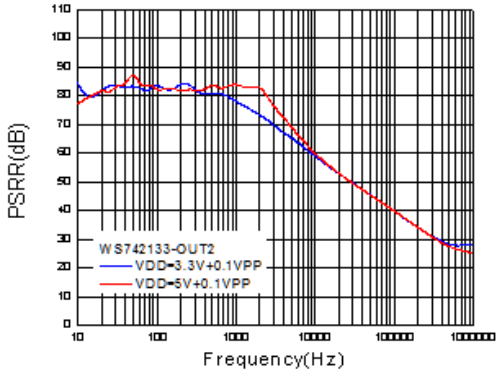
Small Signal Response



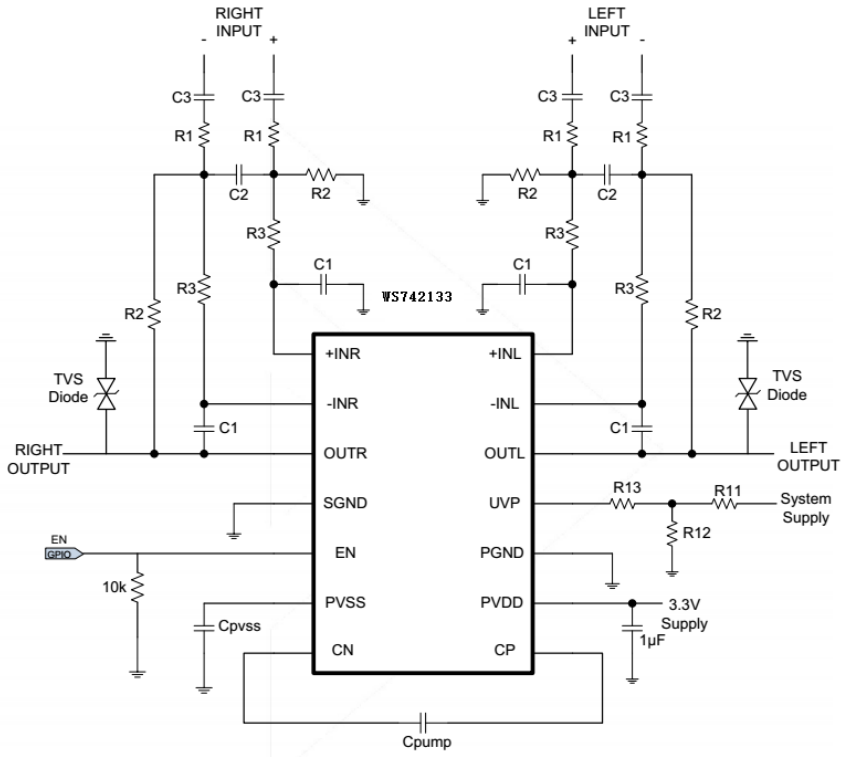
Large Signal Response



PSRR vs. Frequency



Application Circuit

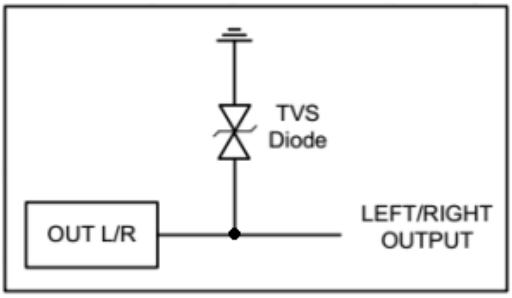


Differential-input, single-ended output, second-order filter R1=15kΩ, R2=30kΩ, R3=47kΩ, C1=33pF, C2=150pF, C3=6.8μF, R11=5.6kΩ, R12=2.43kΩ, R13=15KΩ, Cpvss=0.33 to 1μF, Cpump=0.33 to 1μF.

Notes

1. In some applications, if the power supply noise needs to be filtered, the ferrite bead is recommended in a value of 600ohm@100MHz, instead of RC network. RC network normally will lower the power supply resulting in the degraded the audio performance. If the resistor is not chosen properly, which can trigger the internal UVP detection circuit and shut down the output. As depicted below.

2. In order to protect the device against the power surge, transient voltage suppressor (TVS) devices are recommended at the output pins OUTL/OUTR.



Application Notes

Gain-Setting Resistors Ranges and Input-Blocking Capacitors

The gain-setting resistors, R_{IN} and R_{FB}, must be chosen so that noise, stability, and input capacitor size of the WS742133 are kept within acceptable limits. Voltage gain is defined as R_{FB} divided by R_{IN}. Table 1 lists the recommended resistor value for different gain settings. Selecting values that are too low remands a large input ac-coupling capacitor C_{IN}. Selecting values that are too high increases the noise of the amplifier. The gain-setting resistor must be placed close to the input pins to minimize capacitive loading on these input pins and to ensure maximum stability.

Table 1. Input Capacitor with 2Hz cutoff and Resistor Values Recommended

Input Res., R_{IN}	Feedback Res., R_{fb}	Inverting Gain
22 kΩ	22 kΩ	-1 V/V
15 kΩ	30 kΩ	-2 V/V
10 kΩ	100 kΩ	-10 V/V

$$f_{CIN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or}$$

$$C_{IN} = \frac{1}{2\pi R_{IN} f_{CIN}}$$

Equation 1. Cutoff decision Cutoff

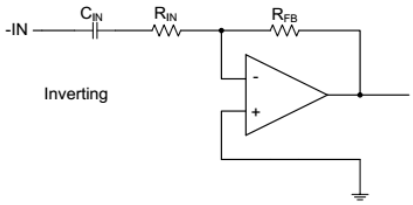


Figure 2. Inverting Gain Configurations

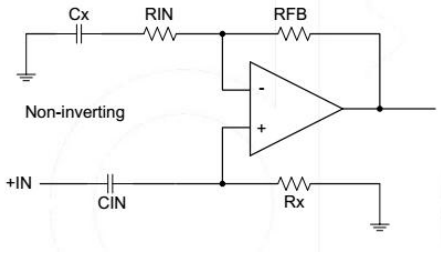


Figure 3. Non-Inverting Gain Configuration

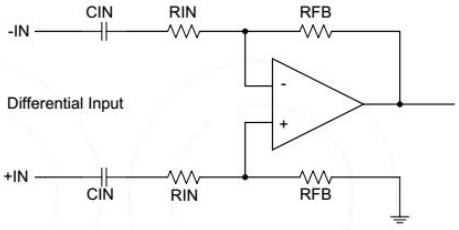


Figure 4. Differential Gain Configuration

INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of WS742133. These capacitors block the dc portion of the audio source and allow WS742133 inputs to be properly biased to provide maximum performance. These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using the equation below. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

2nd Order Filter Typical Application

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the WS742133, as it can be used like a standard OPAMP. Several filter topologies can be implemented, both single-ended and differential. In Figure 5, a multi-feedback (MFB) with differential input and single-ended input is shown. An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc-gain to 1, helping reducing the output dc-offset to minimum. The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling capacitor.

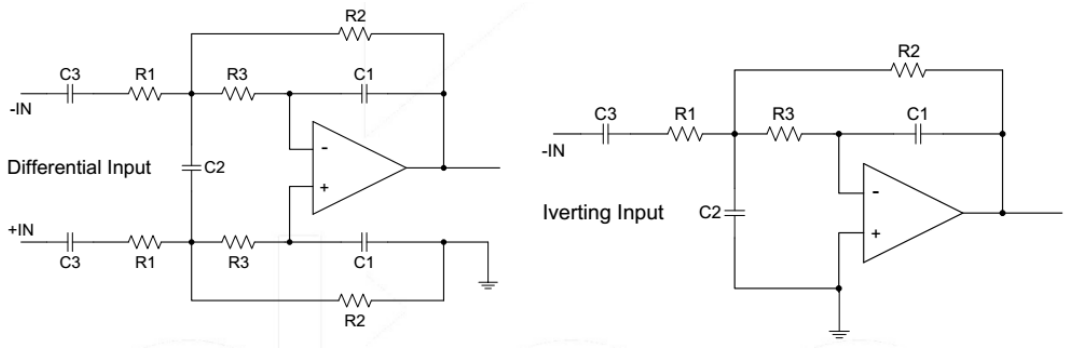


Figure 5. Second-Order Active Low-Pass Filter

Charge Pump Flying Capacitor and PVSS Capacitor

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR X5R or X7R capacitors are recommended selection, a value of typical 0.33μF is recommended for C_{PUMP}, and a value of typical 1μF is recommended for PVSS. Capacitor values can be smaller than the value recommended, but the maximum output voltage may be reduced and the device may not operate to specifications.

Decoupling Capacitors

The WS742133 requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) X5R or X7R ceramic capacitor, typically a combine of paralleled 0.1μF and 10μF, placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the WS742133 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10μF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

Pop-Free Power-Up

Pop-free power up is ensured by keeping the EN (shut down pin) low during power-supply ramp up and ramp down. The EN pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN pin high to achieve pop-less power up. Figure6 illustrates the preferred sequence.

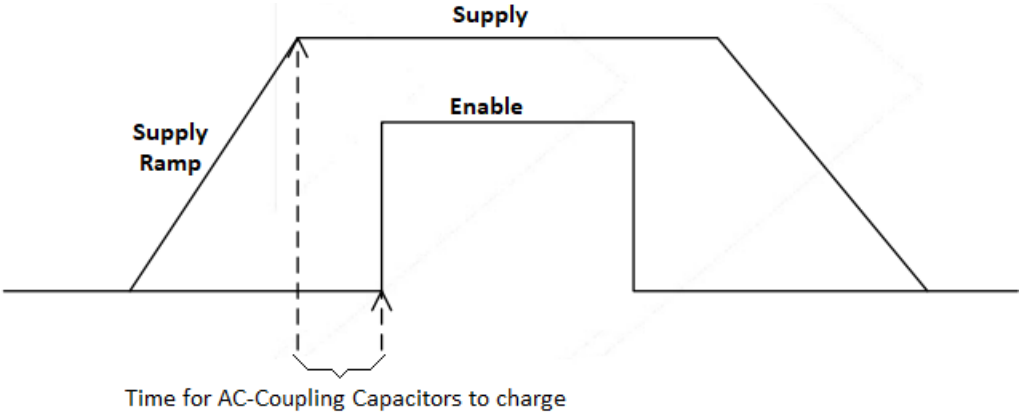
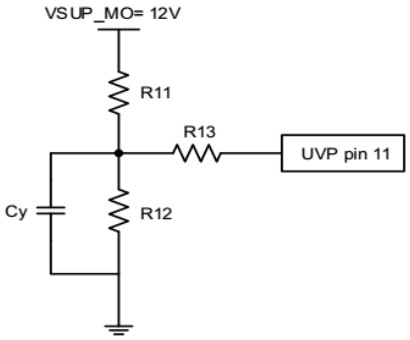


Figure 6. Power-Up Sequences

External Under-voltage Detection

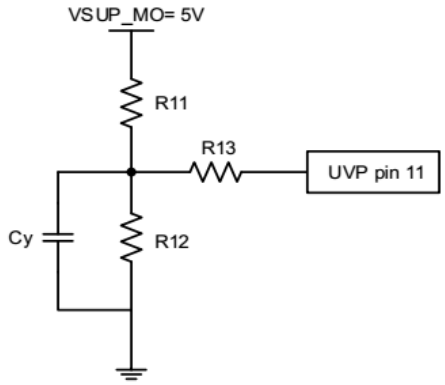
External under-voltage detection can be used to shut down the WS742133 before an input device can generate a pop noise. Although the shut down voltage is 1.21V, customers need to consider the accuracy of system passive components such as resistors and associated temperature variation. Users often select a resistor divider to obtain the power-on and shut down threshold for the specific application. The typical thresholds can be calculated as follows, respectively for VSUP_MO at 5V and 12V. Usually for best power down noise performance, 12V supply is recommended for UVP circuitry as below. Typically this 12V is the power supply which generates the 5V supply for WS742133 PVDD pins.

Case 1: VSUP_MO=12V (Recommended)



V_{UVP}=(1.21V-4.7μA*R13)*(R11+R12)/R12; $V_{hysteresis}$=4.7μA*R13*(R11+R12)/R12; With the condition R13>>R11//R12. For example, if R11=11k, R12=1.4k and R13=47k, then V_{UVP}=8.76V; $V_{hysteresis}$=1.957V. Here, V_{UVP} is the shut down threshold. In this case, the voltage at UVP pin 11 is greater than 1.431V under worst case of VSUP_MO ripples.

Case 2: VSUP_MO=5.0V



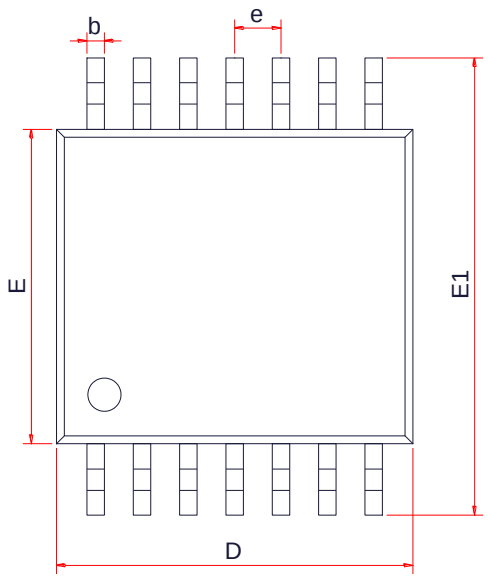
V_{UVP}=(1.21V-4.7μA*R13)*(R11+R12)/R12; $V_{hysteresis}$=4.7μA*R13*(R11+R12)/R12; With the condition R13>>R11//R12. For example, if R11=5.6k, R12=2.2k and R13=47k, then V_{UVP}=3.506V; $V_{hysteresis}$=0.783V. Here, V_{UVP} is the shut down threshold. In this case, the voltage at UVP pin 11 is greater than1.431V under worst case of VSUP_MO ripples.

Capacitive Load

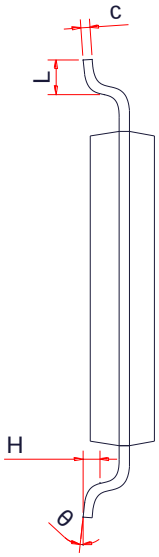
The WS742133 has the ability to drive a high capacitive load up to 220pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

PACKAGE OUTLINE DIMENSIONS

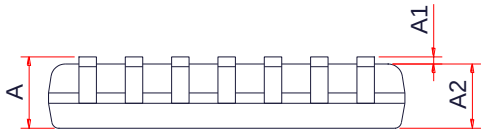
TSSOP-14L



TOP VIEW



SIDE VIEW

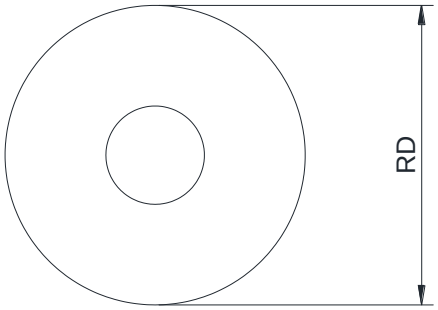


SIDE VIEW

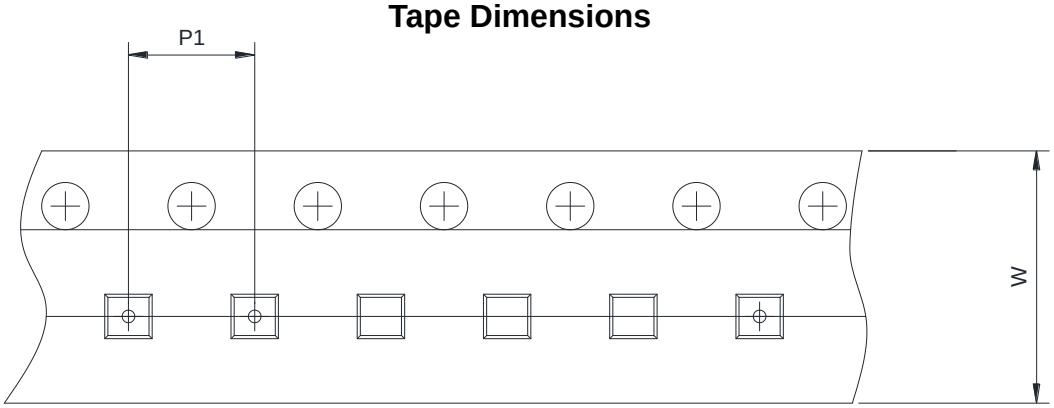
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	0.90	1.00
b	0.19	-	0.30
c	0.09	-	0.20
D	4.90	5.00	5.10
E	4.30	4.40	4.50
E1	6.25	6.40	6.55
e	0.65 BSC		
L	0.50	0.60	0.70
H	0.25Typ		
θ	1 °	-	7 °

TAPE AND REEL INFORMATION

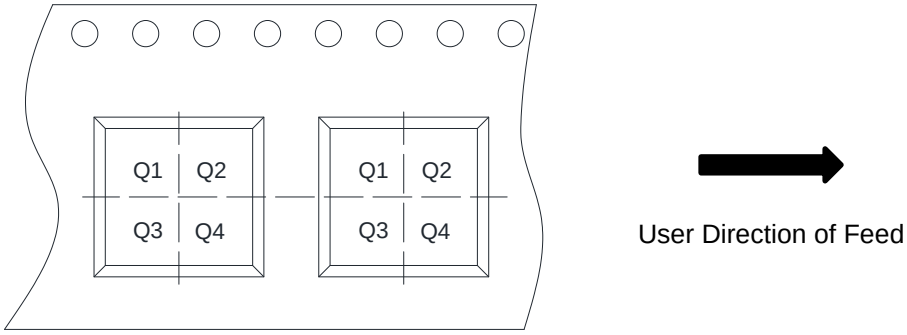
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☐ 7inch ☑ 13inch
W	Overall width of the carrier tape	☐ 8mm ☑ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☐ 4mm ☑ 8mm
Pin1	Pin1 Quadrant	☑ Q1 ☐ Q2 ☐ Q3 ☐ Q4