深圳市华远显示器件有限公司

SHENZHEN HUAYUAN DISPLAY CO.,LTD.

液晶显示模块规格书

Specification for Liquid Crystal Display Module

HYG16016076G-FF64L-VE

Prepared By	Reviewed By	Approved By
Date:	Date:	Date:

REVISION HISTORY

The following table tracks the history of the changes made to this document.

SN	Rev.	Content	Date	Design
1	R00	Origin Released	2013-08-06	

CONTENTS

1. 0 GENERAL DESCRIPTION

The HYG16016076G-FF64L-VE is a 160x160 dots dot-matrix LCD module. It has a FSTN panel composed of 160 segments and 160 commons. The LCM can be easily accessed by microcontroller via 8080 series interface.

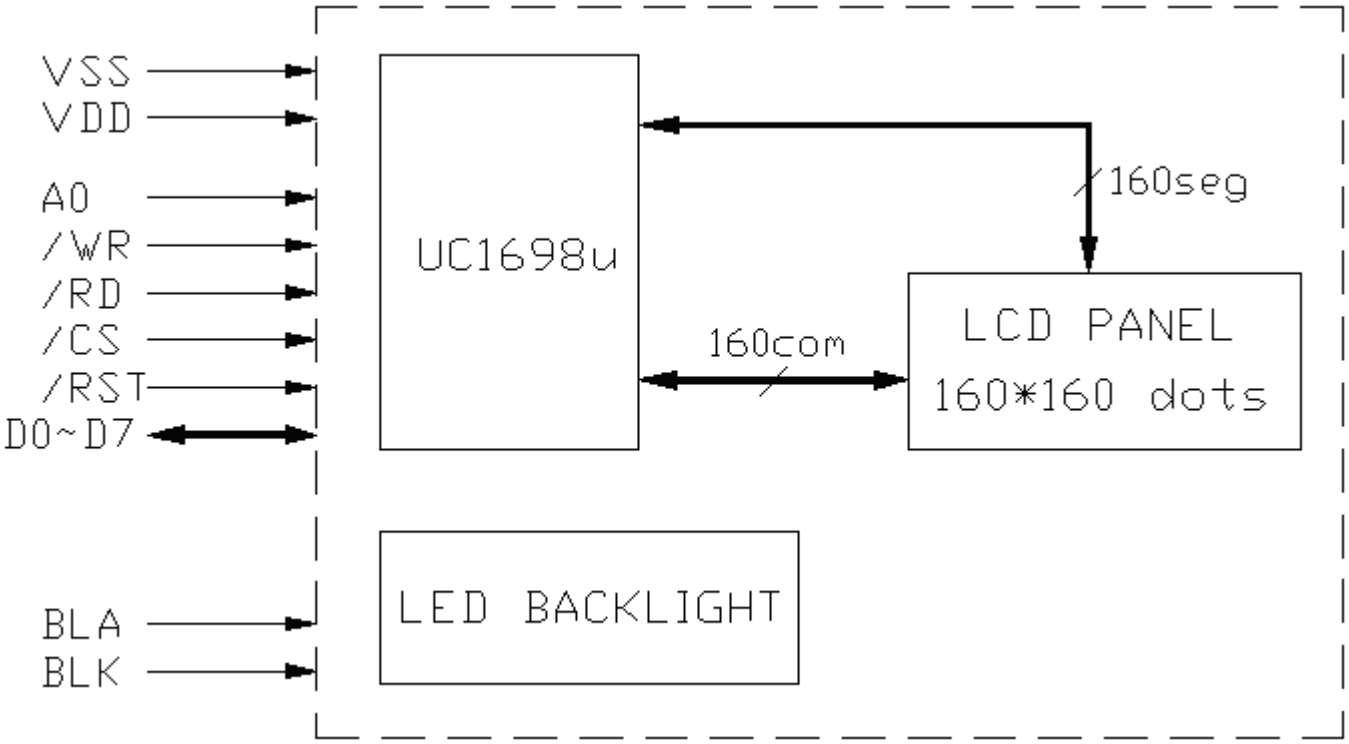
2. 0 FEATURES

Display Format	160 x 160 dots
LCD Type	FSTN-POSTIVE
Polarizer Mode	TRANSFLECTIVE
Drive Method	1/160 Duty, 1/10 Bias, Vop=16.5V
Viewing Direction	6 O'clock
Controller	UC1698u
Interface	8080 Series 8-Bit Parallel Interface
Backlight	White LED Backlight

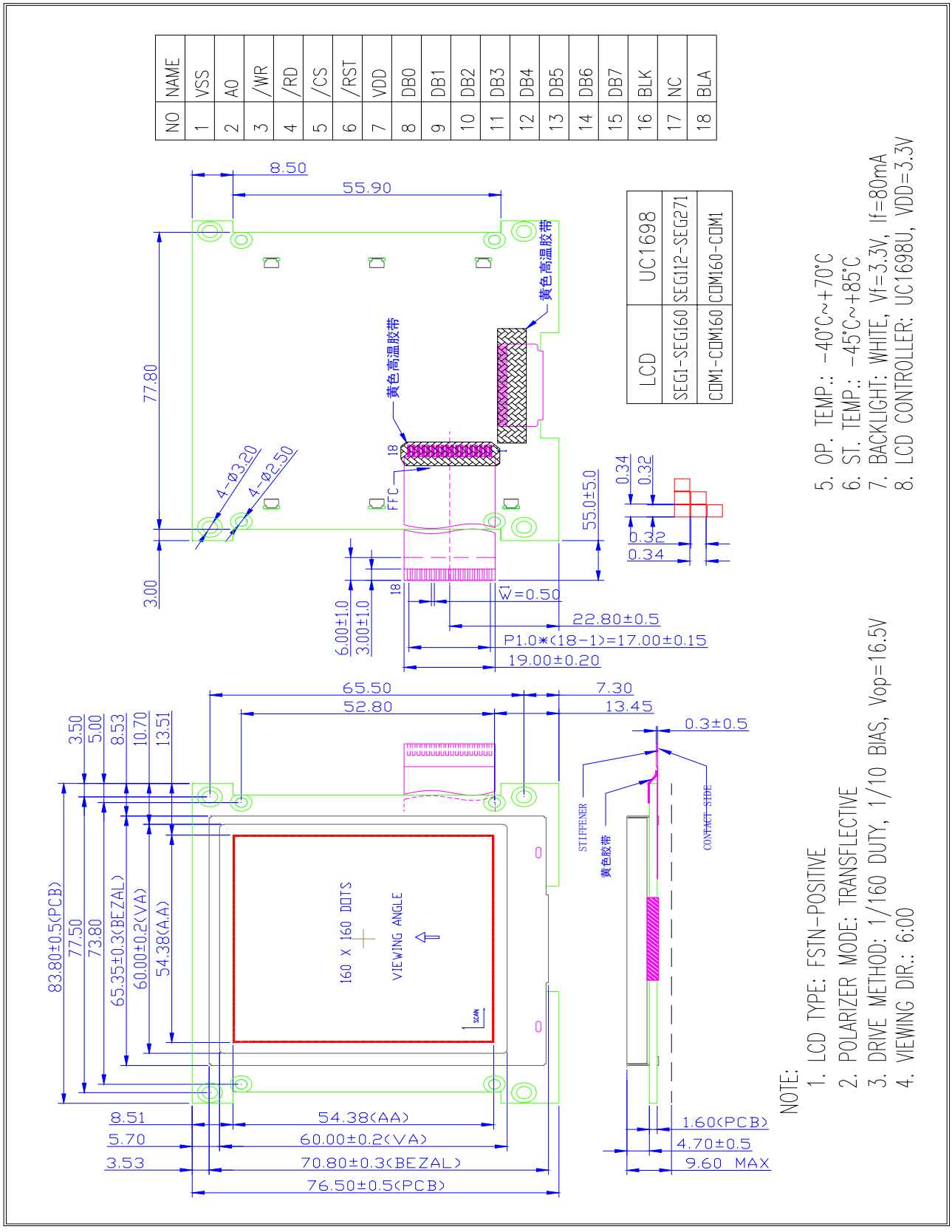
3. 0 MECHANICAL SPECIFICATION

Item	Description	Unit
Module Dimension	83.8(W) × 76.5(H) × 9.6(Max)(T)	mm
Viewing Area	60.0(W) × 60.0(H)	mm
Active Area	54.38(W) × 54.38(H)	mm
Dot Size	0.32(W) × 0.32(H)	mm
Dot Pitch	0.34(W) × 0.34(H)	mm
Character Size	——	mm

4. 0 BLOCK DIAGRAM



5. 0 EXTERNAL DIMENSIONS



6. 0 INTERFACE PIN DESCRIPTIONS

PIN No.	Symbol	Level	Description
1	V_{SS}	P	Power supply for logic(0V)
2	A0	H/L	Selects Control data or Display data for read/write operation. ”L”: Control data ”H”: Display data
3	/WR	H/L	Write operation when /WR=”L”
4	/RD	H/L	Read operation when /RD=”L”
5	/CS	H/L	Chip Select. Chip is selected when /CS =”L”
6	/RST	H/L	When /RST=”L”, all control registers are re-initialized by their default states.
7	V_{DD}	P	Power supply for logic(+3.3V)
8	D0	H/L	Data Bit 0
9	D1	H/L	Data Bit 1
10	D2	H/L	Data Bit 2
11	D3	H/L	Data Bit 3
12	D4	H/L	Data Bit 4
13	D5	H/L	Data Bit 5
14	D6	H/L	Data Bit 6
15	D7	H/L	Data Bit 7
16	BLK	P	Power supply for LED Backlight (0V)
17	NC	——	No Connection
18	BLA	P	Power supply for LED Backlight (+3.3V)

7. 0 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Supply Voltage (Logic)	V_{DD}-V_{SS}	-0.3	+4.0	V
Supply Voltage (LCD)	V_0-Vss	-0.3	+19.8	V
Input Voltage	VI	-0.4	V_{DD}+0.5	V
Operating Temperature	Topr	-40	+70	℃
Storage Temperature	Tstg	-45	+85	℃

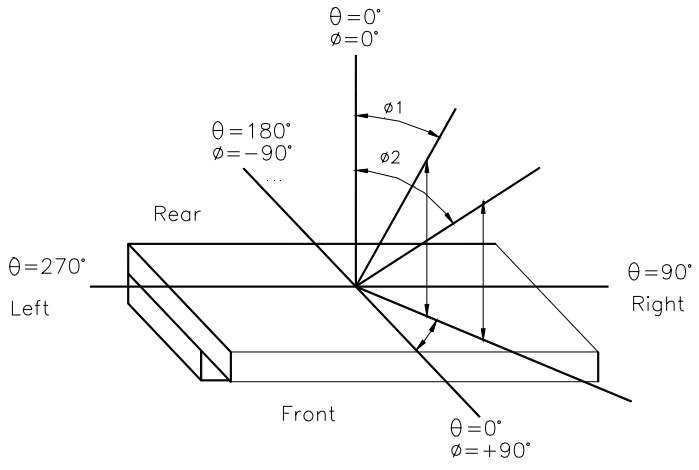
8. 0 ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply voltage for Logic	V_{DD}	--	3.0	3.3	3.5	V
LCD Operating Voltage	V_0-V_{SS}	-40℃				V
		+25℃	16.2	16.5	16.7	V
		+70℃				V
Input voltage H level	V_{IH}		0.8V_{DD}	---	V_{DD}	V
Input voltage L level	V_{IL}		0	---	0.2V_{DD}	V
Output High Voltage	V_{OH}		0.8V_{DD}	---	V_{DD}	V
Output Low Voltage	V_{OL}		0	---	0.2V_{DD}	V
Standby current	I_{SB}	VDD=3.3V	---	---	50	uA
Input leakage current	I_{IL}				1.5	uA

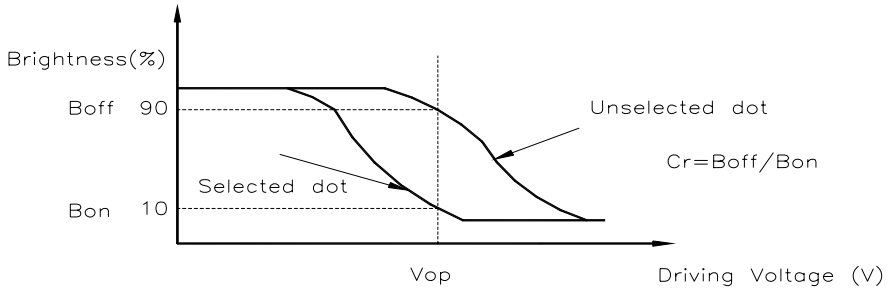
9. 0 OPTICAL CHARACTERISTICS

Item	Symbol	Condition		Min	Typ	Max	Unit
Response time	Ton	θ=0 ° and Ta=-40℃			--		ms
		θ=0 ° and Ta=+25℃			--		ms
		θ=0 ° and Ta=+70℃			--		ms
	Toff	θ=0 ° and Ta=-40℃			--		ms
		θ=0 ° and Ta=+25℃			--		ms
		θ=0 ° and Ta=+70℃			--		ms
Contrast ration	CR(MAX)	Ta=25℃		5	10		---
Viewing Angle	Ø	Deg θ=0 °	CR≥2.0 Ta=25℃		50		Deg
		Deg θ=90 °			35		
		Deg θ=180 °			30		
		Deg θ=270 °			35		
Crosstalk		Ta=25℃			1.2		---

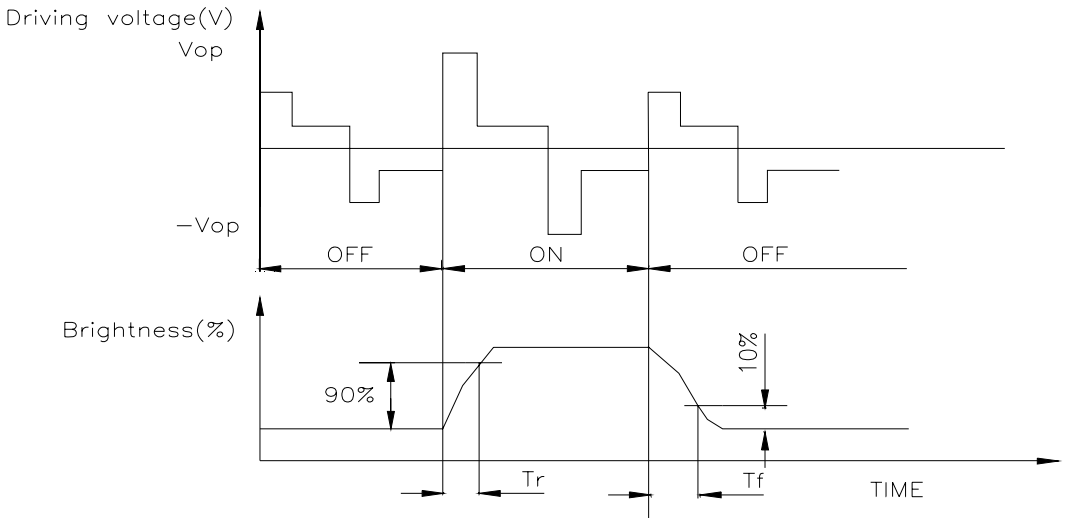
9.1 Viewing Angle θ , Ø and Viewing Angle Range: Δ Ø =|Ø2-Ø1|



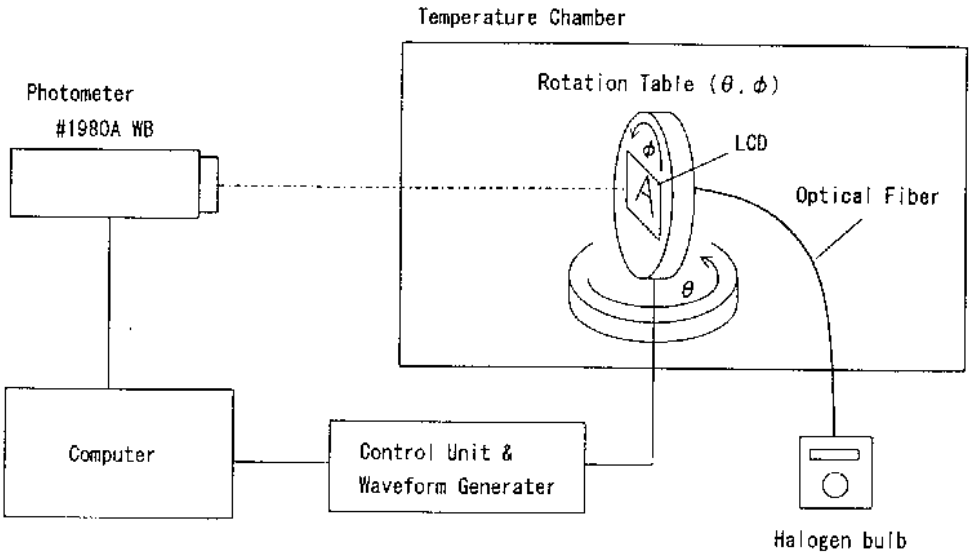
9.2 Contrast ratio(CR)



9.3 Response Time

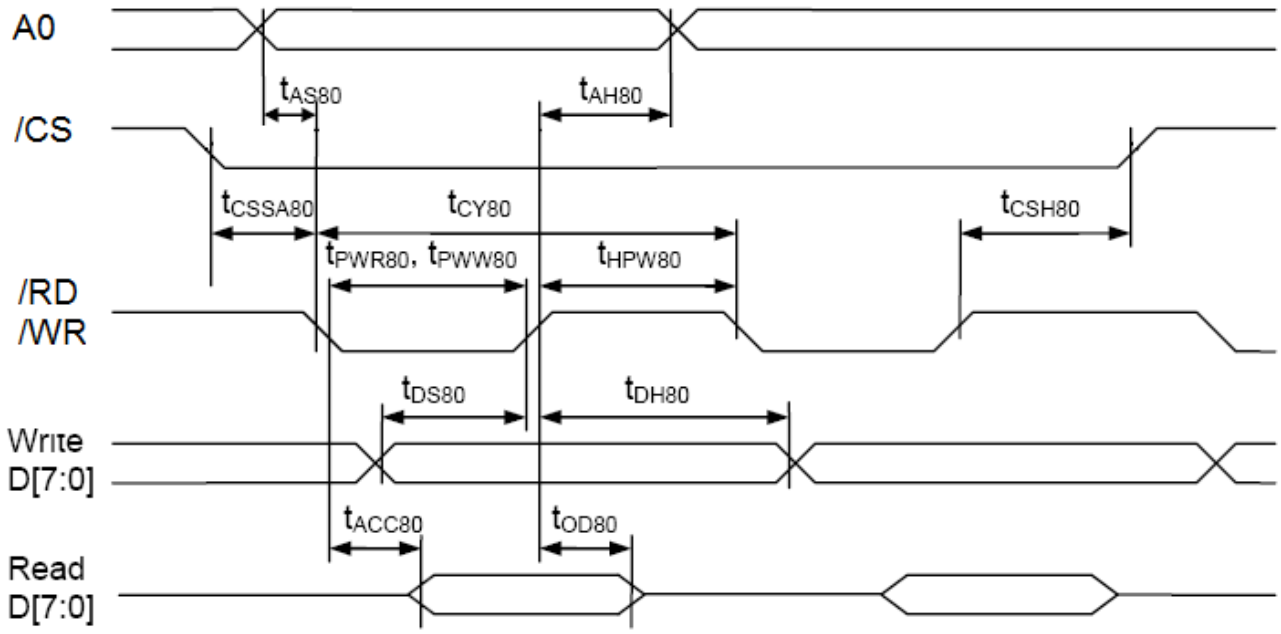


9.4 Optical Measurement System



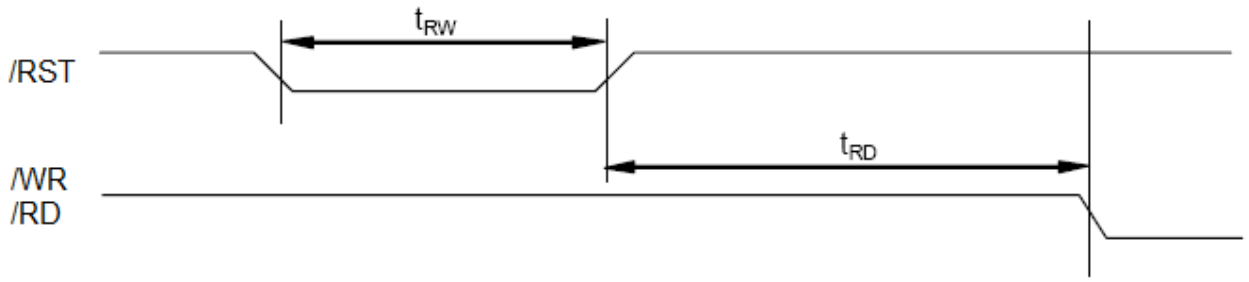
10. 0 TIMING CHARACTERICS

10.1 Microcontroller interface timing for writing (8080)



Symbol	Signal	Description		Condition	Min.	Max.	Units
tAS80 tAH80	A0	Address setup time Address hold time			0 0	–	nS
tCY80		System cycle time	(read) (write)	LC[7:6]=10b LC[7:6]=01b	100 80 90	–	nS
tPWR80	/RD	Pulse width			50	–	nS
tPWW80	/WR	Pulse width		LC[7:6]=10b LC[7:6]=01b	40 45	–	nS
tHPW80	/WR /RD	High pulse width	(read) (write)	LC[7:6]=10b LC[7:6]=01b	50 40 45	–	nS
tDS80 tDH80	D0~D7	Data setup time Data hold time			30 0	–	nS
tACC80 tOD80		Read access time Output disable time		CL = 100pF	– 15	60 30	nS
tCSSA80 tCSH80	/CS	Chip select setup time			5 5		nS

10.2 Reset timing



Symbol	Signal	Description	Condition	Min.	Max.	Units
tRW	RST	Reset low pulse width		3	–	μS
tRD	RST, /WR, /RD	Reset to WR pulse delay		10	–	mS

11. 0 BACKLIGHT CHARACTERISTICS

11.1 ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

Item	Symbol	Condition	Rating	Unit
Reverse Voltage	Vr		5.0	V
Absolute maximum forward current	Ifm		100	mA
Forward Current	If		80	mA
Power Description	Pd		240	mW
Operating temperature range	Topr		-40~+70	^{0}C
Storage temperature range	Tst		-45~+85	^{0}C

11.2 ELECTRICAL/OPTLCAL CHARACTERISTICS

(Ta=25℃)

Item	Symbol	Min	Typ	Max	Unit	Condition
Forward Voltage	Vf	3.2	3.3	3.5	V	If=80mA
Reverse Current	Ir		40		uA	Vr=5.0V
Dominant wave length	λp				nm	If=80mA
Spectral Line Half width	Δ λ					If=80 mA
Luminance	Lv				cd/㎡	If=80 mA
Color Coordinate	X		White			If= 80mA
	Y					

12. 0 OPERATING PRINCIPLES & METHODS

12.1 LCD VOLTAGE SETTING

- **MULTIPLEX RATES**

Multiplex Rate is completely software programmable in UC1698u via registers CEN, DST, DEN, FLT, FLB, and partial display control flags LC[8] and LC[0].

Combined with low power partial display mode and a low bias ratio of 6, UC1698u can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

- **BIAS RATIO SELECTION**

UC1698u supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	5	10	11	12

Table 1: Bias Ratios

- **TEMPERATURE COMPENSATION**

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ℃	-0.00	-0.05	-0.15	-0.25

Table 2: Temperature Compensation

- **VLCD GENERATION**

VLCD may be supplied either by internal charge pump or by external power supply. The source of VLCD is controlled by PC[1].

When VLCD is generated internally, the voltage level of VLCD is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and TC (Temperature Compensation), with the following relationship:

$$V_{LCD}=(C_{V0}+C_{PM}\times PM)\times(1+(T-25)\times C_T\%)$$

where

CV0 and CPM are two constants, whose value depends on the setting of BR register;

PM is the numerical value of PM register;

T is the ambient temperature in ℃, and;

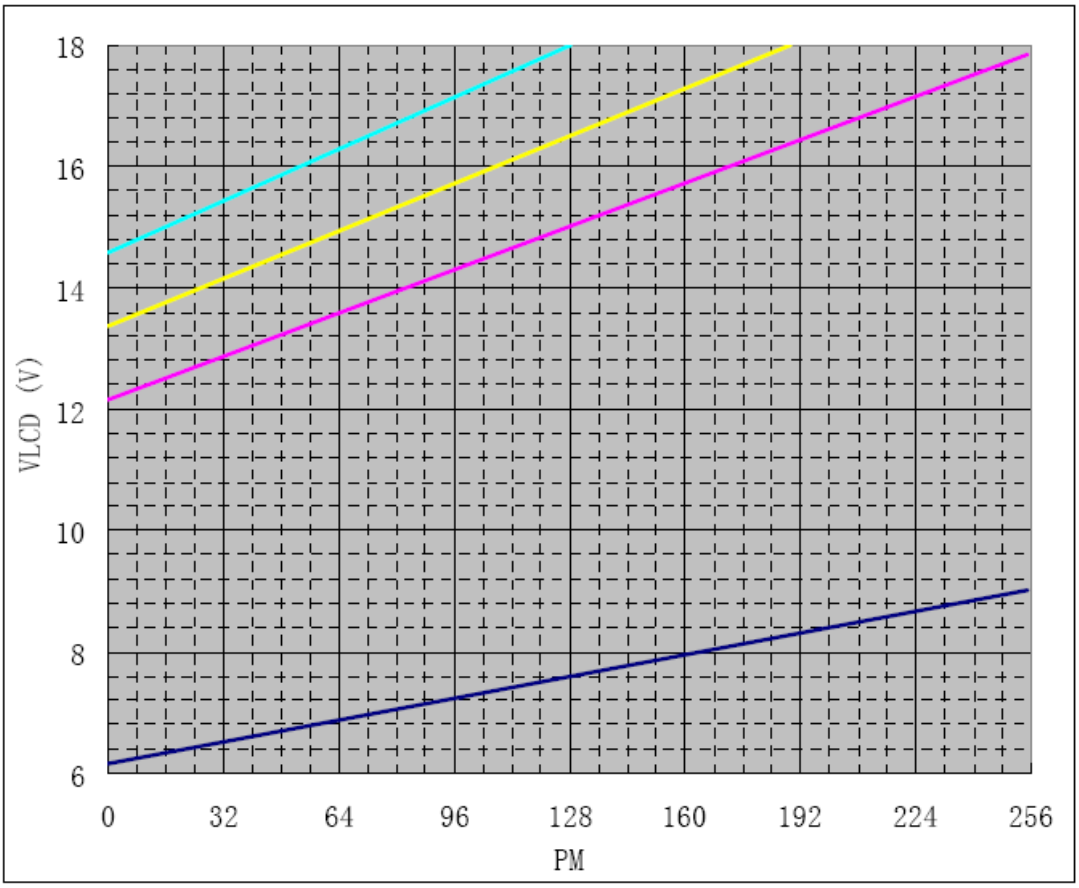
CT is the temperature compensation coefficient as selected by TC register.

- **VLCD AND CONTRAST FINE TUNING**

LCD is sensitive to even a 0.5% mismatch between IC driving voltage and the VOP of LCD. It is very difficult for LCD makers to guarantee such high precision matching of parts from different venders.

It is therefore necessary to adjust VLCD to precisely match the actual VOP of each LCD.

V_{LCD} QUICK REFERENCE



BR	CV0 (V)	CPM (mV)	PM_reg	VLCD (V)
5	6.154	11.22	0	6.154
			255	9.015
10	12.157	22.26	0	12.157
			255	17.833
11	13.369	24.45	0	13.369
			189	17.991
12	14.580	26.61	0	14.580
			128	17.986

12.2 DISPLAY DATA MEMORY

Row Adderss	RAM	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H		COM1	COM17	COM160	COM16
01H		COM2	COM18	COM159	COM15
02H		COM3	COM19	COM158	COM14
03H		COM4	COM20	COM157	COM13
04H		COM5	COM21	COM156	COM12
05H		COM6	COM22	COM155	COM11
06H		COM7	COM23	COM154	COM10
07H		COM8	COM24	COM153	COM9
08H		COM9	COM25	COM152	COM8
09H		COM10	COM26	COM151	COM7
0AH		COM11	COM27	COM150	COM6
0BH		COM12	COM28	COM149	COM5
0CH		COM13	COM29	COM148	COM4
0DH		COM14	COM30	COM147	COM3
0EH		COM15	COM31	COM146	COM2
0FH		COM16	COM32	COM145	COM1
10H		COM17	COM33	COM144	COM160
11H		COM18	COM34	COM143	COM159
12H		COM19	COM35	COM142	COM158
13H		COM20	COM36	COM141	COM157
14H		COM21	COM37	COM140	COM156
15H		COM22	COM38	COM139	COM155
16H		COM23	COM39	COM138	COM154
17H		COM24	COM40	COM137	COM153
18H		COM25	COM41	COM136	COM152
19H		COM26	COM42	COM135	COM151
1AH		COM27	COM43	COM134	COM150
1BH		COM28	COM44	COM133	COM149
1CH		COM29	COM45	COM132	COM148
88H		COM137	COM153	COM24	COM40
89H		COM138	COM154	COM23	COM39
8AH		COM139	COM155	COM22	COM38
8BH		COM140	COM156	COM21	COM37
8CH		COM141	COM157	COM20	COM36
8DH		COM142	COM158	COM19	COM35
8EH		COM143	COM159	COM18	COM34
8FH		COM144	COM160	COM17	COM33
90H		COM145	COM1	COM16	COM32
91H		COM146	COM2	COM15	COM31
92H		COM147	COM3	COM14	COM30
93H		COM148	COM4	COM13	COM29
94H		COM149	COM5	COM12	COM28
95H		COM150	COM6	COM11	COM27
96H		COM151	COM7	COM10	COM26
97H		COM152	COM8	COM9	COM25
98H		COM153	COM9	COM8	COM24
99H		COM154	COM10	COM7	COM23
9AH		COM155	COM11	COM6	COM22
9BH		COM156	COM12	COM5	COM21
9CH		COM157	COM13	COM4	COM20
9DH		COM158	COM14	COM3	COM19
9EH		COM159	COM15	COM2	COM18
9FH		COM160	COM16	COM1	COM17

MX	SEG1	SEG2	SEG3	SEG4	SEG5			SEG380	SEG381	SEG382	SEG383	SEG384
0												
1	SEG382	SEG383	SEG384	SEG379	SEG380			SEG5	SEG6	SEG1	SEG2	SEG3

Example for memory mapping: let MX = 0, MY = 0, SL = 0, LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color), according to the data shown in the above table (R: 11111b, G: 111111b, B: 11111b):

⇒ 1st Byte write data: 11111111b

⇒ 2nd Byte write data: 11111111b

12.3 CONTROL REGISTERS

The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands,

Name: The Symbolic reference of the register.Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in Bold font are default values after Power-Up-Reset and System-Reset.

Name	Bits	Default	Description
SL	8	0H	Scroll Line. Scroll the displayed image up by SL rows. The valid SL value is between 0 (for no scrolling) and (159 – 2x(FLT+FLB)). Setting SL outside of this range causes undefined effect on the displayed image.
FLT	4	0H	Fixed Lines. The first FLTx2 lines and the last FLBx2 lines (relative to CEN)
FLB	4	0H	of each frame are fixed and are not affected by scrolling (SL). When FLT and/or FLB are non-zero, the screen is effectively separated into three regions: one scrollable, surrounded by two non-scrollable regions. When partial display mode is activated, the display of these 2xFLT and 2xFLB lines is also controlled by LC[0]. When LC[0]=1, the display will have three sections: 2xFLT on one side non-scrollable, 2xFLB on the other side also non-scrollable, and scrollable DST~DEN in the middle.
CA	7	0H	Display Data RAM Column Address (counted in RGB triplet) (Used in Host to Display Data RAM access)
RA	8	0H	Display Data RAM Row Address (Used in Host to Display Data RAM access)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_{BIAS}. 00b: 5 01b: 10 10b: 11 **11b: 12**
TC	2	0H	Temperature Compensation (per ℃) **00b: -0.00%** 01b: -0.05% 10b: -0.15% 11b: -0.25%
PM	8	40H	Electronic Potentiometer to fine tune V_{BIAS} and V_{LCD}
PMO	7	00H	PM offset. PMO[6]=1b: The effective PM value, PMV = PM - PMO[5:0] PMO[6]=0b: The effective PM value, PMV = PM + PMO[5:0]
PC	2	2H	Power Control. PC[0]: **0b: LCD ≦ 13nF** 1b: 13nF < LCD≦22nF PC[1]: 0b: External VLCD **1b: Internal VLCD (10x charge pump)**

Continued

Name	Bits	Default	Description
AC	4	1H	Address Control. AC[0]: WA: Automatic column/row Wraparound (Default **1 : ON**) AC[1]: Auto-Increment order **0b : Column (CA) first** 1b : Row (RA) first AC[2]: RID: RA (row address) Auto Increment Direction **(L : +1** H : -1) AC[3] : Window Program Mode **0b : Inside Mode:** Write to SRAM within the window defined by (WPC0,WPP0) and (WPC1,WPP1) 1b : Outside Mode: Write to SRAM but skip the window defined by (WPC0,WPP0) and (WPC1,WPP1)
DC	5	18H	Display Control: DC[0]: PXV: Pixels Inverse. Bit-wise data inversion. (Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) DC[3]: Gray-shade Modulation mode. 0 : On/Off mode **1 : 32-shade Mode** DC[4]: Green Enhance Mode. Only valid in 4K-color mode. 0 : Enable. Allows an extra display bit for green color. **1 : Disable**
LC	9	090H	LCD Control: LC[0]: Enable the top FLTx2 and bottom FLBx2 lines in partial display mode (Default **0: OFF**). LC[1]: MX, Mirror X. SEG/Column sequence inversion (Default: **0: OFF**) LC[2]: MY, Mirror Y. COM/Row sequence inversion (Default: **0: OFF**) LC[4:3]: Line Rate (Klps: Kilo-Line-per-second) 00b: 25.2. Klps 01b: 30.5 Klps **10b: 37.0 Klps** 11b: 44.8 Klps Line Rate (for On/Off mode) 00b: 8.5 Klps 01b: 10.4 Klps **10b: 12.6 Klps** 11b: 15.2 Klps (Line-Rate = Frame-Rate x Mux-Rate) LC[5] : RGB filter order (as mapped to SEG1, SEG2, SEG3) **0 : BGR-BGR** 1 : RGB-RGB LC[7:6] : Color and input mode when DC[4]=1: 01b : 4K color mode. 4R-4G-4B (12-bit/RGB) **10b : 64K color mode. 5R-6G-5B (16-bit/RGB)** when DC[4]=0: 01b : 4K color mode. 4R-5G-3B (12-bit/RGB) 10b : 64K color mode. 5R-6G-5B (16-bit/RGB) LC[8] : Partial Display Control **0b: Disable Mux-Rate = CEN+1 (DST, DEN not used)** 1b: Enabled Mux-Rate = DEN-DST+1+LC[0] x (FLT+FLB) x 2

Continued

Name	Bits	Default	Description
NIV	5	1DH	N-Line Inversion: NIV[2:0]: 000b: 11 lines 001b: 19 lines 010b: 21 lines 011b: 25 lines 100b: 29 lines **101b: 31 lines** 110b: 37 lines 111b: 43 lines NIV[3]: 0b: no-XOR **1b: XOR** NIV[4]: 0b: Disable NIV **1b: Enable NIV**
CSF	3	0H	COM Scan Function CSF[0]: Interlace Scan Function **0b: LRM sequence: AEBCD-AEBCD** 1b: LRM sequence: AEBCD-EBCDA CSF[1]: FRC function **0: Disable FRC** 1: Enable FRC CSF[2]: Shade-1 / Shade-30 option **0: Dither directly on input data (SRAM Change)** 1: PWM (Pulse-width modulation) on SEG output stage
CEN DST DEN	8 8 8	9FH 00H 9FH	COM scanning end (last COM with full line cycle, 0 based index) Display start (first COM with active scan pulse, 0 based index) Display end (last COM with active scan pulse, 0 based index) Please maintain the following relationship: CEN = the actual number of pixel rows on the LCD - 1 CEN≥ DEN ≥ DST+ 9
WPC0	7	00H	Window program starting column address. Value range: 0 ~127.
WPP0	8	00H	Window program starting row address. Value range: 0~159.
WPC1	7	7FH	Window program ending column address. Value range: 0~127.
WPP1	8	9FH	Window program ending row address. Value range: 0~159
MTPC	5	10H	MTP Programming Control: MTPC[2:0] : MTP command **000 : Idle** 001 : Read 010 : Erase 011 : Program 1xx : For UltraChip's debug use only MTPC[3] : MTP Enable (automatically cleared after each MTP command) MTPC[4] : Ignore/Use MTP. 0: Ignore **1: Use**
MTP	7	--	Multiple-Time Programming. For VLCD fine tune.

Continued

Name	Bits	Default	Description
MTPID	2	--	Multiple-Time Programming. For LCM manufacturer's configuration.
MTPM	7	00H	MTP Write Mask. Bit =1: program, Bit=0: no action.
MTPM1	2	0H	MTP Write Mask. Bit =1: program, Bit=0: no action.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
MD	1	–	MTP option flag: 1 for MTP version, 0 for non-MTP version.
MS	1	–	MTP programming in-progress
WS	1	–	MTP Operation Succeeded
ID	2	PIN	Access the connected status of ID pins.

13. 0 INSTRUCTION DESCRIPTION

13.1 INSTRUCTION TABLE

	Command	A0	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status & PM	0	1	GE	MX	MY	WA	DE	WS	MD	MS		
				VER	PMO[6:0]								
				Product Code(8h)				PID[1:0		MID[1:0]			
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	0	#	#	#	Set CA[6:4]	0
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	0
6	Set Power Control	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Adv. Program Control (double-byte command)	0 0	0 0	0 #	0 #	1 #	1 #	0 #	0 #	0 #	R #	Set APC[R][7:0], R = 0 or 1	N/A
8	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0
	Set Scroll Line MSB	0	0	0	1	0	1	#	#	#	#	Set SL[7:4]	0
9	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	0
	Set Row Address MSB	0	0	0	1	1	1	#	#	#	#	Set RA[7:4]	0
10	Set V_{BIAS} Potentiometer (double-byte command)	0	0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set PM[7:0]	40H
11	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[8]	0
12	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13	Set Fixed Lines	0	0	1 #	0 #	0 #	1 #	0 #	0 #	0 #	0 #	Set {FLT, FLB}	0
14	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	10b
15	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0
16	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0
17	Set Display Enable	0	0	1	0	1	0	1	#	#	#	Set DC[4:2]	110b
18	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	0

Continued

	Command	A0	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
19	Set N-Line Inversion	0	0	1 -	1 -	0 -	0 #	1 #	0 #	0 #	0 #	Set NIV[4:0]	1DH
20	Set Color Pattern	0	0	1	1	0	1	0	0	0	#	Set LC[5]	0 (BGR)
21	Set Color Mode	0	0	1	1	0	1	0	1	#	#	Set LC[7:6]	10b
22	Set COM Scan Function	0	0	1	1	0	1	1	#	#	#	Set CSF[2:0]	000b
23	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
24	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
25	Set Test Control (double-byte command)	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
26	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 12
27	Set COM End	0	0	1 -	1 #	1 #	1 #	0 #	0 #	0 #	1 #	Set CEN[6:0]	159
28	Set Partial Display Start	0	0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	0 #	Set DST[6:0]	0
29	Set Partial Display End	0	0	1 -	1 #	1 #	1 #	0 #	0 #	1 #	1 #	Set DEN[6:0]	159
30	Set Window Program Starting Column Address	0	0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Set WPC0	0
31	Set Window Program Starting Row Address	0	0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #	Set WPP0	0
32	Set Window Program Ending Column Address	0	0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	0 #	Set WPC1	127
33	Set Window Program Ending Row Address	0	0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #	Set WPP1	159
34	Window Program Mode	0	0	1	1	1	1	1	0	0	#	Set AC[3]	0: Inside

Note:

A0 : 0: Control, 1: Data

W/R: 0: Write Cycle, 1: Read Cycle

#: Useful Data bits –: Don't Care

13.2 DESCRIPTION OF INSTRUCTION

(1) WRITE DATA TO DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data written to SRAM							

UC1698u will convert input RAM data to 16-bit of RGB data. Please refer to command ***Set Color Mode*** for detail of data-write sequence.

(2) READ DATA FROM DISPLAY MEMORY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data read from SRAM							

Each RGB triplet is stored as 16-bit in the display RAM. Each 16-bit of RGB data takes 1 (/ 2) RAM read cycles for 16 (/ 8) –bit bus mode, respectively. The read out RGB data is after-extension for 64K color mode.

R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
1st 8-bit Read								2nd 8-bit Read							

Write/Read Data Byte (commands (1) and (2)) operation uses internal Row Address register (RA) and Column Address register (CA). RA and CA can be programmed by issuing commands ***Set Row Address*** and ***Set Column Address.*** If wrap-around (WA, AC[0]) is OFF (0), CA will stop incrementing after reaching the CA boundary, and system programmers need to set the values of RA and CA explicitly. If WA is ON (1), when CA reaches end of column address, CA will be reset to 0 and RA will be increased or decreased, depending on the setting of Row Increment Direction (RID, AC[2]). When RA reaches the boundary of RAM (i.e. RA = 0 or 127), RA will be wrapped around to the other end of RAM and continue.

(3) GET STATUS &PM

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	1	0	GE	MX	MY	WA	DE	WS	MD	MS
			VER	PMO[6:0]						
			Product Code(8h)				PID[1:0		MID[1:0]	

Status1 definitions:

GE : Green Enhancing enable flag. Green Enhance Mode is disabled when GE = 1.

MX : Status of register LC[1], mirror X.

MY : Status of register LC[2], mirror Y.

WA : Status of register AC[0]. Automatic column/row wrap around.

DE : Display enable flag. DE=1 when display is enabled

WS : MTP Operation succeeded

MD : MTP Option (1 for MTP version, 0 for non-MTP version)

MS : MTP action status

Status2 definitions:

Ver : IC Version Code. 0 or 1.

PMO[6:0] : PM offset value.

Status3 definitions:

Product Code : 1000b (8h)

PID[1:0] : Provide access to ID pins connection status.

MID[1:0] : LCM manufacturer's configuration.

If multiple Get Status commands are issued consecutively within one single CD 1□0□1 transaction, the Get Status command will return {Status1, Status2, Status3, Status1, Status2, Status3, Status1..} alternately.

(4) SET COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	0	0	0	0	CA3	CA2	CA1	CA0
Set Column Address MSB CA[6:4]	0	0	0	0	0	1	0	CA6	CA5	CA4

Set SRAM column address for read/write access. CA is counted in RGB triplets, not individual SEG electrode.

CA value range: 0~127

(5) SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	0	0	1	0	0	1	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b = -0.00%/oC 01b = -0.05%/oC 10b = -0.15%/oC 11b = -0.25%/oC

(6) SET POWER CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[1:0]	0	0	0	0	1	0	1	0	PC1	PC0

Set PC[0] according to the capacitance loading of LCD panel.

Panel loading definition: 0b : LCD 13nF 1b : 13nF < LCD≤22nF

Set PC[1] to program the build-in charge pump stages. Before changing PC[1] value, always ensure the IC is in a RESET state. Avoid changing PC[1] when the display is enabled.

Pump control definition: 0b = External VLCD **1b = Internal VLCD (x10)**

(7) SET ADVANCED PROGRAM CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[R][7:0]	0	0	0	0	1	1	0	0	0	R
(Double-byte command)	0	0	APC register parameter							

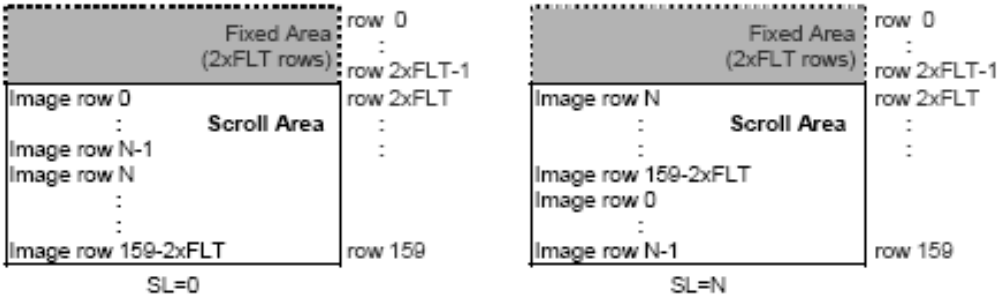
For UltraChip only. Please do NOT use.

(8) SET SCROLL LINE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line LSB SL[3:0]	0	0	0	1	0	0	SL3	SL2	SL1	SL0
Set Scroll Line MSB SL[7:4]	0	0	0	1	0	1	SL7	SL6	SL5	SL4

Set the scroll line number.

Scroll line setting will scroll the displayed image up by SL rows. The valid value for SL is between 0 (no scrolling) and 159-2x(FLT+FLB) (full scrolling). FLT and FLB are the register values programmed by the ***Set Fixed Lines*** command.



(9) SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address LSB RA [3:0]	0	0	0	1	1	0	RA3	RA2	RA1	RA0
Set Row Address MSB RA [7:4]	0	0	0	1	1	1	RA7	RA6	RA5	RA4

Set SRAM row address for read/write access. Possible value = 0~159

(10) SET V_{BIAS} POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0]	0	0	1	0	0	0	0	0	0	1
(Double-byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD Voltage Setting for more detail. Effective range: 0 ~ 255

(11) SET PARTIAL DISPLAY CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC[8]	0	0	1	0	0	0	0	1	0	LC8

This command is used to enable partial display function.

LC[8] : **0b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)**

1b: Enable Partial Display, Mux-Rate = DEN-DST+1+ LC[0]x(FLT+FLB)x2

(12) SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	1	0	0	0	1	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic column/row wrap around.

0: CA or RA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary

1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increment by one step.

AC[1]: Auto-Increment order

0 : column (CA) increment (+1) first until CA reaches CA boundary, then RA will increment by (+/-1).

1 : row (RA) increment (+/-1) first until RA reach RA boundary, then CA will increment by (+1).

AC[2]: RID, row address (RA) auto increment direction (0/1 = +/- 1)

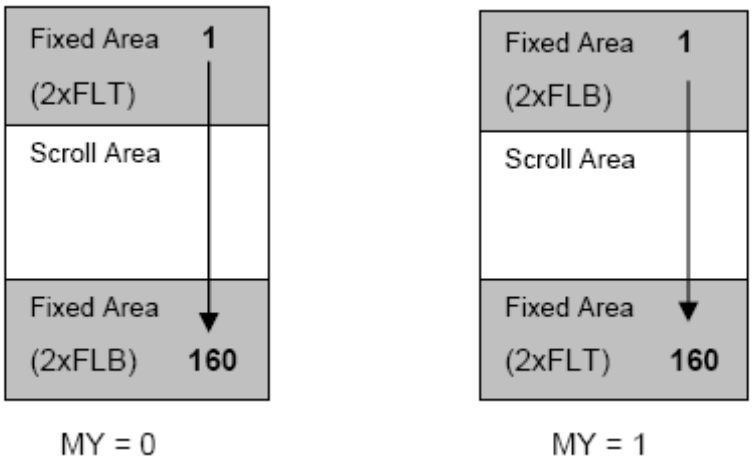
When WA=1 and CA reaches CA boundary, RID controls whether row address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. For Window Program mode (AC[3]=ON), see section Command Description (32) ~ (35) for more details. If WPC[1:0] and WPP[1:0] values are the default values, the behavior of CA, RA auto-increment will be the same, no matter what the setting of AC[3] is.

(13) SET FIXED LINES

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines {FLT,FLB}	0	0	1	0	0	1	0	0	0	0
(Double-byte command)	0	0	FLT[3:0]				FLB[3:0]			

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. The Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFLT and bottom 2xFLB rows for mirror Y (MY) is 0, or covers the top 2xFLB and bottom 2xFLT rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



When partial display mode is activated, the display of these 2x(FLT+FLB) lines is also controlled by LC[0]. Before turning on LC[0], ensure:

MY=0 DST FLTx2 MY=1 DST FLBx2 DEN (CEN-FLBx2). DEN (CEN-FLTx2)

(14) SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	1	0	1	0	0	0	LC4	LC3

Program LC [4:3] for line rate setting (Frame-Rate = Line-Rate / Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 108, 80, 56, and 40.

The following are line rates at Mux Rate = 109 ~ 160.

00b: 25.2 Klps 01b: 30.5 Klps **10b:37.0 Klps** 11b: 44.8 Klps

In On/Off Mode

00b: 8.5 Klps 01b: 10.4 Klps **10b: 12.6 Klps** 11b: 15.2 Klps

(Klps: Kilo-Line-per-second)

(15) SET ALL PIXEL ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	1	0	1	0	0	1	0	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM

(16) SET INVERSE DISPLAY

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	1	0	1	0	0	1	1	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

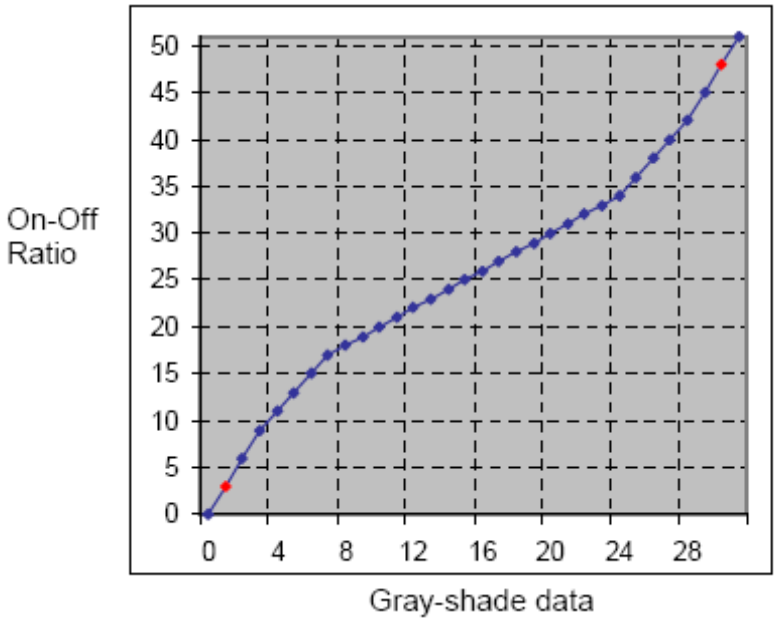
(17) SET DISPLAY ENABLE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC [4:2]	0	0	1	0	1	0	1	DC4	DC3	DC2

This command is for programming register DC[4:2].

When DC[2] is set to **0**, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1698u will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

DC[3] controls the gray shade modulation modes. UC1698u has two gray shade modulation modes: an On/Off mode and a 32-shade mode. The modulation curves are shown below. Horizontal axes are the gray shade data. The vertical axes are the ON-OFF ratio.



DC[4] Green Enhance Mode. Refer to command Set Color Mode for more information.

0b: Green Enhancing Mode enabled **1b: Green Enhancing Mode disabled**

NOTE:

For red and blue colors, when PWM is off, the shades mapped to data 1 and 30 (shown as red points above) are achieved by special dithering. When PWM is on, these shades are produced by PWM.

Green shades are created by combining FRC (default: Off) and special dithering. When PWM is off, six of the shades (1, 2, 3, 59, 60, and 61) are created by special dithering while they are created by PWM when PWM is on. Data 62 and 63 are mapped to the same shade.

When the internal DC-DC converter starts to operate and pump out current to VLCD, there will be an inrush pulse current between VDD2 and VSS2 initially. To avoid this current pulse from causing potential harmful noise, do NOT issue any command or write any data to UC1698u for 5~10mS after setting DC[2] to 1.

(18) SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	1	1	0	0	0	MY	MX	LC0

This command is used for programming LC[2:0] to control COM (row) mirror (MY), SEG (column) mirror (MX).

LC[2] controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by the MY action. MY will have immediate effect on the display image.

LC[1] controls Mirror X (MX): MX is implemented by selecting the CA or 127-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

LC[0] controls whether soft icon sections (2xFLT, 2xFLB) are displayed during partial display mode.

(19) SET N-LINE INVERSION

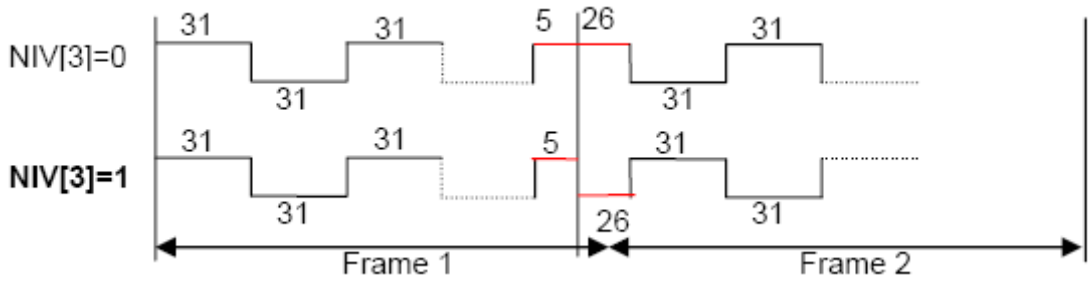
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set N-line inversion NIV[3:0]	0	0	1	1	0	0	1	0	0	0
(Double-byte command)	0	0	-	-	-	NIV4	NIV3	NIV2	NIV1	NIV0

N-Line Inversion:

NIV[2:0]: 000b: 11 lines 001b: 19 lines 010b: 21 lines 011b: 25 lines
100b: 29 lines **101b: 31 lines** 110b: 37 lines 111b: 43 lines

NIV[3]: 0b: non-XOR **1b: XOR**

NIV[4]: 0b: Disable NIV **1b: Enable NIV**



(20) SET COLOR PATTERN

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Pattern LC [5]	0	0	1	1	0	1	0	0	0	LC5

UC1698u supports on-chip swapping of RGB data mapping to the SEG drivers

LC[5]	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	…	SEG382	SEG383	SEG384
0	B	G	R	B	G	R	…	B	G	R
1	R	G	B	R	G	B	…	R	G	B

The definition of R/G/B input data is determined by LC[7:6], as described in ***Set Color Mode*** below.

(21) SET COLOR MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Color Mode LC [7:6]	0	0	1	1	0	1	0	1	LC7	LC6

Program color mode and RGB input pattern. Color mode (LC[7:6]) definition:

Note: For serial bus modes, please refer to 8-bit tables below.

- Green Enhance Mode disabled (DC[4]=1):

LC[7:6] = 01b (RRRR-GGGG-BBBB, 4K-color)

12 bits of input RGB data are stored to 16 RAM bits. No dither is performed. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	D[7:0]							
1st Write Data Cycle	R3	R2	R1	R0	G3	G2	G1	G0
2nd Write Data Cycle	B3	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G3	G2	G1	G0	B3	B2	B1	B0

LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color)

16 bits of input data are stored to 16 RAM bits directly.

Data Write Sequence (8-bit)	D[7:0]							
1st Write Data Cycle	R4	R3	R2	R1	R0	G5	G4	G3
2nd Write Data Cycle	G2	G1	G0	B4	B3	B2	B1	B0

- Green Enhance Mode disabled (DC[4]=0):

LC[7:6] = 01b (RRRR-GGGGG-BBB, 4K-color)

12 bits of input data are extended and stored to 16 RAM bits. Every 3 bytes of input data will be merged into 2 sets of RGB data.

Data Write Sequence (8-bit)	D[7:0]							
1st Write Data Cycle	R3	R2	R1	R0	G4	G3	G2	G1
2nd Write Data Cycle	G0	B2	B1	B0	R3	R2	R1	R0
3rd Write Data Cycle	G4	G3	G2	G1	G0	B2	B1	B0

LC[7:6] = 10b (RRRRR-GGGGGG-BBBBB, 64K-color)

The behaviors of 8-bit input mode and 16-bit input mode do not change with DC[4] setting. Refer to previous section for more information on these two input modes.

(22) SET COM SCAN FUNCTION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set COM Scan Function CSF[2:0]	0	0	1	1	0	1	1	CSF2	CSF1	CSF0

COM scan function
CSF[0]: Interlace Scan Function
0b: LRM sequence: AEBCD-AEBCD
1b: LRM sequence: AEBCD-EBCDA
CSF[1]: FRC Function
0b: FRC Disable
1b: FRC Enable
CSF[2]: Shade-1, Shade-30 option
0 : Dither directly on input data(SRAM Change)
1 : PWM on SEG output stage

(23) SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

(24) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	1	1	1	0	0	0	1	1

This command is used for “no operation”.

(25) SET TEST CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	1	1	1	0	0	1	TT	
(Double-byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Do NOT use.

(26) SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition: 00b =5 01b = 10 10b = 11 **11b = 12**

(27) SET COM END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN	0	0	1	1	1	1	0	0	0	1
(Double-byte command)	0	0	-	CEN register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 160 pixel rows, the LCM designer should set CEN to N-1 (where N is the number of pixel rows) and use COM1 through COM-N as COM driver electrodes.

(28) SET PARTIAL DISPLAY START

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST	0	0	1	1	1	1	0	0	1	0
(Double-byte command)	0	0	-	DST register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

(29) SET PARTIAL DISPLAY END

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN	0	0	1	1	1	1	0	0	1	1
(Double-byte command)	0	0	-	DEN register parameter						

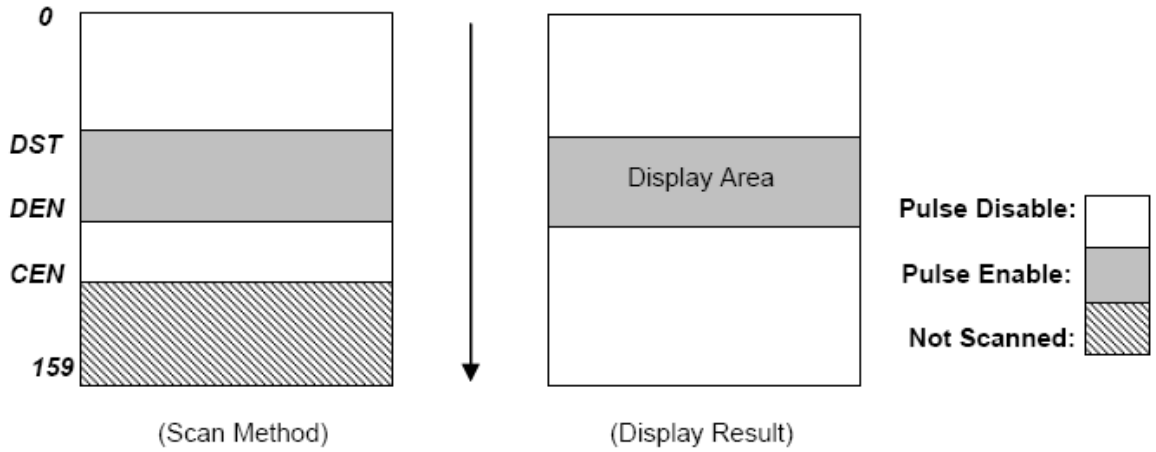
This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[8]=1b, the Mux-Rate is narrowed down to DST-DEN+1+(FLT+FLB)xLC[0]x2. When MUX rate is reduced, reduce the line rate accordingly to reduce power. Changing MUX rate also require BR and VLCD to be reduced.

For minimum power consumption, set LC[8]=1b, set (DST, DEN, FLT, FLB, CEN) to minimize MUX rate, use slowest line rate which satisfies the flicker requirement, use On/Off mode, set PC[0]=0b, disable N-Line Inversion, and use lowest BR, lowest VLCD which satisfies the contrast requirement. When Mux-Rate is under 40, it is recommended to set BR=5 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



(30) SET WINDOW PROGRAM STARTING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC0	0	0	1	1	1	1	0	1	0	0
(Double-byte command)	0	0	-	WPC0[6:0] register parameter						

This command is to program the starting column address of RAM program window.

(31) SET WINDOW PROGRAM STARTING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP0	0	0	1	1	1	1	0	1	0	1
(Double-byte command)	0	0	WPP0[7:0] register parameter							

This command is to program the starting row address of RAM program window.

(32) SET WINDOW PROGRAM ENDING COLUMN ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPC1 (Double-byte command)	0	0	1	1	1	1	0	1	1	0
	0	0	-	WPC1[6:0] register parameter						

This command is to program the ending column address of RAM program window.

(33) SET WINDOW PROGRAM ENDING ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set WPP1	0	0	1	1	1	1	0	1	1	1
(Double-byte command)	0	0	WPP1[7:0] register parameter							

This command is to program the ending row address of RAM program window.

(34) SET WINDOW PROGRAM MODE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Window Program Enable AC[3]	0	0	1	1	1	1	1	0	0	AC3

This command controls the Window Program function.

AC[3]=0: Inside Mode

When Window Programming is under “Inside” mode , the CA and RA increment and wrap-around will be performed automatically around the boundaries as defined by registers WPC0, WPC1, WPP0, and WPP1, so that the CA/RA address will stay within the defined window of SRAM address, and therefore allow effective data update within the window.

AC[3]=1: Outside Mode

When Window Programming is under “Outside” mode, the CA and RA increment and wrap-around boundary will cover the entire UC1698u SRAM map (CA: 0~127, RA:0~159). However, when CA/RA points to a memory location within the window defined by registers WPC0, WPC1, WPP0, and WPP1, the SRAM data update operation will be suspended, the existing data will be retained and the input data will be ignored.

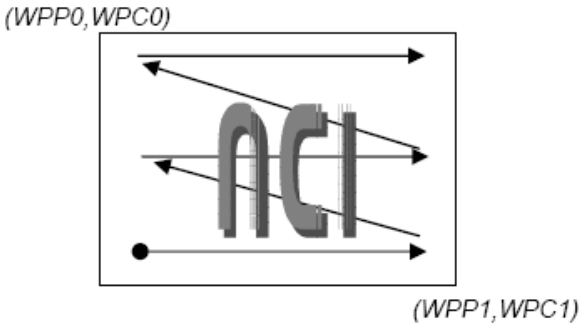
The direction of Window Program will depend on the WA (AC[0]), RID (AC[2]), auto-increment order (AC[1]) and MX (LC[1]) register setting.

- WA (AC[0]) decides whether the program RAM address advances to next row / column after reaching the specified window column / row boundary.
- RID (AC[2]) controls the RAM address increasing from WPP0 toward WPP1 (RID=0) or the reverse direction (RID=1).
- Auto-increment Order (AC[1]) directs the RAM address increasing vertically (AC[1]=1) or horizontally (AC[1]=0).
- MX (LC[1]) results the RAM column address increasing from 127-WPC0 to 127-WPC1 (MX=1) or from WPC0 to WPC1 (MX=0).

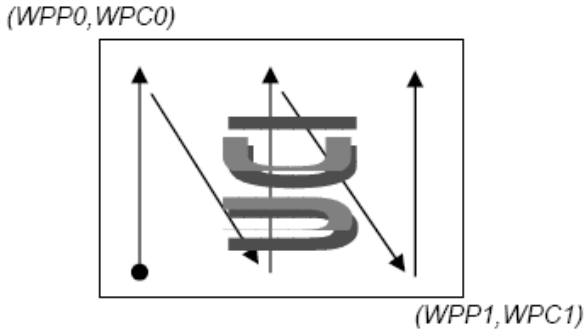
By different combination of RID, AC[1], MX, and by setting CA, RA at proper corners of the “window”, effects such as mirrors and rotations can be easily achieved.

Setting or resetting AC[3] does not affect the values of CA and RA. So, always remember to reposition CA and RA properly after changing the setting of AC[3].

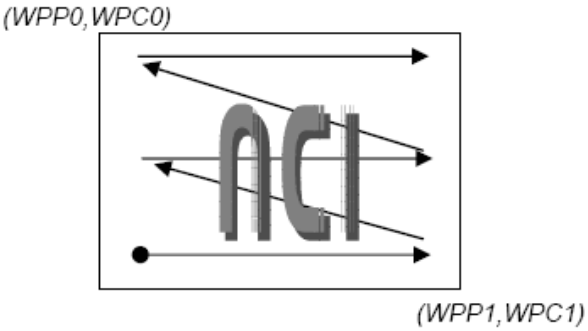
Auto-increment order = 0 MX=0 RID = 0



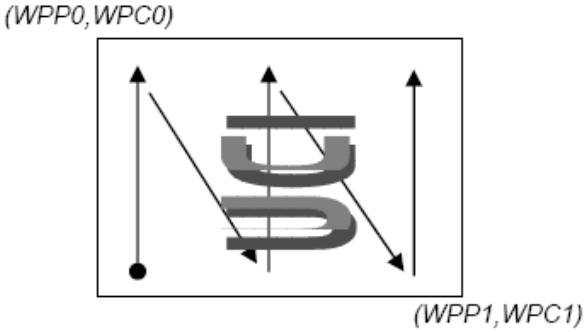
Auto-increment order = 1 MX=0 RID = 1



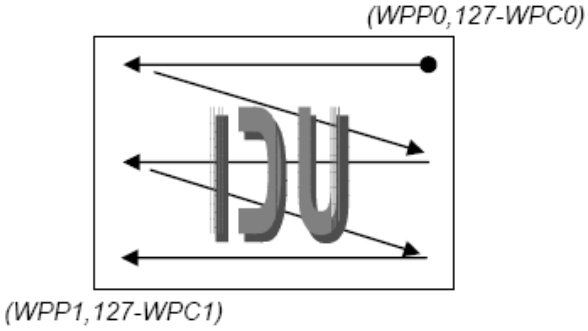
Auto-increment order = 0 MX=0 RID = 1



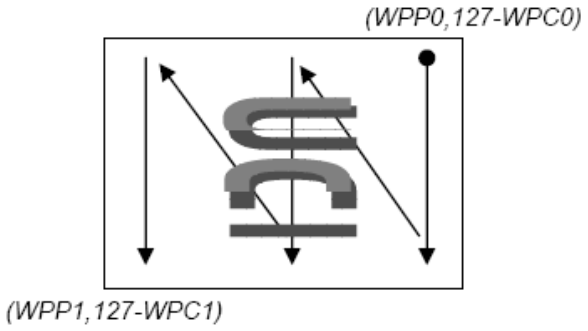
Auto-increment order = 1 MX=0 RID = 1



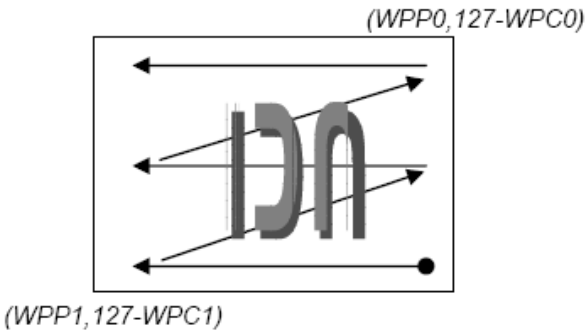
Auto-increment order = 0 MX=1 RID = 0



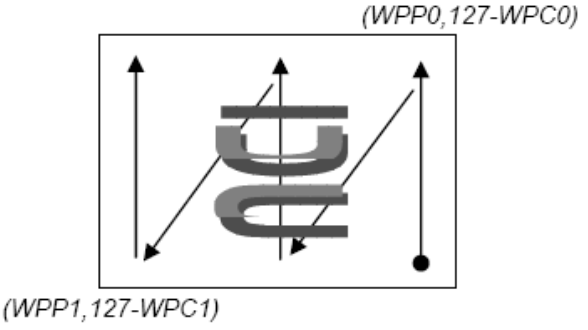
Auto-increment order = 1 MX=1 RID = 0



Auto-increment order = 0 MX=1 RID = 1



Auto-increment order = 1 MX=1 RID = 1



14. 0 QUALITY GUARANTEE

14.1 ACCEPTABLE QUALITY LEVEL

Inspection items	Sampling procedures	AQL
Visual-operating (Electro-optical)	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	0.65
Visual-not operating	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	1.5
Dimension measurement	GB2828-81 Inspection level Ⅱ Normal inspection Single sample inspection	1.5

14.2 Conditions of Cosmetic Inspection

- Environmental condition

The inspection should be performed at the 1m of height from the LCD module under 2 pieces of 40W white fluorescent lamps (Normal temperature 20~25℃ and normal humidity 60±15%RH).

- Inspection method

The visual check should be performed vertically at more than 30cm distance from the LCD panel.

- Driving voltage

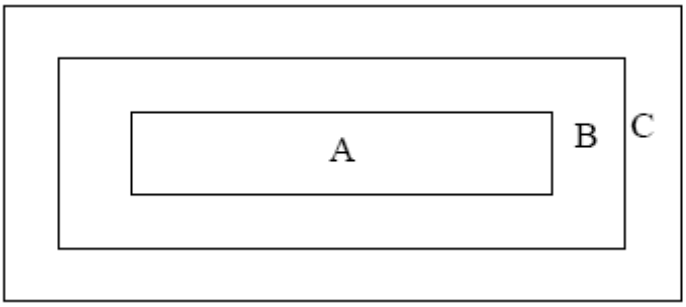
The V0 value which the most optimal contrast can be obtained near the specified V0 in the specification. (Within ±0.5V of the typical value at 25℃.).

14.3 Definition of inspection zone in LCD

Zone A: character/Digit area

Zone B: viewing area except Zone A (ZoneA+ZoneB=minimum Viewing area)

Zone C: Outside viewing area (invisible area after assembly in customer's product)



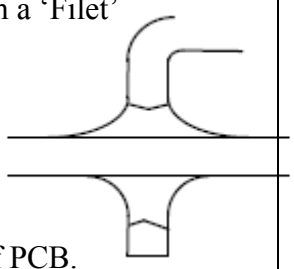
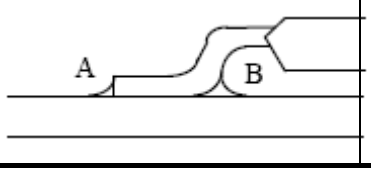
Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble for quality and assembly of customer's product.

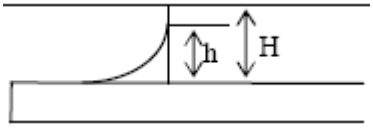
14.4 Inspection Standard

- **Major Defect**

Item No	Items to be inspected	Inspection Standard	Classification of defects
1	All functional defects	1) No display 2) Display abnormally 3) Missing vertical，horizontal segment 4) Short circuit 5) Back-light no lighting, flickering and abnormal lighting.	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed.	

- **Module Cosmetic Criteria**

No.	Item	Judgment Criterion	Partition
1	Difference in Spec.	None allowed	Major
2	Pattern peeling	No substrate pattern peeling and floating	Major
3	Soldering defects	No soldering missing No soldering bridge No cold soldering	Major Major Minor
4	Resist flaw on substrate	Invisible copper foil (∅0.5mm or more) on substrate pattern	Minor
5	Accretion of metallic Foreign matter	No soldering dust No accretion of metallic foreign matters (Not exceed ∅0.2mm)	Minor Minor
6	Stain	No stain to spoil cosmetic badly	Minor
7	Plate discoloring	No plate fading, rusting and discoloring	Minor
8	Solder amount 1. Lead parts	a. Soldering side of PCB Solder to form a ‘Filet’ all around the lead. Solder should not hide the lead form perfectly. (too much) b. Components side (In case of ‘Through Hole PCB’) Solder to reach the Components side of PCB. 	Minor
	2. Flat packages	Either ‘Toe’ (A) or ‘Seal’ (B) of the lead to be covered by ‘Filet’. Lead form to be assume over solder. 	Minor

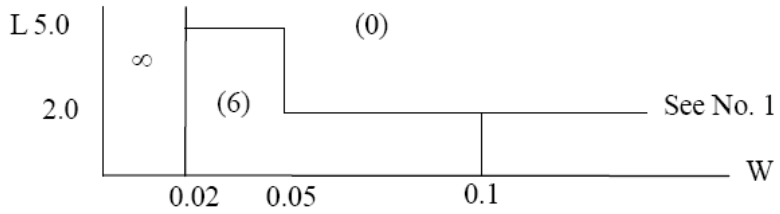
No.	Item	Judgment Criterion	Partition
8	3. Chips	(3/2) H ≥ h ≥ (1/2) H 	Minor

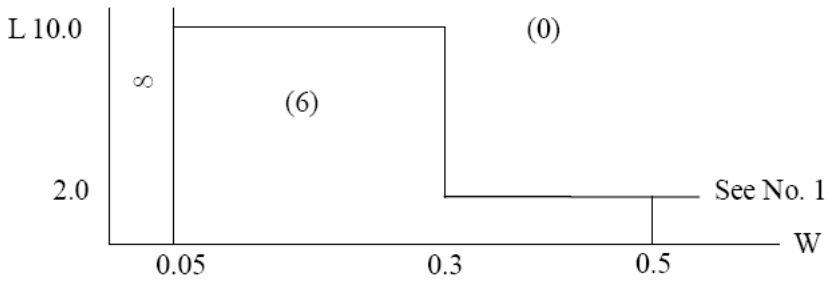
● Screen Cosmetic Criteria (Non-Operating)

No.	Defect	Judgement Criterion	Partition
1	Spots	In accordance with *Screen Cosmetic Criteria (Operating) No.1*.	Minor
2	Lines	In accordance with *Screen Cosmetic Criteria (Operating) No.2*.	Minor
3	Bubbles in polarizer	<table><tr><td>Size : d</td><td>mm</td><td>Acceptable Qty in active area</td></tr><tr><td>d</td><td>≤ 0.3</td><td>Disregard</td></tr><tr><td>0.3 < d</td><td>≤ 1.0</td><td>3</td></tr><tr><td>1.0 < d</td><td>≤ 1.5</td><td>1</td></tr><tr><td>1.5 < d</td><td></td><td>0</td></tr></table>	Minor
4	Scratch	In accordance with spots and lines operating cosmetic criteria. When the light reflects on the panel surface, the scratches are not to be remarkable.	Minor
5	Allowable density	Above defects should be separated more than 30mm each other.	Minor
6	Coloration	Not to be noticeable coloration in the viewing area of the LCD panels. Back-lit type should be judged with back-lit on state only.	Minor
7	Contamination	Not to be noticeable.	Minor

Note: Size : d = (long length + short length) / 2

● Screen Cosmetic Criteria (Operating)

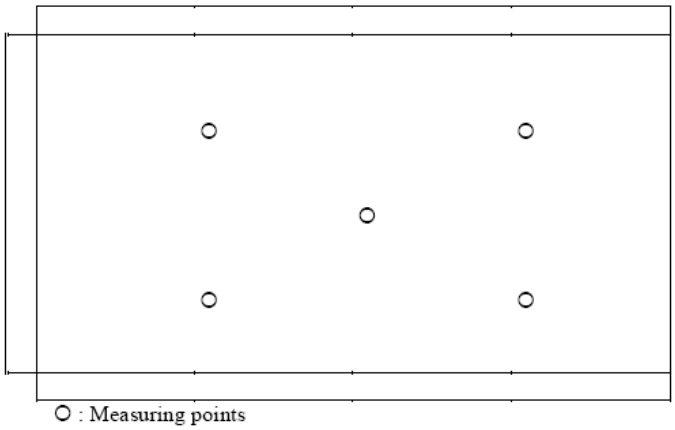
<table>
<tr><th>No.</th><th>Defect</th><th>Judgment Criterion</th><th>Partition</th></tr>
<tr><td>1</td><td>Spots</td><td>A) Clear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.1</td><td>Disregard</td></tr>
<tr><td>0.1 < d ≤ 0.2</td><td>6</td></tr>
<tr><td>0.2 < d ≤ 0.3</td><td>2</td></tr>
<tr><td>0.3 < d</td><td>0</td></tr>
</table>
Note : Including pin holes and defective dots which must be within one pixel size.
B) Unclear
<table>
<tr><th>Size : d mm</th><th>Acceptable Qty in active area</th></tr>
<tr><td>d ≤ 0.2</td><td>Disregard</td></tr>
<tr><td>0.2 < d ≤ 0.5</td><td>6</td></tr>
<tr><td>0.5 < d ≤ 0.7</td><td>2</td></tr>
<tr><td>0.7 < d</td><td>0</td></tr>
</table></td><td>Minor</td></tr>
<tr><td>2</td><td>Lines</td><td>A) Clear
 

Note :
( ) - Acceptable Qty in active area
L - Length (mm)
W - Width (mm)
∞ - Disregard
B) Unclear
 

‘Clear’ = The shade and size are not changed by Vop.
‘Unclear’ = The shade and size are changed by Vop.</td><td>Minor</td></tr>
</table>

Note: Size : d = (long length + short length) / 2

● Screen Cosmetic Criteria (Operating) (Continued)

No.	Defect	Judgment Criterion	Partition
3	Rubbing line	Not to be noticeable.	Minor
4	Allowable density	Above defects should be separated more than 10mm each other.	Minor
5	Rainbow	Not to be noticeable.	Minor
6	Dot size	To be 95% ~ 105% of the dot size (Typ.) in drawing. Partial defects of each dot (ex. pin-hole) should be treated as pot'. (see *Screen Cosmetic Criteria (Operating) No.1*)	Minor
7	Uneven brightness (only back-lit type module)	Uneven brightness must be BMAX / BMIN ≤ 2 - BMAX : Max. value by measure in 5 points - BMIN : Min. value by measure in 5 points Divide active area into 4 vertically and horizontally. Measure 5 points shown in the following figure.  	Minor

Note :

(1) The limit samples for each item have priority.

(2) Complex defects are defined item by item, but if the numbers of defects are defined in above table, the total number should not exceed 10.

(3) In case of 'concentration', even the spots or the lines of 'disregarded' size should not allowed. Following three situations should be treated as 'concentration'.

- 7 or over defects in circle of Æ5mm.
- 10 or over defects in circle of Æ10mm.
- 20 or over defects in circle of Æ20mm.

15. 0 RELIABILITY

15.1 Content of Reliability Test

No.	Test Item	Test Condition	Inspection after test
1	High Temperature Storage	+85℃±2℃/200 hours	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Sealleak; 3.Non-display; 4.missing segments; 5.Glass crack; 6.Current Idd is twice higher than initial value.
2	Low Temperature Storage	-45℃±2℃/200 hours	
3	High Temperature Operating	+70℃±2℃/120 hours	
4	Low Temperature Operating	-40℃±2℃/120 hours	
5	Temperature Cycle	-40℃±2℃~+25℃~+70℃±2℃×10cycles (30min.) (5min.) (30min.)	
6	High Temperature / Humidity operation	+50℃±5℃×90%RH/120 hours	
7	Vibration Test	Frequency：10Hz~55Hz~10Hz Amplitude：1.5mm, X，Y，Z direction for total 3hours (Packing condition)	
8	Drooping test	Drop to the ground from 1m height, one time, and every side of carton. (Packing condition)	
9	Static electricity test	Voltage:±8KV R: 330Ω C: 150pF Air discharge, 10time	

Remark:

1. The test samples should be applied to only one test item.
2. Sample size for each test item is 5~10pcs.
3. For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.
4. In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judge as a good part.
5. EL evaluation should be excepted from reliability test with humidity and temperature: Some defects such as black spot/blemish can happen by natural chemical reaction with humidity and Fluorescence EL has.
6. Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

16. 0 PRECAUTIONS FOR USING LCD MODULES

16.1 Handing Precautions

(1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it or impact.

(2) If the display panel is damaged and the liquid crystal substance leaks out, be sure not to get any in your mouth. If the substance contacts your skin or clothes, wash it off using soap and water.

(3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

(5) If the display surface becomes contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is heavily contaminated, moisten cloth with one of the following solvents :

- Isopropyl alcohol
- Ethyl alcohol

(6) Solvents other than those above-mentioned may damage the polarizer. Especially, do not use the following.

- Water
- Ketone
- Aromatic solvents

(7) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets, moisture condensation or a current flow in a high-humidity environment.

(8) Install the LCD Module by using the mounting holes. When mounting the LCD module make sure it is free of twisting, warping and distortion. In particular, do not forcibly pull or bend the I/O cable or the backlight cable.

(9) Do not attempt to disassemble or process the LCD module.

(10) NC terminal should be open. Do not connect anything.

(11) If the logic circuit power is off, do not apply the input signals.

(12) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

- Be sure to ground the body when handling the LCD modules.
- Tools required for assembling, such as soldering irons, must be properly grounded.
- To reduce the amount of static electricity generated, do not conduct assembling and other work under dry conditions.
- The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

16.2 Storage Precautions

When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps. Keep the modules in bags (avoid high temperature / high humidity and low temperatures below 0°C). Whenever possible, the LCD modules should be stored in the same conditions in which they were shipped from our company.

16.3 Others

Liquid crystals solidify under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the module is subject to a low temperature.

If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.

To minimize the performance degradation of the LCD modules resulting from destruction caused by static electricity etc., exercise care to avoid holding the following sections when handling the modules.

- Exposed area of the printed circuit board.
- Terminal electrode sections.

17. 0 USING LCD MODULES

17.1 About Liquid Crystal Display Modules

LCD is composed of glass and polarizer. Pay attention to the following items when handling.

(1) Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peel-off may occur with high temperature and high humidity.

(2) Do not touch, push or rub the exposed polarizer with anything harder than an HB pencil lead (glass, tweezers, etc.).

(3) N-hexane is recommended for cleaning the adhesives used to attach front/rear polarizer and reflectors made of organic substances which will be damaged by chemicals such as acetone, toluene, ethanol and isopropyl alcohol.

(4) When the display surface becomes dusty, wipe gently with absorbent cotton or other soft material like chamois soaked in petroleum benzin. Do not scrub hard to avoid damaging the display surface.

(5) Wipe off saliva or water drops immediately, contact with water over a long period of time may cause deformation or color fading.

(6) Avoid contacting oil and fats.

(7) Condensation on the surface and contact with terminals due to cold will damage, stain or dirty the polarizer. After products are tested at low temperature they must be warmed up in a container before coming is contacting with room temperature air.

(8) Do not put or attach anything on the display area to avoid leaving marks on.

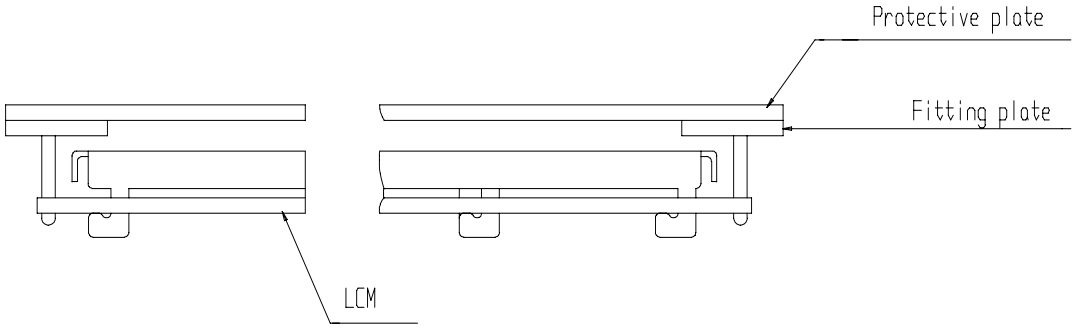
(9) Do not touch the display with bare hands. This will stain the display area and degradate insulation between terminals (some cosmetics are determinate to the polarizer).

(10) As glass is fragile. It tends to become or chipped during handling especially on the edges. Please avoid dropping or jarring.

17.2 Installing LCD Modules

The hole in the printed circuit board is used to fix LCM as shown in the picture below. Attend to the following items when installing the LCM.

(1) Cover the surface with a transparent protective plate to protect the polarizer and LC cell.



(2) When assembling the LCM into other equipment, the spacer to the bit between the LCM and the fitting plate should have enough height to avoid causing stress to the module surface, refer to the individual specifications for measurements. The measurement tolerance should be ±0.1mm.

17.3 Electro-Static Discharge Control

Since this module uses a CMOS LSI, the same careful attention should be paid to electrostatic discharge as for an ordinary CMOS IC.

(1) Make certain that you are grounded when handing LCM.

(2) Before remove LCM from its packing case or incorporating it into a set, be sure the module and your body have the same electric potential.

(3) When soldering the terminal of LCM, make certain the AC power source for the soldering iron does not leak.

(4) When using an electric screwdriver to attach LCM, the screwdriver should be of ground potentiality to minimize as much as possible any transmission of electromagnetic waves produced sparks coming from the commutation of the motor.

(5) As far as possible make the electric potential of your work clothes and that of the work bench the ground potential.

(6) To reduce the generation of static electricity be careful that the air in the work is not too dried. A relative humidity of 50%-60% is recommended.

17.4 Soldering to the LCM

(1) Observe the following when soldering lead wire, connector cable and etc. to the LCM.

- Soldering iron temperature : 280°C ± 10°C.
- Soldering time : 3-4 sec.
- Solder : eutectic solder.

If soldering flux is used, be sure to remove any remaining flux after finishing to soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended that you protect the LCD surface with a cover during soldering to prevent any damage dur to flux spatters.

(2) When soldering the electroluminescent panel and PC board, the panel and board should not be detached more than three times. This maximum number is determined by the temperature and time conditions mentioned above, though there may be some variance depending on the temperature of the soldering iron.

(3) When remove the electroluminescent panel from the PC board, be sure the solder has completely melted, the soldered pad on the PC board could be damaged.

17.5 Operation

(1) Viewing angle varies with the change of liquid crystal driving voltage (VO). Adjust VO to show the best contrast.

(2) Driving the LCD in the voltage above the limit shortens its life.

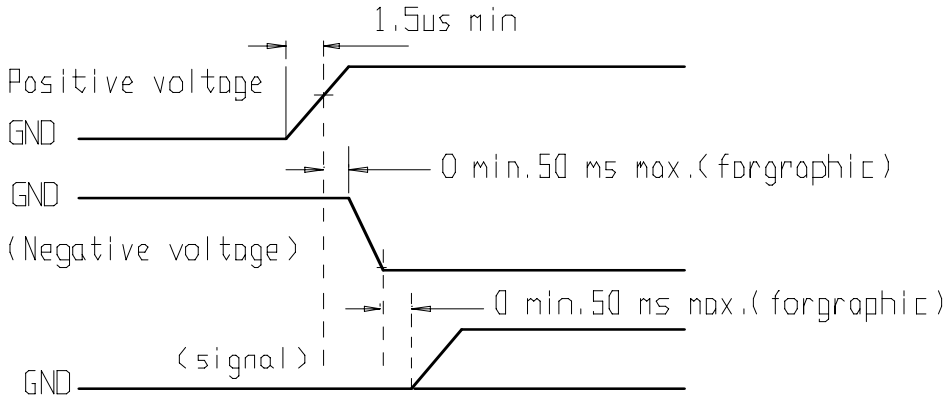
(3) Response time is greatly delayed at temperature below the operating temperature range. However, this does not mean the LCD will be out of the order. It will recover when it returns to the specified temperature range.

(4) If the display area is pushed hard during operation, the display will become abnormal. However, it will return to normal if it is turned off and then back on.

(5) Condensation on terminals can cause an electrochemical reaction disrupting the terminal circuit.

Therefore, it must be used under the relative condition of 40°C , 50% RH.

(6) When turning the power on, input each signal after the positive/negative voltage becomes stable.



17.6 Storage

When storing LCDs as spares for some years, the following precaution are necessary.

(1) Store them in a sealed polyethylene bag. If properly sealed, there is no need for dessicant.

(2) Store them in a dark place. Do not expose to sunlight or fluorescent light, keep the temperature between 0°C and 35°C.

(3) The polarizer surface should not come in contact with any other objects. (We advise you to store them in the container in which they were shipped.)

(4) Environmental conditions :

- Do not leave them for more than 168hrs. at 60°C.
- Should not be left for more than 48hrs. at -20°C.

17.7 Safety

(1) It is recommended to crush damaged or unnecessary LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned.

(2) If any liquid leakes out of a damaged glass cell and comes in contact with the hands, wash off thoroughly with soap and water.

17.8 Limited Warranty

Unless agreed between HYDISPLAY and customer, HYDISPLAY will replace or repair any of its LCD modules which are found to be functionally defective when inspected in accordance with HYDISPLAY LCD/LCM acceptance standards (copies available upon request) for a period of one year from date of shipments. Cosmetic/visual defects must be returned to HYDISPLAY within 90 days of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of HYDISPLAY limited to repair and/or replacement on the terms set forth above. HYDISPLAY will not be responsible for any subsequent or consequential events.

17.9 Return LCM under warranty

No warranty can be granted if the precautions stated above have been disregarded. The typical examples of violations are :

- Broken LCD glass.
- PCB eyelet's damaged or modified.
- PCB conductors damaged.
- Circuit modified in any way, including addition of components.
- PCB tampered with by grinding, engraving or painting varnish.
- Soldering to or modifying the bezel in any manner.

Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects. Any connectors or cable installed by the customer must be removed completely without damaging the PCB eyelet, conductors and terminals.

18. 0 APPENDIX

18.1 Initialization Code

```
void wr_cmd(uchar uc_cmd)
{
    LCD_RD = 1;
    LCD_A0 = 0;
    LCD_CS = 0;
    LCD_WR = 0;
    P1 = uc_cmd;
    LCD_WR = 1;
    LCD_CS = 1;
}

void wr_dat(uchar uc_dat)
{
    LCD_RD = 1;
    LCD_A0 = 1;
    LCD_CS = 0;
    LCD_WR = 0;
    P1 = uc_dat;
    LCD_WR = 1;
    LCD_CS = 1;
}

void Intitial(void)
{
    wr_cmd(0xE2);//System Reset
    delay(100);
    wr_cmd(0xAE);//Set Display Disable

    wr_cmd(0x26);//Set Temperature Compensation // 10-0.15%
    wr_cmd(0x2A);//Set Power Control (Internal VLCD; Panel loading definition <=13nF)
    wr_cmd(0xE9); //Set LCD Bias ratio:1/10

    wr_cmd(0x81); //Set gain and potentiometer Mode
    wr_cmd(0xC8); //Program Gain:01;PM value:xx

    wr_cmd(0x89); //Set RAM Address Control
    wr_cmd(0xC4); //Set LCD Maping Control (MY=1, MX=0)

    wr_cmd(0xDE); //Set COM Scan Function
```

```
    wr_cmd(0xC8); //Set N-Line Inversion
    wr_cmd(0x18); //Set COM Scan Function

    wr_cmd(0xA0); //Set Line Rate

    wr_cmd(0xD5); //Set Color Mode (4K)
    wr_cmd(0xD1); //Set Color Pattern (RGB)

    wr_cmd(0x84); //Set Partial Display Off

    wr_cmd(0xF4); //Set Windows Program Starting Column Address
    wr_cmd(0x25); //
    wr_cmd(0xF6); //Set Windows Program Ending Column Address
    wr_cmd(0x5A); //
    wr_cmd(0xF5); //Set Windows Program Starting Row Address
    wr_cmd(0x00); //
    wr_cmd(0xF7); //Set Windows Program Ending Row Address
    wr_cmd(0x9F); //
    wr_cmd(0xF8); //Set Windows Program Mode: Inside Mode

    wr_cmd(0xAD); //Set Display Enable
}
```

18.2 LCM Application Circuit