

## NTZD5110NT1G-VB Datasheet

### Dual N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
V <sub>DS</sub> (V)	R <sub>DS(on)max</sub> (Ω)	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)
60	1.200 at V <sub>GS</sub> = 10 V	0.3	0.75
	1.300 at V <sub>GS</sub> = 8 V	0.28	
	1.500 at V <sub>GS</sub> = 4.5V	0.25	
	1.650 at V <sub>GS</sub> = 2.5V	0.15	

#### FEATURES

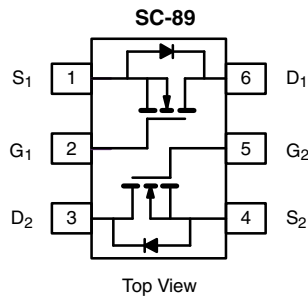
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- Gate-Source ESD Protected: 1000 V



RoHS  
COMPLIANT

#### APPLICATIONS

- Load/Power Switching for Portable Devices
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories
- Battery Operated Systems
- Power Supply Converter Circuits



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	± 12	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>a</sup>	I <sub>D</sub>	T <sub>A</sub> = 25 °C	0.30 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	0.25 <sup>a, b</sup>
Pulsed Drain Current	I <sub>DM</sub>	2	A
Continuous Source-Drain Diode Current	I <sub>S</sub>	0.18 <sup>a, b</sup>	A
Maximum Power Dissipation <sup>a</sup>	P <sub>D</sub>	T <sub>A</sub> = 25 °C	0.22 <sup>a, b</sup>
		T <sub>A</sub> = 70 °C	0.14 <sup>a, b</sup>
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Typ.	Max.	Unit
Maximum Junction-to-Ambient <sup>b</sup>	R <sub>thJA</sub>	t ≤ 5 s	470	565
		Steady State	560	675

Notes:

- a. Surface mounted on 1" x 1" FR4 board.  
b. t = 5 s.

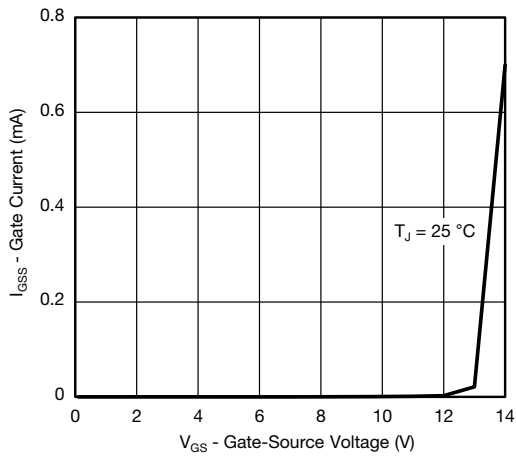
SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		17		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-1.8		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		1.6		V
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 8\text{ V}$			$\pm 30$	$\mu\text{A}$
		$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			$\pm 1$	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 85\text{ }^\circ\text{C}$			1 3	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 4.5\text{ V}$	2			A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 0.3\text{ A}$		1.200		$\Omega$
		$V_{GS} = 8\text{ V}, I_D = 0.2\text{ A}$		1.300		
		$V_{GS} = 4.5\text{ V}, I_D = 0.2\text{ A}$		1.500		
		$V_{GS} = 2.5\text{ V}, I_D = 0.15\text{ A}$		1.650		
Forward Transconductance	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 0.5\text{ A}$		7.5		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		40		pF
Output Capacitance	$C_{oss}$			14		
Reverse Transfer Capacitance	$C_{rss}$			8		
Total Gate Charge	$Q_g$	$V_{DS} = 10\text{ V}, V_{GS} = 8\text{ V}, I_D = 0.6\text{ A}$		1.3	2	nC
				0.75	1.2	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 0.6\text{ A}$		0.15		
Gate-Drain Charge	$Q_{gd}$			0.13		
Gate Resistance	$R_g$		$f = 1\text{ MHz}$	2.4	12.2	24.4
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V}, R_L = 20\text{ }\Omega$ $I_D \equiv 0.5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		11	20	ns
Rise Time	$t_r$			16	24	
Turn-Off Delay Time	$t_{d(off)}$			26	39	
Fall Time	$t_f$			11	20	
<b>Drain-Source Body Diode Characteristics</b>						
Pulse Diode Forward Current <sup>a</sup>	$I_{SM}$				2	A
Body Diode Voltage	$V_{SD}$	$I_S = 0.5\text{ A}$		0.8	1.2	V
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 0.5\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}$		10	15	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			2	4	nC
Reverse Recovery Fall Time	$t_a$			5		ns
Reverse Recovery Rise Time	$t_b$			5		

Notes:

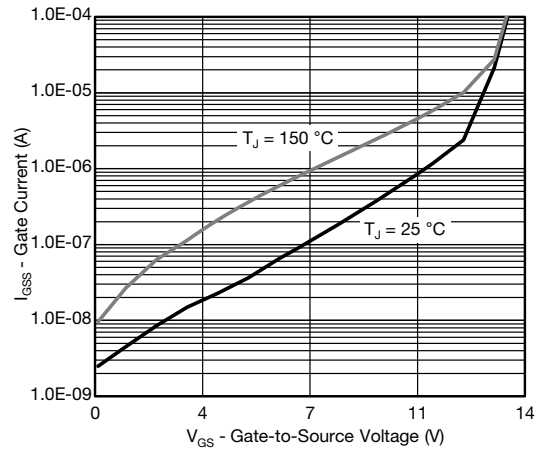
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

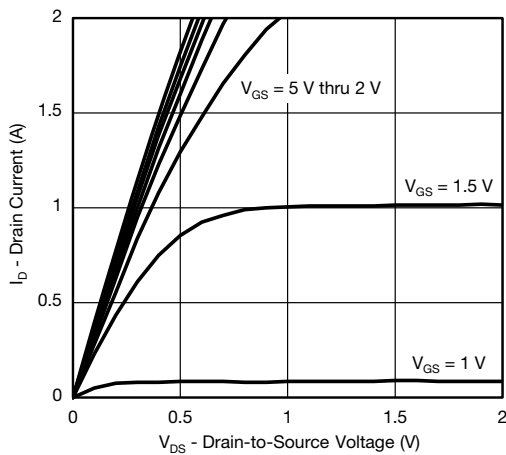
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



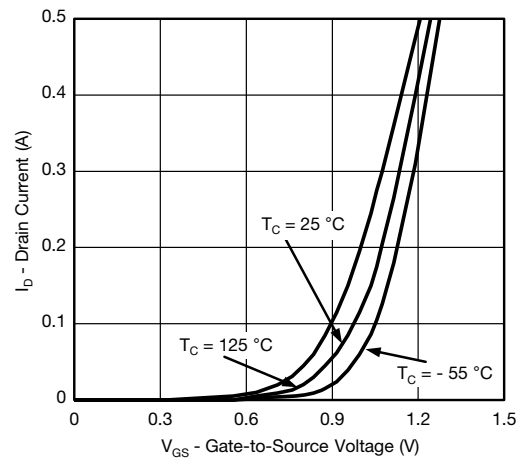
**Gate Current vs. Gate-Source Voltage**



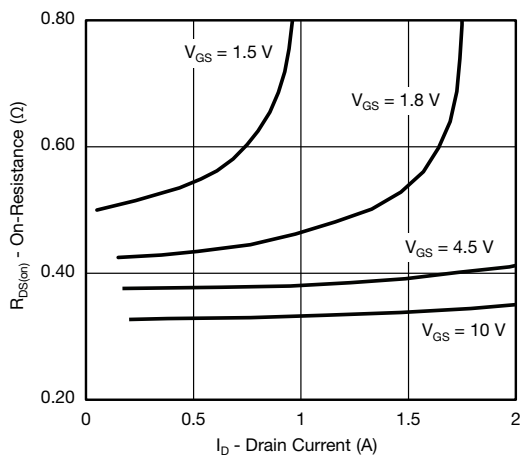
**Gate Current vs. Gate-Source Voltage**



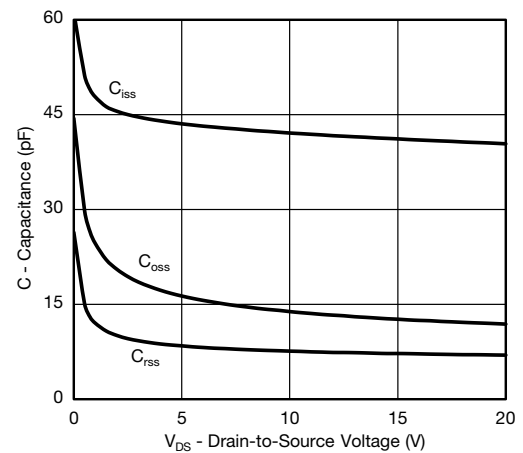
**Output Characteristics**



**Transfer Characteristics**

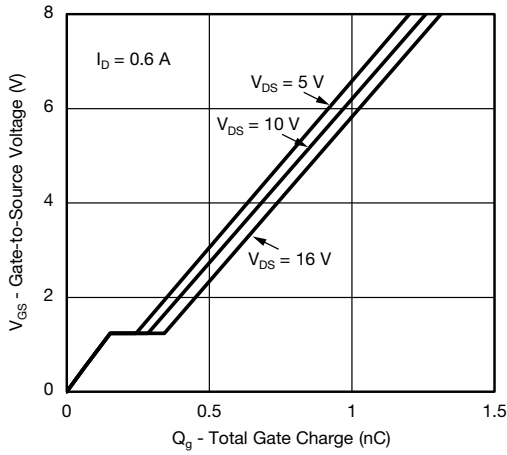


**On-Resistance vs. Drain Current**

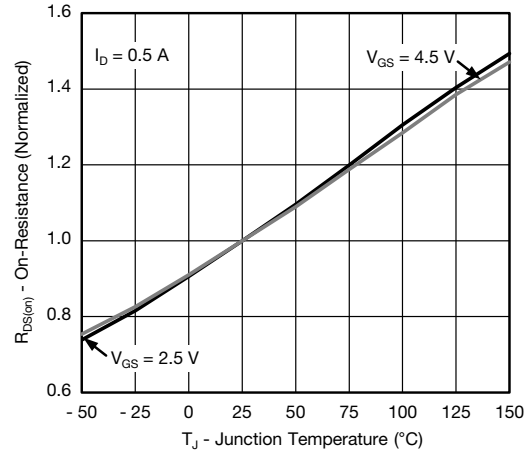


**Capacitance**

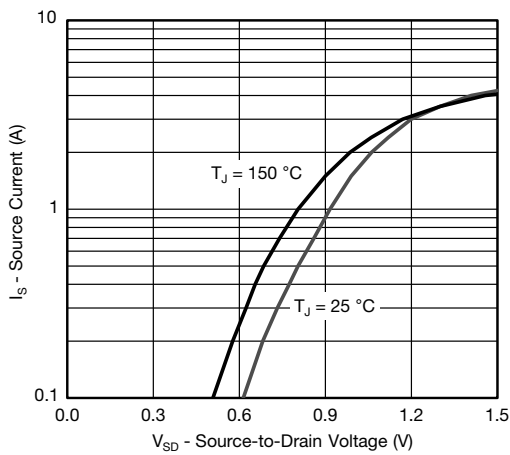
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



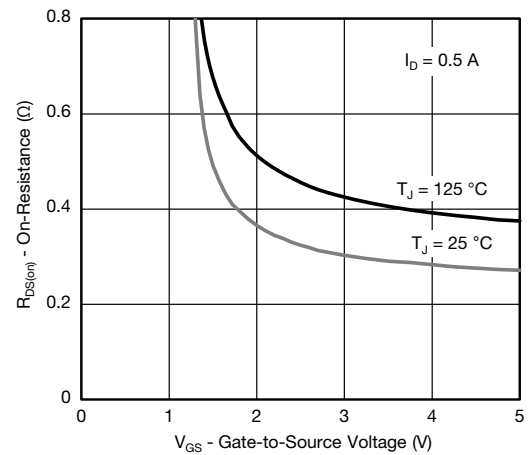
**Gate Charge**



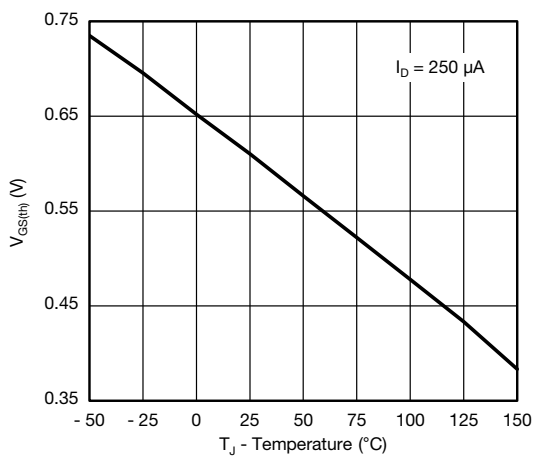
**On-Resistance vs. Junction Temperature**



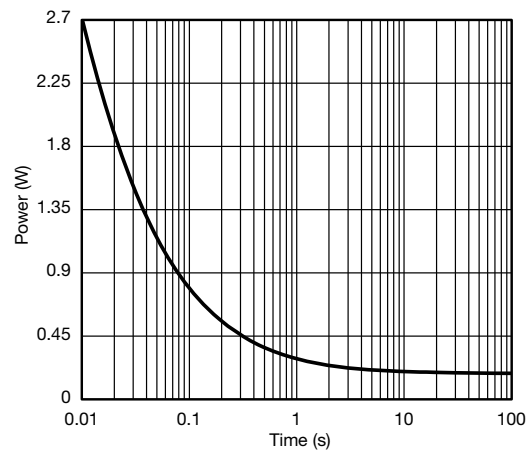
**Source-Drain Diode Forward Voltage**



**On-Resistance vs. Gate-to-Source Voltage**

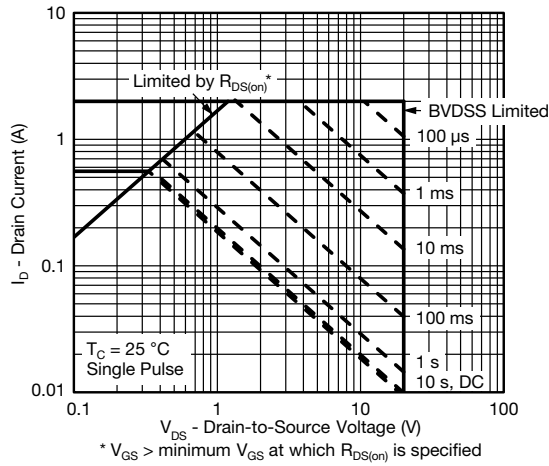


**Threshold Voltage**

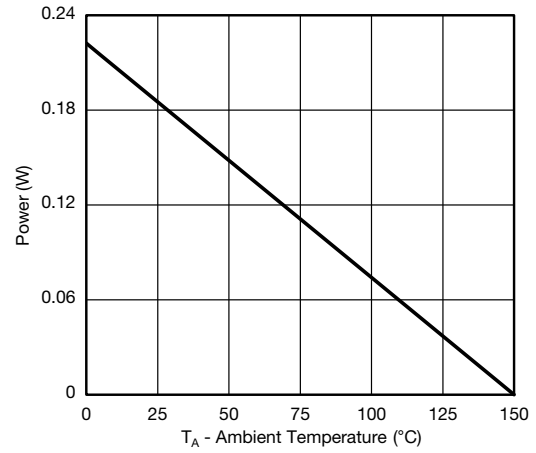


**Single Pulse Power, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

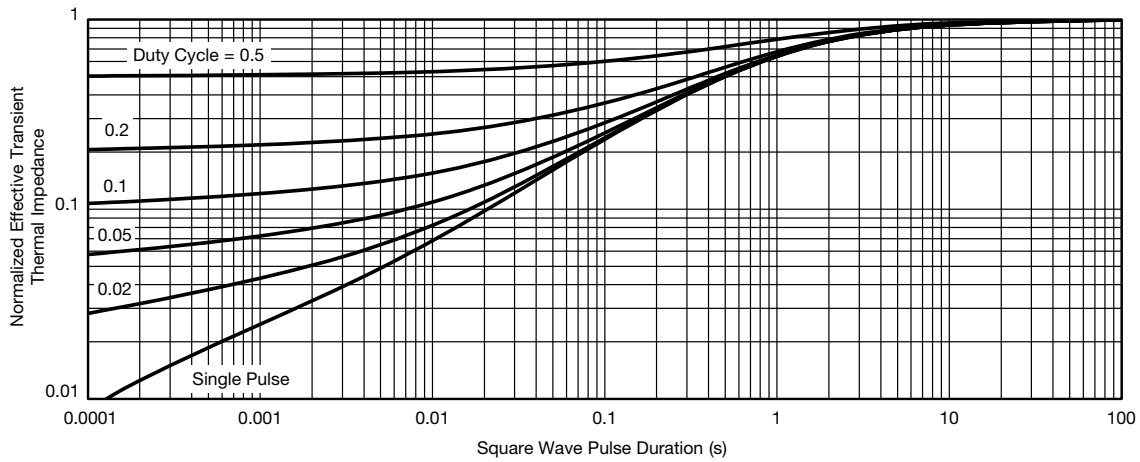


**Safe Operating Area, Junction-to-Ambient**



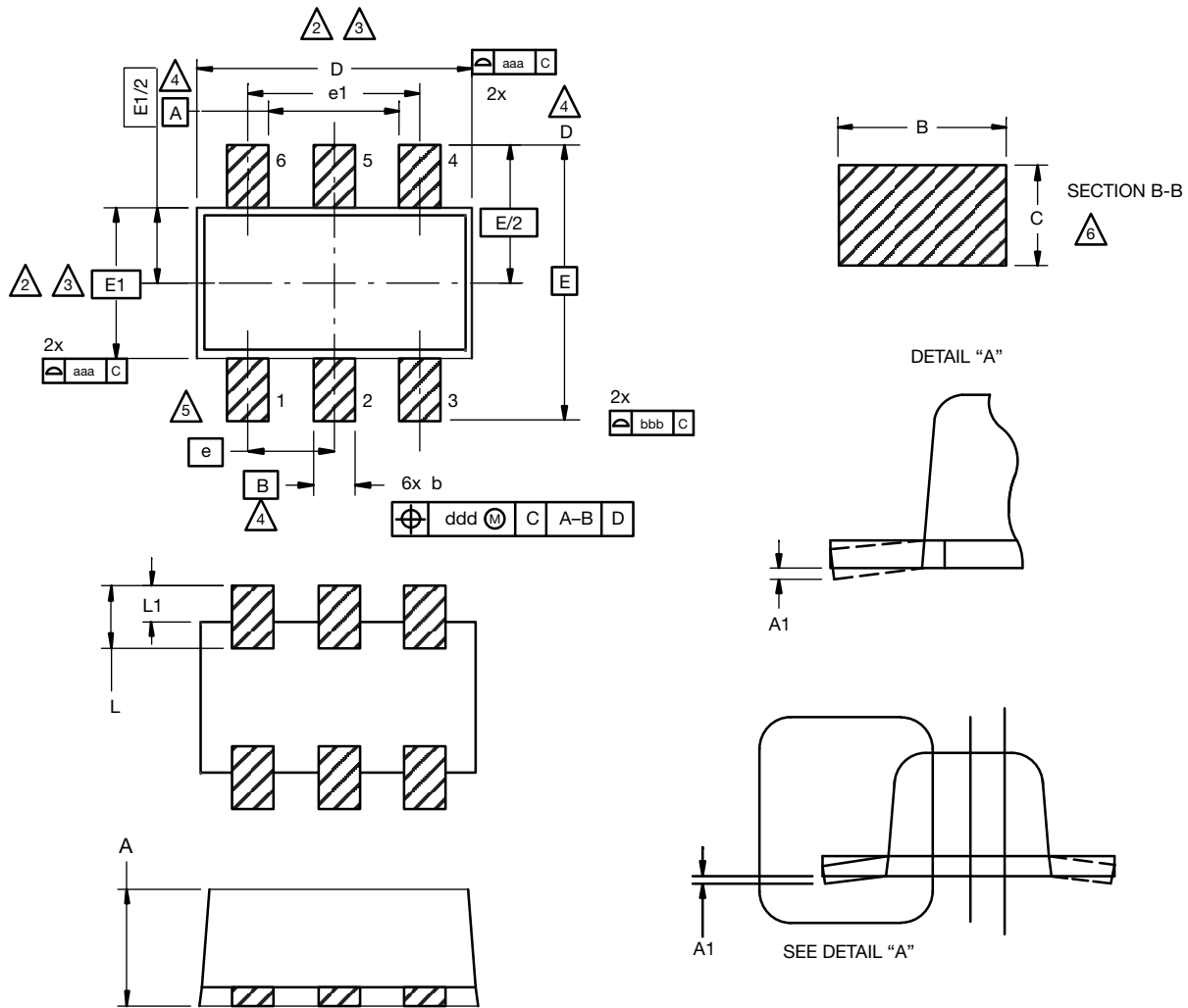
**Power Derating, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150\text{ °C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

### SC-89 6-Leads (SOT-563F)

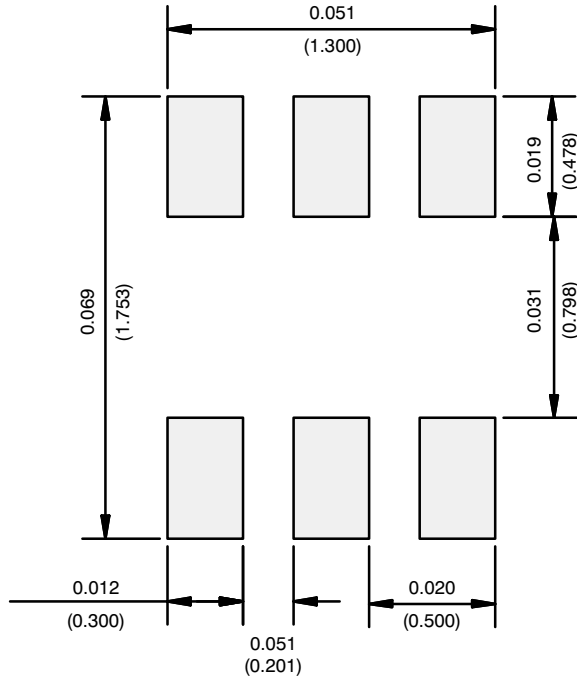


**Notes**

1. Dimensions in millimeters.
2. Dimension D does not include mold flash, protrusions or gate burrs. Mold flush, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
3. Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
4. Datums A, B and D to be determined 0.10 mm from the lead tip.
5. Terminal numbers are shown for reference only.
6. These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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