NS2510/NS2520/NS2530

HD Video Transmitter

Revision 0.90

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Norelsys

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1. Introduction

NS2510/NS2520/NS2530 are HD video transmitters supporting Advanced Video Transport (AVT) technology with visually lossless digital video compression. They also support uncompressed video transmission and are compatible with SMPTE SD-SDI, HD-SDI and 3G-SDI.

NS2510 supports up to HD 720p30 and HD 1080p15, NS2520 supports up to HD 720p60 and HD 1080p30. NS2530 also supports HD 1080p50/60.

NS2510/NS2520/NS2530 employ Norelsys' advanced video compression and serial data adaptation technologies. It can extend the reach of HD video over 500 meters on 75-3 coaxial cable. Norelsys' advanced digital video compression technologies achieve better video quality at less than half of the data rate required by MJPEG. The chips also include Norelsys' serial data adaptation engine which automatically adjusts data equalization, transfer rate and compression ratio based on cable quality and cable length. A programmable Reed-Solomon FEC block is implemented for increased reliability.

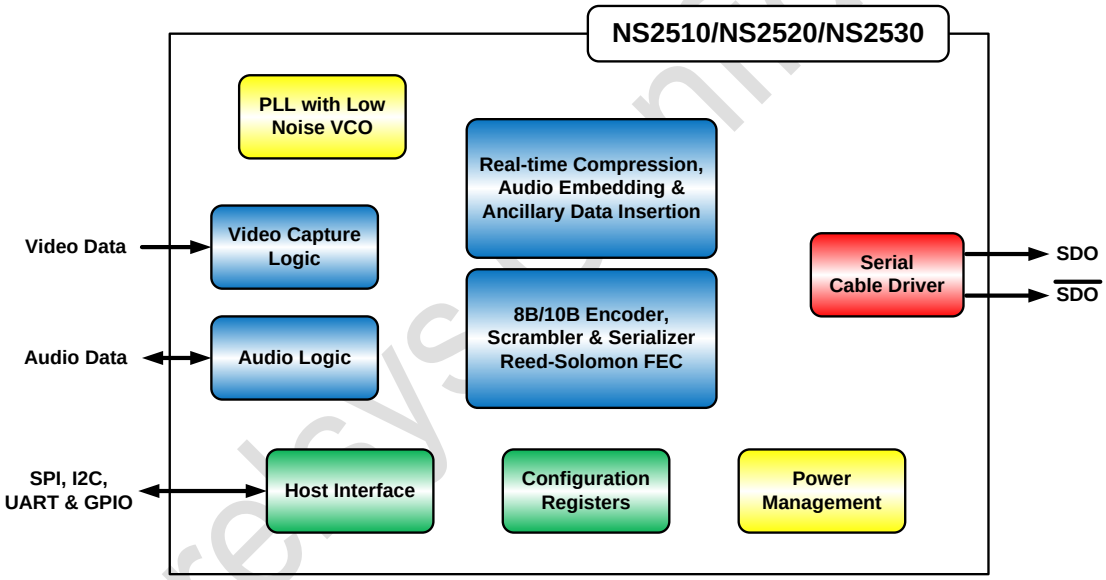


Figure 1. Functional Block Diagram

NS2510/NS2520/NS2530 implement advanced features such as transmission of downstream (camera to DVR) audio/control and upstream (DVR to Camera) audio/control over the same cable.

NS2510/NS2520/NS2530 support both coaxial cable and STP cable.

1.1. Related Documents

- EDN-5076, NS2511/NS2521/NS2531 Dual-port HD Video Receiver
- EDN-5077, NS2532 Dual-port Full HD Video Receiver

1.2. Applications

- Automotive camera and video

- Video surveillance
- Industrial camera and video

1.3. Features

Table 1. NS2510/NS2520/NS2530 Features

	NS2510	NS2520	NS2530
AVT Serial Interface			
Serial data rate	AVT compressed video: - 30Mbps-270Mbps Uncompressed video: - 270Mbps, 742.5Mbps	AVT compressed video: - 30Mbps-270Mbps Uncompressed video: - 270Mbps, 742.5Mbps, 1.485Gbps	AVT compressed video: - 30Mbps-371.25Mbps Uncompressed video: - 270Mbps, 742.5Mbps, 1.485Gbps, 2.970Gbps
Video formats (NS2510/NS2520/NS2530 support an extensive selection of video formats, for more details, see section 3.2.4)	Selective video formats AVT compressed mode: - HD 720p 24/25/30, HD 1080p 12/12.5/15 Uncompressed video mode: - SD-SDI, HD@742.5Mbps	Selective video formats AVT compressed mode: - HD 720p 24/25/30/50/60, HD 1080p 12/12.5/15/24/25/30 Uncompressed video mode: - SD-SDI, HD@742.5Mbps, HD-SDI	Selective video formats AVT compressed mode: - HD 720p 24/25/30/50/60, HD 1080p 12/12.5/15/24/25/30, HD 1080p 50/60 Uncompressed mode: - SD-SDI, HD@742.5Mbps, HD-SDI, 3G-SDI
Compression ratio	2 to 30		
Automatic adaptation of compression ratio	Yes		
Support forward error correction for compressed video	Yes, Reed-Solomon		
Embedded audio and AUX data forwarding from Pixel Interface	Yes		
Support loss of cable detection	Yes		
Supported cable types	Single-ended coaxial cable Shielded twisted pair cable		
Pixel Interface			
Pixel interface width	8/10/16 bits		
Pixel clock	Up to 148.5MHz		
Pixel interface sampling	SDR, sampled by pixel clock rising or falling edge; Setup/hold time programmable		
Pixel interface format	BT.656, BT.1120, DVP (Omnivision) YCbCr4:2:2 RGB (uncompressed video only)		

Pixel interface voltage	1.8/2.7/3.3V
Audio Interface	
Support bi-directional audio	Yes
Audio interface and format	Downstream (camera to DVR): - I2S master/slave, SPDIF slave - 2 channels - 8/16/24/32/44.1/48/96K samples per second - 16/20/24 bits per sample Upstream (DVR to camera): - I2S master/slave - 1 channel - 8K samples per second - 16 bits per sample
Support forward error correction for downstream (camera to DVR) audio	Yes, ECC
I2C and UART Interfaces	
Support bi-directional control	Yes, I2C and UART
I2C port	1 port, master or slave
UART port	Tx and Rx
SPI Flash Interface	
Support in-system programming of SPI Flash	Yes
Support sharing SPI Flash with ISP or other chips	Yes
Other	
Support clock output	Programmable 6/12/18/24/27/30/54/74.5MHz
Support RESETN output	Controlled by on-chip MCU
External crystal	27MHz, 300ppm
ESD	HBM pin 32 and 33 +/-8KV, other pins +/-4KV
CDM	+/-1KV
Package	QFN50, 7x5.5mm

2. Pin Assignment and Description

2.1. Pin Assignment

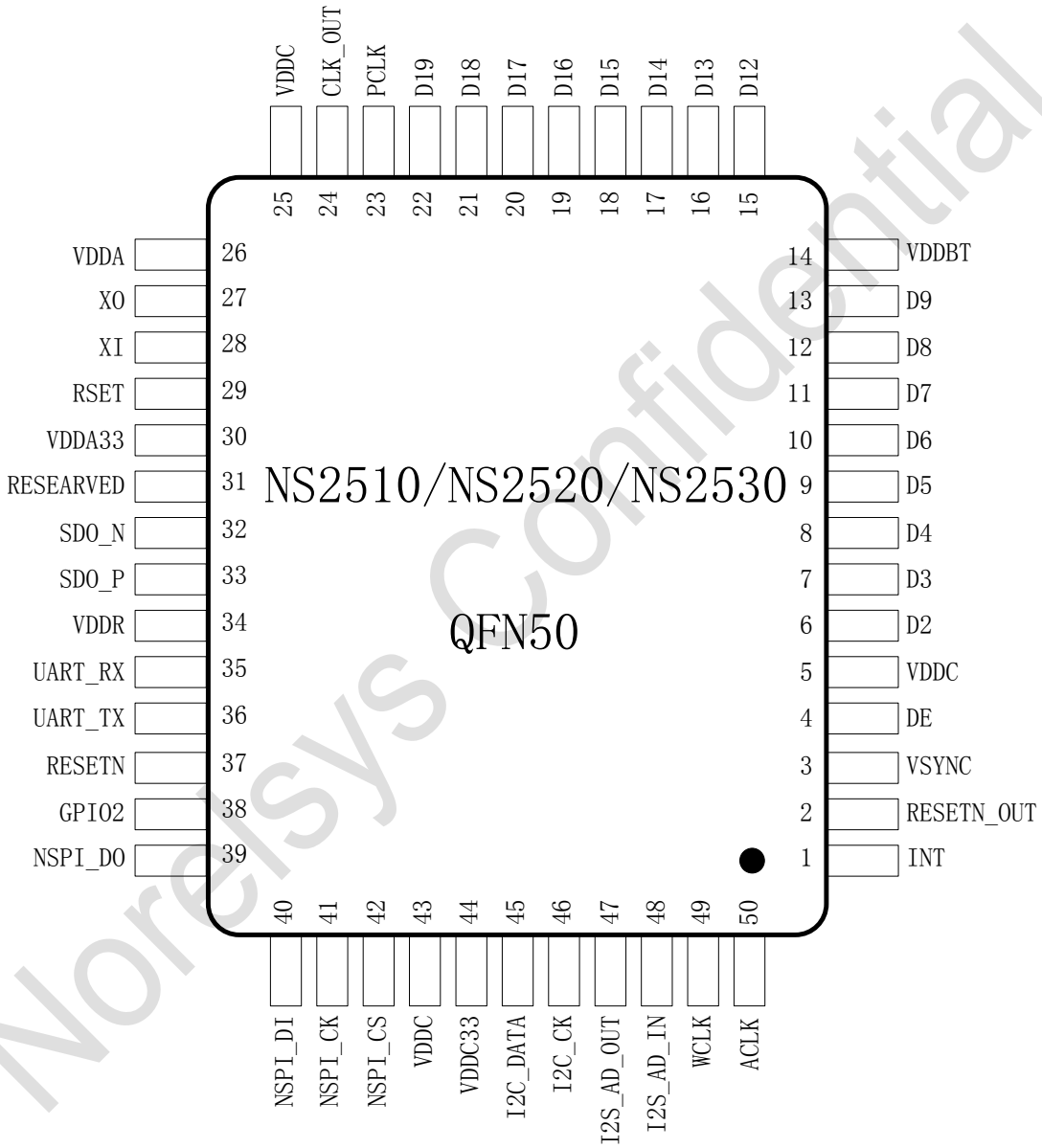


Figure 2. QFN50 Package Pin Assignment

2.2. Pin Descriptions

Table 2. Pin Type Definitions

Type	Description
I	Input
O	Output
I/O	Input/output
OD	Open drain driver
Hi-Z	Output in Hi-Z state
PH	Pull high resistor, nominal 100K
PL	Pull low resistor, nominal 100K
Off	PH and/or PL resistors are off
PH/PL/Off	Programmable PH on, PL on or both are off

Table 3. Pin Descriptions

Pin	Pin Name	Pin Type				Power Supply	Description
		During operation RESETN=HIGH		At reset RESETN=LOW			
		Type	PH/PL	Type	PH/PL		
AVT Serial Interface							
32	SDO_N	O	-	O	-	-	AVT Serial Interface signals.
33	SDO_P	O	-	O	-	-	
Pixel Interface							
6	D2	I	PH/PL/Off	I	Off	VDDBT	Pixel interface data input.
7	D3	I	PH/PL/Off	I	Off	VDDBT	
8	D4	I	PH/PL/Off	I	Off	VDDBT	
9	D5	I	PH/PL/Off	I	Off	VDDBT	
10	D6	I	PH/PL/Off	I	Off	VDDBT	
11	D7	I	PH/PL/Off	I	Off	VDDBT	
12	D8	I	PH/PL/Off	I	Off	VDDBT	
13	D9	I	PH/PL/Off	I	Off	VDDBT	
15	D12	I	PH/PL/Off	I	Off	VDDBT	
16	D13	I	PH/PL/Off	I	Off	VDDBT	
17	D14	I	PH/PL/Off	I	Off	VDDBT	
18	D15	I	PH/PL/Off	I	Off	VDDBT	
19	D16	I	PH/PL/Off	I	Off	VDDBT	
20	D17	I	PH/PL/Off	I	Off	VDDBT	
21	D18	I	PH/PL/Off	I	Off	VDDBT	
22	D19	I	PH/PL/Off	I	Off	VDDBT	
3	VSYNC	I	PH/PL/Off	I	Off	VDDBT	Pixel interface vertical sync.
4	DE	I	PH/PL/Off	I	Off	VDDBT	Pixel interface data enable.

23	PCLK	I	PH/PL/Off	I	Off	VDDBT	Pixel clock.
24	CLK_OUT	O	PH/PL/Off	Hi-Z	Off	VDDBT	Clock out (VDDBT power supply). Frequency is programmable to one of the following: 6, 12, 18, 24, 27, 30, 54, 74.25MHz.
1	INT	I/O	PH/PL/Off	I	Off	VDDBT	Interrupt output or GPIO.
2	RESETN_OUT	I/O	PH/PL/Off	I	Off	VDDBT	RESETN output (VDDBT power supply) or GPIO.
Audio Interface							
47	I2S_ AD_OUT	I/O	PH	I	PH	VDDC33	I2S_AD_OUT or GPIO.
48	I2S_ AD_IN	I/O	PH	I	PH	VDDC33	I2S_AD_IN or SPDIF_AD_IN or GPIO.
49	WCLK	I/O	PH	I	PH	VDDC33	I2S WCLK or GPIO.
50	ACLK	I/O	PH	I	PH	VDDC33	I2S ACLK or GPIO.
I2C and UART Interface							
35	UART_RX	I/O	PL	I	PL	VDDC33	UART_RX or RESETN_OUT33 or GIPO. UART_RX: UART Rx input. RESETN_OUT33: When set to RESETN_OUT33, this pin is similar to RESETN_OUT with the following differences (1) the internal PL is turned on for this pin during chip reset (RESETN=LOW) (2) this pin is powered by VDDC33 while RESETN_OUT is powered by VDDBT.
36	UART_TX	I/O	PH	I	PH	VDDC33	UART_TX or GPIO.
45	I2C_DATA	I/O, OD	-	I	-	VDDC33	I2C_DATA or GPIO.
46	I2C_CK	I/O, OD	-	I	-	VDDC33	I2C_CK or GPIO.
SPI Flash Interface							
39	NSPI_DO	I/O	PH	I	PH	VDDC33	Data output to SPI Flash or GPIO.
40	NSPI_DI	I/O	PH	I	PH	VDDC33	Data input from SPI Flash or LED0 or GPIO.
41	NSPI_CK	I/O	PH	I	PH	VDDC33	Clock output to SPI Flash or LED1 or GPIO.
42	NSPI_CS	I/O	PH	I	PH	VDDC33	Chip select to SPI Flash or GPIO.
Other							
37	RESETN	I	-	I	-	VDDC33	Chip RESETN input. Active low.

38	GPIO2	I/O	PH	I	PH	VDDC33	GPIO2 or CLK_OUT33 (VCC33 power supply). When set to CLK_OUT33, this pin is similar to CLK_OUT, the only difference is that this pin is powered by VDDC33 while CLK_OUT is powered by VDDBT. Frequency is programmable to one of the following: 6, 12, 18, 24, 27, 30, 54, 74.25MHz.
Analog Signals							
27	XO	O	-	O	-	VDDA33	Crystal output.
28	XI	I	-	I	-	VDDA33	Crystal input.
29	RSET	I	-	I	-	VDDA33	Analog input, a 750Ohm resistor should be connected between RSET and VDDA33.
31	Reserved	-	-	I	-	-	Reserved.
Power and Ground							
5, 25, 43	VDDC	Power	-	Power	-	-	1.2V digital power supply.
14	VDDBT	Power	-	Power	-	-	Digital power supply for pixel interface. It can be set to 1.8/2.7/3.3V.
26	VDDA	Power	-	Power	-	-	1.2V analog power supply.
30	VDDA33	Power	-	Power	-	-	3.3V analog power supply.
34	VDDR	Power	-	Power	-	-	1.2V digital power supply for serial interface.
44	VDDC33	Power	-	Power	-	-	3.3V digital power supply.
51	GND	GND	-	GND	-	-	Ground pad.

3. Functional Description

3.1. AVT Technologies

AVT (Advanced Video Transport) is a visual lossless compression and transmission technology, and it employs a low delay intra-frame video compression, using Norelsys proprietary algorithm. The required transmission bandwidth is only half of MJPEG algorithm in order to obtain the same image quality. Furthermore, the AVT technology supports configurable compression ratio to obtain the best image quality.

NS2510/NS2520/NS2530 not only makes use of the AVT technology but also integrates an on-chip FEC (forward error correction) module, using the Reed-solomon algorithm to correct the occurrence of transmission errors. NS2510/NS2520/NS2530 also integrates a serializer and a cable driver, supports from 30Mbps to 2.97Gbps transmission rate. In uncompressed mode, NS2510 is compatible with SD-SDI standard, NS2520 is compatible with SD/HD-SDI standard, while NS2530 is also compatible with 3G-SDI standard.

NS2510/NS2520/NS2530 supports reverse audio and control data transmission, and integrates a reverse direction signal receiving circuit, which makes it capable to transmit video, audio and control signals in forward direction (downstream) while receiving reverse (upstream) audio and control signals transferred on the same cable and at the same time. In addition I2C, UART TX/RX and audio input/output pins are also provided to communicate with the external devices.

3.2. Pixel Interface

The parallel video interface (Pixel Interface) supports RGB (uncompressed mode) and YCbCr 4:2:2 (compressed mode or uncompressed mode) color space, and supports BT.656, BT.1120 and OmniVision DVP input formats. The parallel video interface is 16-bit wide, which can receive 8/10/16 bits input video data. The Pixel Interface is powered by VDDBT and the voltage can be 3.3V, 2.7V or 1.8V.

The Pixel Interface contains D2~D9, D12~D19, a total of 16 data pins, a vertical synchronous signal VSYNC, a data enable signal DE, and a video clock signal PCLK. When the synchronization signal is embedded in the video data (for example, BT.656/BT.1120), VSYNC and DE are not used. When the input video employs an external synchronization mode (for example, DVP), the synchronization is based on VSYNC and DE.

The video input data, D2~D9, D12~D19, VSYNC and DE, are sampled by PCLK in single data rate (SDR) mode and the highest clock frequency of PCLK is 148.5MHz. The rising edge or falling edge of PCLK can be selected to capture input data. In addition, the specific sampling position (relative to the PCLK rising edge or falling edge) can also be finely tuned to provide maximum timing compatibility with the video source chip (Sensor or ISP, etc.).

In the example timing diagram of this chapter, the rising edge of PCLK is used to sampling data.

3.2.1. BT.656 YCbCr 4:2:2

In BT.656 format, the synchronization signal is embedded in the video stream. SAV and EAV are used to indicate the start and the end of active video in each line and occupy for 4 clock cycles. The space between EAV and SAV is the horizontal blanking area. The timing diagram is shown in Figure 3.

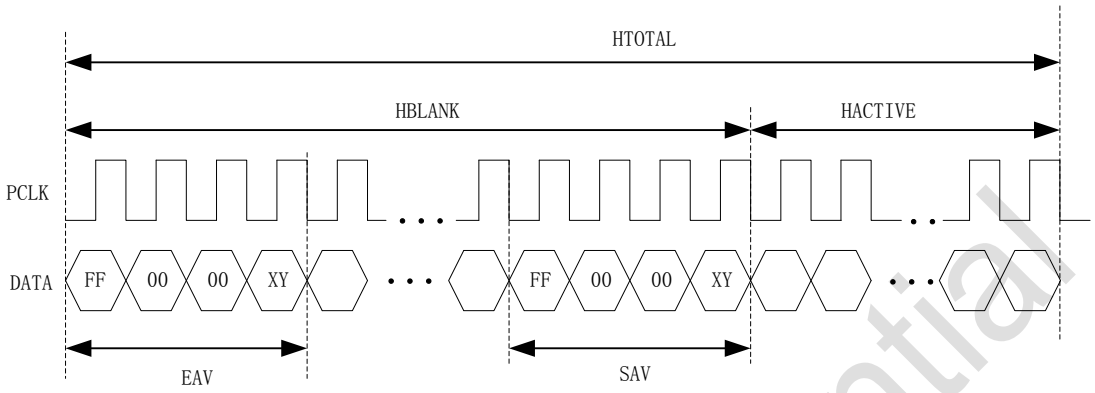


Figure 3. BT.656 Htotal Encoding

The timing diagram of active video area in each line is shown in Figure 4.

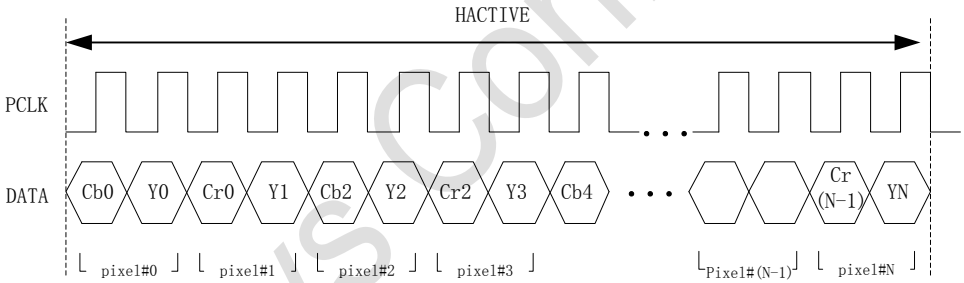


Figure 4. BT.656 Hactive Encoding YCbCr 4:2:2

In addition, NS2510/NS2520/NS2530 includes versatile pin-mapping features which provide maximum flexibility for users, as shown in Table 4 and Table 5.

Table 4. Pin Mapping for 8-bit BT.656, 8-bit BT.1120 and 8-bit DVP

Pin Name	8bit Default				8bit Bus-swap[1]				8bit Bit-swap			
	Pixel#0		Pixel#1		Pixel#0		Pixel#1		Pixel#0		Pixel#1	
	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2
D12	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D13	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D14	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D15	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D16	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D17	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D18	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D19	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]

Notes:

1、 With 8-bit width, bus-swap is only supported in compressed mode and is only supported in BT.656 and DVP formats.

2、 Bus-swap and bit-swap can be chosen at the same time.

Table 5. Pin Mapping for 10-bit BT.656, 10-bit BT.1120 and 10-bit DVP

Pin Name	10bit Default				10bit Bus-swap[1]				10bit Bit-swap			
	Pixel#0		Pixel#1		Pixel#0		Pixel#1		Pixel#0		Pixel#1	
	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2	Edge1	Edge2
D8	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]	Y0[0]	Cb0[0]	Y1[0]	Cr0[0]	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]
D9	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]	Y0[1]	Cb0[1]	Y1[1]	Cr0[1]	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]
D12	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]	Y0[2]	Cb0[2]	Y1[2]	Cr0[2]	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]
D13	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]	Y0[3]	Cb0[3]	Y1[3]	Cr0[3]	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]
D14	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]	Y0[4]	Cb0[4]	Y1[4]	Cr0[4]	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]
D15	Cb0[5]	Y0[5]	Cr0[5]	Y1[5]	Y0[5]	Cb0[5]	Y1[5]	Cr0[5]	Cb0[4]	Y0[4]	Cr0[4]	Y1[4]
D16	Cb0[6]	Y0[6]	Cr0[6]	Y1[6]	Y0[6]	Cb0[6]	Y1[6]	Cr0[6]	Cb0[3]	Y0[3]	Cr0[3]	Y1[3]
D17	Cb0[7]	Y0[7]	Cr0[7]	Y1[7]	Y0[7]	Cb0[7]	Y1[7]	Cr0[7]	Cb0[2]	Y0[2]	Cr0[2]	Y1[2]
D18	Cb0[8]	Y0[8]	Cr0[8]	Y1[8]	Y0[8]	Cb0[8]	Y1[8]	Cr0[8]	Cb0[0]	Y0[0]	Cr0[0]	Y1[0]
D19	Cb0[9]	Y0[9]	Cr0[9]	Y1[9]	Y0[9]	Cb0[9]	Y1[9]	Cr0[9]	Cb0[1]	Y0[1]	Cr0[1]	Y1[1]

Notes:

1、 With 10-bit width, bus-swap is only supported in compressed mode and is only supported in BT.656 and DVP formats.

2、 Bus-swap and bit-swap can be chosen at the same time.

3.2.2. BT.1120 YCbCr 4:2:2

BT.1120 format is similar to BT.656 format, except that SAV and EAV in each line occupy for 8 clock cycles. The timing diagram of 8/10-bit BT.1120 is shown in Figure 5.

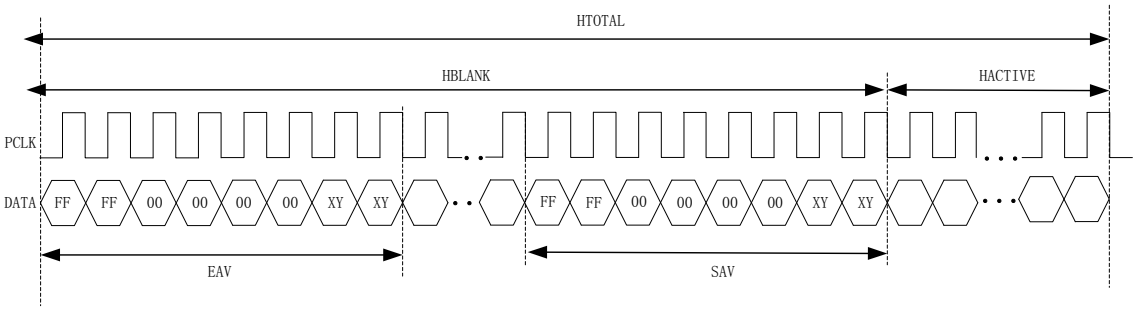


Figure 5. 8/10-bit BT.1120 Htotal Encoding

For BT.1120 format, NS2510/NS2520/NS2530 also supports various pin-mapping modes, as shown in above Table 4 and Table 5, except that 8/10-bit BT.1120 format does not support bus-swap function.

The timing diagram of 16-bit BT.1120 is shown in Figure 6.

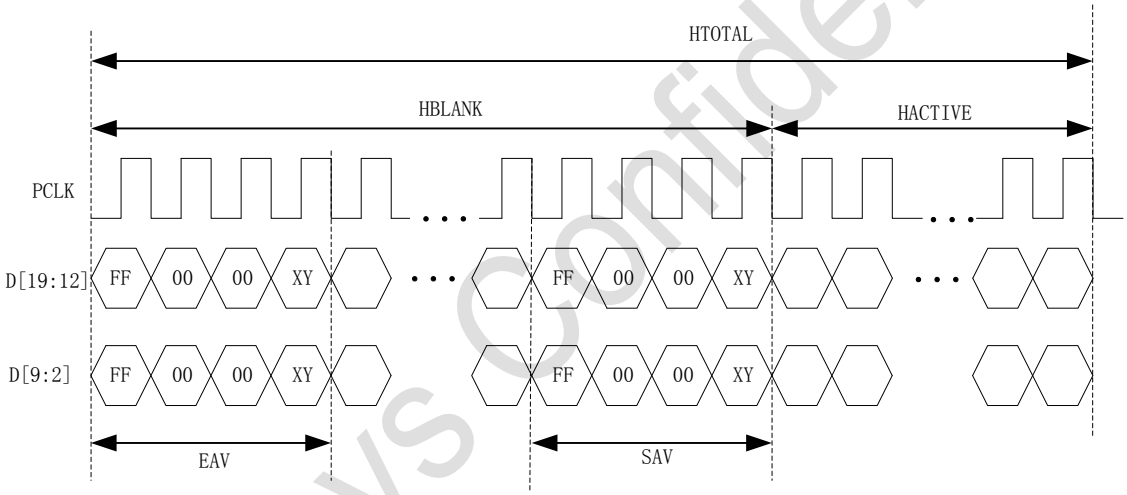


Figure 6. 16-bit BT.1120 Htotal Encoding

The timing diagram of active video area in each line is shown in Figure 7.

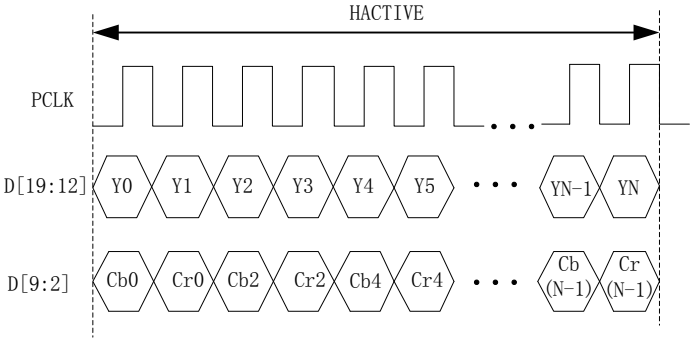


Figure 7. 16-bit BT.1120 Hactive Encoding YCbCr 4:2:2

The pin-mapping modes supported by 16-bit BT.1120 format in shown in Table 6.

Table 6. Pin Mapping for 16-bit BT.1120

Pin Name	16bit Default		16bit Bus-swap		16bit Bit-swap	
	Pixel#0	Pixel#1	Pixel#0	Pixel#1	Pixel#0	Pixel#1
D2	Cb0[0]	Cr0[0]	Y0[0]	Y1[0]	Cb0[7]	Cr0[7]
D3	Cb0[1]	Cr0[1]	Y0[1]	Y1[1]	Cb0[6]	Cr0[6]
D4	Cb0[2]	Cr0[2]	Y0[2]	Y1[2]	Cb0[5]	Cr0[5]
D5	Cb0[3]	Cr0[3]	Y0[3]	Y1[3]	Cb0[4]	Cr0[4]
D6	Cb0[4]	Cr0[4]	Y0[4]	Y1[4]	Cb0[3]	Cr0[3]
D7	Cb0[5]	Cr0[5]	Y0[5]	Y1[5]	Cb0[2]	Cr0[2]
D8	Cb0[6]	Cr0[6]	Y0[6]	Y1[6]	Cb0[1]	Cr0[1]
D9	Cb0[7]	Cr0[7]	Y0[7]	Y1[7]	Cb0[0]	Cr0[0]
D12	Y0[0]	Y1[0]	Cb0[0]	Cr0[0]	Y0[7]	Y1[7]
D13	Y0[1]	Y1[1]	Cb0[1]	Cr0[1]	Y0[6]	Y1[6]
D14	Y0[2]	Y1[2]	Cb0[2]	Cr0[2]	Y0[5]	Y1[5]
D15	Y0[3]	Y1[3]	Cb0[3]	Cr0[3]	Y0[4]	Y1[4]
D16	Y0[4]	Y1[4]	Cb0[4]	Cr0[4]	Y0[3]	Y1[3]
D17	Y0[5]	Y1[5]	Cb0[5]	Cr0[5]	Y0[2]	Y1[2]
D18	Y0[6]	Y1[6]	Cb0[6]	Cr0[6]	Y0[1]	Y1[1]
D19	Y0[7]	Y1[7]	Cb0[7]	Cr0[7]	Y0[0]	Y1[0]

Notes:

1、 Bus-swap and bit-swap can be chosen at the same time.

3.2.3. DVP YCbCr 4:2:2

For DVP format, a new frame is indicated by a long period of high level for VSYNC, and the active video is indicated by the high level for DE. The polarity of VSYNC and DE can also be changed with register control . The timing diagram of DVP format is shown in Figure 8.

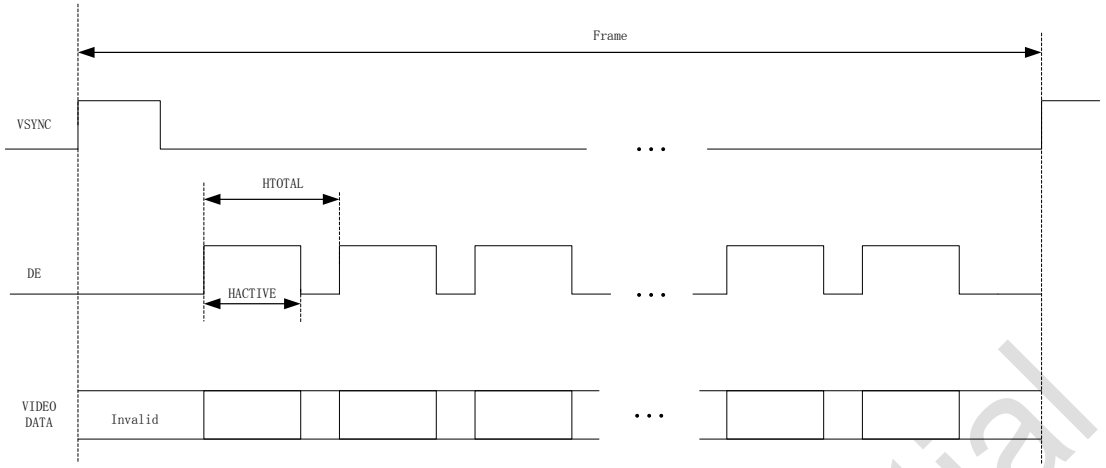


Figure 8. DVP Frame Definition

The timing diagram of active video area (HACTIVE) in each line for DVP format is shown in Figure 4.

For DVP format, various pin-mapping modes are also available，specifically reference to the above Table 4 and Table 5.

3.2.4. Supported Video Formats YCbCr 4:2:2

Table 7 lists the common video formats and the corresponding parameters supported by the YCbCr 4:2:2 color space. The main configurable parameters include the clock frequency of PCLK, compression ratio, Htotal, Vtotal, Hactive, Vactive and so on. NS2510/NS2520/NS2530 also supports more video formats that are not listed in the table.

In uncompressed mode, NS2510 is compatible with SD-SDI standard, NS2520 is compatible with SD/HD-SDI standard, while NS2530 is also compatible with 3G-SDI standard.

NS2510/NS2520/NS2530 supports more video formats in compressed mode but does not support interlaced video format.

Table 7. Supported Video Formats YCbCr 4:2:2

Type	Format	Frame Rate	Htotal (pixel)	Vtotal (pixel)	Hactive (pixel)	Vactive (pixel)	PCLK(MHz)		NS2510		NS2520		NS2530	
							8/10 bits	16 bits						
									uncompressed	compressed	uncompressed	compressed	uncompressed	compressed
SD-SDI [1]	525i	59.94	858	525	720	480	27	-	●		●		●	
		59.94	858	525	720	487	27	-	●		●		●	
		59.94	858	525	720	507	27	-	●		●		●	
	625i	50	864	625	720	576	27	-	●		●		●	
-	720p25RHB	25	1980	750	1280	720	74.25	37.125	●	●	●	●	●	●
-	720p30RHB	30	1650	750	1280	720	74.25	37.125	●	●	●	●	●	●
HD-SDI	720p24	24	4125	750	1280	720	148.5	74.25		●	●	●	●	●
	720p25	25	3960	750	1280	720	148.5	74.25		●	●	●	●	●
	720p30	30	3300	750	1280	720	148.5	74.25		●	●	●	●	●
	720p50	50	1980	750	1280	720	148.5	74.25			●	●	●	●
	720p60	60	1650	750	1280	720	148.5	74.25			●	●	●	●
-	1920x1080p12	12	2750	1125	1920	1080	74.25	37.125	●	●	●	●	●	●
-	1920x1080p12.5	12.5	2640	1125	1920	1080	74.25	37.125	●	●	●	●	●	●
-	1920x1080p15	15	2200	1125	1920	1080	74.25	37.125	●	●	●	●	●	●
HD-SDI	1080p24	24	2750	1125	1920	1080	148.5	74.25			●	●	●	●
	1080p25	25	2640	1125	1920	1080	148.5	74.25			●	●	●	●
	1080p30	30	2200	1125	1920	1080	148.5	74.25			●	●	●	●
	1080i50	50i	2640	1125	1920	1080	148.5	74.25			●		●	
	1080i60	60i	2200	1125	1920	1080	148.5	74.25			●		●	
3G-SDI	1080p50	50	2640	1125	1920	1080	-	148.5					●	●
	1080p60	60	2200	1125	1920	1080	-	148.5					●	●
-	1280x960p12.5	12.5	2160	1000	1280	960	54	27		●		●		●
-	1280x960p15	15	1800	1000	1280	960	54	27		●		●		●
-	1280x1024p15	15	1688	1066	1280	1024	54	27		●		●		●
-	1280x960p25	25	2160	1000	1280	960	108	54				●		●
-	1280x960p30	30	1800	1000	1280	960	108	54				●		●
-	1280x1024p30	30	1688	1066	1280	1024	108	54				●		●
VESA	1280x960p50	50	2160	1000	1280	960	-	108						●
	1280x960p60	60	1800	1000	1280	960	-	108						●
VESA	1280x1024p60	60	1688	1066	1280	1024	-	108						●

Note: [1] Pixel Interface should be set to 8/10 bits BT.656 for SD formats.

3.3. Audio Embedding and Control

NS2510/NS2520/NS2530 support audio embedding and control packets transmission in horizontal and vertical blanking region of digital video through AVT serial link. The embedded audio and control packets are compatible with SMPTE 272, SMPTE 299 and SMPTE 291 standard.

In non-compression case, there are four operation modes in which audio and control packets can be manipulated described as below.

3.3.1. Pass-through Mode

In pass-through mode, audio and control packets in the video stream will remain unchanged. Altering or inserting new audio and control packets is not permitted.

3.3.2. Appending Mode

In appending mode, the original embedded audio and control packets in the video stream will not be altered, furthermore, new embedded audio and control packets can be superimposed on this basis. Except for that if the audio packets already exists in the video stream, the embedded audio packets cannot be superimposed.

3.3.3. Replacing Mode

In replacing mode, the original embedded audio and control packets in the video stream will be deleted, and the audio data from the audio interface is packaged which conforms to the SMPTE 272 or SMPTE 299 standard. The control information that needs to be sent is also packaged which conforms to the SMPTE 291 standard. Then the audio and control packets will be embedded in the video stream.

3.3.4. Eliminating Mode

The eliminating mode is similar to the replacing mode, except that no packets will be inserted after the original embedded audio and control packets in the video stream are removed.

In compression case, the embedded audio and control packet operations are in the same way as in non-compression case. However, because the bandwidth of the blanking region in the AVT serial link is much smaller than that of the parallel video interface, the user should pay attention to the bandwidth consumed by the embedded audio and control packets is not exceeding the limitation of the AVT serial link.

3.4. Audio Interface

NS2510/NS2520/NS2530 supports I2C and SPDIF interfaces. The I2C interface supports audio input and output and can be configured as master or slave mode. The SPDIF interface only supports audio input and shares the data pin with I2C interface.

Table 8. Audio interface signals

Signal Name	Description
I2S_AD_OUT	I2S data output.
I2S_AD_IN	I2S data input or SPDIF data input.
WCLK	Left/Right channel clock. This signal is input in I2S slave mode or output in I2S master mode.
ACLK	Bit clock. This signal is input in I2S slave mode or output in I2S master mode.

I2S_AD_IN is the audio input pin of forward transmission channel, which can be configured as I2C or SPDIF input, and supports two channel audio, 8/16/24/32/44.1/48/96KHz sampling rate, 16/20/24 bits sampling accuracy, left-justified/right-justified data format and configurable WCLK polarity.

I2S_AD_OUT is the audio output pin of reverse transmission channel, which supports only mono audio up to 8KHz sampling rate, 16bits sampling accuracy, left-justified/right-justified data format and configurable WCLK polarity.

Four typical audio configuration modes are shown in Figure 9.

- Mode1: audio input/output configured as I2S interface, master mode.
- Mode2: audio input/output configured as I2S interface, slave mode.
- Mode3: audio input configured as SPDIF interface, and audio output configured as I2S interface, master mode.
- Mode4: audio input configured as SPDIF interface, and audio output configured as I2S interface, slave mode.

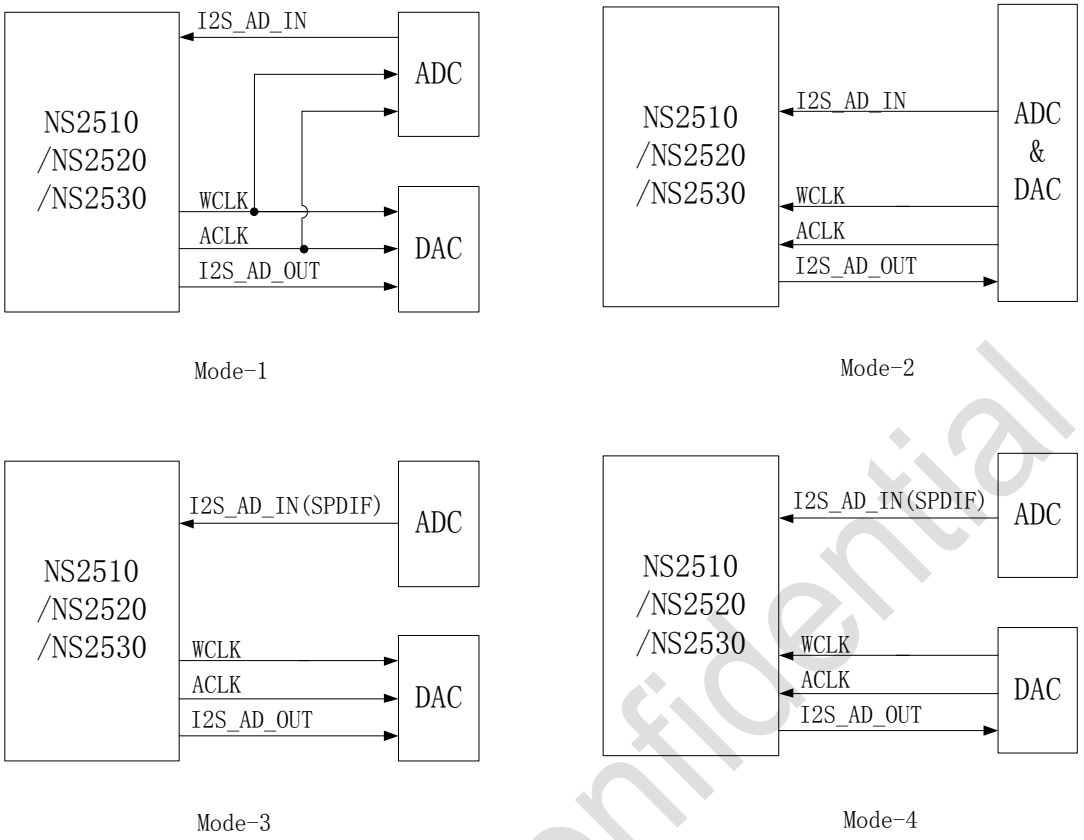


Figure 9. Audio Interface Topologies

3.5. I2C and UART Interface

NS2510/NS2520/NS2530 supports a standard I2C interface which is in slave mode after power on. The firmware can then configure it as master or slave mode. NS2510/NS2520/NS2530 also supports a standard UART TX and UART RX interface.

NS2510/NS2520/NS2530 supports the transmission of bidirectional control signals. The I2C and UART RX interface can be used as the initiator of the forward control flow, transmitting commands through the AVT serial link to the receiving end of the video stream, to configure the I2C/UART/GPIO/Register or other functions of the receiving end. The I2C interface and UART TX can also be used as the executer of the reverse control flow to receive and execute commands from the receiving end of the video stream.

3.6. SPI Flash Interface

NS2510/NS2520/NS2530 contains an SPI Flash Interface to connect external SPI Flash devices in which the firmware code can be stored. NS2510/NS2520/NS2530 also supports the sharing of external SPI Flash with other chips (such as Sensor or ISP chips) to reduce system costs and reduce PCB area.

3.7. Boot, Firmware Loading and Update

After power on and reset operation, the bootloader inside NS2510/NS2520/NS2530 will first attempt to load firmware code from the external SPI Flash. If the external SPI Flash does not exist, or if there is no valid firmware, then bootloader will wait to receive firmware from I2C interface. After the effective firmware is

loaded to the on-chip SRAM, bootloader will switch control to firmware, and complete firmware loading process.

NS2510/NS2520/NS2530 supports accessing external SPI Flash and updating firmware through I2C interface. This function can be used to realize initial burning of firmware to external SPI Flash.

NS2510/NS2520/NS2530 also supports accessing external SPI Flash and updating firmware through the reverse transmission channel. This function can be used to realize remote firmware update.

3.8. Reset and Clock Output

NS2510/NS2520/NS2530 provides reset and clock output signals in order to improve the system integration.

RESETN_OUT and CLK_OUT are powered by VDDBT, the voltage can be 3.3V, 2.7V or 1.8V. These two pins also can be configured as GPIOs when not used as reset and clock output signals.

When used as reset output signal, the RESETN_OUT pin requires an external pull-down resistor which provides an active low reset signal to other chips such as Sensor or ISP. After the firmware runs, the RESETN_OUT can be driven high at the appropriate time to remove Sensor or ISP resets.

When used as clock output signal, the CLK_OUT can be configured to output one of the following frequencies: 6/12/18/24/27/30/54/74.25MHz.

NS2510/NS2520/NS2530 also provides another set of reset and clock output signals RESETN_OUT33 and CLK_OUT33 which are powered by VDDC33, fixed at 3.3V voltage.

RESETN_OUT33 can be used as UART_RX or GPIO function. The RESETN_OUT33 pin has a built-in pull-down resistor, so there is no need to add an external resistor. CLK_OUT33 also can be used as GPIO function. When configured as clock output, its function is the same as CLK_OUT.

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 9. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VDDC/VDDA/VDDR	1.2V supply voltage	-0.3 to 1.5	V
VDDA33/VDDC33	3.3V supply voltage	-0.3 to 4.0	V
VDDBT	Pixel interface supply voltage 1.8V/2.7V/3.3V	-0.3 to 4.0	V
$T_{STORAGE}$	Storage temperature	-65 to 150	℃
T_J	Junction temperature	-40 to 125	℃

4.2. Recommended Operating Conditions

Table 10. Recommended Operating Conditions

Symbol	Parameter	Min	Type	Max	Unit
VDDC/VDDA/VDDR	1.2V supply voltage	1.14	1.2	1.32	V
VDDA33/VDDC33	3.3V supply voltage	3.0	3.3	3.6	V
VDDBT	1.8V supply voltage	1.7	1.8	1.9	
	2.7V supply voltage	2.5	2.7	2.9	
	3.3V supply voltage	3.0	3.3	3.6	V
T_A	Operating free-air temperature range	-40	-	105	℃

4.3. Clock Requirements

Table 11. Clock Requirements

Parameter	Min	Type	Max	Unit
Crystal frequency	-	27	-	MHz
Crystal frequency tolerance	-300	-	300	ppm
PCLK frequency	-	-	148.5	MHz
PCLK duty cycle	40	-	60	%

4.4. DC Characteristics for Digital IO

Table 12. DC Characteristics for Digital IO

Symbol	Parameter	Min	Type	Max	Unit
V_{IH18}	Input high level for 1.8V digital IO	1.1	-	-	V
V_{IL18}	Input low level for 1.8V digital IO	-	-	0.4	V
V_{OH18}	Output high level for 1.8V digital IO	1.3	-	-	V
V_{OL18}	Output low level for 1.8V digital IO	-	-	0.2	V
V_{IH27}	Input high level for 2.7V digital IO	1.6	-	-	V
V_{IL27}	Input low level for 2.7V digital IO	-	-	0.6	V
V_{OH27}	Output high level for 2.7V digital IO	2.0	-	-	V
V_{OL27}	Output low level for 2.7V digital IO	-	-	0.3	V
V_{IH33}	Input high level for 3.3V digital IO	2.0	-	-	V
V_{IL33}	Input low level for 3.3V digital IO	-	-	0.8	V
V_{OH33}	Output high level for 3.3V digital IO	2.4	-	-	V
V_{OL33}	Output low level for 3.3V digital IO	-	-	0.4	V

4.5. Power Up and Reset Timing

The Power Up and Reset Timing rules are defined in this section. Designers should follow all the rules for external power designs. Detailed explanations are listed below:

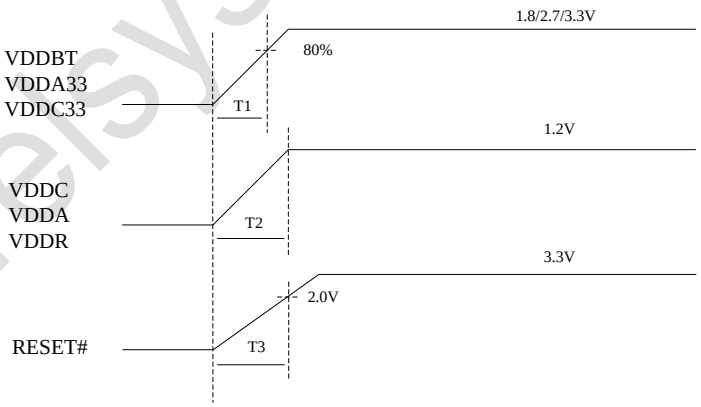


Figure 10. Power Up and Reset Timing

T1: Rise time for VDDBT/VDDA33/VDDC33 power rail form 0V to 80% of target voltages

T2: Rise time for VDDC/VDDA/VDDR power rail form 0V to 1.2V

T3: Rise time for RESET# signal from 0V to 2.0V

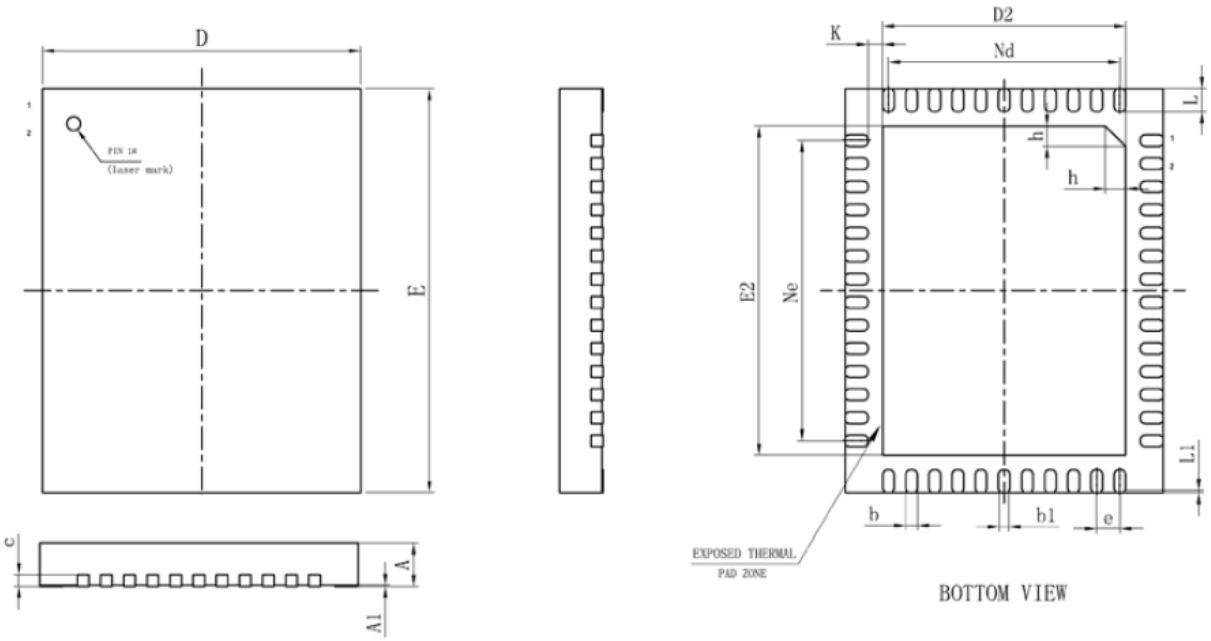
The recommended power sequence and timing requirements are listed in Table 13.

Table 13. Power Up and Reset Timing Requirement

Time	Min	Max
T1	0.01ms	1ms
T2	0.01ms	1ms
T3	15ms	-

5. Package Information

5.1. 50 pin QFN (7x5.5) package



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
b1	0.11	0.16	0.21
c	0.203REF		
D	5.40	5.50	5.60
D2	4.10	4.20	4.30
e	0.40BSC		
Nd	4.00BSC		
Ne	5.20BSC		
E	6.90	7.00	7.10
E2	5.60	5.70	5.80
L	0.35	0.40	0.45
L1	—	0.04	0.07
K	0.20	—	—
h	0.30	0.35	0.40
L/F载体尺寸 (Mil)	173X232		

Figure 11. 50pin QFN Package Mechanical Data