

## LMK6x Low Jitter, High-Performance BAW Oscillator

### 1 Features

- High-performance differential and single-ended output Oscillator, supporting any fixed frequency within the below range:
  - LMK6D: 1 to 400 MHz, LVDS output
  - LMK6H: 1 to 400 MHz, HCSL output
  - LMK6P: 1 to 400 MHz, LVPECL output
  - LMK6C: 1 to 200 MHz, LVCMS output
- Ultra-low jitter:
  - LMK6D/LMK6H/LMK6P: 100-fs typical / 125-fs maximum RMS jitter at 156.25 MHz (12 kHz to 20 MHz)
  - LMK6C: 350-fs typical / 500-fs maximum RMS jitter at 100 MHz (12 kHz to 20 MHz)
  - LMK6H: PCIe Gen 1 to Gen 6 compliant
- $\pm 25$  ppm total frequency stability inclusive of 10 years aging and all other factors
- Smallest industry standard DLE and DLF packages
- Support extended industrial temperature grade:
  - LMK6P/LMK6D/LMK6H:  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
  - LMK6C:  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$
- Integrated LDO for robust supply noise immunity:
  - $-72$  dBc PSRR at 500 kHz ripple
- Start-up time: < 5 ms
- Standard frequencies:
  - LVCMS (MHz): 4, 8.192, 12, 20, 24, 25, 33.333, 40, 50, 60, 65.53, 74.25, 100, 125 and 156.25
  - Differential (MHz): 51.84, 100, 122.88, 125, 148.5, 155.52, 156.25, 161.1328125, 200 and 312.5
- Device can support any frequency between 1 MHz to 400 MHz. Contact TI representative for any frequency and samples needed

### 2 Applications

- 56G/112G PAM4 clocking
- 100G/200G/400G/800G Optical Transport Network and Coherent Optics
- Network equipment, switches, routers, line cards, SAN, data centers and baseband units (BBU)
- PCIe Gen 1 to Gen 6 compliant reference clock
- Industrial applications
- Test and measurement
- ASIC, FPGA, MCU reference clocking
- High-performance crystal oscillator replacement

### 3 Description

Texas Instruments' Bulk-Acoustic Wave (BAW) is a micro-resonator technology that enables integration of high-precision BAW resonator directly into packages with ultra-low jitter clock circuitry. BAW is fully designed and manufactured at TI factories like other silicon-based fabrication processes.

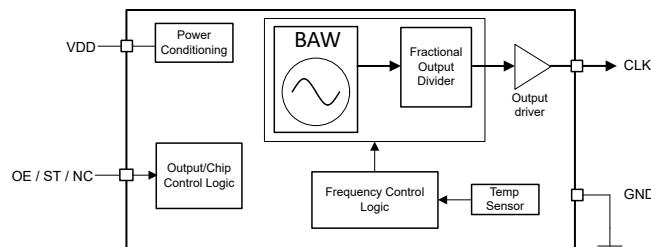
The LMK6x device is an ultra-low jitter, fixed-frequency oscillator which incorporates the BAW as the resonator source. The device is factory-programmed per specific operation mode, including frequency, voltage, output type, and function pin. With a high-performance fractional frequency divider, the LMK6x is capable of producing any frequency within the specified range providing a single device family for all frequency needs.

The high-performance clocking, mechanical stability, flexibility, and small package options for this device are designed for reference and core clocks in high-speed SERDES used in telecommunications, data and enterprise network, and industrial applications.

### Package Information

PART NUMBER	OUTPUT TYPE	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
LMK6C	LVCMS	VSON (DLE-4)	3.20 mm x 2.50 mm
LMK6C		VSON (DLF-4)	2.50 mm x 2.00 mm
LMK6D	LVDS, HCSL, LVPECL	VSON (DLE-6)	3.20 mm x 2.50 mm
LMK6H			
LMK6P			
LMK6D	VSON (DLF-6)		
LMK6H			
LMK6P			2.50 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



LMK6C Simplified Block Diagram



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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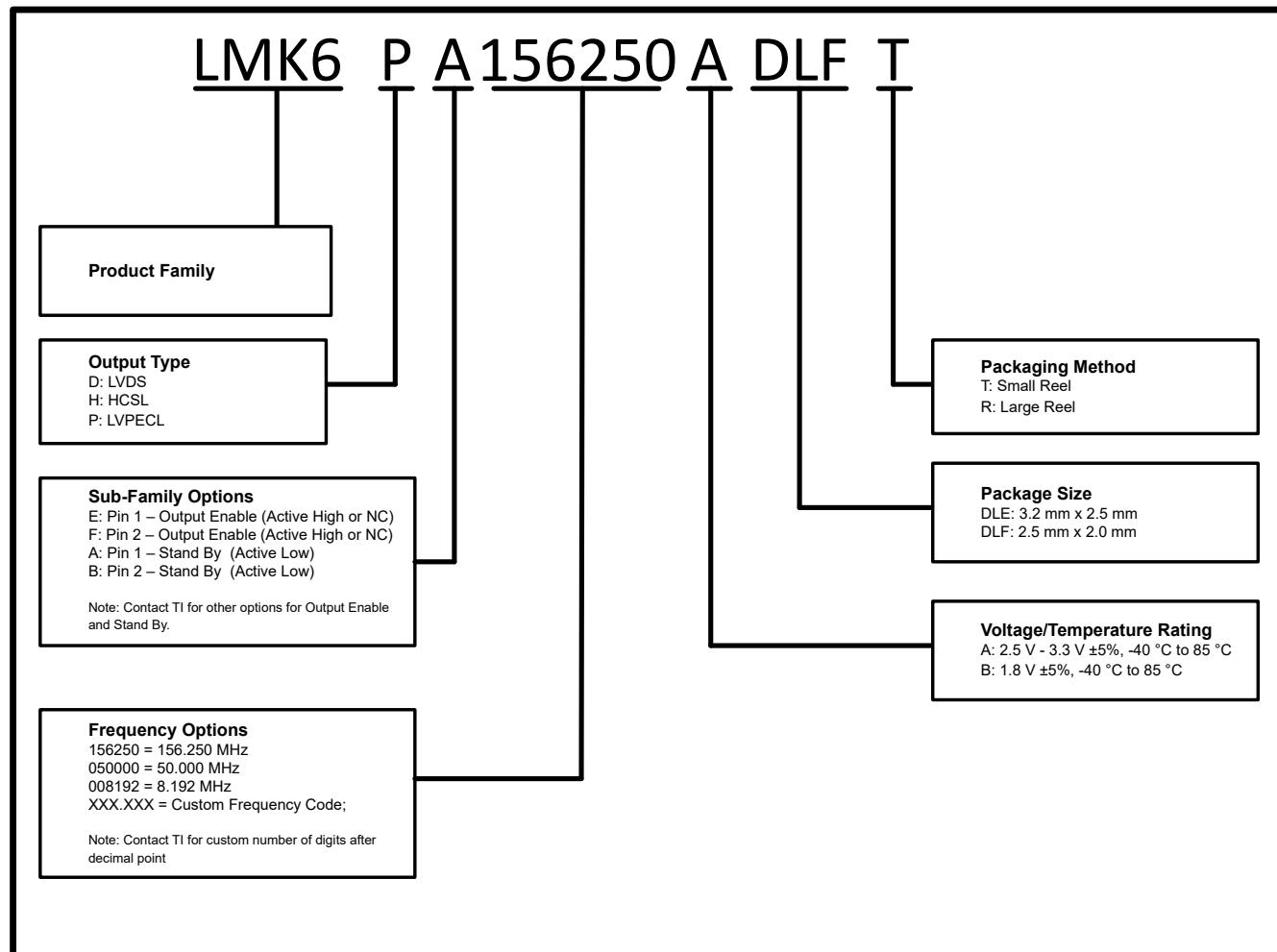
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision C (December 2022) to Revision D (February 2023)</b>	<b>Page</b>
• Changed the NO. column to DLE/DLF in the <i>Pin Functions</i> table for the DLF package release.....	<b>5</b>
<hr/>	
<b>Changes from Revision B (November 2022) to Revision C (December 2022)</b>	<b>Page</b>
• Changed the data sheet status from Advanced Information to Production Data.....	<b>1</b>
• Removed the preview note from the LMK6D, LMK6H, and LMK6P devices.....	<b>1</b>

## 5 Device Ordering Information

Use [Figure 5-1](#) and [Figure 5-2](#) to understand the device nomenclature of the LMK6x orderable options.



**Figure 5-1. Part Number Guide: LMK6D, LMK6H, and LMK6P**

Note: Contact a TI representative to pre-order specific devices. Email: [ti\\_osc\\_customer\\_requirement@list.ti.com](mailto:ti_osc_customer_requirement@list.ti.com)

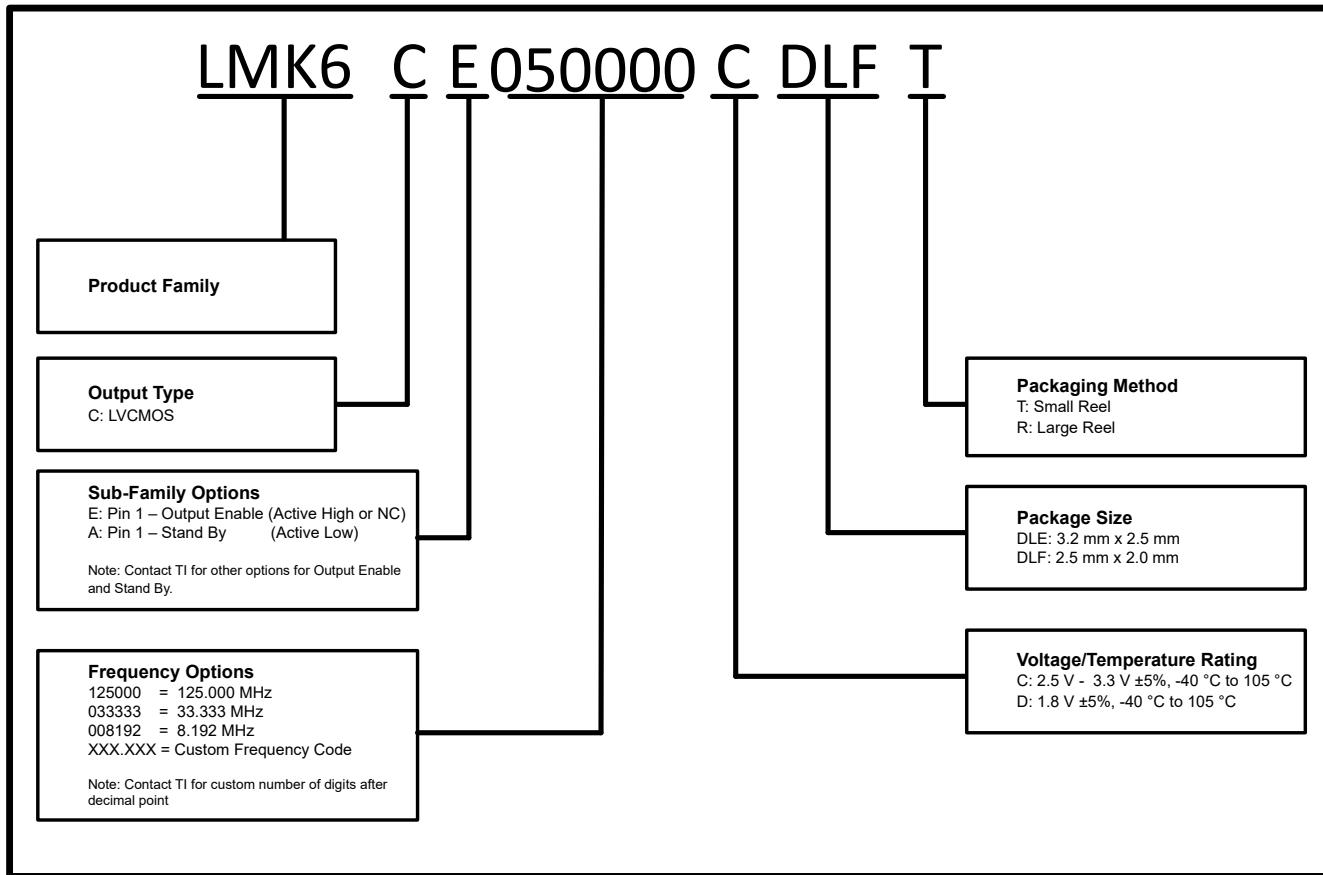
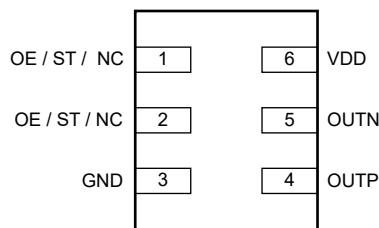


Figure 5-2. Part Number Guide: LMK6C

Note: Contact a TI representative to pre-order specific devices. Email: [ti\\_osc\\_customer\\_requirement@list.ti.com](mailto:ti_osc_customer_requirement@list.ti.com)

## 6 Pin Configuration and Functions

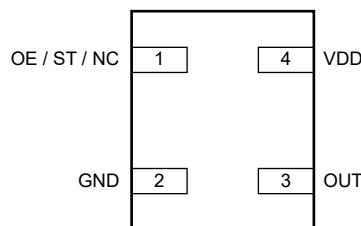


**Figure 6-1. LMK6P, LMK6D, or LMK6H 6-Pin VSON (Top View)**

**Table 6-1. LMK6P, LMK6D, or LMK6H Pin Functions**

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	DLE/DLF		
OE / ST / NC	1	I / NC	Output Enable (OE) or Standby (ST) pin or No Connect (NC). See <a href="#">Table 9-1</a> for more details.
OE / ST / NC	2	NC / I	Output Enable (OE) or Standby (ST) pin or No Connect (NC). See <a href="#">Table 9-1</a> for more details.
GND	3	G	Device ground
OUTP	4	O	Positive differential output clock
OUTN	5	O	Negative differential output clock
VDD	6	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect (can be left floating).



**Figure 6-2. LMK6C 4-Pin VSON (Top View)**

**Table 6-2. LMK6C Pin Functions**

PIN		I/O <sup>(1)</sup>	DESCRIPTION
NAME	DLE/DLF		
OE / ST / NC	1	I / NC	Output Enable (OE) or Standby (ST) pin or No Connect (NC). See <a href="#">Table 9-2</a> for more details.
GND	2	G	Device ground
OUT	3	O	LVCMS output clock
VDD	4	P	Device power supply

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power, NC = No Connect (can be left floating).

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
VDD	Device Supply Voltage <sup>(2)</sup>	-0.3	3.63	V
	Device Supply Voltage <sup>(3)</sup>	-0.3	1.98	V
EN	Logic Input Voltage	-0.3	VDD + 0.3	V
OUTP, OUTN	Clock Output Voltage <sup>(4)</sup>	-0.3	VDD + 0.3	V
OUT	Clock Output Voltage <sup>(5)</sup>	-0.3	VDD + 0.3	V
T <sub>J</sub>	Junction Temperature		125	°C
T <sub>STG</sub>	Storage Temperature		150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) For all devices with Recommended Operating Voltage of 2.5 V +/- 5% and 3.3 V +/- 5%

(3) For all devices with Recommended Operating Voltage of 1.8 V +/- 5%

(4) For all differential outputs - LMK6D, LMK6H, and LMK6P.

(5) For single ended outputs - LMK6C.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Environmental Compliance

		VALUE	UNIT
Mechanical Shock Resistance	MIL-STD-883F, Method 2002, Condition A	1500	g
Mechanical Vibration Resistance	MIL-STD-883F, Method 2026, Condition C	10	g
	MIL-STD-883F, Method 2007, Condition A	20	g
Moisture Sensitivity Level (MSL)		MSL1	

### 7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device Supply Voltage <sup>(1)</sup>	1.7	1.8	1.9	V
	Device Supply Voltage <sup>(2)</sup>	2.37	2.5, 3.3	3.5	V
T <sub>A</sub>	Ambient temperature <sup>(3)</sup>	-40		85	°C
	Ambient temperature <sup>(4)</sup>	-40		105	°C
T <sub>J</sub>	Junction temperature			125	°C
t <sub>RAMP</sub>	VDD power-up ramp time <sup>(1) (2)</sup>	0.1		100	ms

(1) For all devices with Recommended Operating Voltage of 1.8V +/- 5%

(2) For all devices with Recommended Operating Voltage of 2.5V +/- 5% and 3.3V +/- 5%

(3) For all differential outputs - LMK6D, LMK6H and LMK6P.

(4) For single-ended output - LMK6C.

## 7.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMK6D/H/P		UNIT
		DLE (VSON)	DLF (VSON)	
		6 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	101.2	107.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	58.6	70.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	31.3	39.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.7	2.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	31.1	39.2	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.6 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMK6C		UNIT
		DLE (VSON)	DLF (VSON)	
		4 PINS	4 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	124.8	128.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	61.2	73.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	42.5	39.8	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	2.8	2.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	42.3	39.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.7 Electrical Characteristics

over recommended operating conditions, typical temperature = 25°C, frequency output = 156.25 MHz, VDD = 3.3 V, LVC MOS output capacitor load = 2.2 pF (unless otherwise specified)<sup>(4)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Current Consumption Characteristics</b>					
$I_{DD}$	Device power consumption (LVPECL, VDD = 2.5 V/3.3 V, excluding load current)	100 MHz	65	82	mA
		156.25 MHz	69	87	mA
		200 MHz	67	85	mA
		312.5 MHz	76	95	mA
		400 MHz	88	108	mA
	Device power consumption (LVPECL, VDD = 1.8 V, excluding load current)	100 MHz	61	79	mA
		156.25 MHz	66	83	mA
		200 MHz	64	82	mA
		312.5 MHz	73	91	mA
		400 MHz	84	104	mA
$I_{DD}$	Device power consumption (HCSL, VDD = 2.5 V/3.3 V, excluding load current)	100 MHz	65	82	mA
		156.25 MHz	69	87	mA
		200 MHz	67	86	mA
		312.5 MHz	76	96	mA
		400 MHz	88	108	mA
	Device power consumption (HCSL, VDD = 1.8 V, excluding load current)	100 MHz	58	75	mA
		156.25 MHz	62	80	mA
		200 MHz	60	78	mA
		312.5 MHz	69	88	mA
		400 MHz	77	97	mA
$I_{DD}$	Device power consumption (LVDS, VDD = 2.5 V/3.3 V, excluding load current)	100 MHz	54	71	mA
		156.25 MHz	58	75	mA
		200 MHz	56	74	mA
		312.5 MHz	65	84	mA
		400 MHz	76	96	mA
	Device power consumption (LVDS, VDD = 1.8 V, excluding load current)	100 MHz	52	68	mA
		156.25 MHz	56	72	mA
		200 MHz	54	71	mA
		312.5 MHz	63	80	mA
		400 MHz	74	92	mA
$I_{DD}$	Device power consumption (LVC MOS, VDD = 2.5 V / 3.3 V, with load)	100 MHz	45	62	mA
		156.25 MHz	55	71	mA
		200 MHz	61	77	mA
	Device power consumption (LVC MOS, VDD = 1.8 V, with load)	100 MHz	44	59	mA
		156.25 MHz	50	65	mA
		200 MHz	56	72	mA
$I_{DD-STBY}$	Device standby current	ST (Standby) = GND	6	13	mA
$I_{DD-PD}$	Device current with output disabled (100 MHz)	OE = GND, LVPECL mode, VDD = 3.3 V	48	67	mA
		OE = GND, HCSL mode, VDD = 3.3 V	49	67	mA
		OE = GND, LVDS mode, VDD = 3.3 V	49	66	mA
		OE = GND, LVC MOS mode, VDD = 3.3 V	40	56	mA

over recommended operating conditions, typical temperature = 25°C, frequency output = 156.25 MHz, VDD = 3.3 V, LVC MOS output capacitor load = 2.2 pF (unless otherwise specified)<sup>(4)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LVPECL Output Characteristics</b>						
$F_{out}$	Output frequency		1	400	400	MHz
$V_{OD}$	Output voltage swing ( $V_{OH} - V_{OL}$ )	AC coupled, VDD = 3.3 V	525	645	765	mV
		AC coupled, VDD = 2.5 V	450	555	660	mV
		AC coupled, VDD = 1.8 V	280	375	470	mV
		DC coupled, VDD = 2.5 V/3.3 V <sup>(1)</sup>	650	800	950	mV
		DC coupled, VDD = 1.8 V <sup>(1)</sup>	450	600	750	mV
$V_{OD,DIFF}$	Differential output peak-peak swing		$2 \times  V_{OD} $		$V_{pp}$	
$V_{OS}$	Output common-mode voltage	VDD = 3.3 V <sup>(1)</sup>	1.5	1.6	1.7	V
		VDD = 2.5 V <sup>(1)</sup>	0.825	0.9	0.975	V
		VDD = 1.8 V <sup>(1)</sup>	0.45	0.5	0.55	V
$t_R/t_F$	Output rise/fall time	20% to 80% of $V_{OD,DIFF}$ , VDD = 2.5 V/3.3 V	120	200	200	ps
		20% to 80% of $V_{OD,DIFF}$ , VDD = 1.8 V	120	200	200	ps
ODC	Output duty cycle	VDD = 2.5 V/3.3 V, measured between 50% points on the waveform	45	50	55	%
		VDD = 1.8 V, measured between 50% points on the waveform	45	50	55	%
<b>LVDS Output Characteristics</b>						
$F_{out}$	Output frequency		1	400	400	MHz
$V_{OD}$	Output voltage swing ( $V_{OH} - V_{OL}$ )	Under LVDS load condition	250	350	450	mV
$V_{OD,DIFF}$	Differential output peak-peak swing		$2 \times  V_{OD} $		$V_{pp}$	
$V_{OS}$	Output common-mode voltage	VDD = 2.5 V/3.3 V	1.025	1.2	1.375	V
		VDD = 1.8 V	0.80	0.9	1.0	V
$t_R/t_F$	Output rise/fall time	20% to 80% of $V_{OD,DIFF}$ , VDD = 2.5 V/3.3 V	150	250	250	ps
		20% to 80% of $V_{OD,DIFF}$ , VDD = 1.8 V	150	250	250	ps
ODC	Output duty cycle	VDD = 2.5 V/3.3 V, measured between 50% points on the waveform	45	50	55	%
		VDD = 1.8 V, measured between 50% points on the waveform	45	50	55	%
<b>HCSL Output Characteristics</b>						
$F_{out}$	Output frequency		1	400	400	MHz
$V_{OH}$	Output high voltage	DC coupled, 50 Ω to ground, VDD = 2.5 V/3.3 V	650	750	850	mV
		DC coupled, 50 Ω to ground, VDD = 1.8 V	460	560	660	mV
$V_{OL}$	Output low voltage	DC coupled, 50 Ω to ground, VDD = 2.5 V/3.3 V	-150	0	150	mV
		DC coupled, 50 Ω to ground, VDD = 1.8 V	-150	0	150	mV
$V_{OD,DIFF}$	Differential output peak-peak swing		$2 \times  V_{OH} - V_{OL} $		V	
$V_{cross}$	Absolute crossing point voltage	VDD = 3.3 V/2.5 V, $f_{out} = 100$ MHz	0.2	0.35	0.50	$V_{pp}$
		VDD = 1.8 V, $f_{out} = 100$ MHz	0.15	0.275	0.40	$V_{pp}$
$V_{cross-delta}$	Absolute crossing point voltage variation	VDD = 3.3 V/2.5 V/1.8 V, $f_{out} = 100$ MHz	0.14		V	
$dV/dt$	Output slew rate	50 Ω to ground; DC coupled load; measured slew rate in ±150 mV from center.	2	12	12	V/ns

over recommended operating conditions, typical temperature = 25°C, frequency output = 156.25 MHz, VDD = 3.3 V, LVC MOS output capacitor load = 2.2 pF (unless otherwise specified)<sup>(4)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ΔdV/dt	Output slew rate variation			20		%
ODC	Output duty cycle			45	50	55
<b>LVC MOS Output Characteristics</b>						
F <sub>out</sub>	Output frequency		1	200		MHz
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 3.6 mA, VDD = 1.8 V			0.36	V
		I <sub>OL</sub> = 5.0 mA, VDD = 2.5 V			0.5	V
		I <sub>OL</sub> = 6.6 mA, VDD = 3.3 V			0.66	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = 3.6 mA, VDD = 1.8 V	1.44			V
		I <sub>OH</sub> = 5.0 mA, VDD = 2.5 V	2			V
		I <sub>OH</sub> = 6.6 mA, VDD = 3.3 V	2.64			V
t <sub>R/F</sub>	Output rise/fall time	20% to 80% of V <sub>OH</sub> – V <sub>OL</sub> , C <sub>L</sub> = 2 pF			0.5	1
ODC	Output duty cycle		45	50	55	%
R <sub>out</sub>	Output impedance	OE = HIGH	40	50	60	Ω
C <sub>L</sub>	Maximum capacitive load	F <sub>out</sub> > 50 MHz <sup>(3)</sup>			15	pF
		F <sub>out</sub> < 50 MHz <sup>(3)</sup>			30	pF
<b>Function Pin Input Characteristics (OE/ST Pin)</b>						
V <sub>IL</sub>	Input low voltage				0.6	V
V <sub>IH</sub>	Input high voltage				1.3	V
I <sub>IL</sub>	Input low current	OE = GND			–40	μA
I <sub>IH</sub>	Input high current	OE = VDD			40	μA
C <sub>IN</sub>	Input capacitance				2	pF
<b>LVDS, HCSL and LVPECL Frequency Tolerance</b>						
F <sub>T</sub>	Total frequency stability	Inclusive of: solder shift, initial tolerance, variation over –40°C to 85°C, variation over rated supply voltage range, and 10 year aging at 25°C.			–25	25
		Inclusive of: solder shift, initial tolerance, variation over –40°C to 85°C, variation over supply voltage range.			–20	20
<b>LVC MOS Frequency Tolerance</b>						
F <sub>T</sub>	Total frequency stability	Inclusive of: solder shift, initial tolerance, variation over –40°C to 105°C, variation over rated supply voltage range, and 10 year aging at 25°C.			–25	25
		Inclusive of: solder shift, initial tolerance, variation over –40°C to 105°C, variation over rated supply voltage range.			–20	20
<b>Differential Output PSRR Characteristics</b>						
PSRR	Spur induced by 50 mV power supply ripple at 156.25 MHz output, VDD = 2.5 V/3.3 V, No power supply decoupling capacitor	Sine wave at 50 kHz			–71	dBc
		Sine wave at 100 kHz			–71	dBc
		Sine wave at 500 kHz			–72	dBc
		Sine wave at 1 MHz			–70	dBc
PSRR	Spur induced by 50 mV power supply ripple at 156.25 MHz output, VDD = 1.8 V, no power supply decoupling capacitor	Sine wave at 50 kHz			–64	dBc
		Sine wave at 100 kHz			–64	dBc
		Sine wave at 500 kHz			–67	dBc
		Sine wave at 1 MHz			–68	dBc
PSRR	Jitter sensitivity to power supply ripple	100 kHz sine wave ripple, 3.3 V supply <sup>(2)</sup>			4	fs/mV

over recommended operating conditions, typical temperature = 25°C, frequency output = 156.25 MHz, VDD = 3.3 V, LVC MOS output capacitor load = 2.2 pF (unless otherwise specified)<sup>(4)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LVC MOS PSRR Characteristics</b>					
PSRR	Spur induced by 50 mV power supply ripple at 50 MHz output, VDD = 2.5 V/3.3 V, no power supply decoupling capacitor	Sine wave at 50 kHz	–72	–70	dBc
		Sine wave at 100 kHz	–71	–70	dBc
		Sine wave at 500 kHz	–70	–69	dBc
		Sine wave at 1 MHz	–69	–68	dBc
PSRR	Spur induced by 50 mV power supply ripple at 50 MHz output, VDD = 1.8 V, no power supply decoupling capacitor	Sine wave at 50 kHz	–50	–48	dBc
		Sine wave at 100 kHz	–50	–48	dBc
		Sine wave at 500 kHz	–52	–50	dBc
		Sine wave at 1 MHz	–55	–53	dBc
PSRR	Jitter sensitivity to power supply ripple;	100 kHz sine wave ripple, 3.3 V supply <sup>(2)</sup>	10	12	fs/mV
<b>Power-On Characteristics</b>					
$t_{START\_UP}$	Start-up Time	Time elapsed from 0.95 x VDD until output is enabled and output is within specification		5	ms
$t_{OE-EN}$	Output enable time	Time elapsed from OE = $V_{IH}$ until output is enabled and output is within specification, $F_{out} > 10$ MHz		25	μs
$t_{OE-DIS}$	Output disable time	Time elapsed from OE = $V_{IL}$ until output is disabled, $F_{out} > 10$ MHz		1	μs
<b>LVPECL - Clock Output Jitter</b>					
$R_J$	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 156.25$ MHz	100	125	fs
$PN_{1k}$	Phase noise at 1 kHz offset	$F_{out} = 156.25$ MHz.	–95	–90	dBc/Hz
$PN_{10k}$	Phase noise at 10 kHz offset		–127	–120	dBc/Hz
$PN_{100k}$	Phase noise at 100 kHz offset		–146	–140	dBc/Hz
$PN_{1M}$	Phase Noise at 1 MHz offset		–156	–150	dBc/Hz
$PN_{10M}$	Phase Noise at 10 MHz offset		–158	–152	dBc/Hz
$R_J$	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 312.5$ MHz	100	125	fs
$PN_{1k}$	Phase noise at 1 kHz offset	$F_{out} = 312.5$ MHz.	–89	–85	dBc/Hz
$PN_{10k}$	Phase noise at 10 kHz offset		–121	–115	dBc/Hz
$PN_{100k}$	Phase noise at 100 kHz offset		–140	–135	dBc/Hz
$PN_{1M}$	Phase noise at 1 MHz offset		–150	–145	dBc/Hz
$PN_{10M}$	Phase noise at 10 MHz offset		–154	–148	dBc/Hz
$R_J$	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 100$ MHz	125	170	fs
		$F_{out} = 125$ MHz	100	125	fs
		$F_{out} = 155.52$ MHz	100	125	fs
		$F_{out} = 161.1328125$ MHz	110	150	fs
		$F_{out} = 200$ MHz	120	150	fs
		$F_{out} = 400$ MHz	100	135	fs
$R_{PeriodJITT,RMS}$	RMS period jitter	$F_{out} \geq 25$ MHz	1.7	2.0	ps
$RJITT,PK-PK$	Peak-peak period jitter	$F_{out} \geq 25$ MHz	13	15	ps
<b>LVDS - Clock Output Jitter</b>					
$R_J$	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 156.25$ MHz	100	125	fs

over recommended operating conditions, typical temperature = 25°C, frequency output = 156.25 MHz, VDD = 3.3 V, LVC MOS output capacitor load = 2.2 pF (unless otherwise specified)<sup>(4)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN <sub>1k</sub>	Phase noise at 1 kHz offset	$F_{out} = 156.25$ MHz		-95		dBc/Hz
PN <sub>10k</sub>	Phase noise at 10 kHz offset			-128		dBc/Hz
PN <sub>100k</sub>	Phase noise at 100 kHz offset			-146		dBc/Hz
PN <sub>1M</sub>	Phase noise at 1 MHz offset			-156		dBc/Hz
PN <sub>10M</sub>	Phase noise at 10 MHz offset			-156.5		dBc/Hz
R <sub>J</sub>	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 312.5$ MHz		100	125	fs
PN <sub>1k</sub>	Phase noise at 1 kHz offset	$F_{out} = 312.5$ MHz		-89		dBc/Hz
PN <sub>10k</sub>	Phase noise at 10 kHz offset			-122		dBc/Hz
PN <sub>100k</sub>	Phase noise at 100 kHz offset			-139		dBc/Hz
PN <sub>1M</sub>	Phase noise at 1 MHz offset			-150		dBc/Hz
PN <sub>10M</sub>	Phase noise at 10 MHz offset			-153.5		dBc/Hz
R <sub>J</sub>	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 100$ MHz		140	170	fs
		$F_{out} = 125$ MHz		110	125	fs
		$F_{out} = 155.52$ MHz		105	140	fs
		$F_{out} = 161.1328125$ MHz		125	160	fs
		$F_{out} = 200$ MHz		125	150	fs
		$F_{out} = 400$ MHz		100	135	fs
R <sub>PeriodJIT</sub> T,RMS	RMS period jitter	$F_{out} \geq 25$ MHz		1.6		ps
R <sub>JITT,PK- PK</sub>	Peak-peak period jitter	$F_{out} \geq 25$ MHz		13		ps

**HCSL - Clock Output Jitter**

J <sub>PCle1-cc</sub>	PCIe Gen 1 common clock jitter (jitter limit = 86 ps)	$F_{out} = 100$ MHz	0.146	6.4	ps
J <sub>PCle1-SRNS</sub>	PCIe Gen 1 SRNS jitter		0.447	6.99	ps
J <sub>PCle2-cc</sub>	PCIe Gen 2 common clock jitter (jitter limit = 3 ps)		0.103	0.554	ps
J <sub>PCle2-SRNS</sub>	PCIe Gen 2 SRNS jitter		0.135	0.56	ps
J <sub>PCle3-cc</sub>	PCIe Gen 3 common clock jitter (jitter limit = 1 ps)		0.029	0.164	ps
J <sub>PCle3-SRNS</sub>	PCIe Gen 3 SRNS jitter		0.033	0.180	ps
J <sub>PCle4-cc</sub>	PCIe Gen 4 common clock jitter (jitter limit = 500 fs)		0.029	0.164	ps
J <sub>PCle4-SRNS</sub>	PCIe Gen 4 SRNS jitter		0.033	0.180	ps
J <sub>PCle5-cc</sub>	PCIe Gen 5 common clock jitter (jitter limit = 150 fs)		0.007	0.070	ps
J <sub>PCle5-SRNS</sub>	PCIe Gen 5 SRNS jitter		0.007	0.074	ps
J <sub>PCle6-cc</sub>	PCIe Gen 6 common clock jitter (jitter limit = 100 fs)		0.007	0.042	ps
J <sub>PCle6-SRNS</sub>	PCIe Gen 6 SRNS jitter		0.009	0.052	ps
R <sub>J</sub>	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 156.25$ MHz	100	125	fs

over recommended operating conditions, typical temperature = 25°C, frequency output = 156.25 MHz, VDD = 3.3 V, LVC MOS output capacitor load = 2.2 pF (unless otherwise specified)<sup>(4)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PN <sub>1k</sub>	Phase noise at 1 kHz offset	$F_{out} = 156.25$ MHz.		–95		dBc/Hz
PN <sub>10k</sub>	Phase noise at 10 kHz offset			–127		dBc/Hz
PN <sub>100k</sub>	Phase noise at 100 kHz offset			–146		dBc/Hz
PN <sub>1M</sub>	Phase noise at 1 MHz offset			–156		dBc/Hz
PN <sub>10M</sub>	Phase noise at 10 MHz offset			–158		dBc/Hz
R <sub>J</sub>	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 312.5$ MHz	100	125		fs
PN <sub>1k</sub>	Phase noise at 1 kHz offset	$F_{out} = 312.5$ MHz.		–89		dBc/Hz
PN <sub>10k</sub>	Phase noise at 10 kHz offset			–121		dBc/Hz
PN <sub>100k</sub>	Phase noise at 100 kHz offset			–140		dBc/Hz
PN <sub>1M</sub>	Phase noise at 1 MHz offset			–150		dBc/Hz
PN <sub>10M</sub>	Phase noise at 10 MHz offset			–154		dBc/Hz
R <sub>J</sub>	RMS jitter (integration BW: 12 kHz to 20 MHz)	$F_{out} = 100$ MHz	125	170		fs
		$F_{out} = 125$ MHz	100	125		fs
		$F_{out} = 155.52$ MHz	100	125		fs
		$F_{out} = 161.1328125$ MHz	110	150		fs
		$F_{out} = 200$ MHz	120	150		fs
		$F_{out} = 400$ MHz	100	135		fs
R <sub>PeriodJIT</sub> T,RMS	RMS period jitter	$F_{out} \geq 25$ MHz		1.7		ps
R <sub>JITT,PK- PK</sub>	Peak-peak period jitter	$F_{out} \geq 25$ MHz		13		ps

over recommended operating conditions, typical temperature = 25°C, frequency output = 156.25 MHz, VDD = 3.3 V, LVC MOS output capacitor load = 2.2 pF (unless otherwise specified)<sup>(4)</sup>

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>LVC MOS - Clock Output Jitter</b>					
R <sub>J</sub>	RMS jitter (integration BW: 12 kHz to 20 MHz) F <sub>out</sub> = 156.25 MHz	0.25	0.5	ps	
PN <sub>1k</sub>	Phase noise at 1 kHz offset	-100			dBc/Hz
PN <sub>10k</sub>	Phase noise at 10 kHz offset	-128			dBc/Hz
PN <sub>100k</sub>	Phase noise at 100 kHz offset	-143			dBc/Hz
PN <sub>1M</sub>	Phase noise at 1 MHz offset	-150			dBc/Hz
PN <sub>10M</sub>	Phase noise at 10 MHz offset	-152			dBc/Hz
R <sub>J</sub>	RMS jitter (integration BW: 12 kHz to 5 MHz) F <sub>out</sub> = 24 MHz F <sub>out</sub> = 25 MHz F <sub>out</sub> = 33.33 MHz	0.25	.5	ps	
		0.25	.5	ps	
		0.25	1	ps	
	RMS jitter (integration BW: 12 kHz to 20 MHz) F <sub>out</sub> = 40 MHz F <sub>out</sub> = 50 MHz F <sub>out</sub> = 66.66 MHz F <sub>out</sub> = 74.25 MHz F <sub>out</sub> = 78 MHz F <sub>out</sub> = 100 MHz F <sub>out</sub> = 125 MHz	0.5	1	ps	
		0.4	1	ps	
		0.5	1	ps	
		0.3	0.5	ps	
		0.35	0.5	ps	
		0.35	0.5	ps	
		0.35	0.5	ps	
R <sub>PeriodJIT</sub> T,RMS	RMS period jitter	F <sub>out</sub> ≥ 25 MHz	1.5		ps
R <sub>JITT,PK-</sub> PK	Peak-peak period jitter	F <sub>out</sub> ≥ 25 MHz	13		ps

(1) DC Load condition

(2) Measured using TI LMK6x Evaluation Module;

(3) Refer to the *Application Curves* section for Rise time and fall time details for different capacitor load values.

(4) The Jitter specifications are based on design and characterization

## 7.8 Timing Diagrams

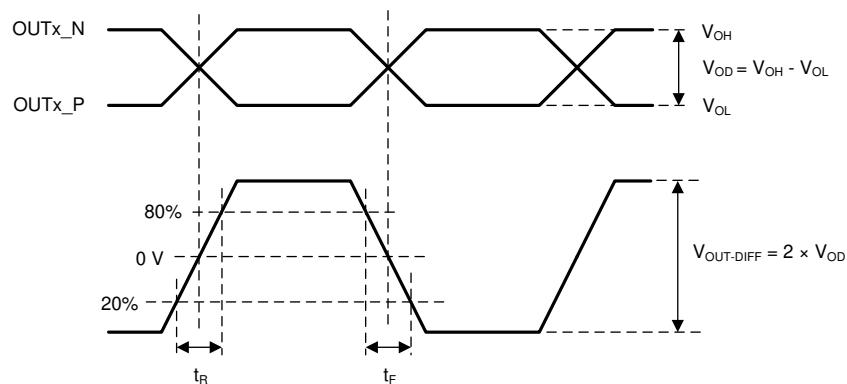


Figure 7-1. Differential Output Voltage and Rise/Fall Time

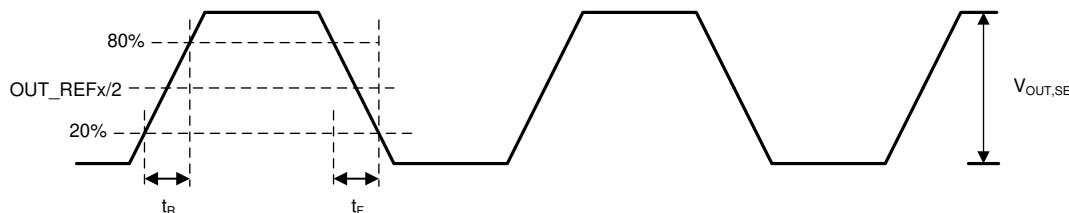


Figure 7-2. Single-Ended Output Voltage and Rise/Fall Time

## 7.9 Typical Characteristics

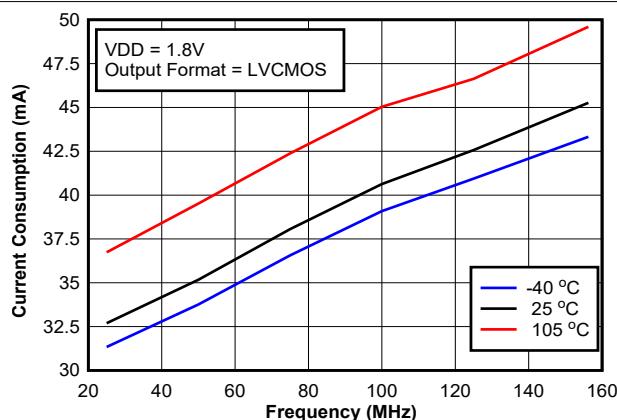


Figure 7-3. Current Consumption vs Frequency  
(LVC MOS, 1.8 V)

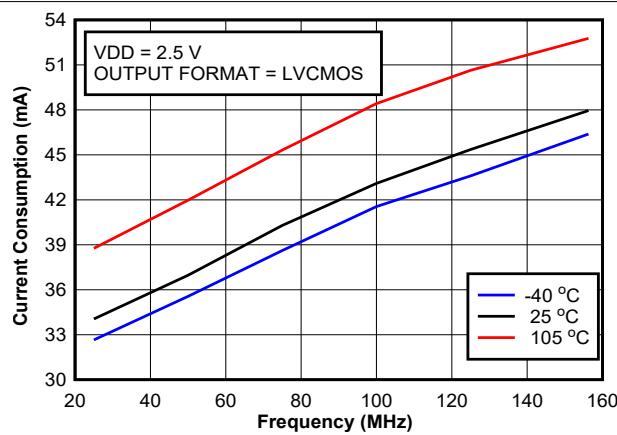


Figure 7-4. Current Consumption vs Frequency  
(LVC MOS, 2.5 V)

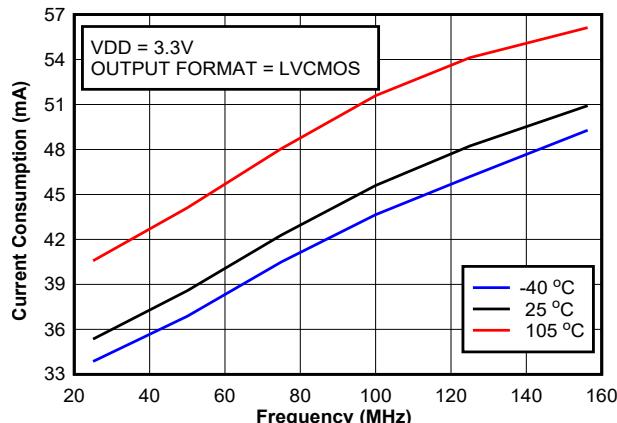


Figure 7-5. Current Consumption vs Frequency  
(LVC MOS, 3.3 V)

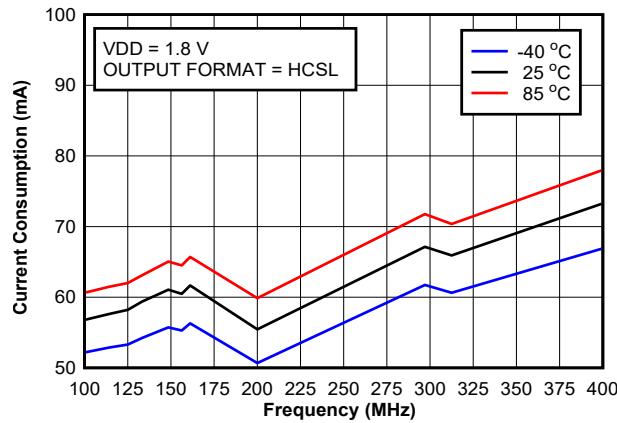


Figure 7-6. Current Consumption vs Frequency  
(HCSL, 1.8 V)

## 7.9 Typical Characteristics (continued)

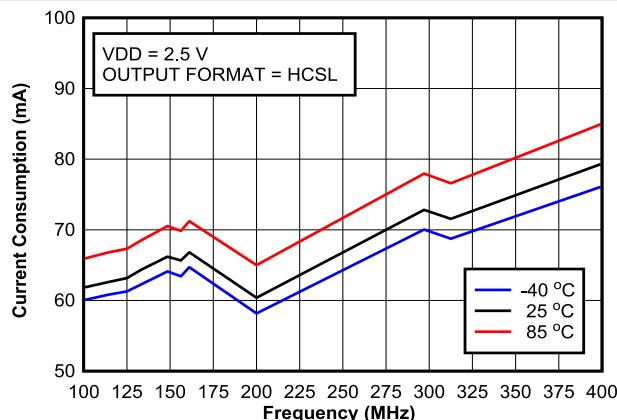


Figure 7-7. Current Consumption vs Frequency (HCSL, 2.5 V)

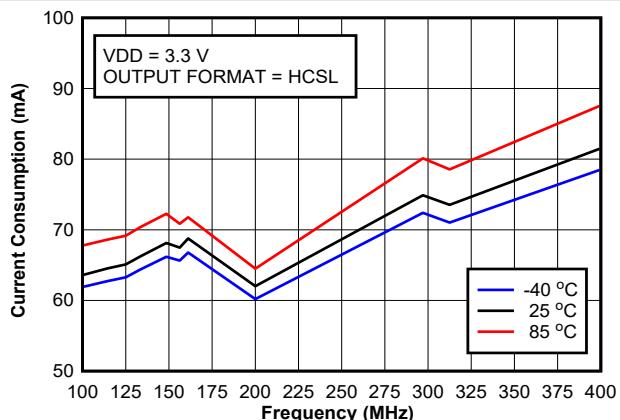


Figure 7-8. Current Consumption vs Frequency (HCSL, 3.3 V)

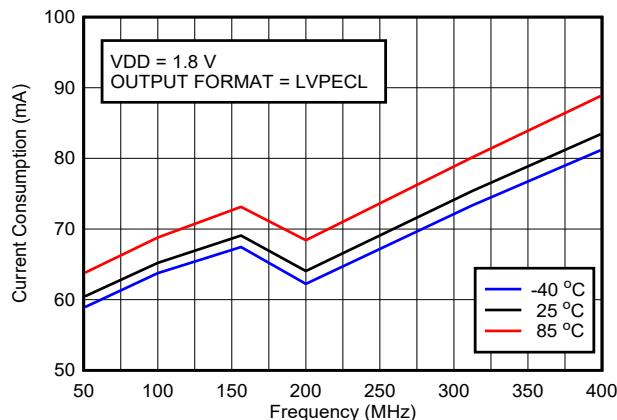


Figure 7-9. Current Consumption vs Frequency (LVPECL, 1.8 V)

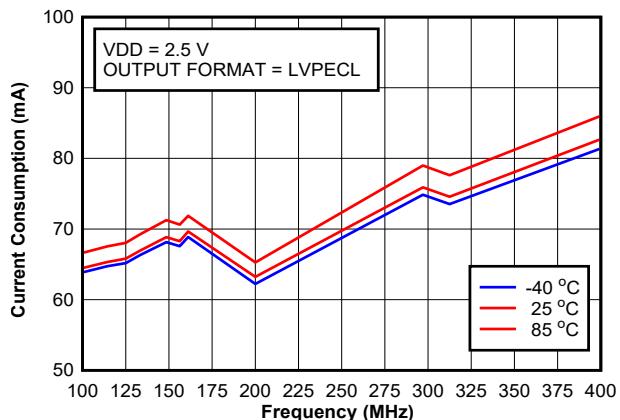


Figure 7-10. Current Consumption vs Frequency (LVPECL, 2.5 V)

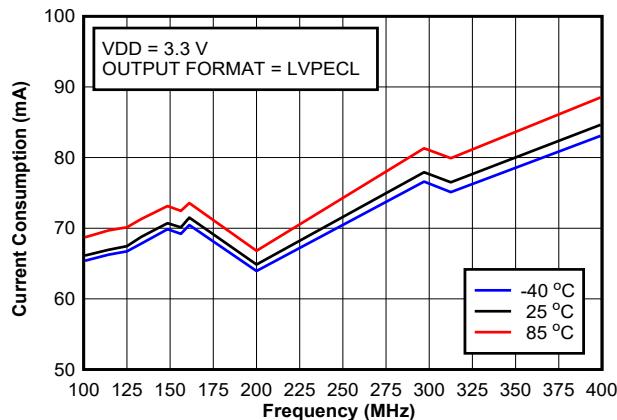


Figure 7-11. Current Consumption vs Frequency (LVPECL, 3.3 V)

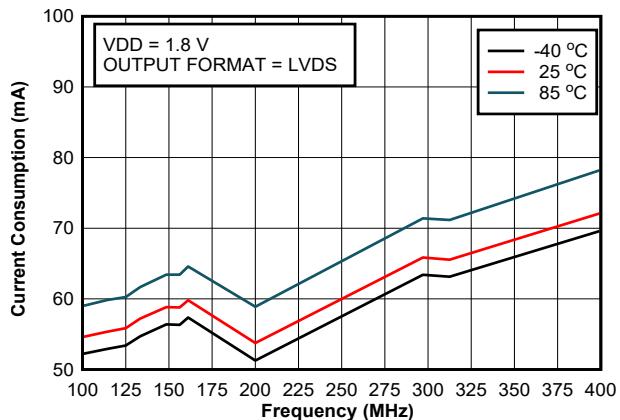
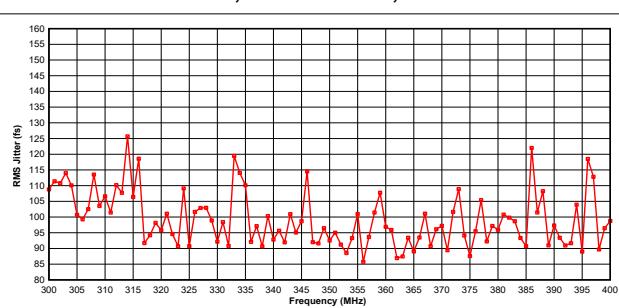
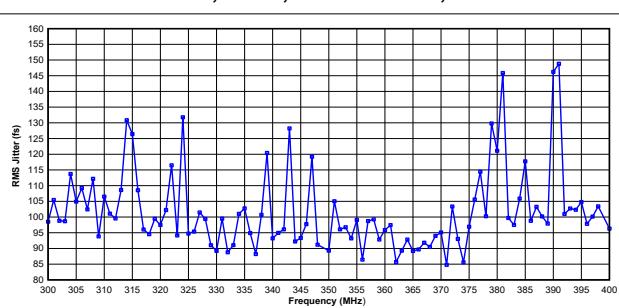
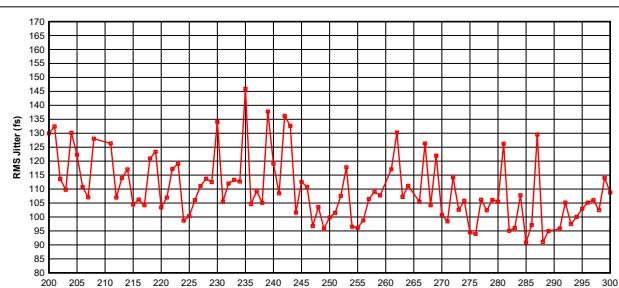
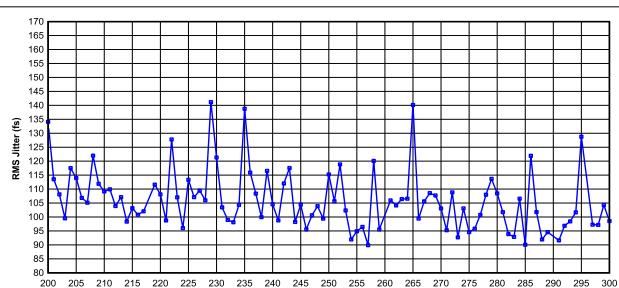
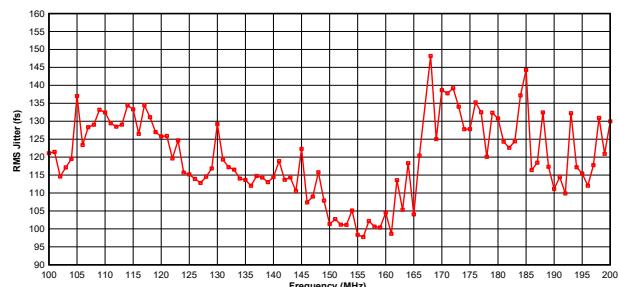
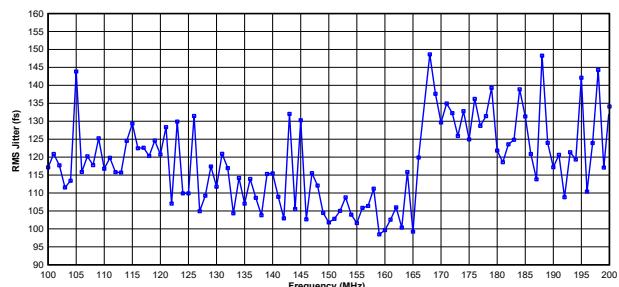
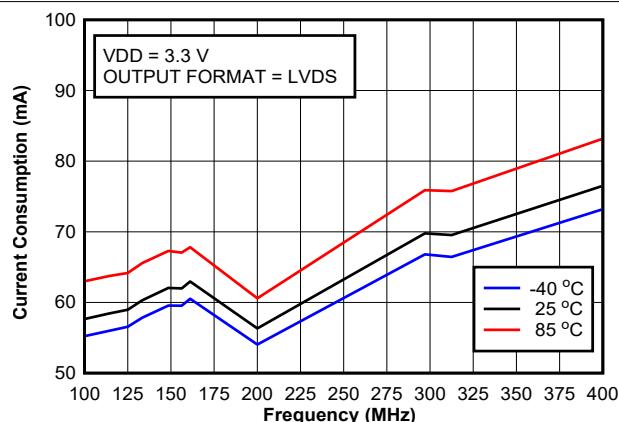
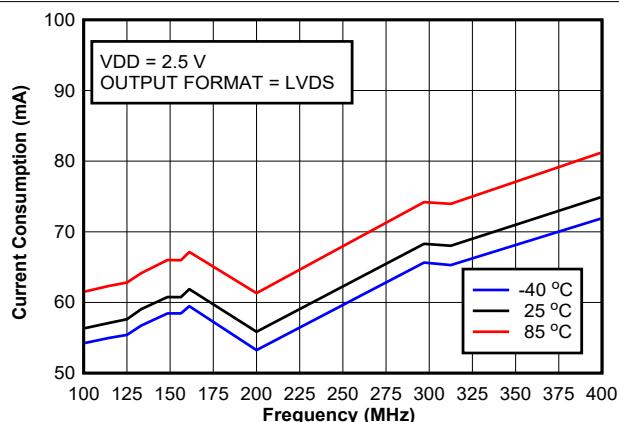


Figure 7-12. Current Consumption vs Frequency (LVDS, 1.8 V)

## 7.9 Typical Characteristics (continued)



## 7.9 Typical Characteristics (continued)

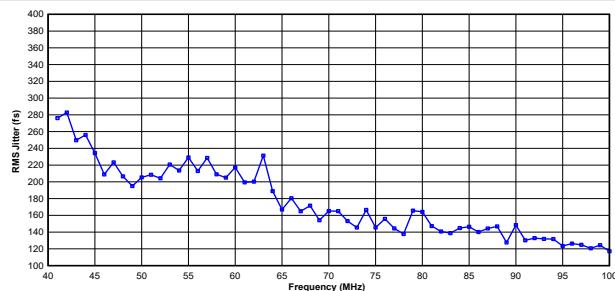


Figure 7-21. RMS Jitter vs Frequency (Below 100 MHz) for LVPECL, HCSL; TYPICAL 3.3 V, 25°C

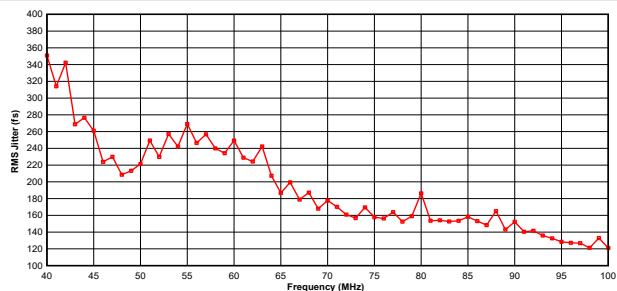


Figure 7-22. RMS Jitter vs Frequency (Below 100 MHz) for LVDS; TYPICAL 3.3 V, 25°C

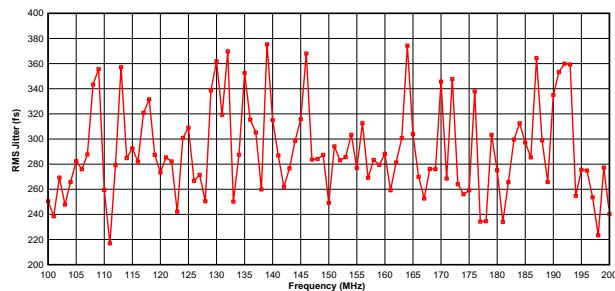


Figure 7-23. RMS Jitter vs Frequency (100 MHz - 200 MHz) for LVCmos; TYPICAL 3.3 V, 25°C

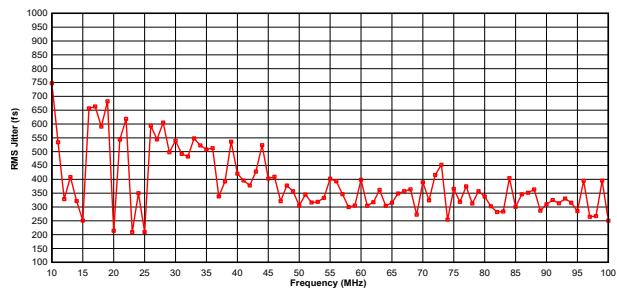


Figure 7-24. RMS Jitter vs Frequency (10 MHz - 100 MHz) for LVCmos; TYPICAL 3.3 V, 25°C

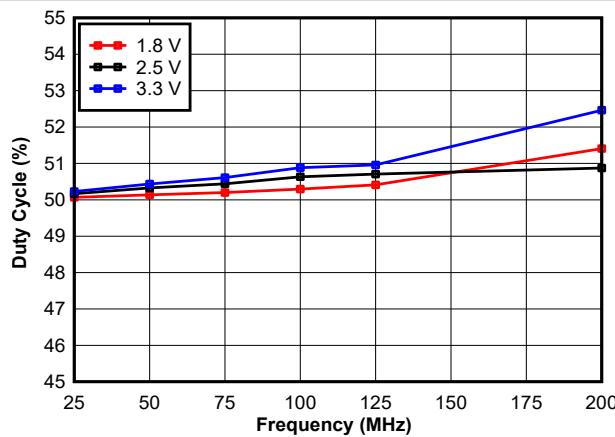


Figure 7-25. Duty Cycle (%) vs Frequency vs Power Supply; 25°C

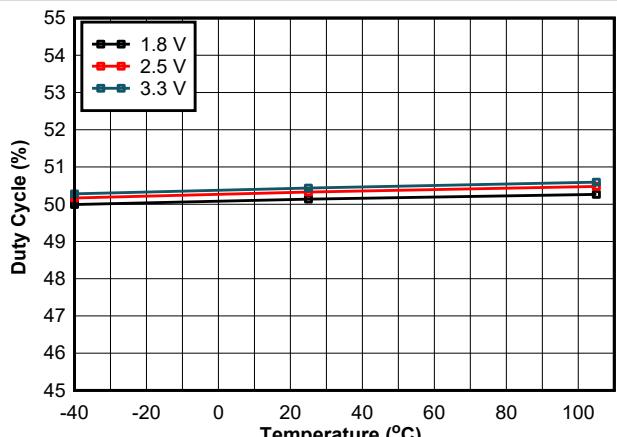


Figure 7-26. Duty Cycle (%) vs Temperature vs Power Supply; 50-MHz Frequency

## 7.9 Typical Characteristics (continued)

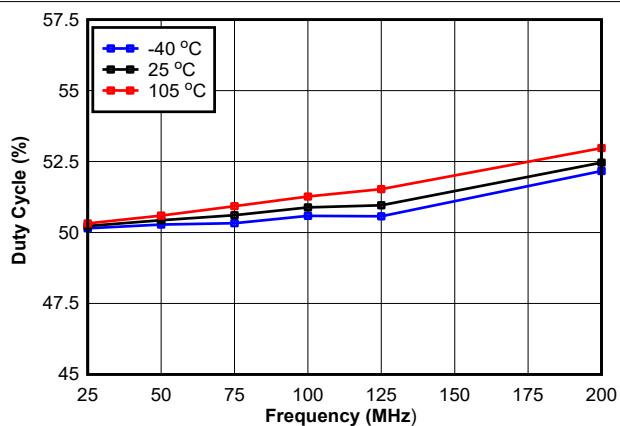


Figure 7-27. Duty Cycle (%) vs Frequency Over Temperature Range for LVC MOS; 3.3 V

## 8 Parameter Measurement Information

### 8.1 Device Output Configurations

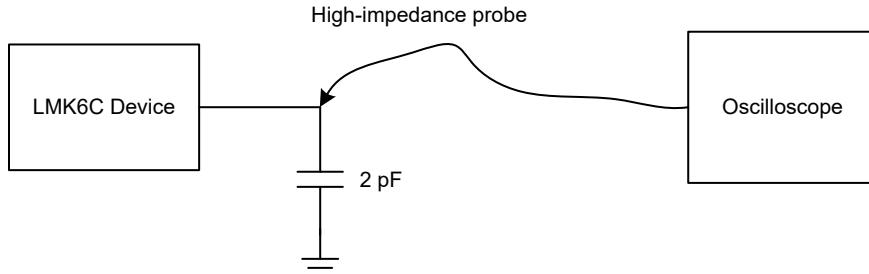


Figure 8-1. LMK6C Output Test Configuration

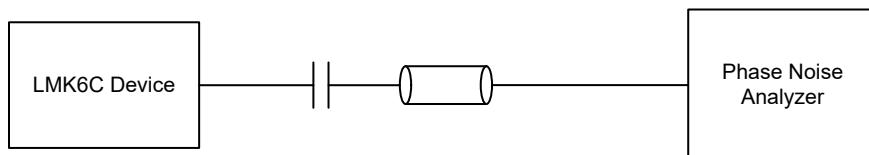


Figure 8-2. LMK6C Output Phase Noise Test Configuration

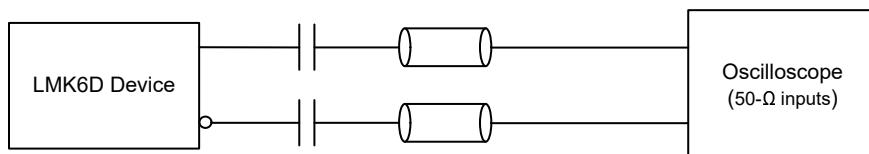


Figure 8-3. LMK6D Output Test Configuration

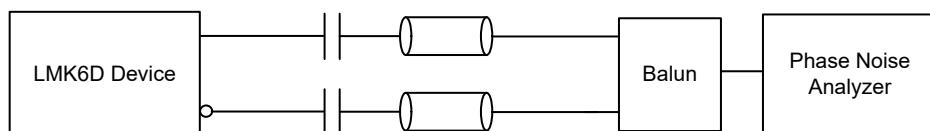


Figure 8-4. LMK6D Output Phase Noise Configuration

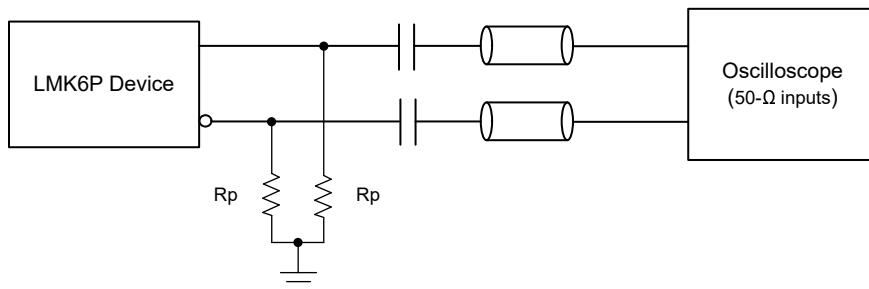
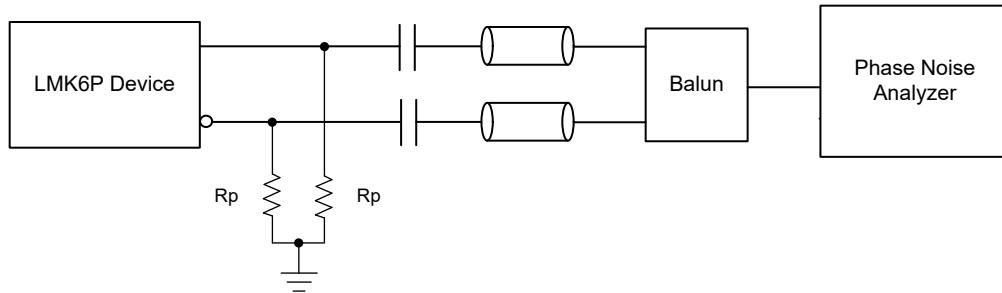


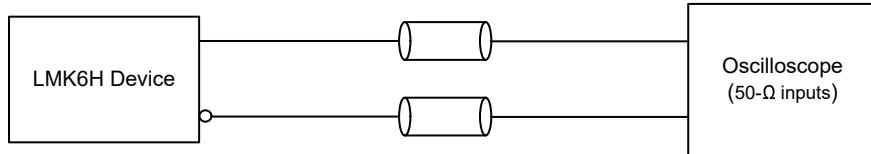
Figure 8-5. LMK6P Output Test Configuration



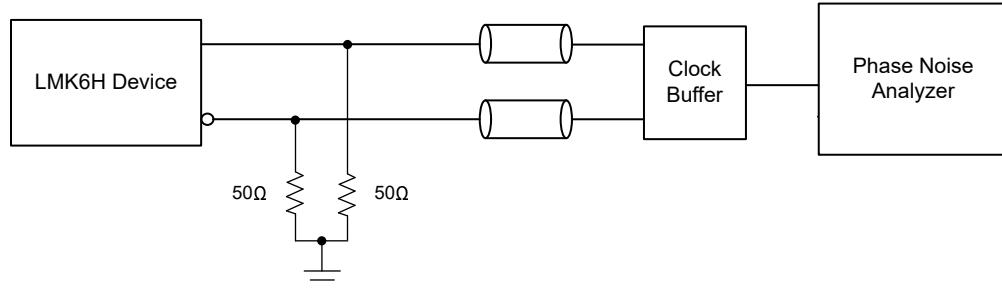
**Figure 8-6. LMK6P Output Phase Noise Configuration**

**Table 8-1. LMK6P Output Test configuration and Phase Noise Configuration Rp Values**

SUPPLY (V)	Rp (Ω)
3.3 V	207.5
2.5 V	112.5
1.8 V	83.3



**Figure 8-7. LMK6H Output Test Configuration**



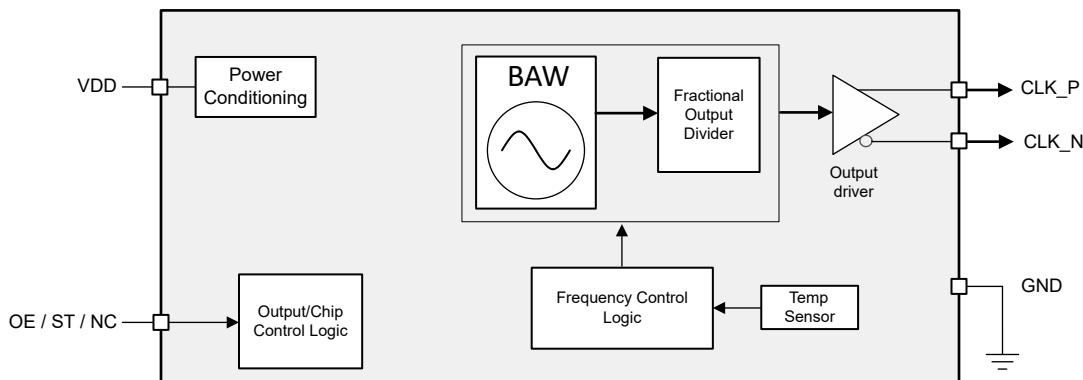
**Figure 8-8. LMK6H Output Phase Noise Configuration**

## 9 Detailed Description

### 9.1 Overview

The LMK6x is a fixed-frequency BAW based oscillator that can provide ultra-low jitter for both differential and single-ended output types.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 Bulk Acoustic Wave (BAW)

TI's BAW resonator technology uses piezoelectric transduction to generate high-Q resonance at 2.5 GHz. The resonator is defined by the quadrilateral area overlaid by top and bottom electrodes. Alternating high- and low-acoustic impedance layers form acoustic mirrors beneath the resonant body to prevent acoustic energy leakage into the substrate. Furthermore, these acoustic mirrors are also placed on top of the resonator stack to protect the device from contamination and minimize energy leakage into the package materials. This unique dual-Bragg acoustic resonator (DBAR) allows efficient excitation without the need of costly vacuum cavities around the resonator. As a result, TI's BAW resonator is immune to frequency drift caused by adsorption of surface contaminants and can be directly placed in a non-hermetic plastic package with the oscillator IC in small standard oscillator footprints. Refer to [BAW](#) for more details on BAW technology.

#### 9.3.2 Device Block-Level Description

The device contains a BAW oscillator, a Fractional Output Divider (FOD), and output driver, which together generates a pre-programmed output frequency. Temperature variations of oscillation frequency are continuously monitored by internal precision temperature sensor and provided as input to the frequency control logic block. Using this frequency control logic block, frequency corrections are performed internally for maintaining the output frequency within  $\pm 25$  ppm across temperature range and aging. The output driver is capable of providing both single-ended LVCMOS and differential LVPECL, LVDS, and HCSL output formats. The device contains an internal LDO which reduces the power supply noise, resulting in low noise clock output.

#### 9.3.3 Function Pin(s)

Pin 1 on the LMK6C and pin 1 or pin 2 on the LMK6P, LMK6D, and LMK6H are the function pins which have multiple functions based on the orderable part number. The function can be used as Output Enable (OE), Stand By (ST) or No Connect (NC). Options for both Active High and Active Low are available for OE and ST. Contact TI for Active Low options. [Table 9-1](#) lists the functions of pin 1 and pin 2 for differential output 6-pin packages and [Table 9-2](#) lists the functions of pin 1 for single-ended outputs.

**Table 9-1. Function Pin Descriptions for 6-Pin Packages (LMK6D, LMK6H, LMK6P)**

ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION	OTHER FUNCTIONAL PIN CONFIGURATION
E (Pin 1)	Output Enable (Active High / NC)	<b>HIGH or No Connect</b> : Output active at Specified Frequency <b>LOW</b> : Output disabled, high impedance; current consumption is given by $I_{DD-PD}$	Pin 2 can be left floating or grounded
F (Pin 2)	Output Enable (Active High / NC)	<b>HIGH or No Connect</b> : Output active at Specified Frequency <b>LOW</b> : Output disabled, high impedance; current consumption is given by $I_{DD-PD}$	Pin 1 can be left floating or grounded
A (Pin 1)	Standby (Active Low)	<b>LOW</b> : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$ <b>HIGH or No Connect</b> : Output active at Specified Frequency	Pin 2 can be left open or grounded
B (Pin 2)	Standby (Active Low)	<b>LOW</b> : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$ <b>HIGH or No Connect</b> : Output active at Specified Frequency	Pin 1 can be left open or grounded

**Table 9-2. Function Pin Descriptions for 4-Pin Packages (LMK6C)**

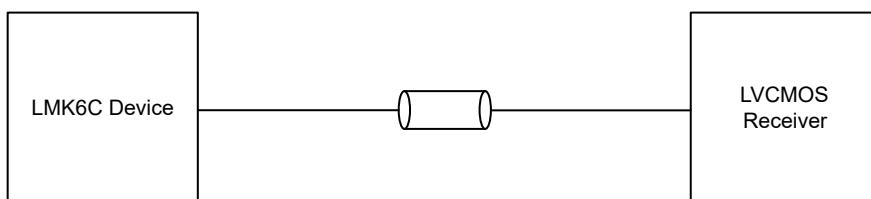
ORDERABLE OPTION	PIN DESCRIPTION	OUTPUT FUNCTION
E (Pin 1)	Output Enable (Active High / NC)	<b>HIGH or No Connect</b> : Output active at Specified Frequency <b>LOW</b> : Output disabled, high impedance; current consumption is given by $I_{DD-PD}$
A (Pin 1)	Standby (Active Low)	<b>LOW</b> : High Impedance; standby mode; current consumption is given by standby current $I_{DD-STBY}$ <b>HIGH or No Connect</b> : Output active at Specified Frequency

In standby mode, all blocks are powered down to provide a maximum current consumption savings equivalent to the standby current provided in the *Current Consumption Characteristics* portion of the [Electrical Characteristics](#) table. The return to the output clock active time corresponds to same as the initial start-up time.

The Function Pin is driven internally with resistance  $>100\text{ k}\Omega$ .

### 9.3.4 Clock Output Interfacing and Termination

These figures show the recommended output interfacing and termination circuits.


**Figure 9-1. LMK6C Output to LVC MOS Receiver**

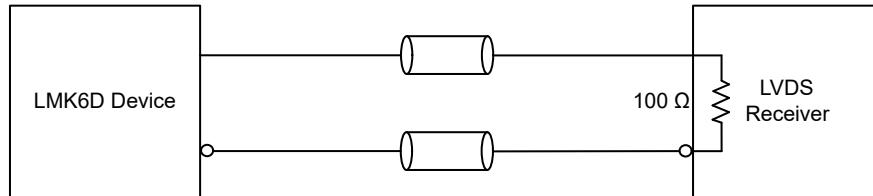


Figure 9-2. LMK6D Output DC-Coupled to LVDS Receiver With Internal Termination/Biasing

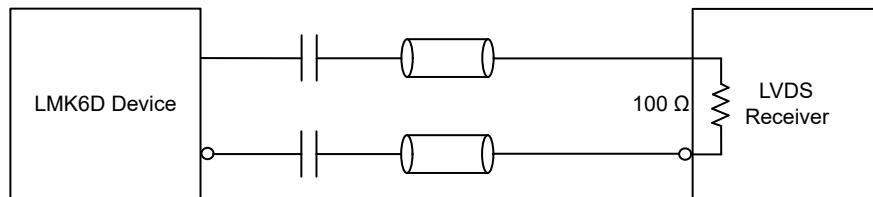


Figure 9-3. LMK6D Output AC Coupled to LVDS Receiver With Internal Termination/Biasing

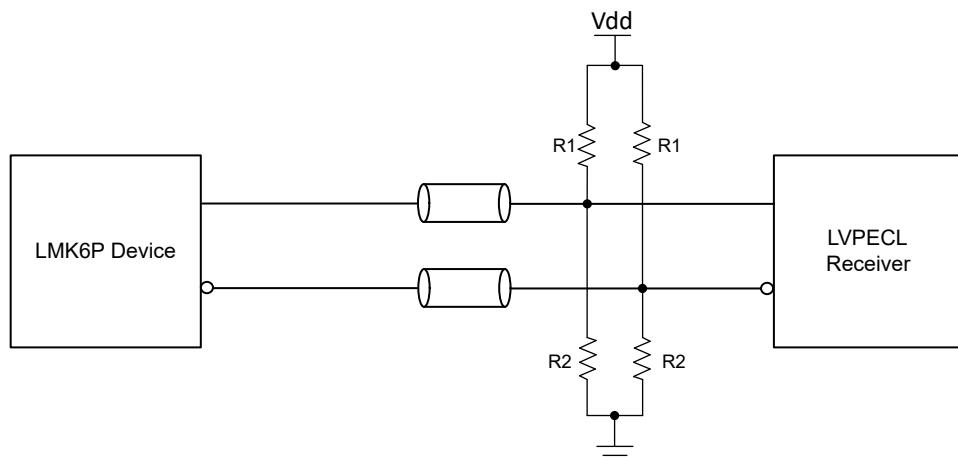
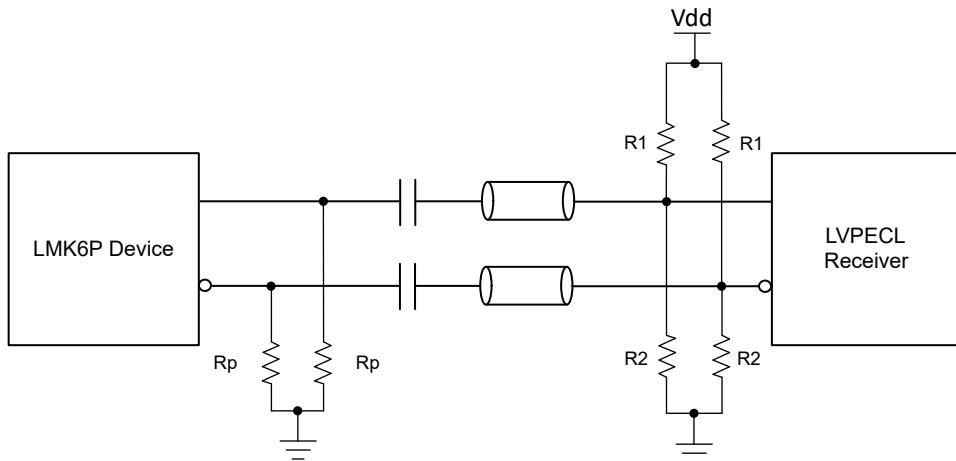


Figure 9-4. LMK6P Output DC-Coupled to LVPECL Receiver With External Termination/Biasing (T-Network)

Table 9-3. LMK6P T-Network DC-Coupled Resistor Values

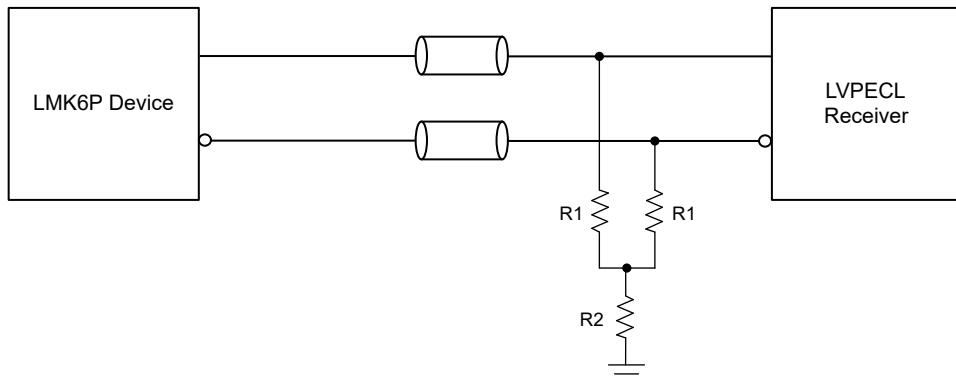
SUPPLY (V)	R1 (Ω)	R2 (Ω)
3.3	133	82
2.5	250	62.5
1.8	450	56.5



**Figure 9-5. LMK6P Output AC-Coupled to LVPECL Receiver With External Termination/Biasing (T-Network)**

**Table 9-4. LMK6P T-Network AC-Coupled Resistor Values**

SUPPLY (V)	Rp (Ω)	R1 (Ω)	R2 (Ω)
3.3	207.5	133	82
2.5	112.5	250	62.5
1.8	83.3	450	56.6



**Figure 9-6. LMK6P Output DC-Coupled to LVPECL Receiver With External Termination/Biasing (Y-Network)**

**Table 9-5. LMK6P Y-Network DC-Coupled Resistor Values**

SUPPLY (V)	R1 (Ω)	R2 (Ω)
3.3	50	78.8
2.5	50	31.3
1.8	50	16.7

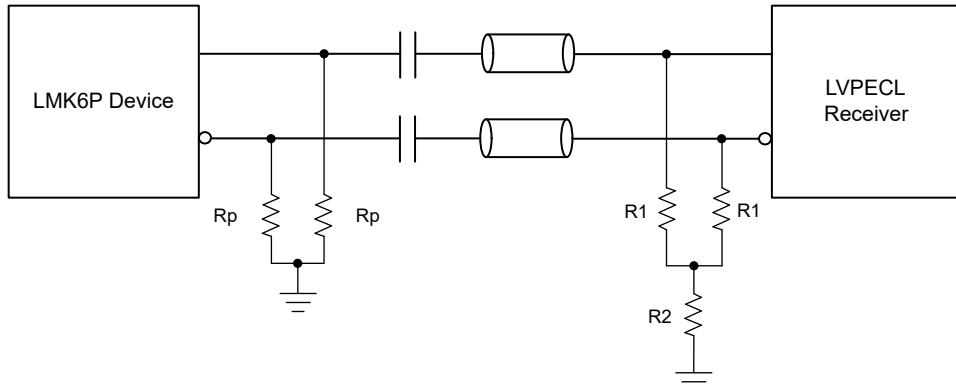


Figure 9-7. LMK6P Output AC-Coupled to LVPECL Receiver With External Termination/Biasing (Y-Network)

Table 9-6. LMK6P Y-Network AC-Coupled Resistor Values

SUPPLY (V)	Rp (Ω)	R1 (Ω)	R2 (Ω)
3.3	207.5	50	78.8
2.5	112.5	50	31.3
1.8	83.3	50	16.7

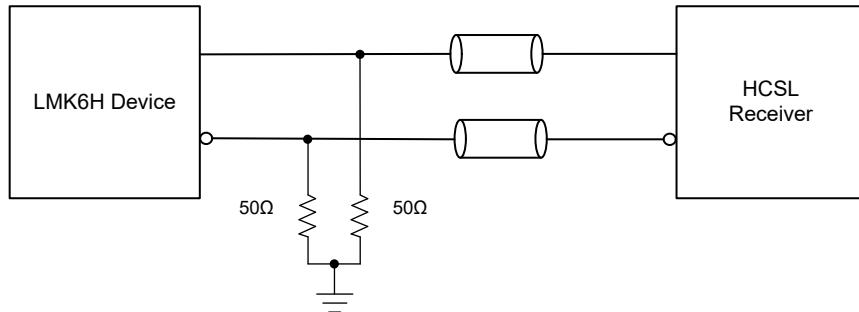


Figure 9-8. LMK6H Output to HCSL Receiver With External Termination

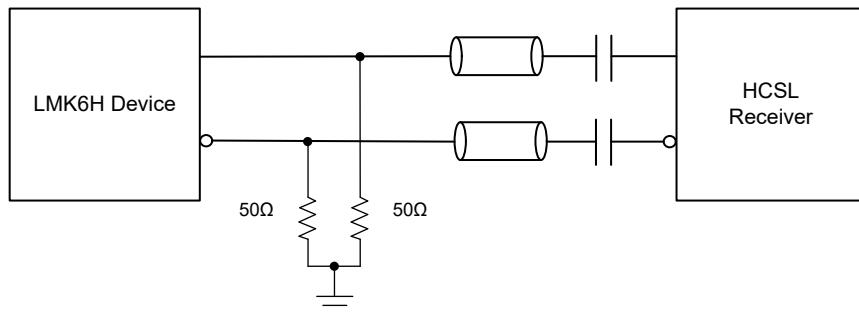
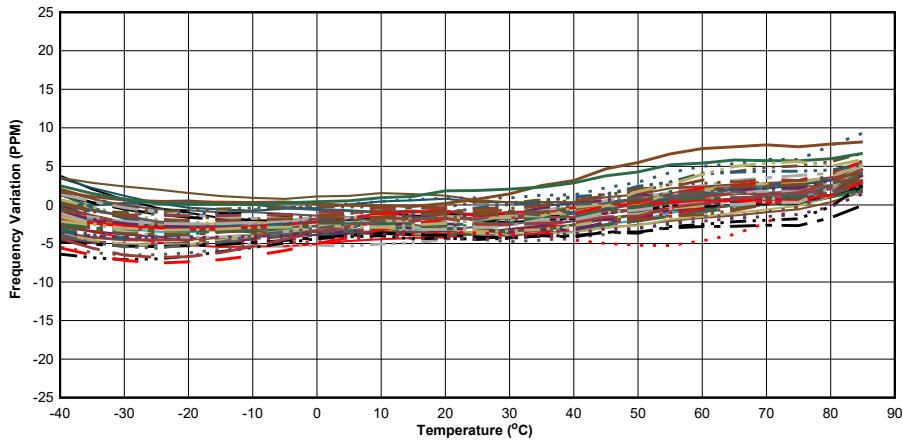


Figure 9-9. LMK6H Output AC-Coupled to HCSL Receiver With External Termination

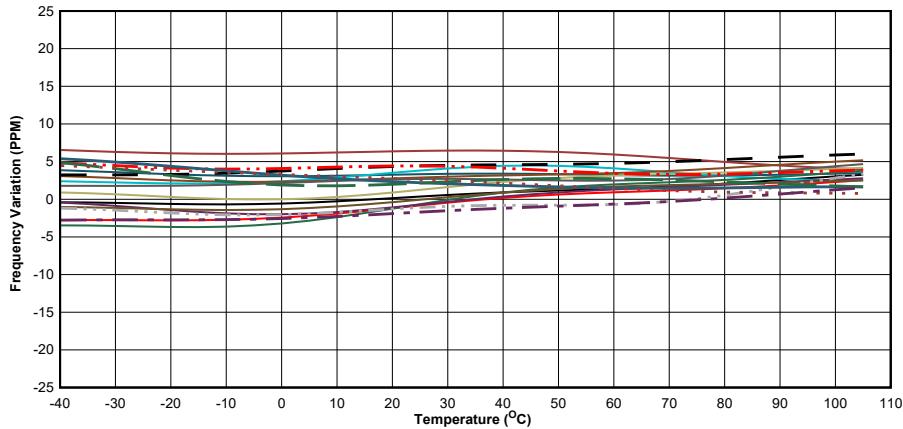
### 9.3.5 Temperature Stability

Figure 9-10 shows the frequency variation of the LMK6x differential output oscillator over the temperature range of  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  for total of 60 units. Figure 9-11 shows the frequency variation of the LMK6C single-ended output oscillator over the operating temperature range of  $-40^{\circ}\text{C}$  to  $105^{\circ}\text{C}$ . These plots represent the typical temperature stability of the device, remaining below  $\pm 10$  ppm. The devices are soldered onto the evaluation

board as per the standard soldering profile and frequency variation measurements are carried out. The output frequency is 156.25 MHz for these tests.



**Figure 9-10. Frequency Change Over Temperature (LMK6x Differential Output Device)**

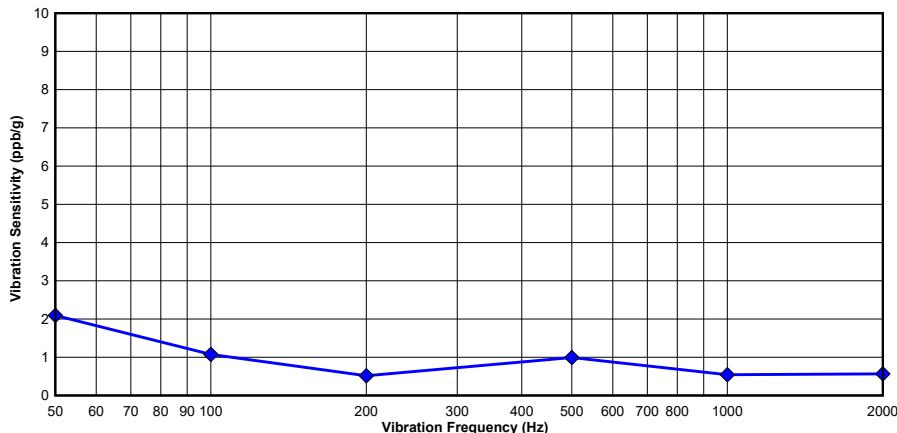


**Figure 9-11. Frequency Change Over Temperature (LMK6C Single-Ended Output Device)**

### 9.3.6 Mechanical Robustness

For reference oscillators, vibration and shock are common causes for increased phase noise and jitter, frequency shift and spikes, or even physical damages to the resonator and the package. Compared to quartz crystals, the BAW resonator is more immune to vibration and shock due to its orders of magnitude, smaller mass, and higher frequency, which means force applied to the device from acceleration is much smaller due to smaller mass.

Figure 9-12 shows the LMK6x BAW oscillator vibration performance. In this test, the LMK6x oscillator mounted on an EVM is subject to 10g acceleration force, ranging from 50 Hz to 2 kHz in x, y, and z-axis. Phase noise trace with spur due to vibration is captured using Keysight E5052B and frequency deviation is calculated from the spur power. Then the frequency deviation is converted to ppb by noting the carrier frequency and normalized to ppb/g. Finally, the RMS sum of ppb/g along all three axes is reported as the Vibration sensitivity in ppb/g. LMK6x performance under vibration is approximately 2 ppb/g while most quartz oscillators best case is 3 ppb/g and worse can be above 10 ppb/g.



**Figure 9-12. LMK6X BAW Oscillator Vibration Performance**

#### 9.4 Device Functional Modes

The LMK6x BAW Oscillator is a fixed output frequency device and does not require any programming. The device pin 1 (and pin 2 for a 6-pin device) has different functions. See the *Function Pin(s)* section for more information on the function pins.

## 10 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

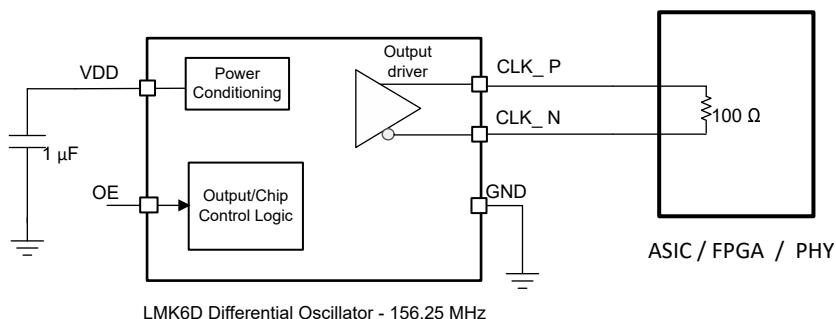
### 10.1 Application Information

The LMK6x is high-performance, fixed-frequency oscillator that can be used as a reference clock. The product family supports any output frequency between 1 MHz to 400 MHz for differential LMK6D, LMK6H, LMK6P or 1 MHz to 200 MHz for singled-ended LVCMOS clock output types, and 1.8-V or 2.5-V through 3.3-V supply rails.

### 10.2 Typical Application

For reference schematic implementation for LMK6x family of oscillators, refer to the [LMK6EVM User's Guide](#) for bypass capacitor and AC-coupling capacitor value recommendations. Refer to the [Clock Output Interfacing and Termination](#) section for output clock required termination and biasing.

Figure 10-1 shows a typical application example. The LMK6D differential oscillator is used as an input to the LVDS buffer input in this example.



**Figure 10-1. Application Example**

#### 10.2.1 Design Requirements

The LMK6x is a fixed-frequency oscillator with no programming needed. Make sure to follow the recommended termination options as described in the [Clock Output Interfacing and Termination](#) section closely. Refer to the [Function Pin\(s\)](#) section to understand the pin 1 and pin 2 functions, and order the part number as per your requirements for Output Enable (OE), Standby (ST) options.

#### 10.2.2 Detailed Design Procedure

The LMK6x has three different options for differential output which are LVDS, LVPECL, HCSL type and one LVCMOS single-ended output type. For designing with the any of the oscillator output type in actual system, use the proper AC or DC termination based on the application requirement. Refer to the [Clock Output Interfacing and Termination](#) section for the details of all the AC and DC termination schemes and use the appropriate option. The figures in this section have all the AC and DC coupling options with the termination resistor values. The LMK6x has an integrated LDO and has excellent PSRR performance as shown in the [Electrical Characteristics](#) table. Refer to the LMK6EVM for the reference layout recommendation while designing the LMK6x BAW oscillator.

For the Function Pin 1 of LMK6C, connect typical 10-kΩ or less resistor to VDD for driving the OE pin High. Note this pin can be left open if you do not want to use pullup resistor as the device has > 100-kΩ internal pullup resistor. For driving the OE pin to Low, use the typical 10 kΩ or less resistor as a pulldown resistor. For the Function Pin 1 or Functional Pin 2 for LMK6D, LMK6H, LMK6P, you can use the similar approach described for LMK6C.

### 10.2.3 Application Curves

The LMK6C LVC MOS output connects to different load capacitances based on the actual application use case in a system. With the different load capacitance, the rise time / fall time varies for the specific output frequency. The following graphs shows the Rise / Fall time for load capacitance of 2.2 pF, 4.7 pF, 10 pF, 15 pF and 22 pF for temperature range from -40°C to 105°C.

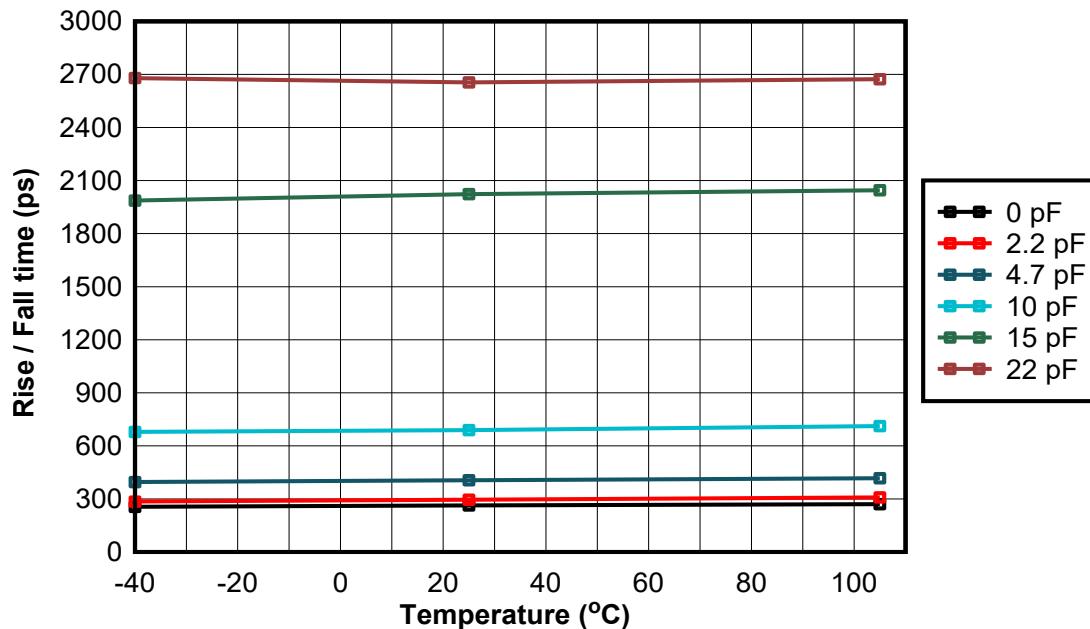


Figure 10-2. Rise / Fall time (ps) vs Temperature for 25-MHz Output Frequency, 3.3-V Supply

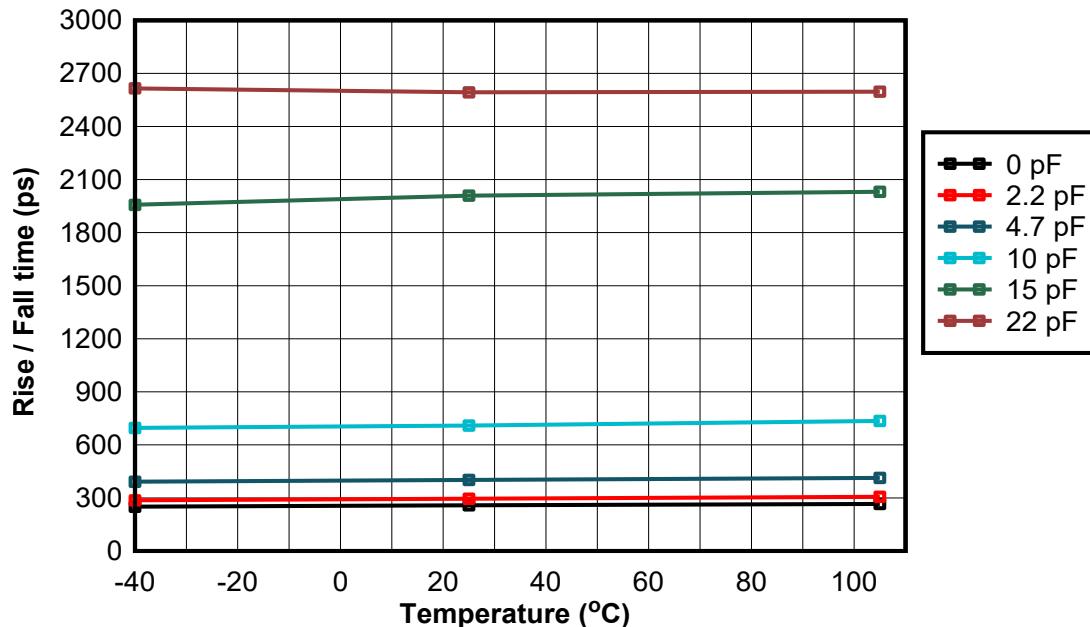
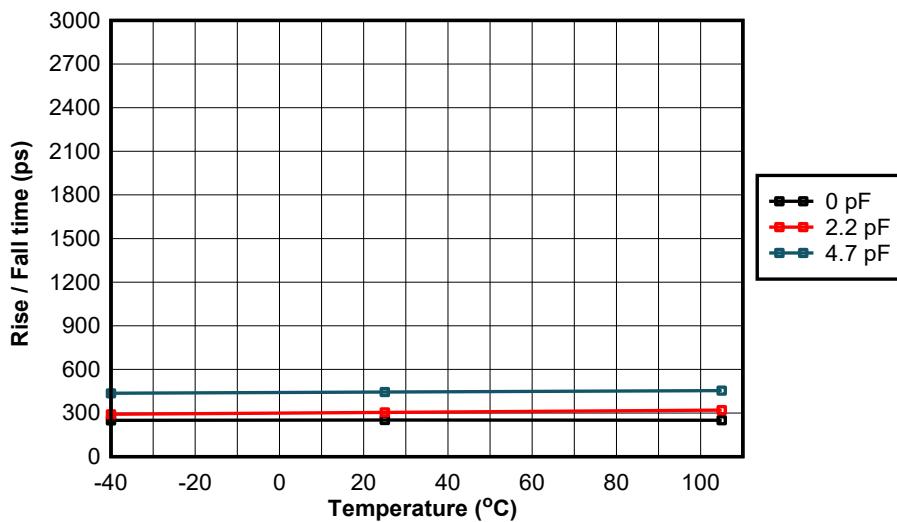
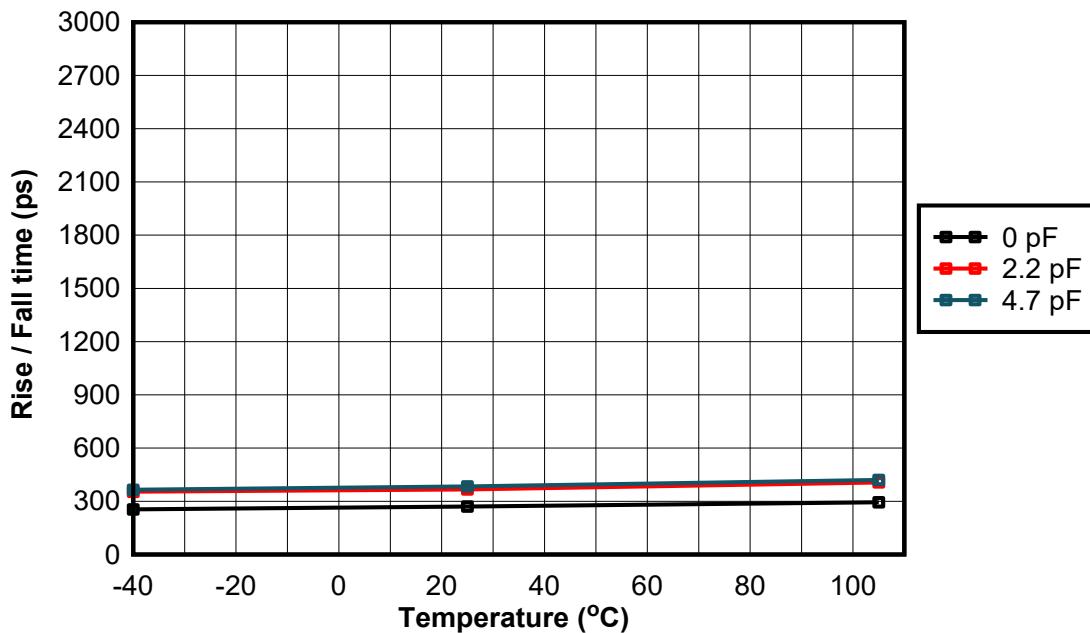


Figure 10-3. Rise / Fall time (ps) vs Temperature for 50-MHz Output Frequency, 3.3-V Supply



**Figure 10-4. Rise / Fall time (ps) vs Temperature for 100-MHz Output Frequency, 3.3-V Supply**



**Figure 10-5. Rise / Fall time (ps) vs Temperature for 200-MHz Output Frequency, 3.3-V Supply**

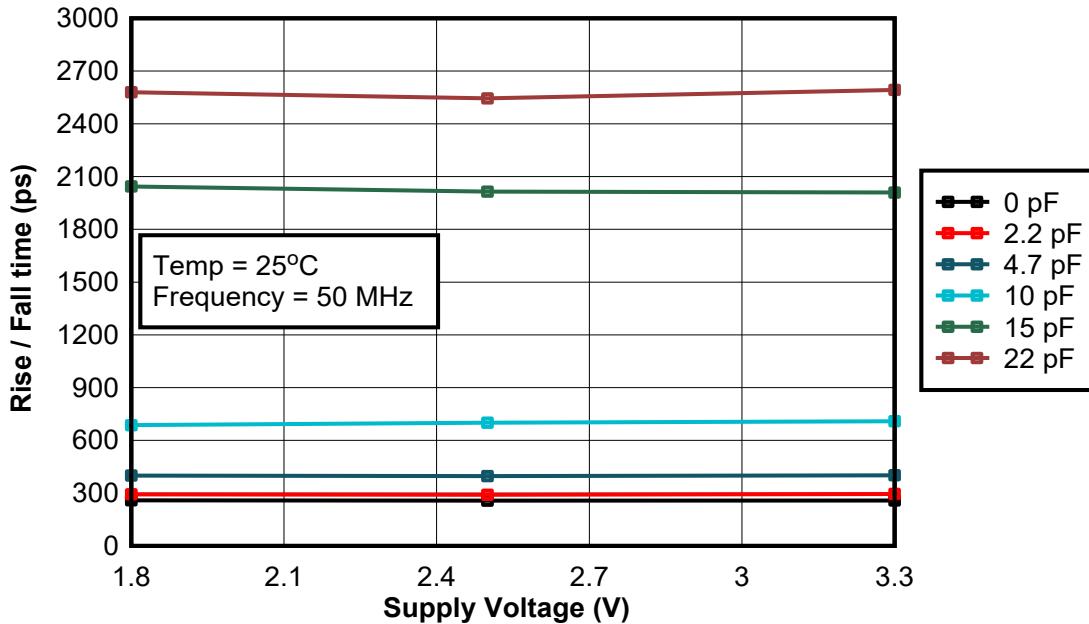


Figure 10-6. Rise / Fall time (ps) vs Supply Voltage vs Load Capacitance

### 10.3 Power Supply Recommendations

For the best electrical performance of the LMK6x, TI recommends use 1  $\mu$ F capacitor on the device power supply bypass network. TI also recommends using component side mounting of the power-supply bypass capacitors, and best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

### 10.4 Layout

#### 10.4.1 Layout Guidelines

The following sections provide recommendations for board layout, solder reflow profile and power-supply bypassing when using the LMK6x to ensure good thermal and electrical performance and signal integrity of the entire system.

##### 10.4.1.1 Ensuring Thermal Reliability

The LMK6x is a high-performance device. Therefore, pay careful attention to device configuration and printed circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more to maximize thermal dissipation out of the package.

The equation below describes the relationship between the PCB temperature around the LMK6x and its junction temperature.

$$T_B = T_J - \Psi_{JB} \times P \quad (1)$$

where

- $T_B$ : PCB temperature around the LMK6x
- $T_J$ : Junction temperature of LMK6x
- $\Psi_{JB}$ : Junction-to-board thermal resistance parameter of LMK6x (refer to the *Thermal Information* tables in the *Specifications* section for this information)
- $P$ : On-chip power dissipation of LMK6x

#### **10.4.1.2 Recommended Solder Reflow Profile**

TI recommends following the solder paste supplier's recommendations to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. It is preferable for the LMK6x to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, Board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well solder manufacturers recommended profile, and capability of the reflow equipment to as confirmed by the SMT assembly operation.

#### 10.4.2 Layout

Refer to the [LMK6EVM User's Guide](#) for printed circuit board layout examples for LMK6D, LMK6H, LMK6P and LMK6C devices. The figures below show the PCB layout example as done on the evaluation module for the LMK6x EVM.

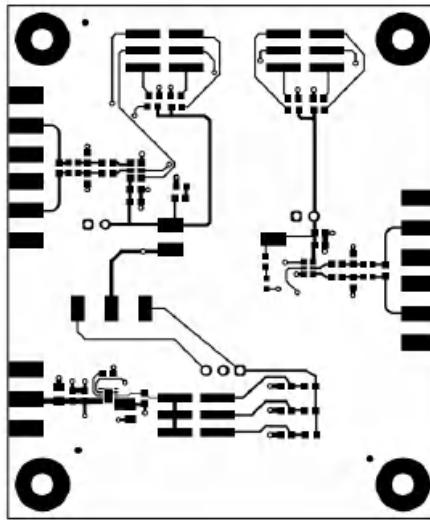


Figure 10-7. PCB Layout Example From LMK6 EVM - Top Layer

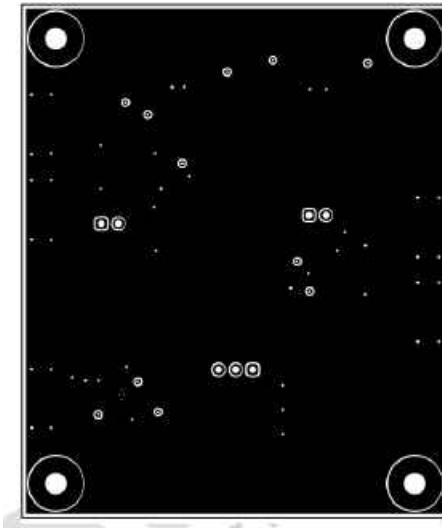


Figure 10-8. PCB Layout Example From LMK6 EVM - GND Layer 1

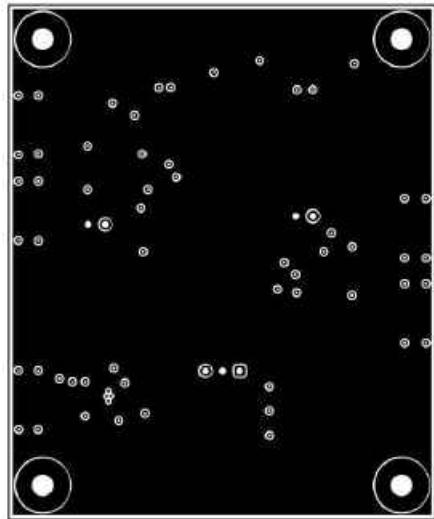


Figure 10-9. PCB Layout Example From LMK6 EVM - GND Layer 2

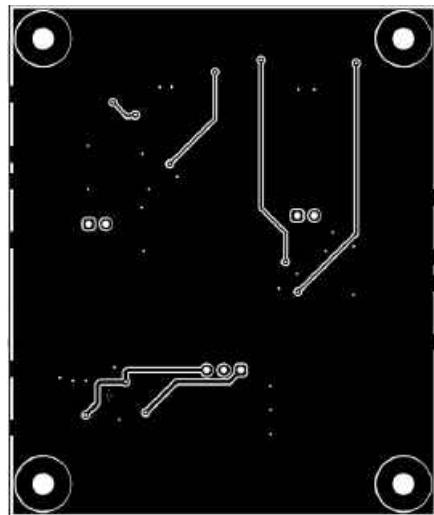


Figure 10-10. PCB Layout Example From LMK6 EVM - Bottom Layer

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [LMK6EVM User's Guide](#)
- Texas Instruments, [Standalone BAW Oscillators Advantages Over Quartz Oscillators application note](#)
- Texas Instruments, [BAW oscillator solutions for Building Automation application note](#)
- Texas Instruments, [BAW oscillator solutions for Factory Automation application note](#)
- Texas Instruments, [BAW oscillator solutions for Grid Infrastructure application note](#)
- Texas Instruments, [BAW oscillator solutions for Optical Modules application note](#)

### 11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 11.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 11.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

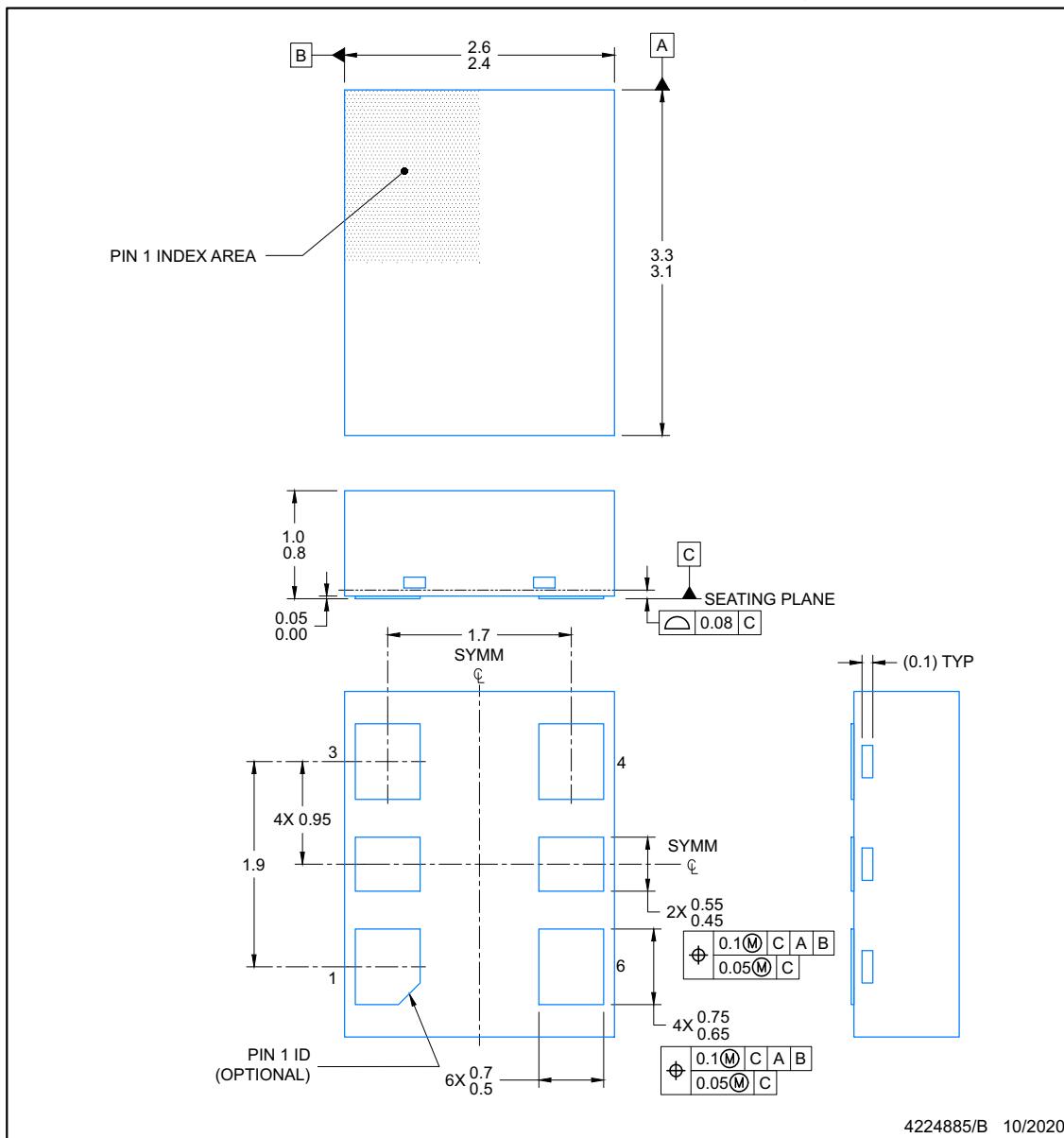
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**DLE0006A**

## PACKAGE OUTLINE

### VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



**NOTES:**

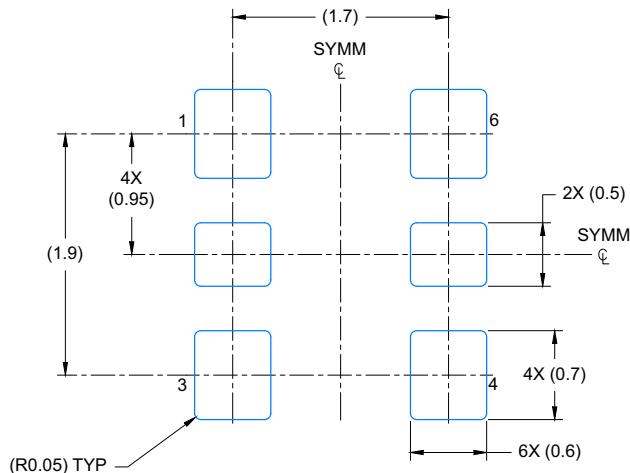
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

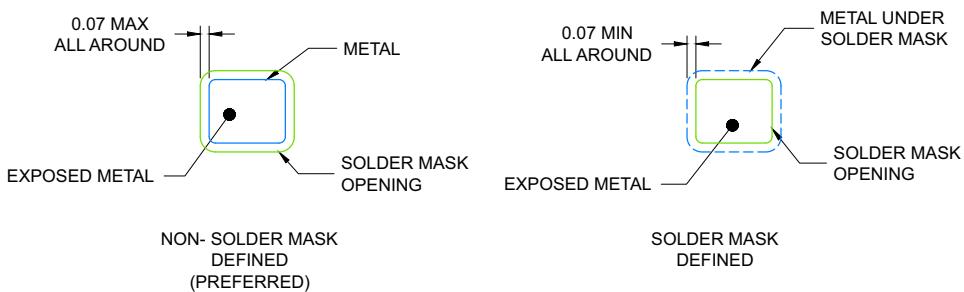
### DLE0006A

### VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

4224885/B 10/2020

NOTES: (continued)

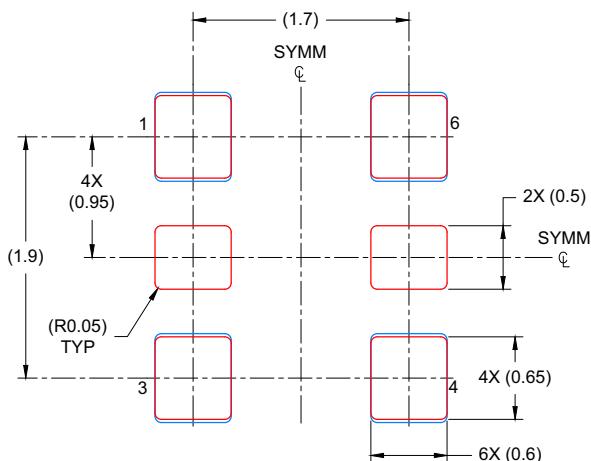
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)) .

## EXAMPLE STENCIL DESIGN

**DLE0006A**

## VSON - 1 mm max height

**PLASTIC QUAD FLAT PACK-NO LEAD**



## SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 1,3,4 & 6: 93%  
SCALE: 20X

4224885/B 10/2020

#### NOTES: (continued)

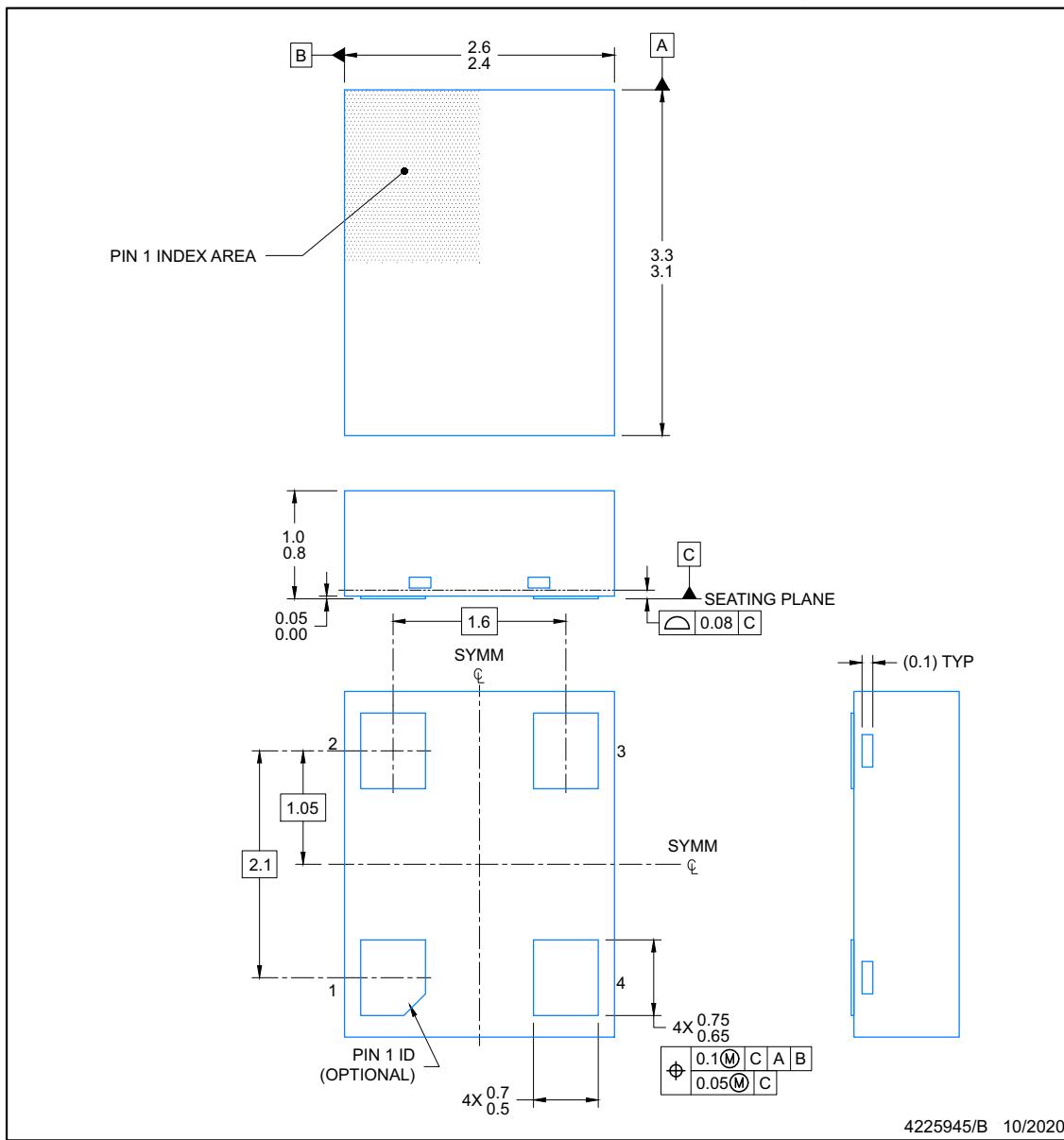
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



**DLE0004A**

**PACKAGE OUTLINE  
VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

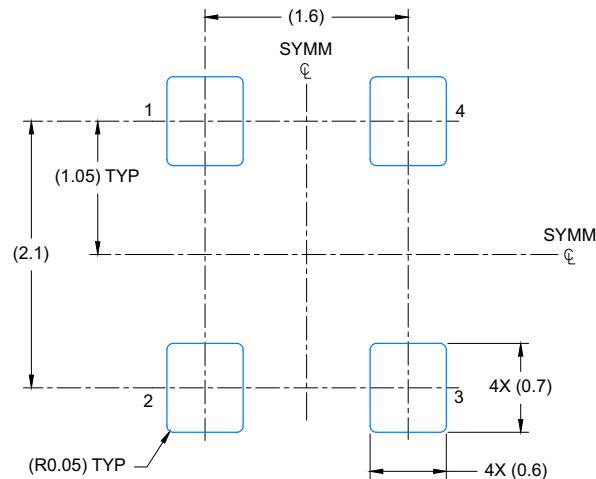
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

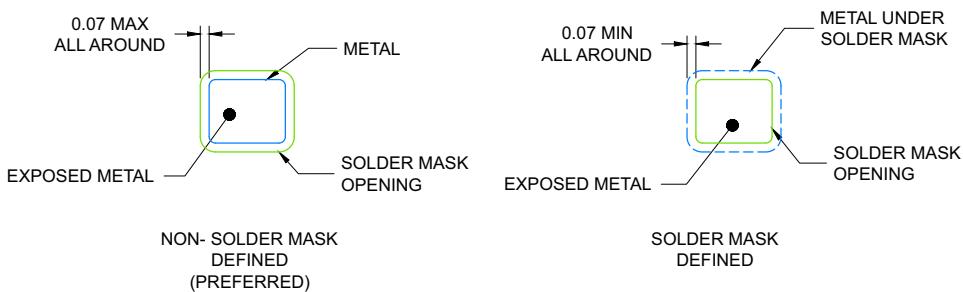
**DLE0004A**

**VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

4225945/B 10/2020

NOTES: (continued)

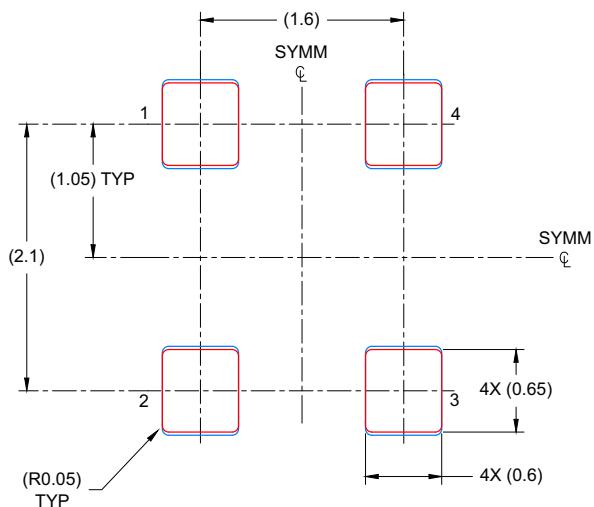
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)) .

## EXAMPLE STENCIL DESIGN

**DLE0004A**

**VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
ALL PADS: 93%  
SCALE: 20X

4225945/B 10/2020

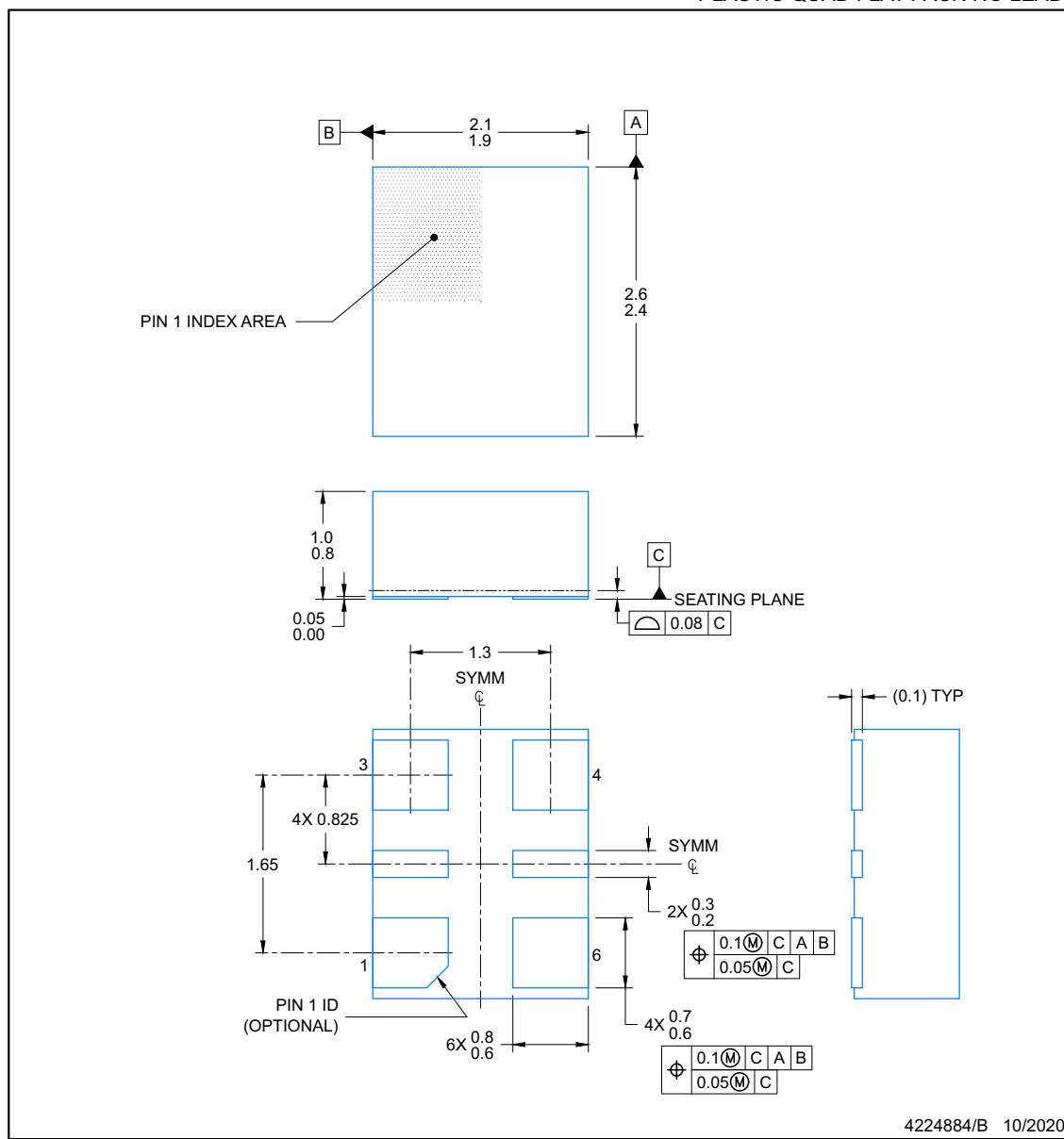
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGE OUTLINE

### VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

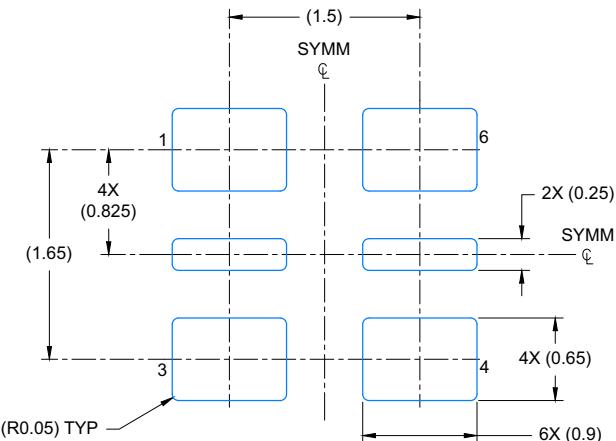
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

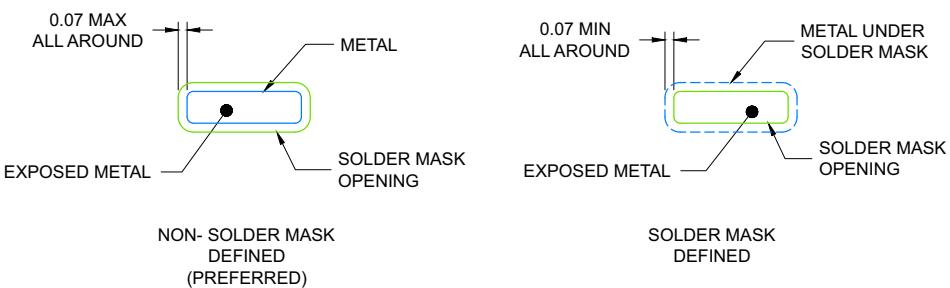
DLF0006A

VSON - 1 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

4224884/B 10/2020

NOTES: (continued)

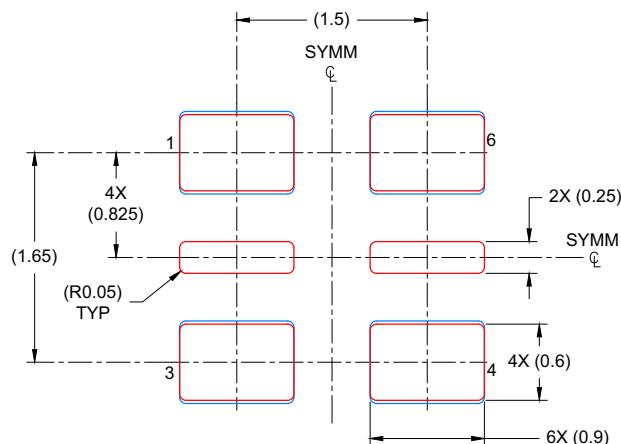
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)) .

## EXAMPLE STENCIL DESIGN

**DLF0006A**

**VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 1,3,4 & 6: 92%  
SCALE: 20X

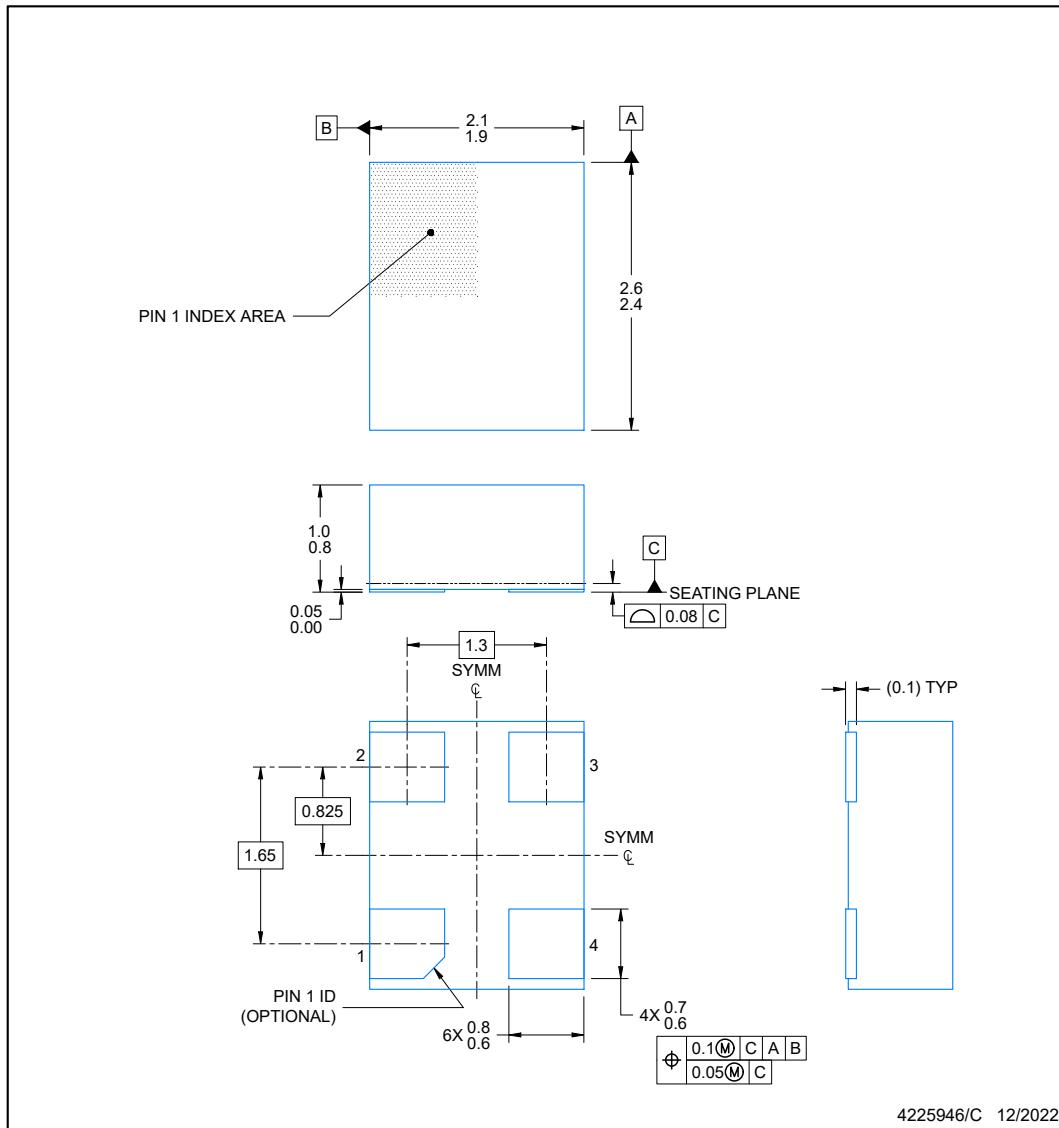
4224884/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGE OUTLINE**  
**DLF0004A**

PLASTIC QUAD FLAT PACK-NO LEAD

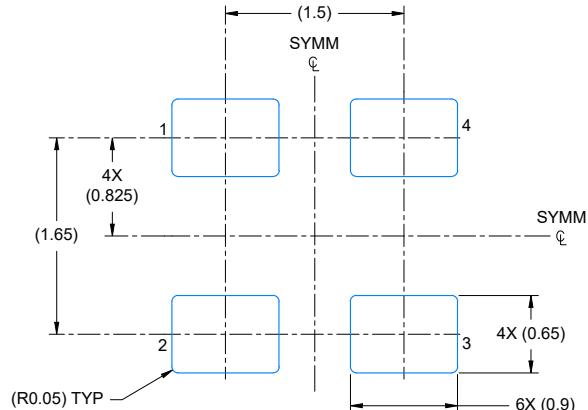


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT DLF0004A

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

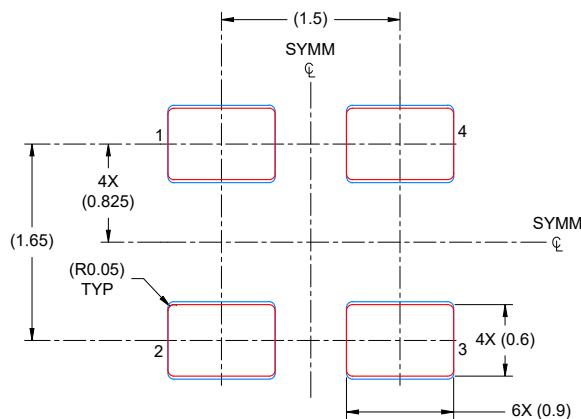
4225946/C 12/2022

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

**EXAMPLE STENCIL DESIGN**  
**DLF0004A**

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 1,3,4 & 6: 92%  
SCALE: 20X

4225946/C 12/2022

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK6CE012288CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBJ	Samples
LMK6CE012288CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBJ	Samples
LMK6CE02500CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBG	Samples
LMK6CE02500CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCBG	Samples
LMK6CE02500DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1G	Samples
LMK6CE02500DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1G	Samples
LMK6CE03333CDLER	ACTIVE	VSON	DLE	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB8	Samples
LMK6CE03333CDLET	ACTIVE	VSON	DLE	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB8	Samples
LMK6CE04000CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB6	Samples
LMK6CE04000CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HCB6	Samples
LMK6CE04800DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1C	Samples
LMK6CE04800DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC1C	Samples
LMK6CE05000CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCCB	Samples
LMK6CE05000CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCCB	Samples
LMK6CE07425DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC19	Samples
LMK6CE07425DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC19	Samples
LMK6CE10000CDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCB8	Samples
LMK6CE10000CDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LCB8	Samples
LMK6CE10000DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC18	Samples
LMK6CE10000DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC18	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK6CE12500CDLER	ACTIVE	VSON	DLE	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCB6	Samples
LMK6CE12500CDLET	ACTIVE	VSON	DLE	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LCB6	Samples
LMK6CE15625DDLFR	ACTIVE	VSON	DLF	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC12	Samples
LMK6CE15625DDLFT	ACTIVE	VSON	DLF	4	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	LC12	Samples
LMK6DA05184ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	HDAH	Samples
LMK6DA05184ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		HDAH	Samples
LMK6DA12288ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA4	Samples
LMK6DA12288ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA4	Samples
LMK6DA12500ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LDA6	Samples
LMK6DA12500ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LDA6	Samples
LMK6DA15552ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA3	Samples
LMK6DA15552ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA3	Samples
LMK6DA20000ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA1	Samples
LMK6DA20000ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HDA1	Samples
LMK6HA10000ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA8	Samples
LMK6HA10000BDLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH18	Samples
LMK6HA10000BDLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LH18	Samples
LMK6HA15625ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA2	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK6HA15625ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LHA2	Samples
LMK6PA15625ADLER	ACTIVE	VSON	DLE	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples
LMK6PA15625ADLET	ACTIVE	VSON	DLE	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples
LMK6PA15625ADLFR	ACTIVE	VSON	DLF	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples
LMK6PA15625ADLFT	ACTIVE	VSON	DLF	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LPA2	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

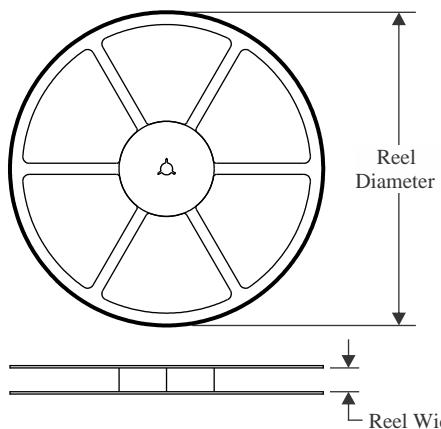
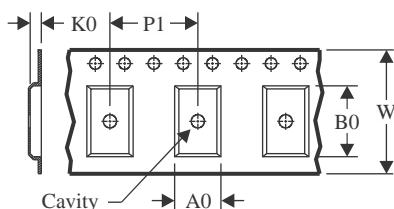
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

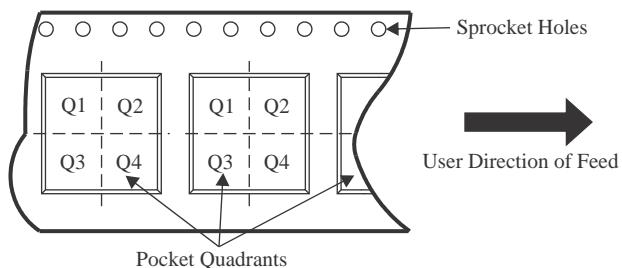
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continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

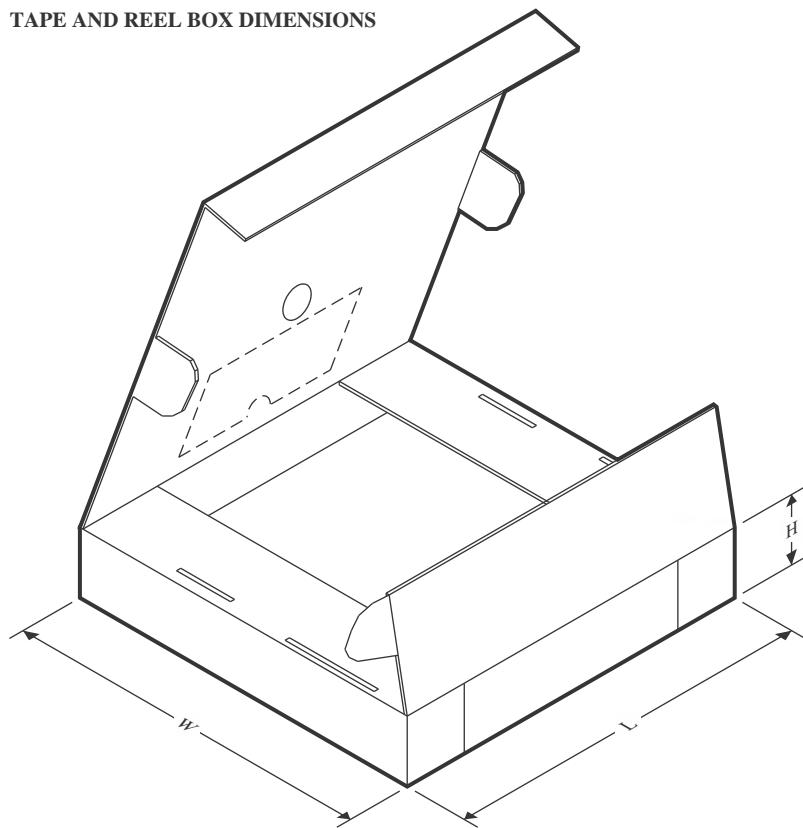
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK6CE012288CDLFR	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE012288CDLFT	VSON	DLF	4	250	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE02500DDLFT	VSON	DLF	4	250	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE04000CDLFR	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE04800DDLFT	VSON	DLF	4	250	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE07425DDLFT	VSON	DLF	4	250	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE10000CDLFR	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE10000CDLFT	VSON	DLF	4	250	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE10000DDLFR	VSON	DLF	4	3000	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6CE10000DDLFT	VSON	DLF	4	250	180.0	8.4	2.25	2.8	1.1	4.0	8.0	Q1
LMK6DA05184ADLER	VSON	DLE	6	3000	330.0	12.4	2.8	3.5	1.2	4.0	12.0	Q1
LMK6DA05184ADLET	VSON	DLE	6	250	180.0	12.4	2.8	3.5	1.2	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK6CE012288CDLFR	VSON	DLF	4	3000	182.0	182.0	20.0
LMK6CE012288CDLFT	VSON	DLF	4	250	182.0	182.0	20.0
LMK6CE02500DDLFT	VSON	DLF	4	250	182.0	182.0	20.0
LMK6CE04000CDLFR	VSON	DLF	4	3000	210.0	185.0	35.0
LMK6CE04800DDLFT	VSON	DLF	4	250	182.0	182.0	20.0
LMK6CE07425DDLFT	VSON	DLF	4	250	182.0	182.0	20.0
LMK6CE10000CDLFR	VSON	DLF	4	3000	182.0	182.0	20.0
LMK6CE10000CDLFT	VSON	DLF	4	250	182.0	182.0	20.0
LMK6CE10000DDLFR	VSON	DLF	4	3000	182.0	182.0	20.0
LMK6CE10000DDLFT	VSON	DLF	4	250	182.0	182.0	20.0
LMK6DA05184ADLER	VSON	DLE	6	3000	346.0	346.0	33.0
LMK6DA05184ADLET	VSON	DLE	6	250	182.0	182.0	20.0

## GENERIC PACKAGE VIEW

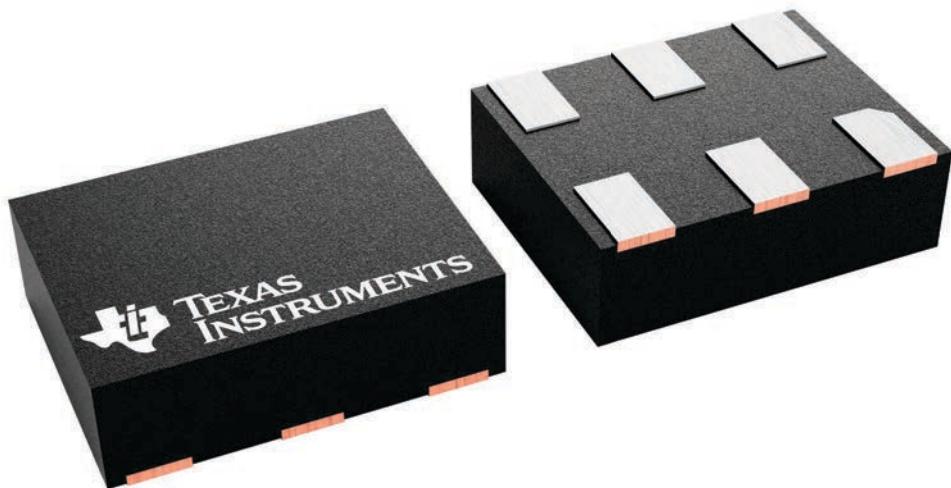
### DLE 6

### VSON - 1 mm max height

2.5 x 3.2, multiple pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



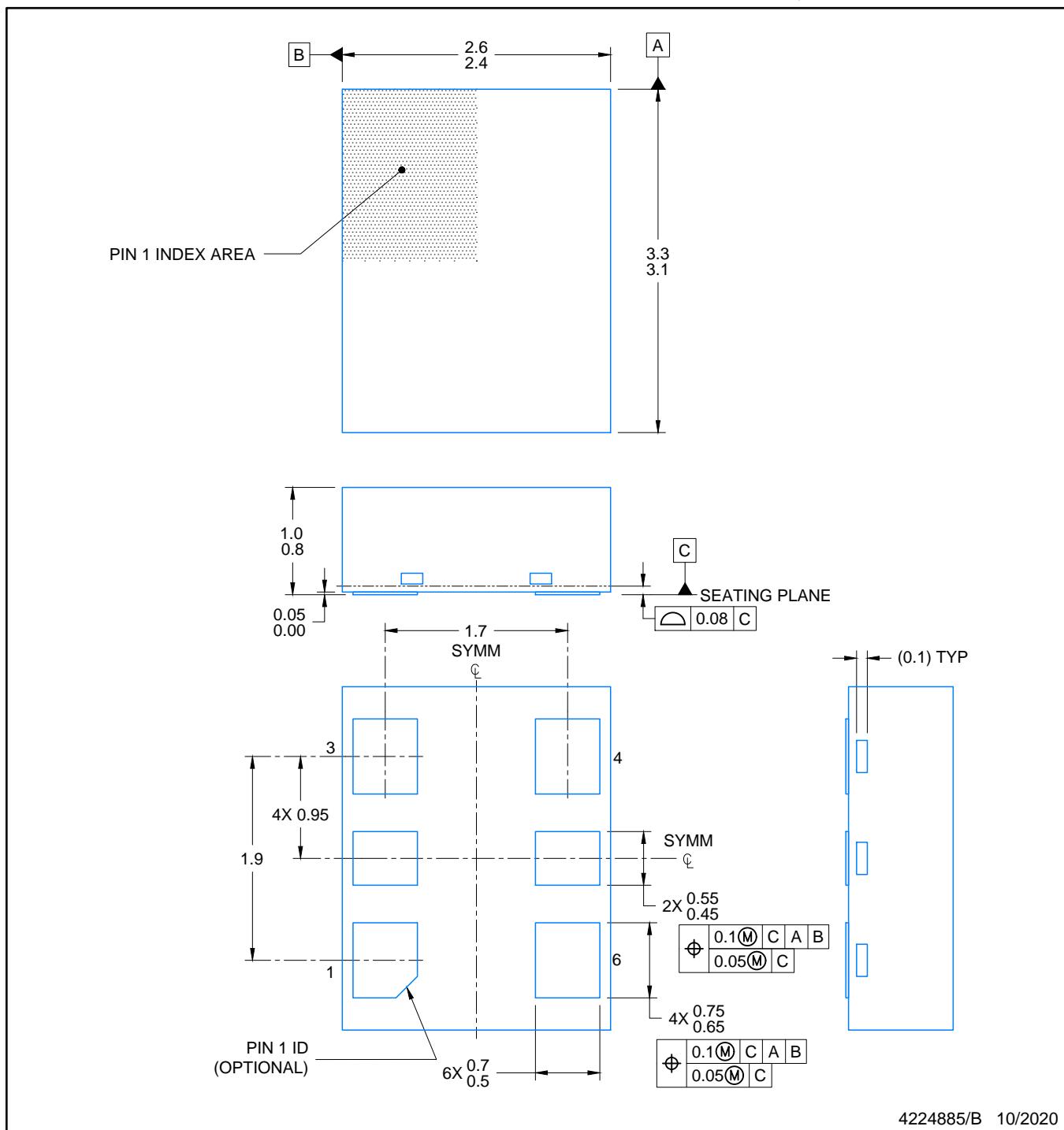
4229714/A

# PACKAGE OUTLINE

## VSON - 1 mm max height

DLE0006A

PLASTIC QUAD FLAT PACK-NO LEAD



NOTES:

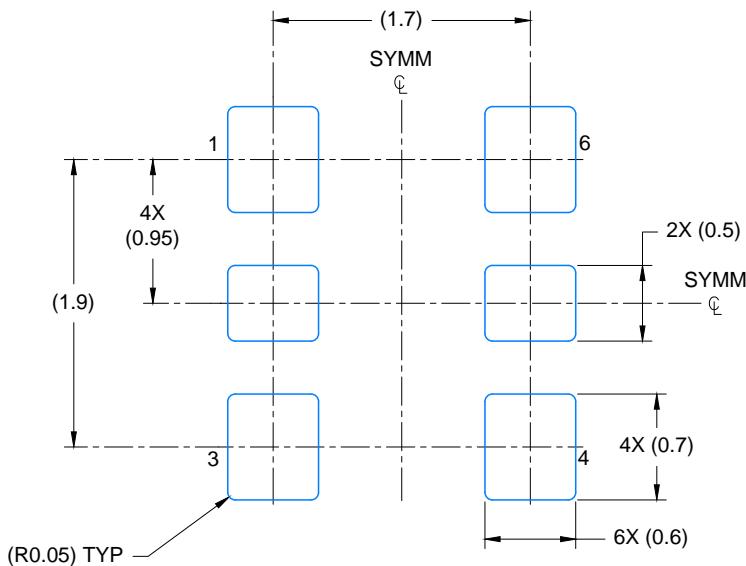
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

VSON - 1 mm max height

DLE0006A

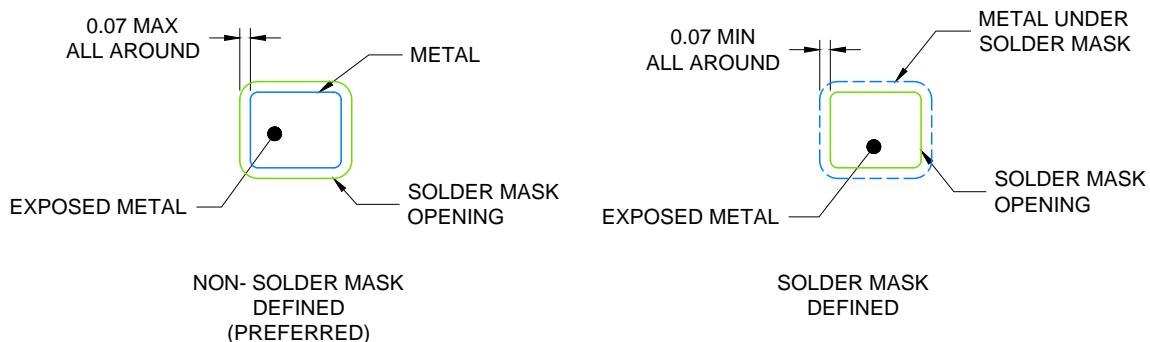
PLASTIC QUAD FLAT PACK-NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



## SOLDER MASK DETAILS

4224885/B 10/2020

NOTES: (continued)

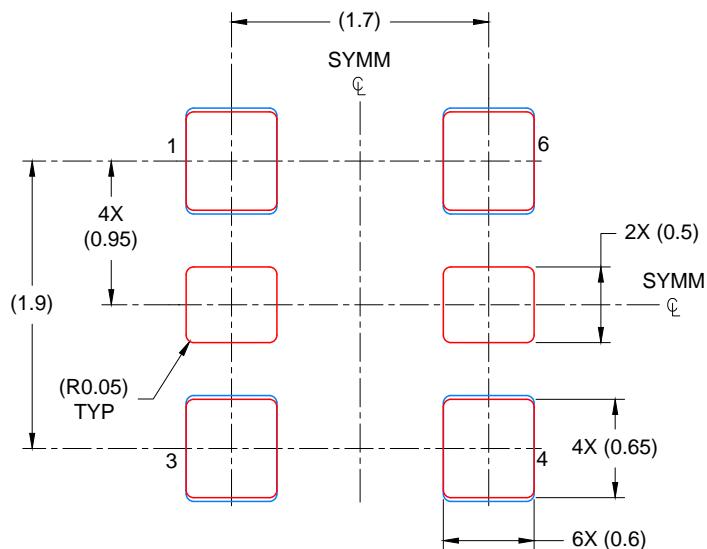
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)) .

# EXAMPLE STENCIL DESIGN

VSON - 1 mm max height

DLE0006A

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 1,3,4 & 6: 93%  
SCALE: 20X

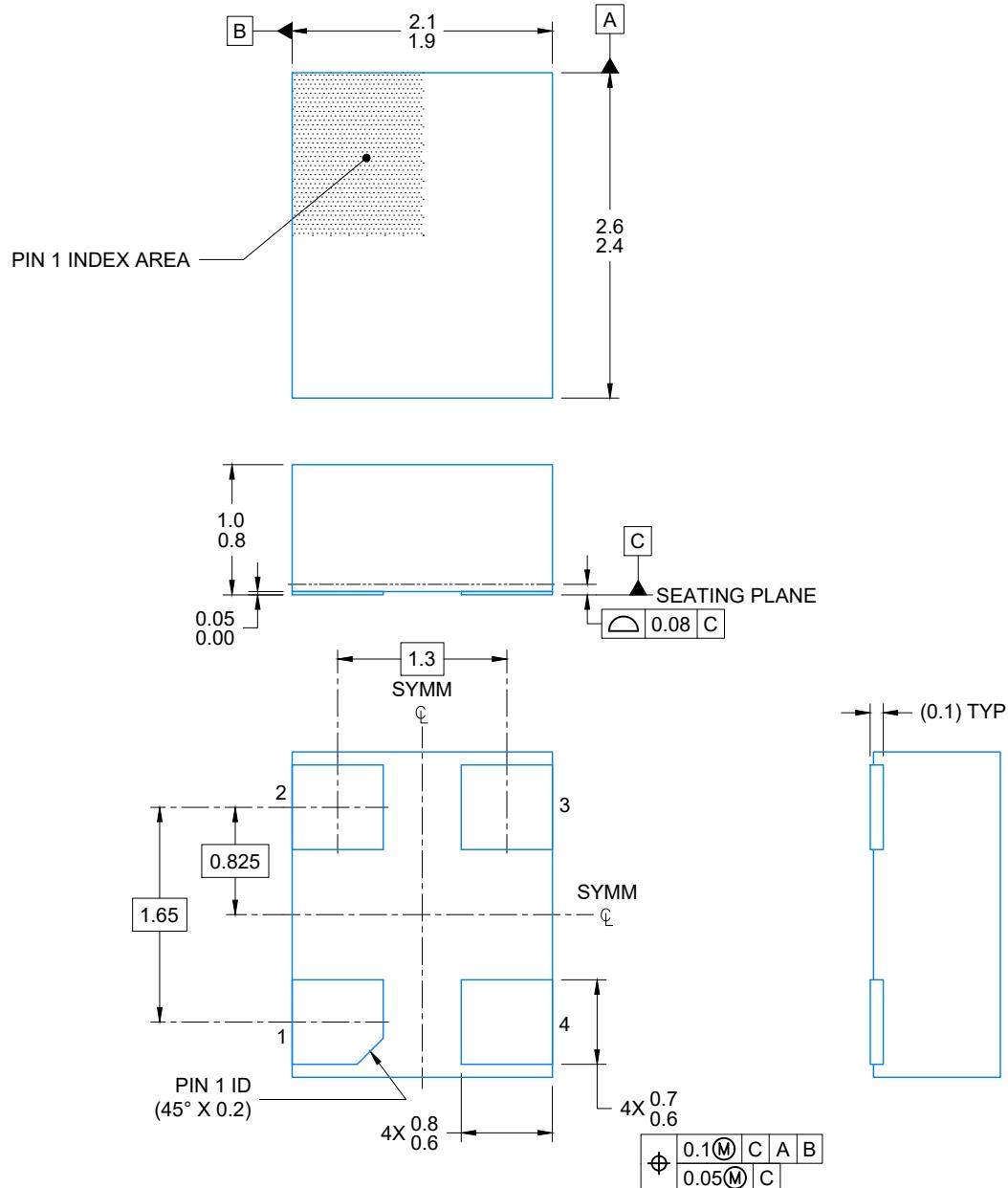
4224885/B 10/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**DLF0004A****PACKAGE OUTLINE  
VSON - 1 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



4225946/D 03/2023

## NOTES:

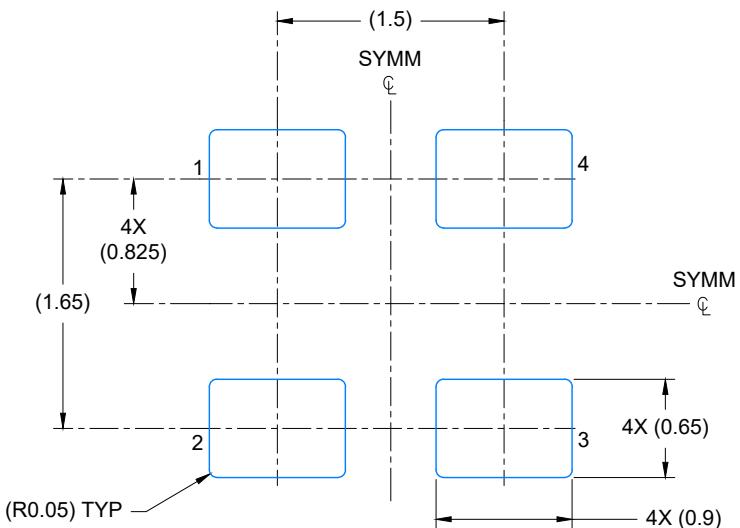
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

VSON - 1 mm max height

DLF0004A

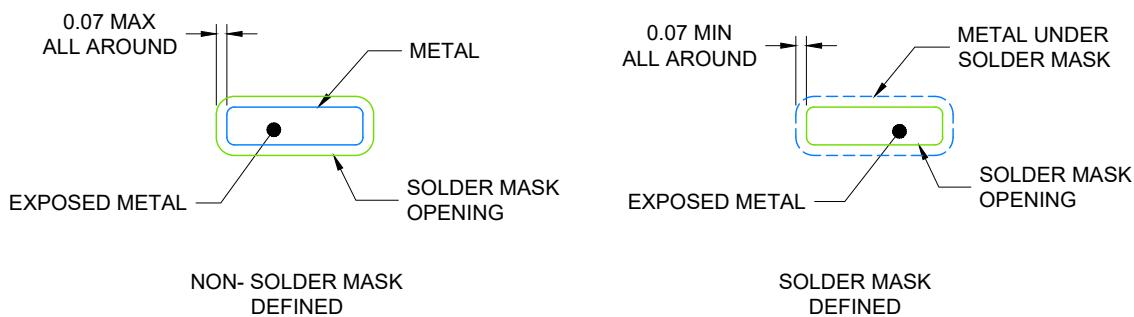
PLASTIC QUAD FLAT PACK-NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



## SOLDER MASK DETAILS

4225946/D 03/2023

NOTES: (continued)

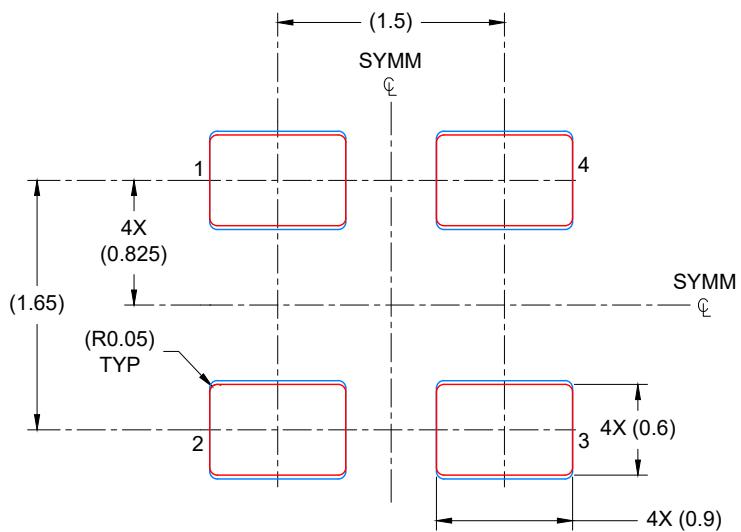
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

VSON - 1 mm max height

DLF0004A

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 1,3,4 & 6: 92%  
SCALE: 20X

4225946/D 03/2023

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# GENERIC PACKAGE VIEW

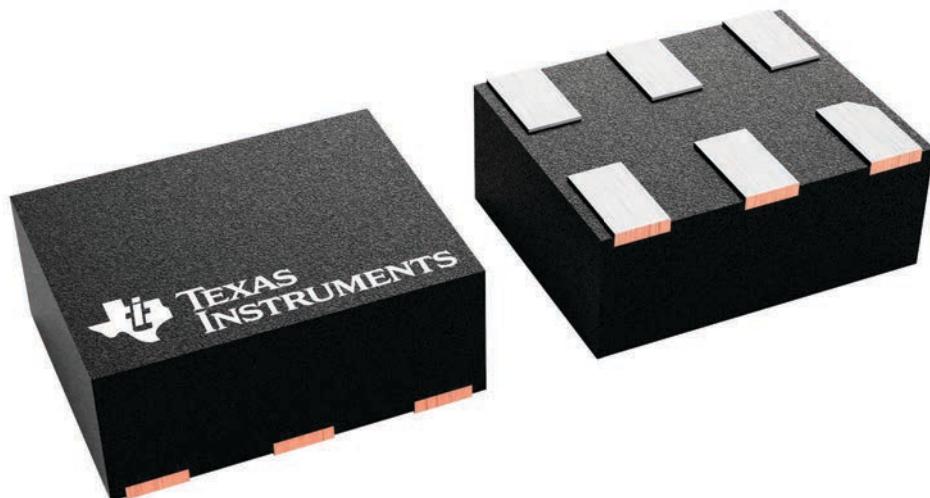
## DLF 6

## VSON - 1 mm max height

2 x 2.5, multiple pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



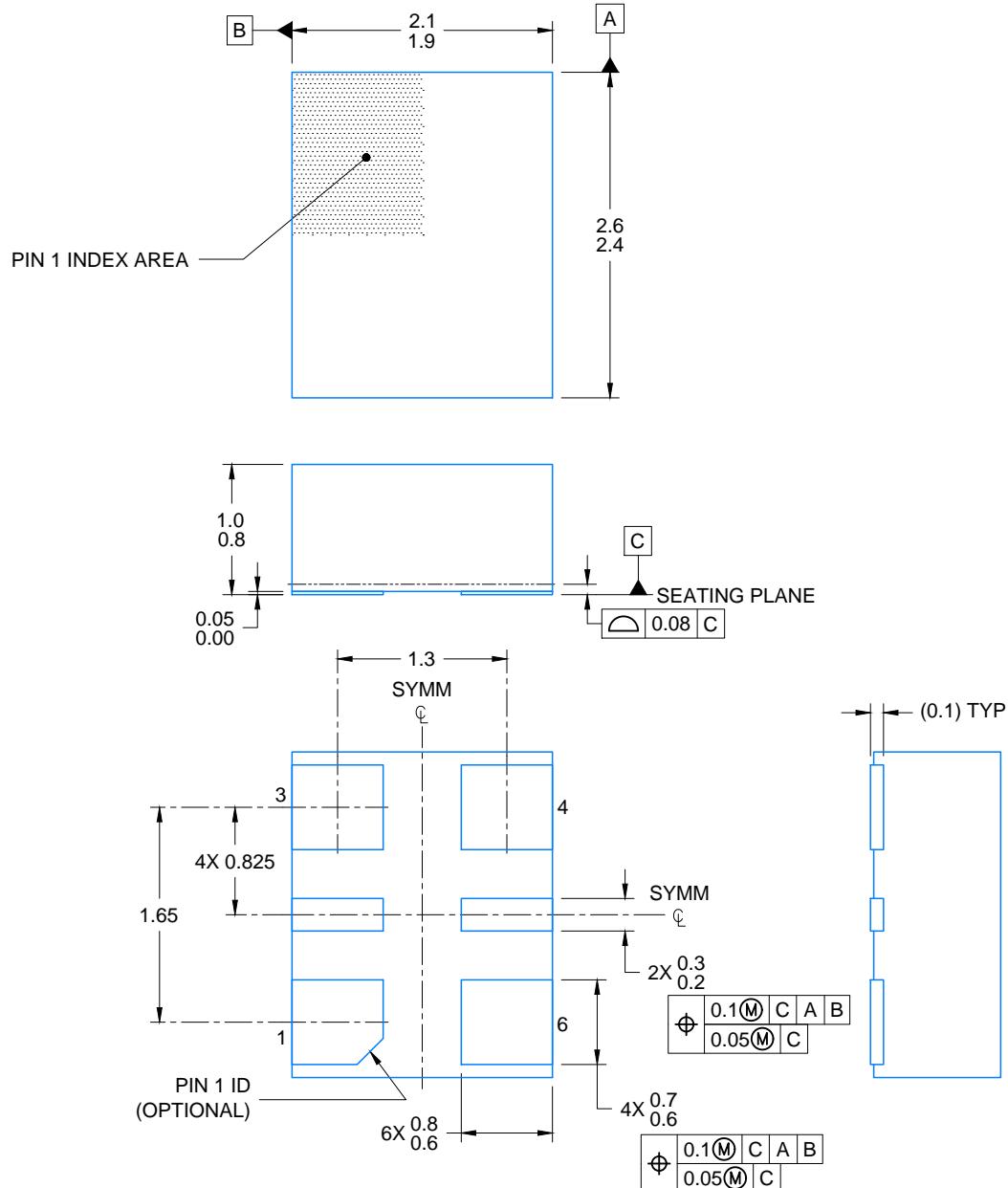
4229715/A

# PACKAGE OUTLINE

## VSON - 1 mm max height

DLF0006A

PLASTIC QUAD FLAT PACK-NO LEAD



4224884/B 10/2020

NOTES:

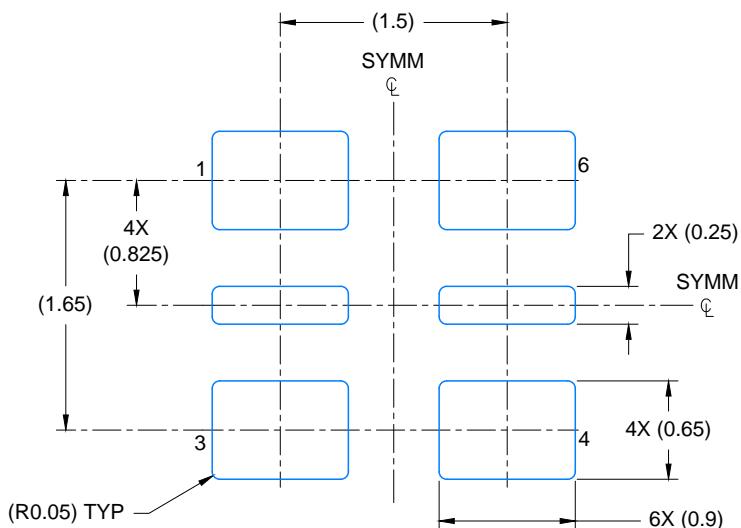
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

VSON - 1 mm max height

DLF0006A

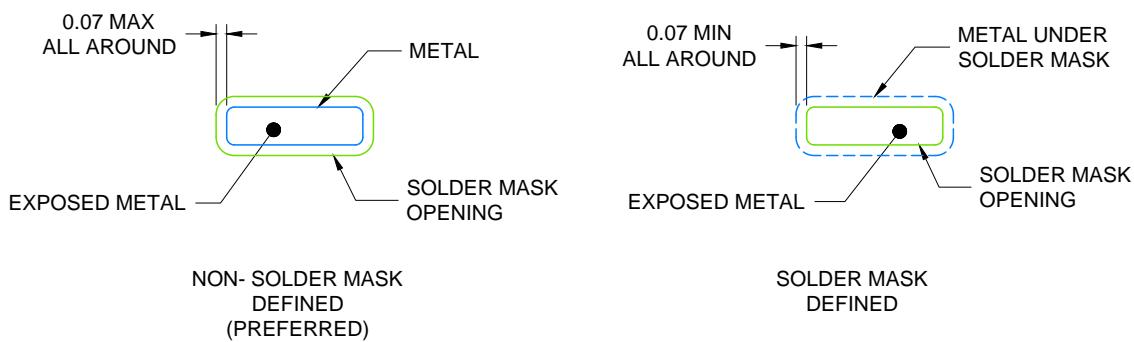
PLASTIC QUAD FLAT PACK-NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



## SOLDER MASK DETAILS

4224884/B 10/2020

NOTES: (continued)

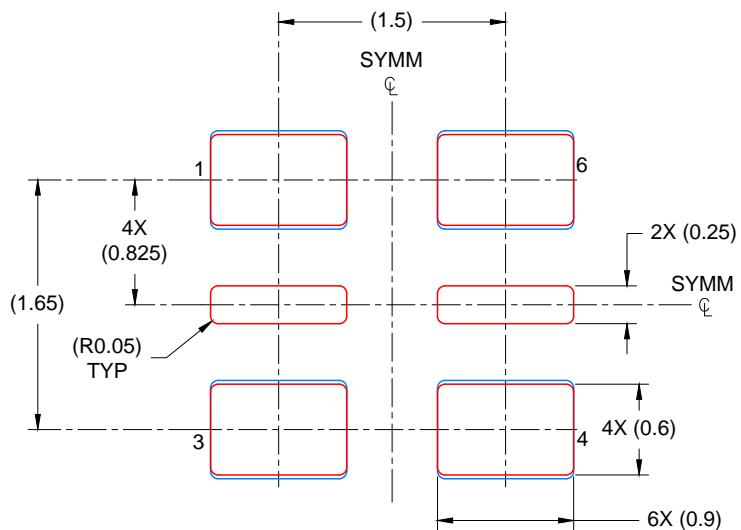
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)) .

# EXAMPLE STENCIL DESIGN

VSON - 1 mm max height

DLF0006A

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
PADS 1,3,4 & 6: 92%  
SCALE: 20X

4224884/B 10/2020

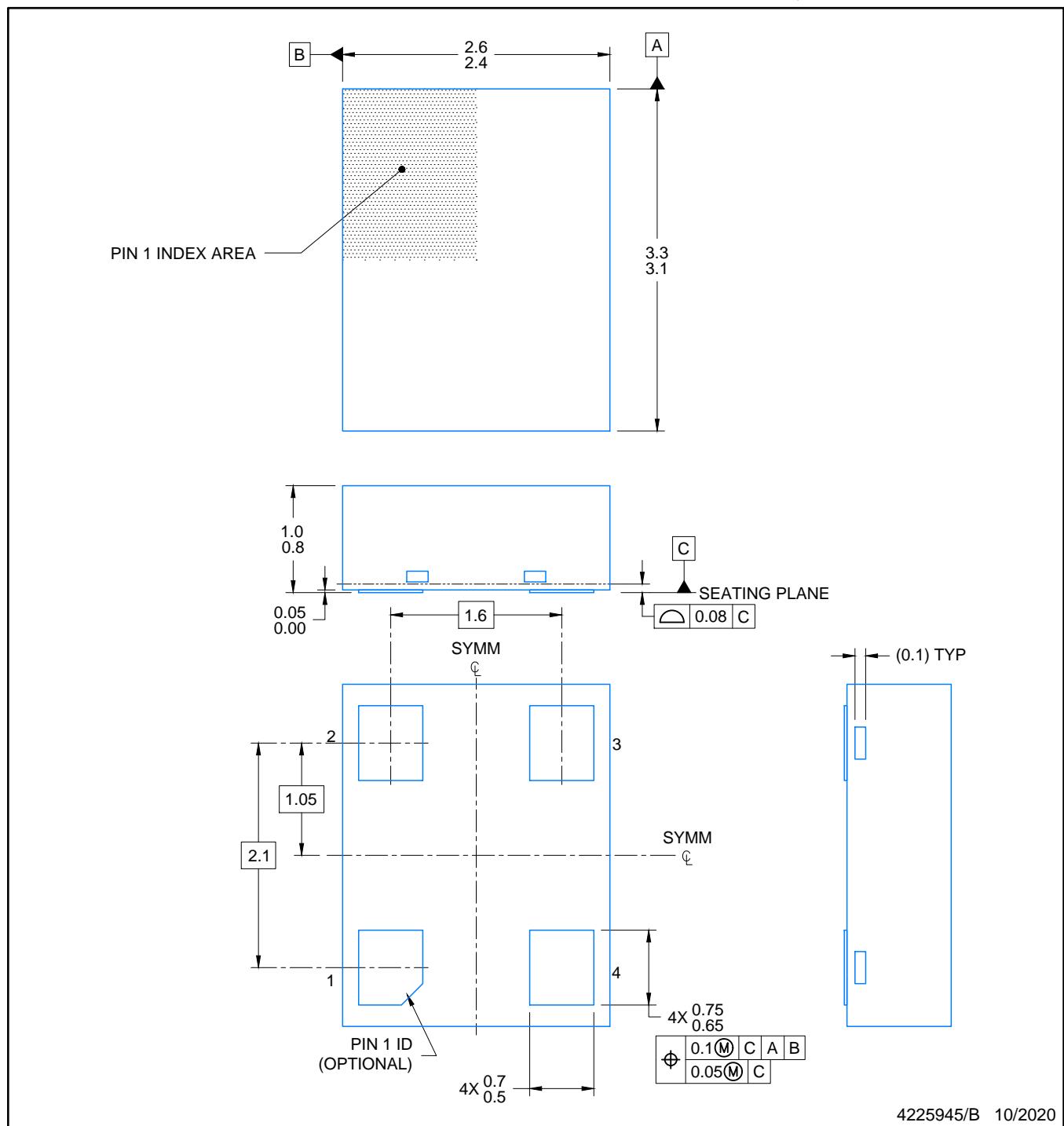
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGE OUTLINE VSON - 1 mm max height

**DLE0004A**

## PLASTIC QUAD FLAT PACK-NO LEAD



**NOTES:**

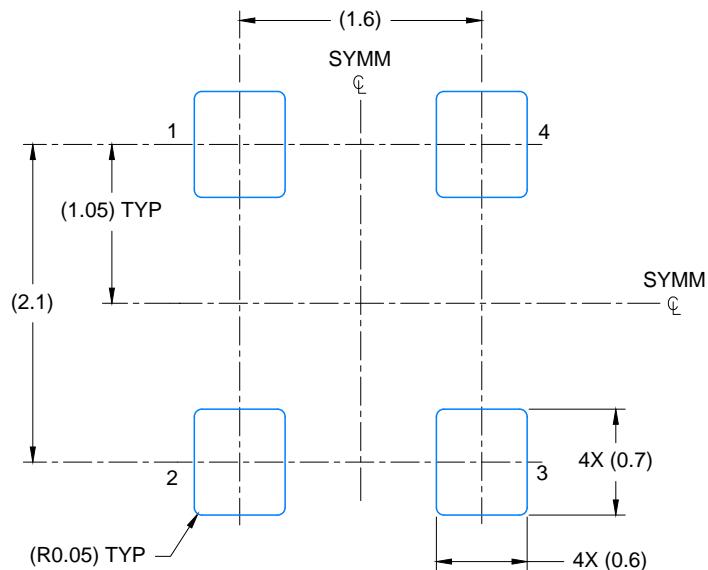
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

VSON - 1 mm max height

DLE0004A

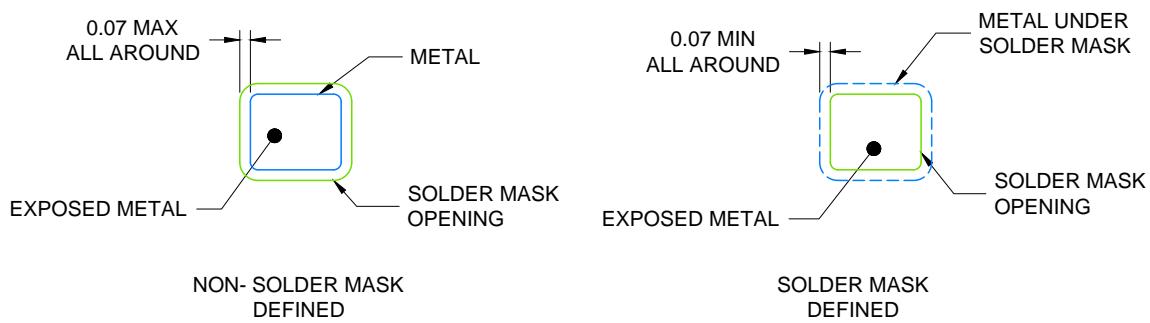
PLASTIC QUAD FLAT PACK-NO LEAD



## LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



## SOLDER MASK DETAILS

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NOTES: (continued)

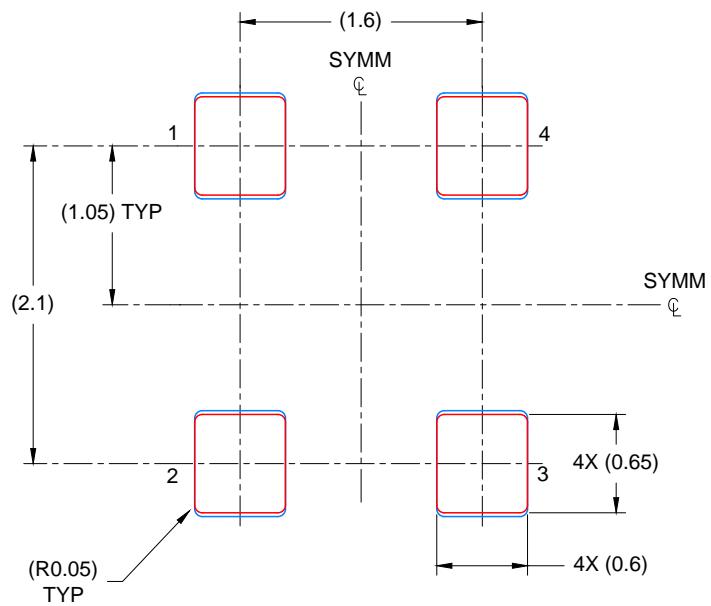
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)) .

# EXAMPLE STENCIL DESIGN

VSON - 1 mm max height

DLE0004A

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
ALL PADS: 93%  
SCALE: 20X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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