MP86950

Intelli-Phase™ Solution, Monolithic Half-Bridge with Integrated Internal Power MOSFETs and Gate Drivers

DESCRIPTION

The MP86950 is a monolithic half-bridge with built-in internal power MOSFETs and gate drivers. The MP86950 achieves 50A of continuous output current over a wide input supply range (4.5V to 16V).

The MP86950 is a monolithic IC that can drive up to 50A of current per phase. The integrated MOSFETs and drivers achieve high efficiency through optimized dead time and reduced parasitic inductance. The MP86950 has an operating range of 100kHz to 2MHz.

The MP86950 offers many features to simplify system design. The MP86950 is compatible with tri-state pulse-width modulation (PWM) signal controllers, has an Accu-Sense™ current sense to monitor the inductor current, and has a temperature sense to report the junction temperature.

The MP86950 is ideal for server applications where high efficiency and small size are critical. The MP86950 is available in a small TLGA-27 (4mmx5mm) package.

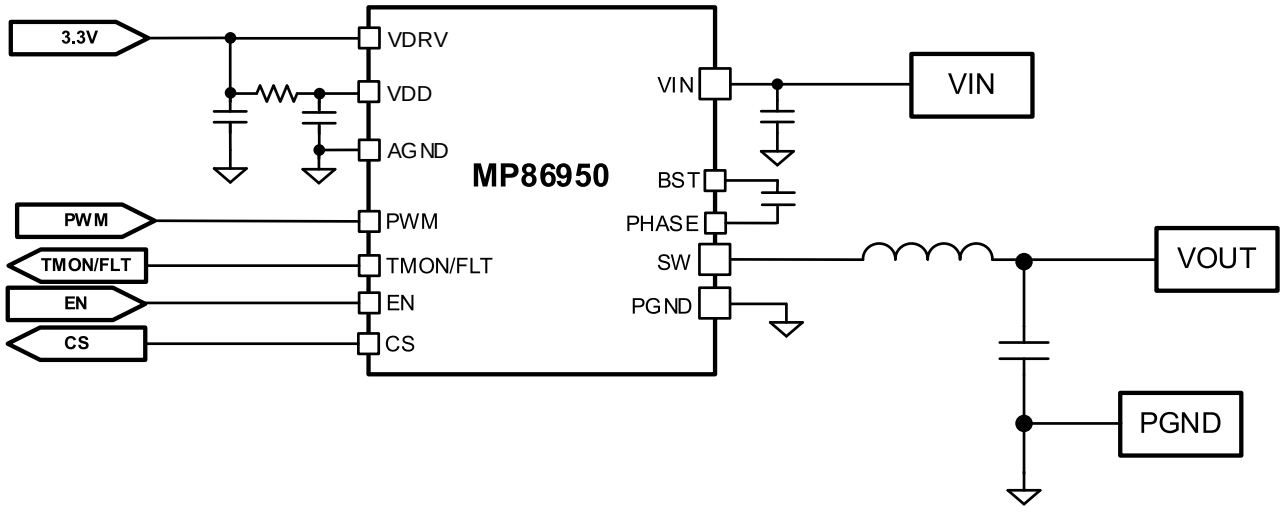
FEATURES

- Wide 4.5V to 16V Operating Input Range
- 50A Output Current
- Current Sense with Accu-Sense™
- Temperature Sense
- Accepts Tri-State Pulse-Width Modulation (PWM) Signal
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in a TLGA-27 (4mmx5mm) Package

APPLICATIONS

- Server Core Voltages
- Graphic Card Core Regulators
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number	Package	Top Marking	MSL Rating
MP86950GLVT	TLGA-27 (4mmx5mm)	*See Below*	3

* For Tape & Reel, add suffix –Z (e.g. MP86950GLVT–Z).

TOP MARKING

MPSYWW

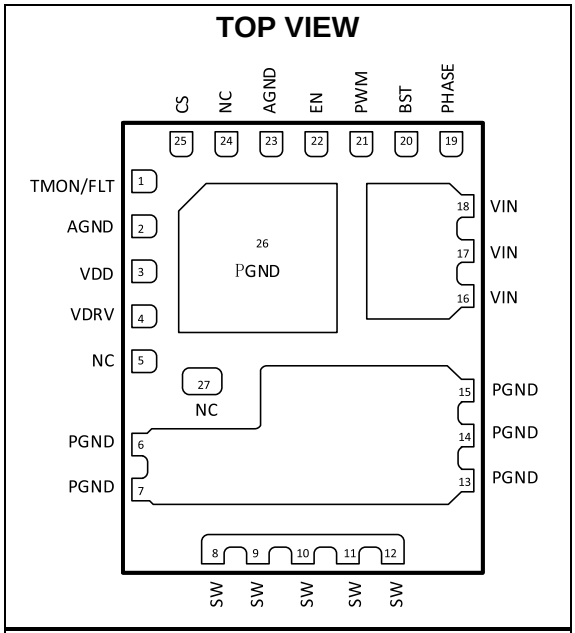
M86950

LLLLLL

T

MPS: MPS prefix
Y: Year code
WW: Week code
M86950: Part number
LLLLLL: Lot number
T: TLGA package

PACKAGE REFERENCE



TLGA-27 (4mmx5mm)

PIN FUNCTIONS

Pin #	Name	Description
1	TMON/FLT	**Single-pin temperature sense and fault reporting.**
2, 23	AGND	**Analog ground.**
3	VDD	**Supply voltage (3.3V) for the internal circuitry.** Decouple VDD using a 1µF or greater ceramic capacitor connected to AGND.
4	VDRV	**Driver voltage.** Connect the VDRV pin to the 3.3V supply. Decouple VDRV with a 1µF to 4.7µF ceramic capacitor.
5, 24, 27	NC	**No connection.**
6, 7, 13, 14, 15, 26	PGND	**Power ground.**
8, 9, 10, 11, 12	SW	**Switch output.**
16, 17, 18	VIN	**Supply voltage.** Place a ceramic input capacitor (C_{IN}) close to the device to support the switching current and minimize parasitic inductance.
19	PHASE	**Switching node for the bootstrap capacitor connection.** The PHASE pin is connected to the SW pin internally.
20	BST	**Bootstrap.** The BST pin requires a 0.1µF to 1µF capacitor to drive the power switch's gate above the supply voltage. Connect BST to the capacitor between PHASE and BST to form a floating supply across the switch driver.
21	PWM	**Pulse-width modulation input.** Float the PWM pin or drive PWM to a middle state to enable diode emulation mode.
22	EN	**Enable.** Pull the EN pin low to disable the device and put SW in a high-impedance state.
25	CS	**Current-sense output.** The CS pin has a bi-directional current output proportional to the inductor current. Connect this pin to the PWM controller's current sense input. Connect a resistor to a common mode voltage, so that the differential voltage is proportional to the inductor current.

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{SW} (DC)..... -0.3V to V_{IN} + 0.3V
V_{SW} (25ns)..... -5V to +25V
VIN - V_{PHASE} (DC) ..... -0.3V to +25V
VIN - V_{PHASE} (10ns)..... -5V to +32V
V_{BST} - V_{PHASE} (25ns)..... 5V
V_{BST} ..... V_{PHASE} + 4V
VDD, VDRV ..... -0.3V to +4V
All other pins ..... -0.3V to VDD + 0.3V
Instantaneous current 90A
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) ..... Class 1C
Charged device model (CDM) ..... Class C2B

Recommended Operating Conditions (2)

Supply voltage (V_{IN}) ..... 4.5V to 16V
Driver voltage (V_{DRV}) ..... 3.0V to 3.6V
Logic voltage (V_{DD})..... 3.0V to 3.6V
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance (3) (4) θ_{JB} θ_{JC_TOP}

TLGA-27 (4mmx5mm) ..... 3.1..... 9.1....°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point.
4) θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DRV} = V_{DD} = V_{EN} = 3.3V, tested at T_A = 25°C for typical values and T_J = -40°C to +125°C for minimum and maximum values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown	I_{VIN_OFF}	EN = low			40	μA
VIN under-voltage lockout (UVLO) rising threshold				2.5	3.0	V
VIN UVLO hysteresis threshold				600		mV
Quiescent current	I_{VDRV}	EN = low			60	μA
	I_{VDRV}	PWM = low		4	5.08	mA
VDD voltage UVLO rising threshold				2.75	2.95	V
VDD voltage UVLO hysteresis threshold				275		mV
High-side (HS) current limit (5)	I_{LIM_FLT}	Cycle-by-cycle, up to four cycles		75		A
Low-side (LS) current limit (5)		Negative cycle-by-cycle current limit, no fault report		-30		A
Negative LS current limit off time (5)				40		ns
HS current limit shutdown counter (5)				4		times
EN input low voltage					0.8	V
EN input high voltage			2.30			V
Dead time rising (5)				3		ns
Dead time falling (5)		Positive inductor current		6		ns
		Negative inductor current		35		ns
PWM high to SW rising delay (5)	t_{RISING}			15		ns
PWM low to SW falling delay (5)	$t_{FALLING}$			15		ns
PWM tri-state to SW Hi-Z delay (5)	t_{LT}			40		ns
	t_{TL}			20		ns
	t_{HT}			40		ns
	t_{TH}			20		ns

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{DRV} = V_{DD} = V_{EN} = 3.3V, tested at T_A = 25°C for typical values and T_J = -40°C to +125°C for minimum and maximum values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PWM minimum pulse width (5)				20		ns
Current-Sense (CS) sense gain accuracy		15A ≤ I_{OUT} ≤ 50A	-2	0	+2	%
CS gain				10		µA/A
CS offset		I_{OUT} = 0A	-7		+7	µA
CS voltage range (5)	V_{CS}		0.7		2.1	V
TMON/FLT sense gain (5)				8		mV/°C
TMON/FLT sense offset (5)		T_J = 25°C		800		mV
Over-temperature shutdown and fault flag (5)				160		°C
Over-temperature hysteresis threshold (5)				30		°C
PWM input current	I_{PWM}	V_{PWM} = 3.3V, V_{EN} = 3.3V		660		µA
		V_{PWM} = 0V, V_{EN} = 3.3V		-550		µA
PWM logic high voltage			2.35			V
PWM tri-state region			1.10		1.90	V
PWM logic low voltage					0.80	V
TMON/FLT pull-up voltage		Sink 0.5mA, 500mΩ pull-up resistor		V_{DD} - 0.25		V

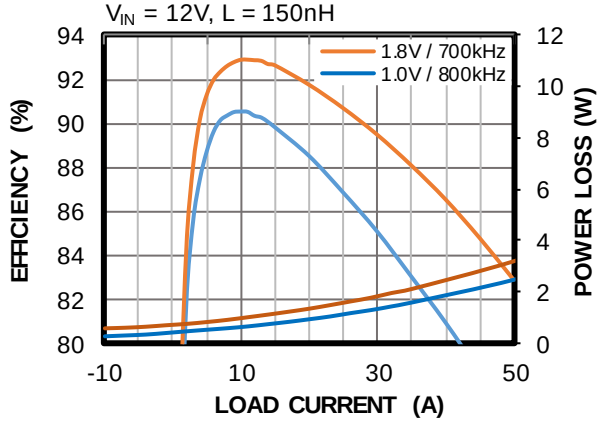
Note:

5) Guaranteed by design or characterization data; not tested in production.

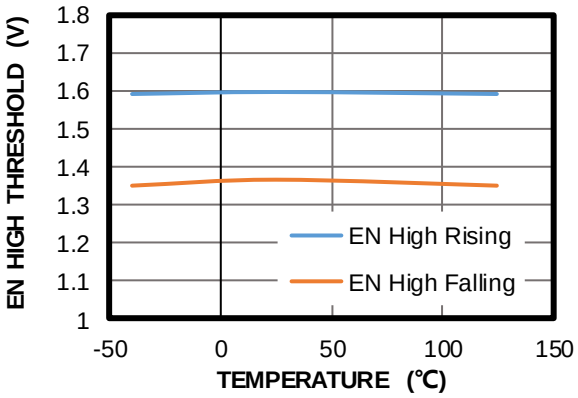
TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs. Load Current

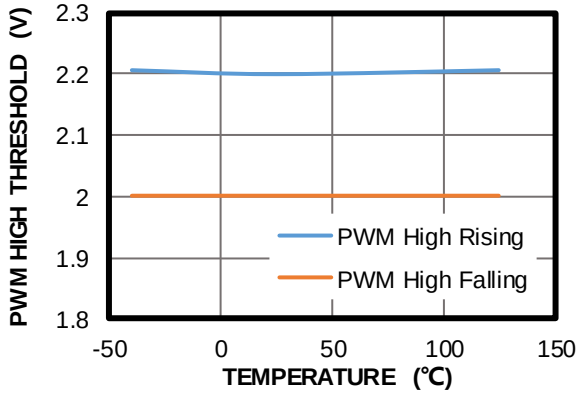
V_{IN} = 12V, L = 150nH



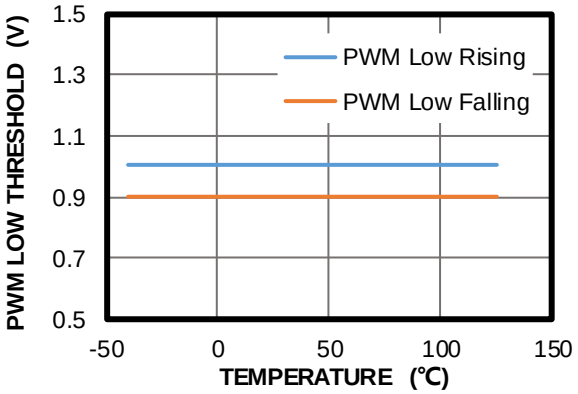
EN High Threshold



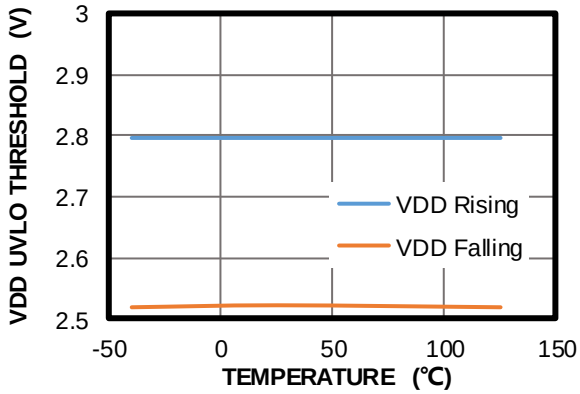
PWM High Threshold



PWM Low Threshold



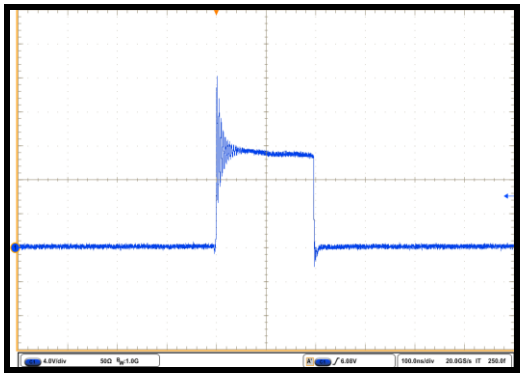
VDD UVLO



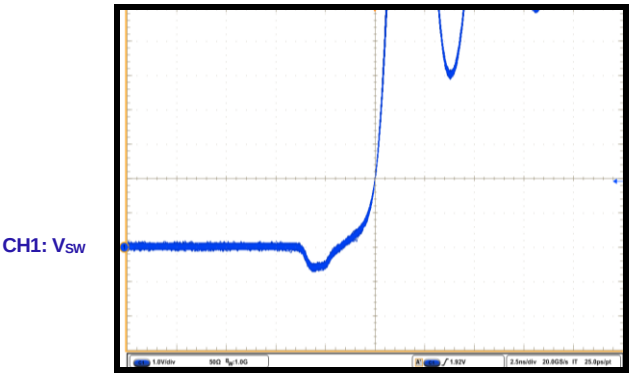
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Switching

V_{IN} = 12V, L = 150nH, load = 30A

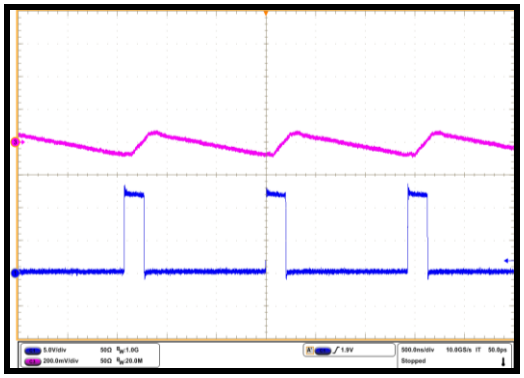


Dead Time at SW Ringing



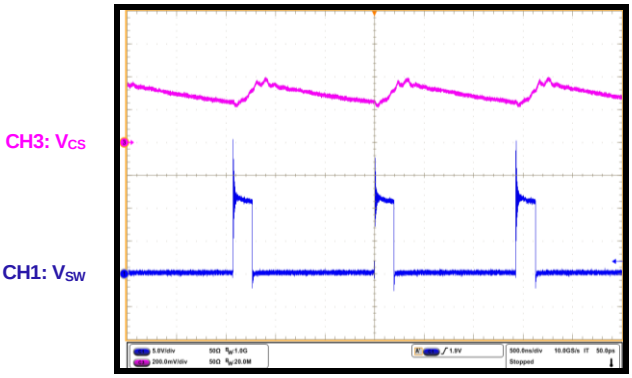
Output Current

Load = 0A

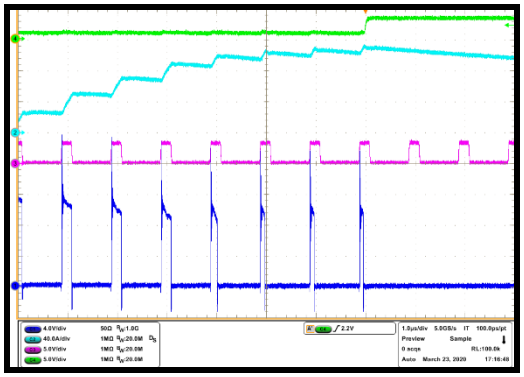


Output Current

Load = 30A



High-Side Current Limit



FUNCTIONAL BLOCK DIAGRAM

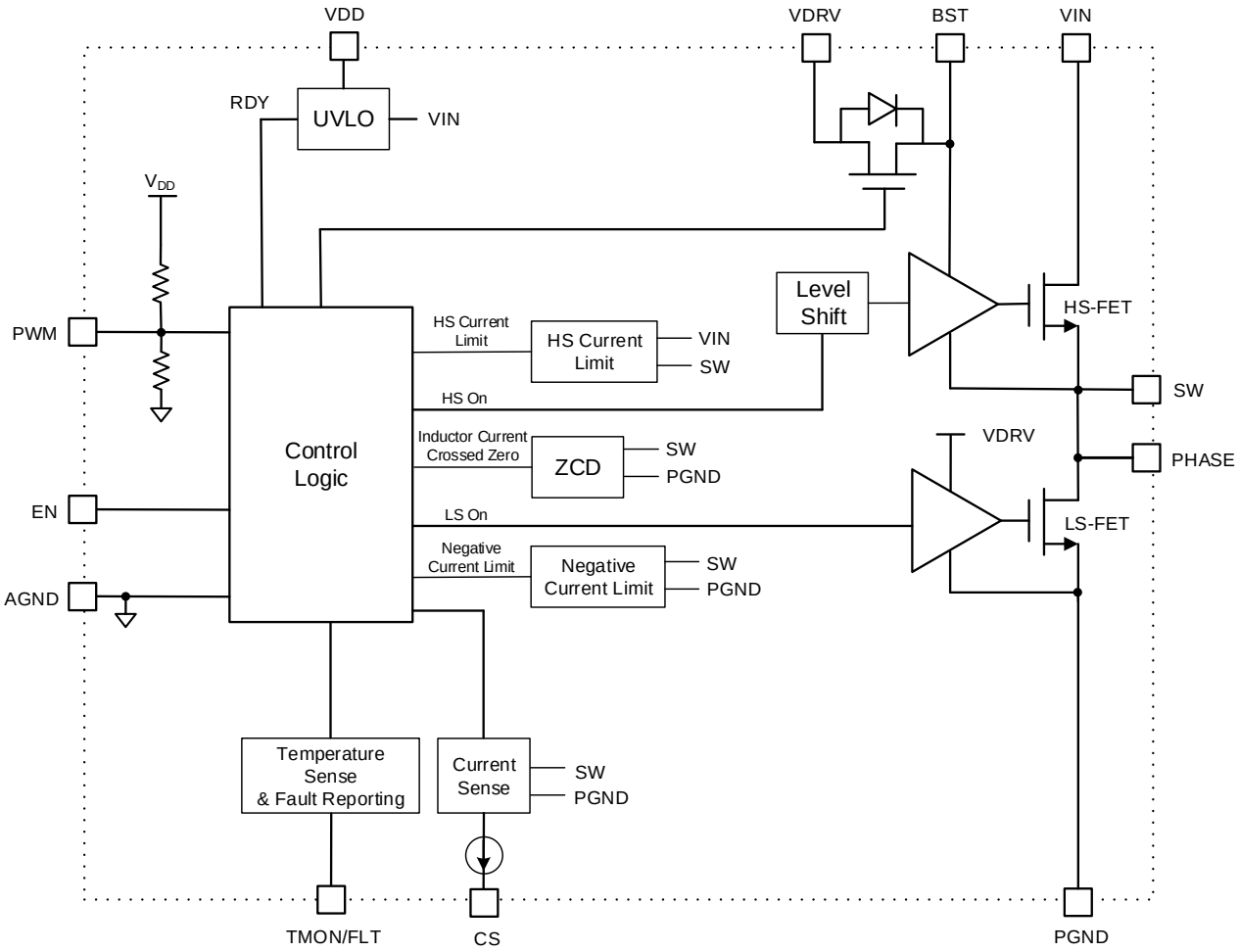


Figure 1: Functional Block Diagram

OPERATION

The MP86950 is a 50A, monolithic, half-bridge driver with integrated power MOSFETs. It is ideal for multi-phase buck regulator applications.

An external 3.3V supply is required to supply both the VDD and VDRV pins. Operation begins when the EN pin transitions from low to high, and the VDD and VIN signals are higher than the UVLO rising threshold.

Pulse-Width Modulation (PWM)

The pulse-width modulation (PWM) input can operate as a tri-state input. When the PWM input signal is within the tri-state threshold window (t_{HT} or t_{LT}) for 40ns, the high-side MOSFET (HS-FET) turns off and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET remains in diode emulation mode until zero-current detection (ZCD). The tri-state PWM input can come from a forced middle-voltage PWM signal or can be made by floating the PWM input so the internal current source charges the signal to a middle voltage. Figure 2 shows the propagation delay definition from PWM to the SW node.

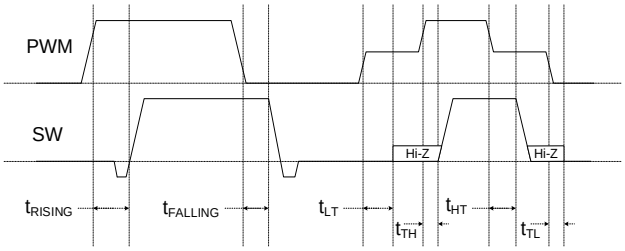


Figure 2: PWM Timing Diagram

Diode Emulation Mode

In diode emulation mode, PWM is in a tri-state input. The LS-FET turns on if the inductor current is positive. The LS-FET turns off if the inductor current is negative or after the inductor current crosses the ZCD threshold. Diode emulation mode can be enabled by driving the PWM pin to a middle state or floating PWM.

Current Sense (CS)

The MP86950's current sense (CS) is a bidirectional current source proportional to the inductor current. The current-sense gain (G_{CS}) is 10μA/A. Typically, a resistor (R_{CS}) from CS to an external voltage is used to sink small currents to provide a 0.7V to 2.1V voltage level shift to meet the CS operating voltage. The CS voltage range keeps the CS output current linearly proportional to the inductor current.

The proper reference voltage (V_{CM}) connected to R_{CS} can be calculated with Equation (1).

$$0.7V < I_{CS} \times R_{CS} + V_{CM} < 2.1V \quad (1)$$

I_{CS} can be estimated with Equation (2):

$$I_{CS} = I_L \times G_{CS} \quad (2)$$

The Intelli-Phase™ CS output is used by the controller to accurately monitor the output current. The cycle-by-cycle current information from CS is used for phase-current balancing, over-current protection, and active voltage positioning (output-voltage droop).

Positive and Negative Inductor Current Limits

If an HS-FET over-current condition is detected for four consecutive cycles, the HS-FET latches off and the TMON/FLT pin is pulled high to VDD's voltage level. The LS-FET turns on until ZCD, and then turns off. Recycling the power on VIN, VDD, or VDRV, or toggling EN releases the latch and restarts the device.

If a -30A current is detected, the LS-FET turns off for 40ns to limit the negative current. The LS-FET's negative current limit will not trigger a fault report.

Over-Temperature Protection (OTP)

When the junction temperature reaches the over-temperature threshold, the HS-FET latches off, the TMON/FLT pin is pulled high to VDD, and the LS-FET turns on until ZCD.

Temperature-Sense Output with Fault Indicator (TMON/FLT)

The TMON/FLT pin has dual functions. It acts as the device's junction temperature sense and fault function. These functions are described below.

Junction Temperature Sense

The TMON/FLT voltage output is proportional to the junction temperature if V_{DD} exceeds its UVLO threshold and the part is in active mode. The gain is 8mV/°C with a 800mV offset at

25°C. For example, the TMON/FLT is 0.8V at T_J = 25°C, and 1.4V at T_J = 100°C.

Fault Function

When a fault occurs, TMON/FLT is pulled to VDD to report the fault event, regardless of the junction temperature. TMON/FLT monitors three different fault events: over-current, over-temperature, and SW to PGND short.

1. Over-current fault: Four consecutive current limit faults trigger an over-current fault. Once a fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches 0A.
2. Over-temperature fault: At T_J > 160°C, once a fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns off when the inductor current reaches 0A.
3. SW to PGND short: Once a fault occurs, the part latches off to turn off the HS-FET.

The fault latch does not reset when it enters standby mode. The fault latch can be released by cycling the power on VIN or VDD.

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient layout is critical for stable operation. For the best results, refer to Figure 3 and follow the guidelines below:

1. Place the MLCC input capacitors as close to VIN and PGND as possible.
2. Place as many VIN and PGND vias underneath the package as possible. Place these vias between the VIN or PGND long pads.
3. Place a VIN copper plane on the second inner layer to form the PCB stack (positive/negative/positive) to reduce parasitic impedance from the MLCC input capacitor to the MP86950. Ensure that the copper plane on the inner layer covers the VIN vias and MLCC input capacitors.
4. Place more PGND vias close to the PGND pin/pad to minimize parasitic resistance, parasitic impedance, and thermal resistance.
5. Place the BST capacitor, BST resistor, and VDRV capacitor as close to the MP86950's pins as possible. For BST routing, use a trace width greater than 20mils. Avoid placing vias on the BST driving path.
6. Place the VDD decoupling capacitor close to the device.
7. Keep the CS signal trace away from high voltages and current slew-rate nodes (such as SW, PWM, the VIN vias, and the PGND vias).

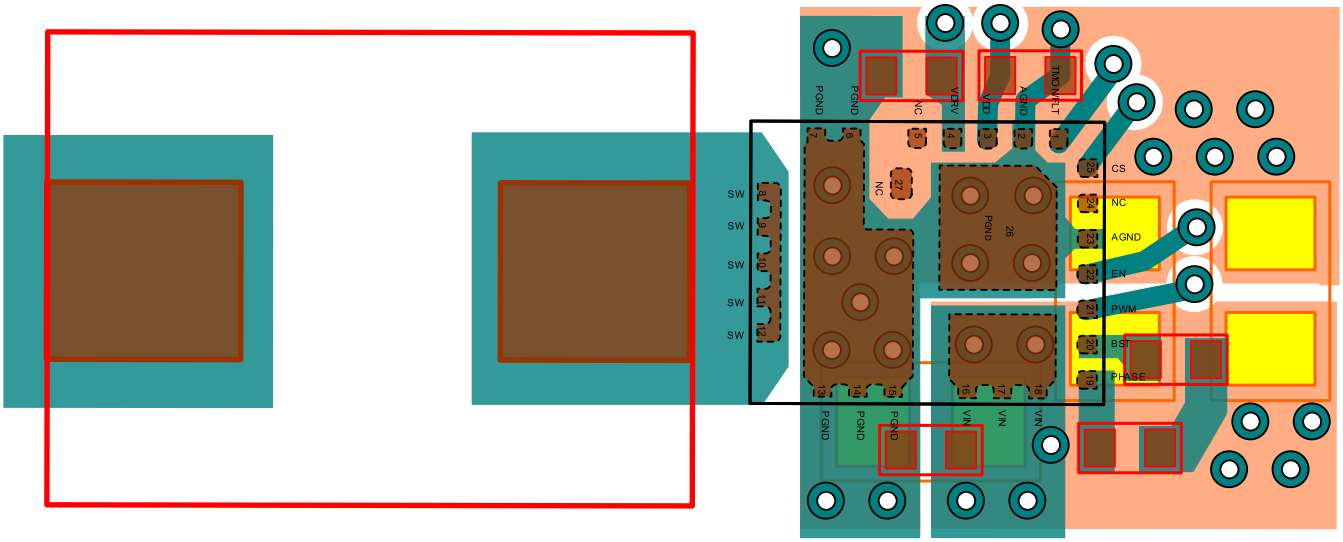


Figure 3: Recommended PCB Layout

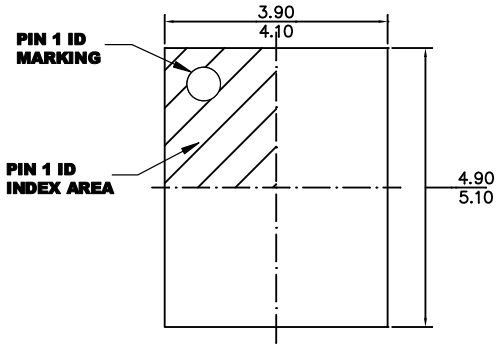
Input Capacitor: 0402 Package (Top Side) and 0805 Package (Bottom Sides)

BST/VDRV/VDD Capacitor/Resistor: 0402 Package

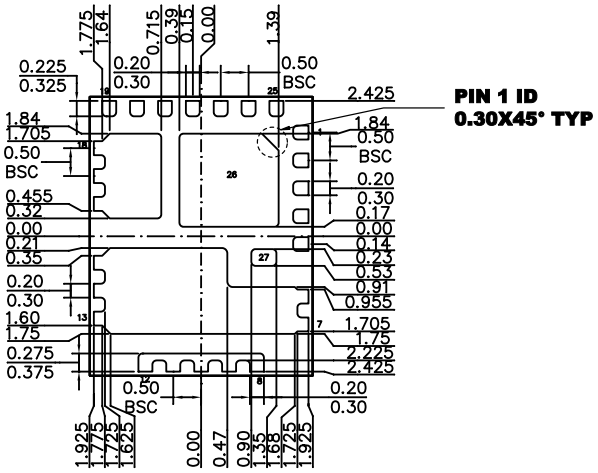
Via Size: 10/20mils

PACKAGE INFORMATION

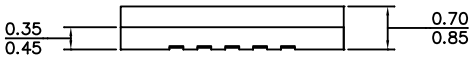
TLGA-27 (4mmx5mm)



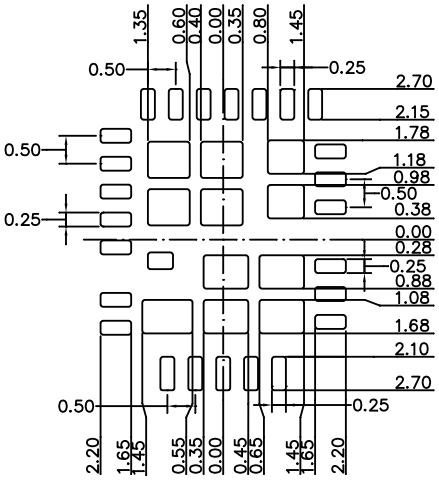
TOP VIEW



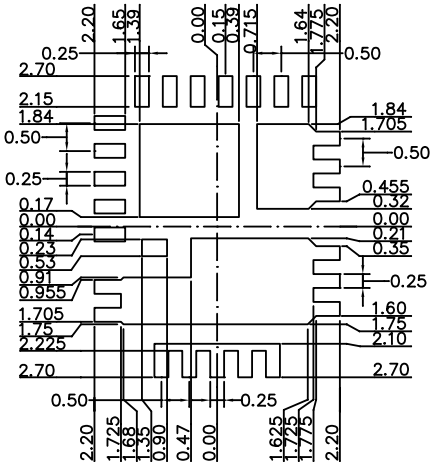
BOTTOM VIEW



SIDE VIEW



RECOMMENDED STENCIL DESIGN

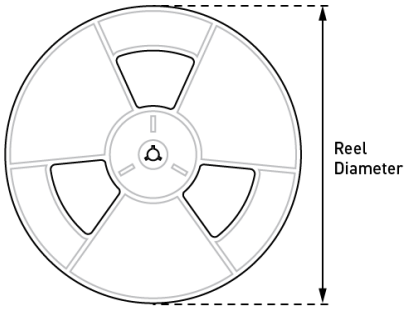


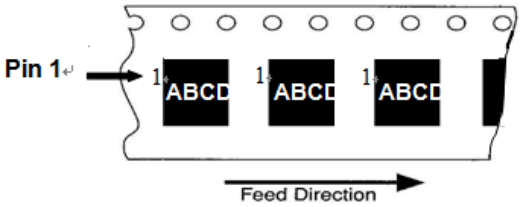
RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.1 MILLIMETERS MAXIMUM.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION





Part Number	Package Description	Quantity /Reel	Quantity /Tube	Quantity /Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP86950GLVT–Z	TLGA-27 (4mmx5mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	12/18/2020	Initial Release	-