

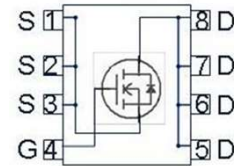
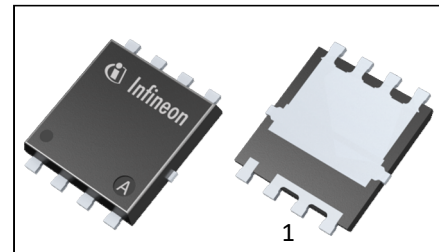
OptiMOS™ -5 Power Transistor

Features

- OptiMOS™ power MOSFET for automotive applications
- N-channel - Enhancement mode - Logic Level
- MSL1 up to 260°C peak reflow
- 175 °C operating temperature
- Green product (RoHS compliant)
- 100% Avalanche tested

Product Summary

| | | |
|------------------|-----|----|
| V_{DS} | 80 | V |
| $R_{DS(on),max}$ | 9.6 | mΩ |
| I_D | 50 | A |

PG-TDSON-8-33


| Type | Package | Marking |
|-----------------|-------------------------------|----------|
| IAUC50N08S5L096 | PG-TDSON-8-33 | 5N08L096 |

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|--|--------------|------|
| Drain current | I_D | $V_{GS}=10\text{ V}$, Chip limitation ^{1,2)} | 50 | A |
| | | $V_{GS}=10\text{V}$, DC current | 50 | |
| | | $T_a=85\text{ °C}$, $V_{GS}=10\text{ V}$, R_{thJA} on 2s2p ^{2,3)} | 16 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$ | 200 | |
| Avalanche energy, single pulse ²⁾ | E_{AS} | $I_D=29\text{ A}$ | 45 | mJ |
| Avalanche current, single pulse | I_{AS} | - | 29 | A |
| Gate source voltage | V_{GS} | - | ±20 | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 60 | W |
| Operating and storage temperature | T_j, T_{stg} | - | -55 ... +175 | °C |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Thermal characteristics²⁾

| | | | | | | |
|--|------------|---|---|------|-----|-----|
| Thermal resistance, junction - case | R_{thJC} | - | - | - | 2.5 | K/W |
| Thermal resistance, junction - ambient ⁴⁾ | R_{thJA} | - | - | 24.9 | - | |

Electrical characteristics, at $T_j=25^\circ\text{C}$, unless otherwise specified
Static characteristics

| | | | | | | |
|----------------------------------|---------------|--|-----|------|------|------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0V, I_D=1mA$ | 80 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}, I_D=24\mu A$ | 1.2 | 1.6 | 2.0 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=80V, V_{GS}=0V, T_j=25^\circ\text{C}$ | - | 0.1 | 1 | μA |
| | | $V_{DS}=80V, V_{GS}=0V, T_j=85^\circ\text{C}^{2)}$ | - | 1 | 20 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20V, V_{DS}=0V$ | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=4.5V, I_D=25A$ | - | 10.3 | 13.9 | m Ω |
| | | $V_{GS}=10V, I_D=25A$ | - | 7.8 | 9.6 | |
| Gate resistance ²⁾ | R_G | - | - | 1.2 | - | Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics²⁾

| | | | | | | |
|------------------------------|--------------|---|---|------|------|----|
| Input capacitance | C_{iss} | $V_{GS}=0V, V_{DS}=40V,$ $f=1MHz$ | - | 1295 | 1684 | pF |
| Output capacitance | C_{oss} | | - | 212 | 276 | |
| Reverse transfer capacitance | C_{rss} | | - | 15 | 23 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=40V, V_{GS}=10V,$ $I_D=25A, R_{G,ext}=3.5\Omega$ | - | 3 | - | ns |
| Turn-off delay time | $t_{d(off)}$ | | - | 14 | - | |
| Rise time | t_r | | - | 2 | - | |
| Fall time | t_f | | - | 6 | - | |

Gate Charge Characteristics²⁾

| | | | | | | |
|-----------------------|---------------|--|---|-----|----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=40V, I_D=25A,$ $V_{GS}=0 \text{ to } 10V$ | - | 4 | 6 | nC |
| Gate to drain charge | Q_{gd} | | - | 5 | 7 | |
| Gate charge total | Q_g | | - | 22 | 29 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 3.1 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|---|---|-----|-----|----|
| Diode continuous forward current ²⁾ | I_S | $T_C=25^\circ C$ | - | - | 50 | A |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | $T_C=25^\circ C$ | - | - | 200 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0V, I_F=25A,$ $T_j=25^\circ C$ | - | 0.9 | 1.2 | V |
| Reverse recovery time ²⁾ | t_{rr} | $V_R=40V, I_F=50A,$ $di_F/dt=100A/\mu s$ | - | 33 | - | ns |
| Reverse recovery charge ²⁾ | Q_{rr} | | - | 26 | - | nC |

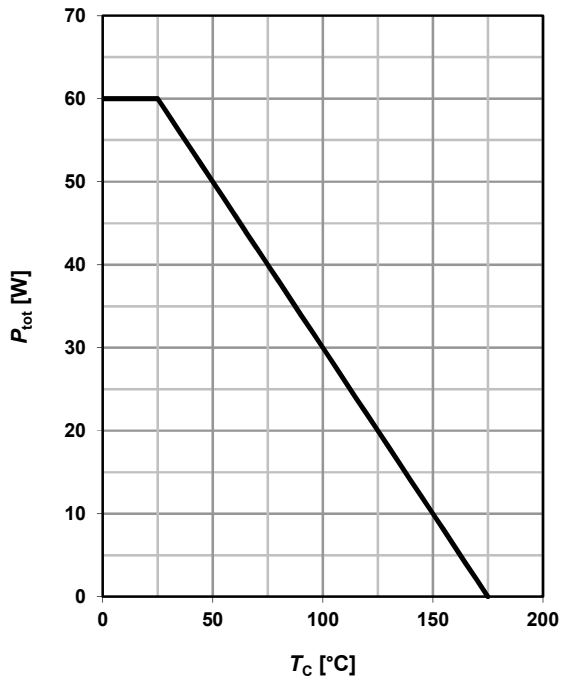
¹⁾ Practically the current is limited by the overall system design including the customer-specific PCB.

²⁾ The parameter is not subject to production test - verified by design/characterization.

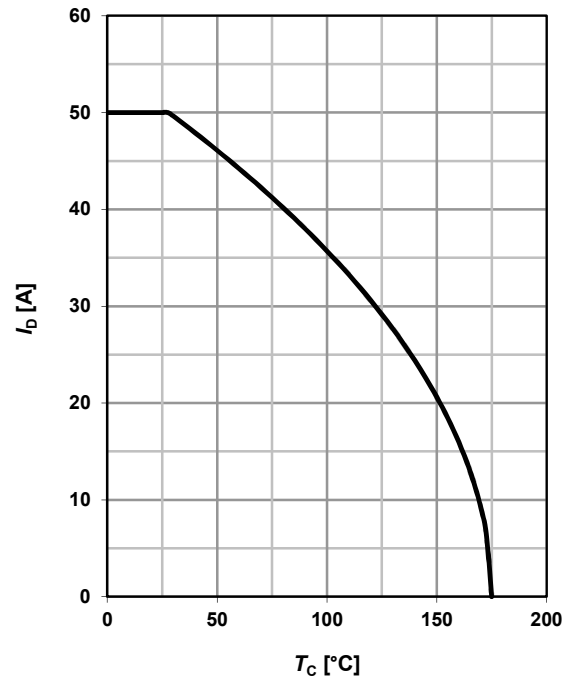
³⁾ Device on a four-layer 2s2p FR4 PCB defined in accordance with JEDEC standards (JESD51-5-7). PCB is vertical in still air.

1 Power dissipation

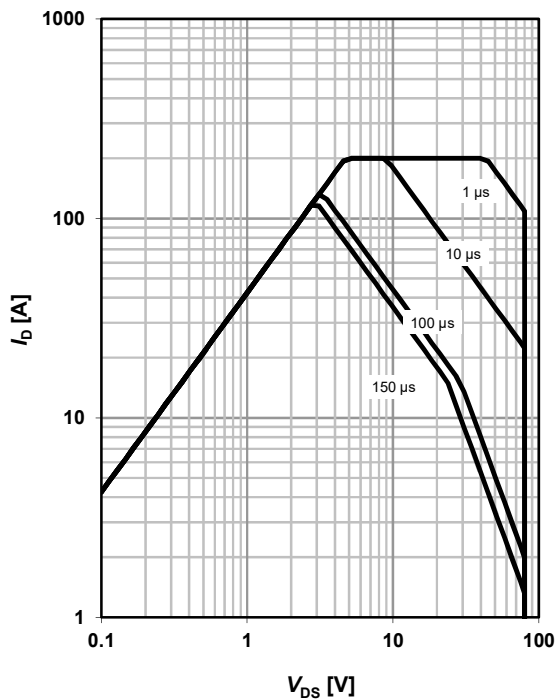
$$P_{\text{tot}} = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


2 Drain current

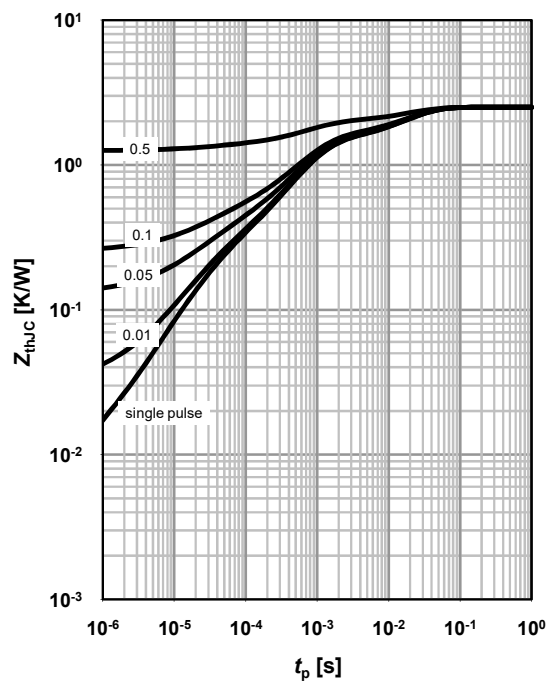
$$I_D = f(T_C); V_{\text{GS}} = 10 \text{ V}$$


3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

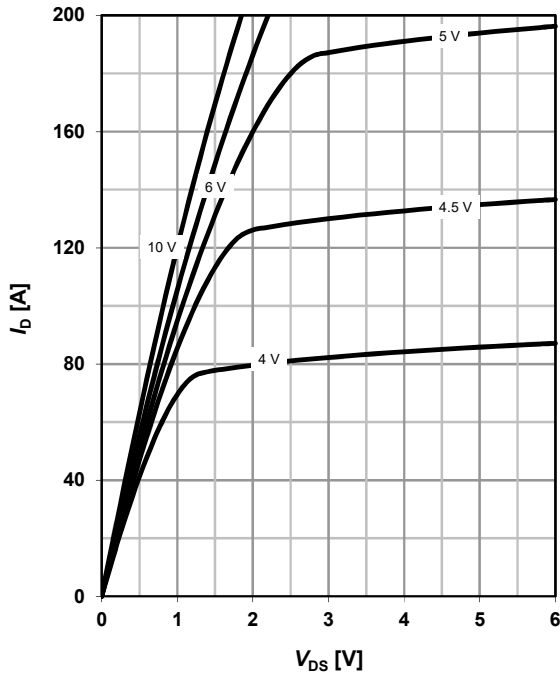
 parameter: t_p

4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

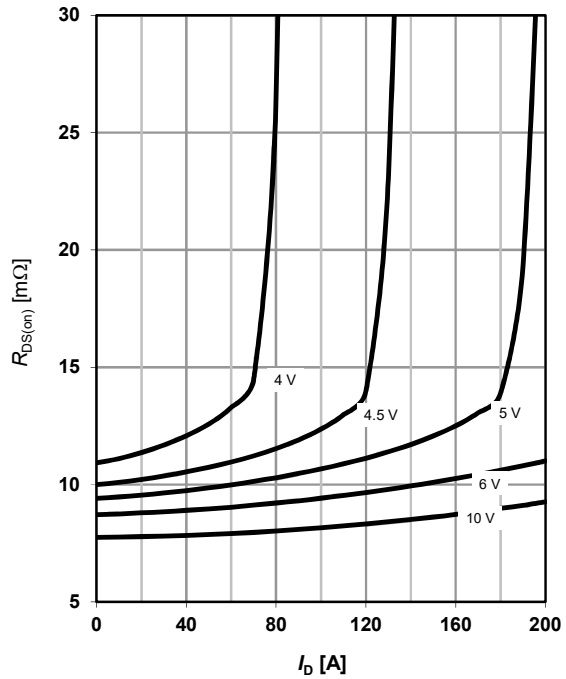
 parameter: $D = t_p/T$


5 Typ. output characteristics

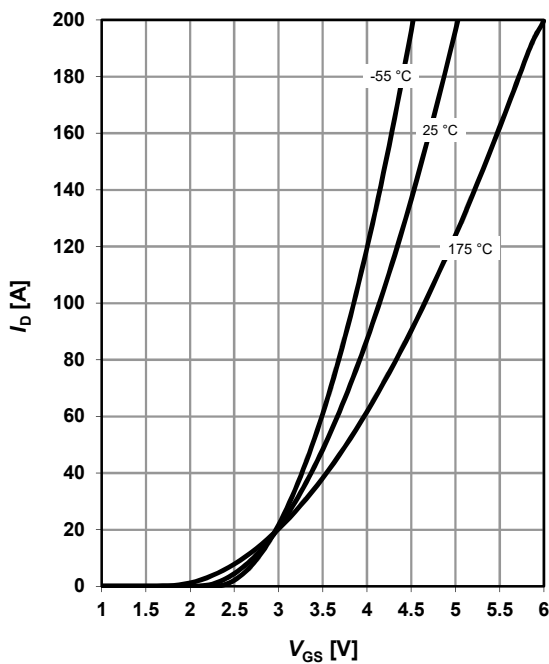
$$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$$

 parameter: V_{GS}

6 Typ. drain-source on-state resistance

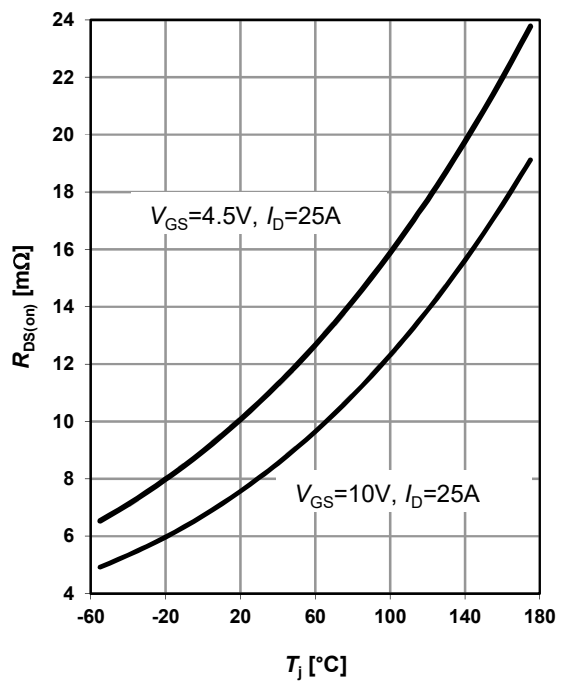
$$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$$

 parameter: V_{GS}

7 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$$

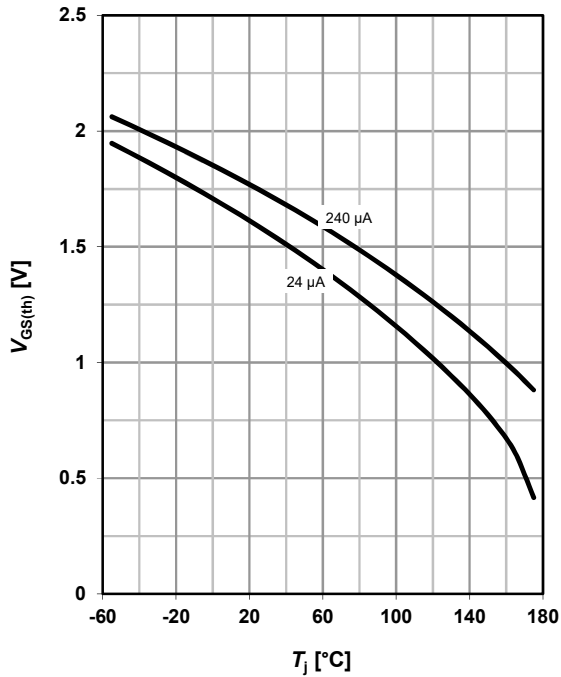
 parameter: T_j

8 Typ. drain-source on-state resistance

$$R_{DS(on)} = f(T_j);$$

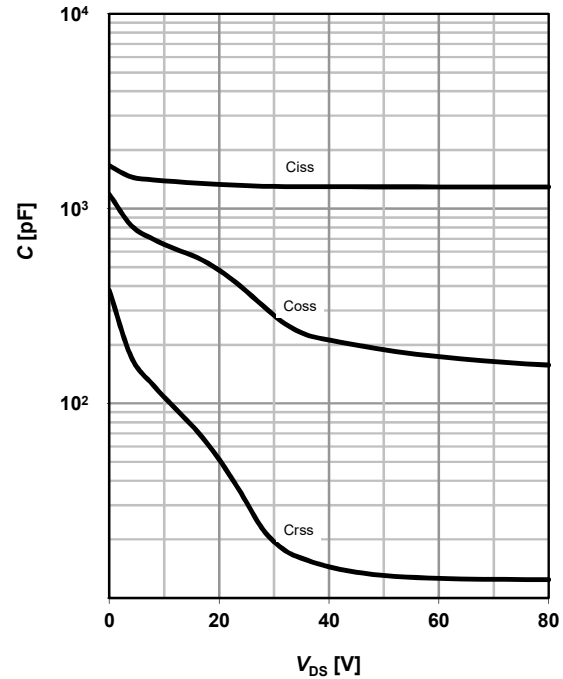
 parameter: I_D, V_{GS}


9 Typ. gate threshold voltage

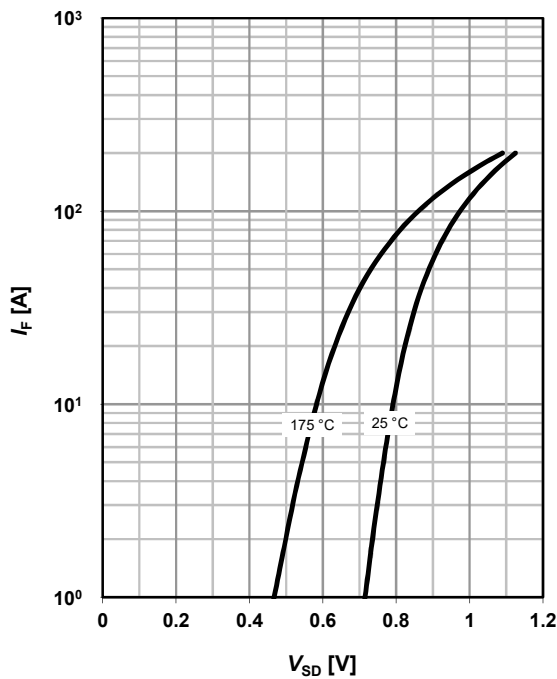
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

 parameter: I_D

10 Typ. capacitances

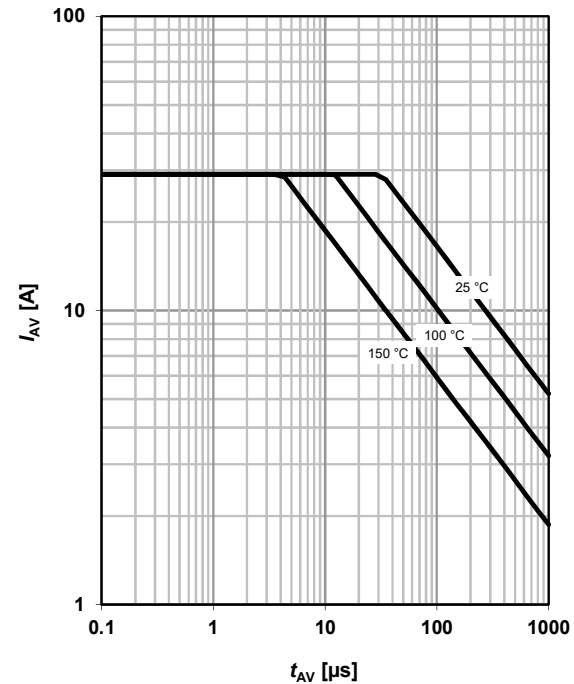
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$


11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

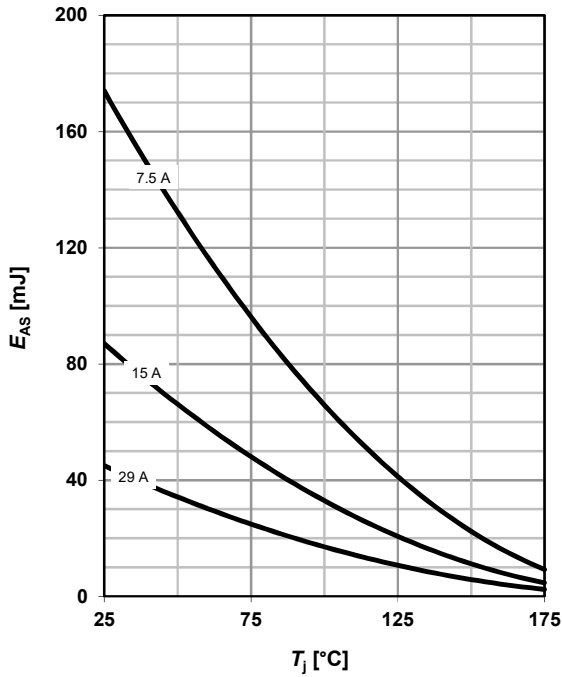
 parameter: T_j

12 Avalanche characteristics

$$I_{AS} = f(t_{AV})$$

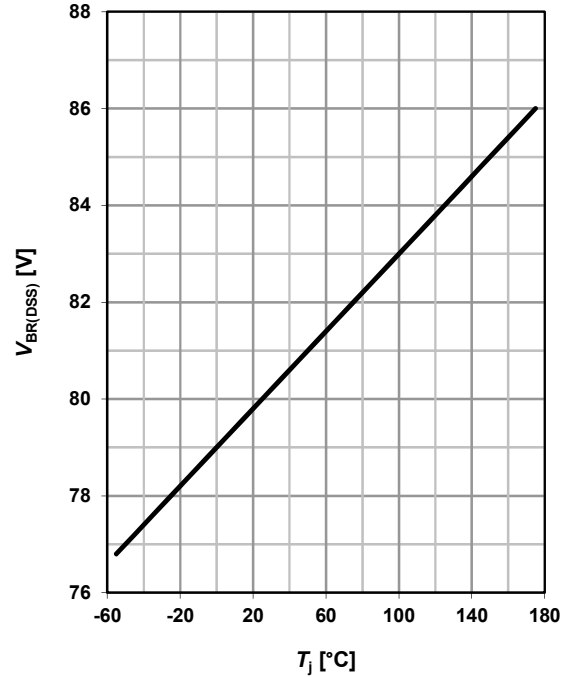
 parameter: $T_{j(start)}$


13 Avalanche energy

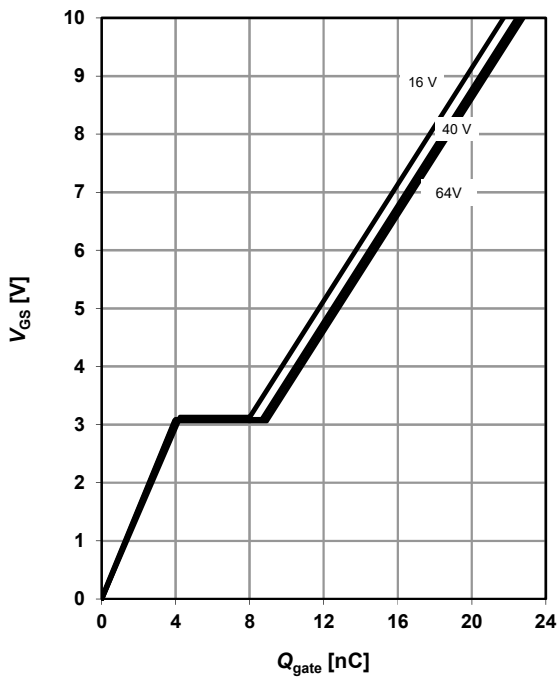
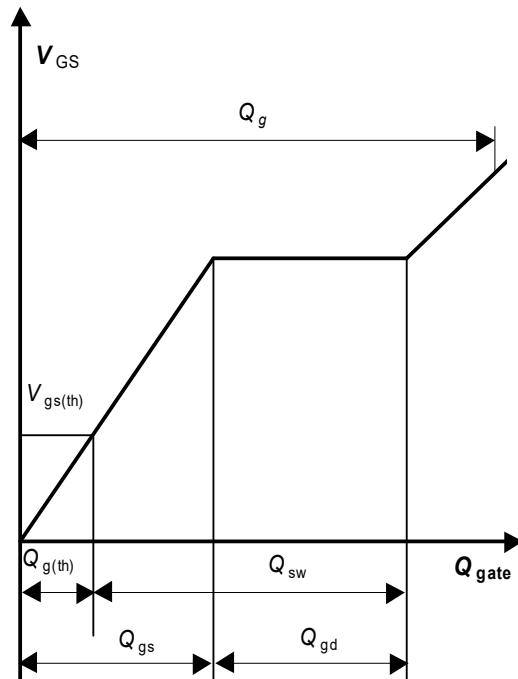
$$E_{AS} = f(T_j)$$

 parameter: I_D

14 Drain-source breakdown voltage

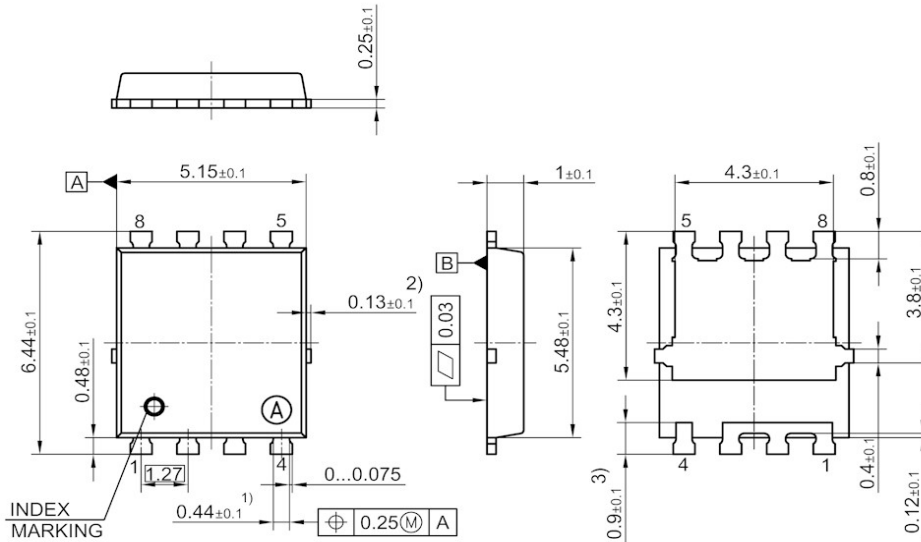
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$


15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 25 \text{ A pulsed}$$

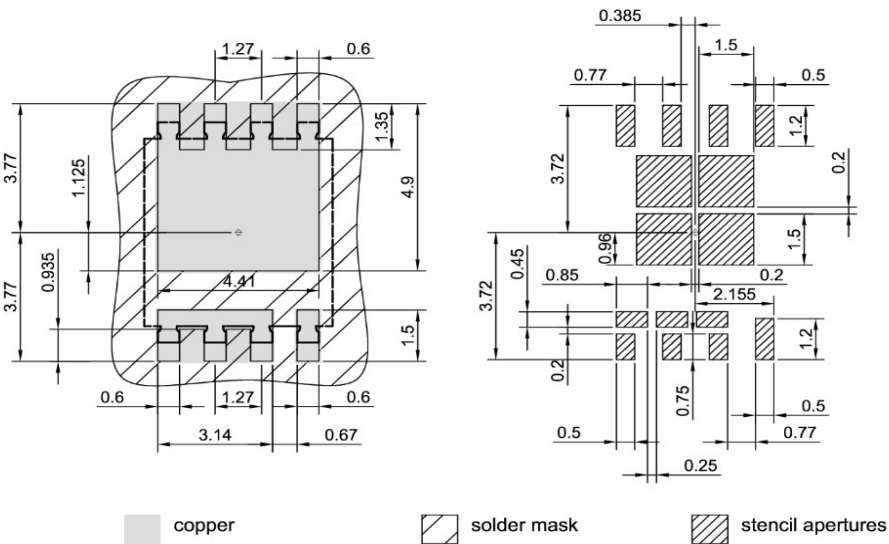
 parameter: V_{DD}

16 Gate charge waveforms


Package Outline



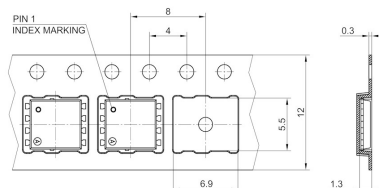
- 1) EXCLUDE MOLD FLASH
 - 2) REMOVAL ON MOLD GATE, INTRUSION 0.1MM AND PROTRUSION 0.1MM
 - 3) LEAD LENGTH UP TO ANTI FLASH LINE
 - 4) ALL METAL SURFACE ARE PLATED, EXCEPT AREA OF CUT
- ALL DIMENSIONS ARE IN UNITS MM
 THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

Footprint



All dimensions are in units mm

Packaging



ALL DIMENSIONS ARE IN UNITS MM
 THE DRAWING IS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 []

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Revision History

| Version | Date | Changes |
|--------------|------------|--|
| Revision 1.0 | 2021-05-14 | Final Data Sheet |
| Revision 1.1 | 2021-06-18 | - Company log size adjusted - Datasheet file name updated |