

## UT6898G-S08-R-VB Datasheet

# **Dual N-Channel 20-V (D-S) MOSFET**

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}(\Omega)$	I <sub>D</sub> (A)	Q <sub>g</sub> (Typ.)		
20	0.009 at V <sub>GS</sub> = 4.5 V	10	15 nC		
	0.012 at V <sub>GS</sub> = 2.5 V	8.0	15110		

 $D_1$ 

 $D_2$ 

SO-8

Top View

# FEATURESHalogen-free

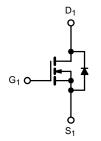
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % UIS Tested
- 100 % R<sub>g</sub> Tested
- Compliant to RoHS Directive 2002/95/EC

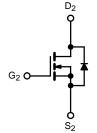


ROHS COMPLIANT HALOGEN FREE

## **APPLICATIONS**

- Set Top Box
- Low Current DC/DC





N-Channel MOSFET

N-Channel MOSFET

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	20	V
Gate-Source Voltage		V <sub>GS</sub>	± 12	V
	$T_C = 25 ^{\circ}\text{C}$ $T_C = 70 ^{\circ}\text{C}$		10 <sup>a</sup> 7.0	
Continuous Drain Current (T <sub>J</sub> = 150 °C)	T <sub>A</sub> = 25 °C	I <sub>D</sub>	8.1 <sup>b, c</sup>	
	T <sub>A</sub> = 70 °C		7.2 <sup>b, c</sup>	Α Α
Pulsed Drain Current		I <sub>DM</sub>	44	, ,
Continuous Source-Drain Diode Current	ous Source-Drain Diode Current  T <sub>C</sub> = 25 °C	I <sub>S</sub>	3.25	
Continuous Gource Brain Blode Gunent	T <sub>A</sub> = 25 °C	.5	1.88 <sup>b, c</sup>	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	6	
Single Pulse Avalanche Energy	L = 0.111111	E <sub>AS</sub>	1.45	mJ
	T <sub>C</sub> = 25 °C		2.7	
Maximum Power Dissipation	T <sub>C</sub> = 70 °C	P <sub>D</sub>	1.77	W
Maximum Fower Dissipation	T <sub>A</sub> = 25 °C	1 'D [	1.78 <sup>b, c</sup>	VV
	T <sub>A</sub> = 70 °C	1	1.14 <sup>b, c</sup>	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient <sup>a, c, d</sup>	t ≤ 10 s	R <sub>thJA</sub>	58	70	°C/W	
Maximum Junction-to-Foot (Drain)	Steady State	$R_{th,IF}$	38	45		

#### Notes:

- a. Package limited, T<sub>C</sub> = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s
- d. Maximum under Steady State conditions is 110 °C/W.



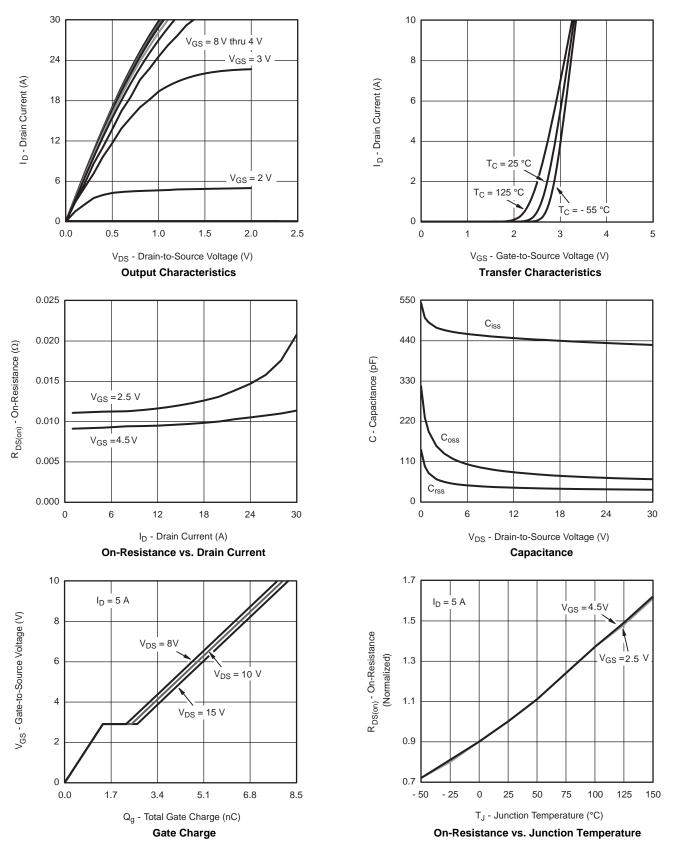
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			•				
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	20			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		32		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I <sub>D</sub> = 250 μA		- 5.0			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	0.5		1.0	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
7. 0. 1/1. 5. 0	I <sub>DSS</sub>	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}$ $V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$			1	μA	
Zero Gate Voltage Drain Current					10		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	10			Α	
		$V_{GS} = 4.5 \text{ V} I_{D} = 5 \text{ A}$	0.009				
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 2.5 \text{ V}, I_D = 4 \text{ A}$		0.012		Ω	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 5 A		16		S	
Dynamic <sup>b</sup>	<u> </u>	- <del>-</del>	<u> </u>			l .	
Input Capacitance	C <sub>iss</sub>			586			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = 10V, V_{GS} = 0 V, f = 1 MHz$		117		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			55			
Total Gate Charge		$V_{DS} = 10 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 5 \text{ A}$		15			
	Qg			3.7	5.6	nC	
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 10V$ , $V_{GS} = 4.5 V$ , $I_{D} = 5 A$		1.4			
Gate-Drain Charge	Q <sub>gd</sub>			1.05			
Gate Resistance	R <sub>g</sub>	f = 1 MHz	0.8	4.3	8.6	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			12	24		
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 3 $\Omega$		55	100		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 5$ A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 $\Omega$		11	22		
Fall Time	t <sub>f</sub>			8	16		
Turn-On Delay Time	t <sub>d(on)</sub>			4	8	ns -	
Rise Time	t <sub>r</sub>	$V_{DD}$ = 10V, $R_L$ = 3 $\Omega$		9	18		
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D\cong 5$ A, $V_{GEN}$ = 10 V, $R_g$ = 1 $\Omega$		10	20		
Fall Time	t <sub>f</sub>			6	12		
<b>Drain-Source Body Diode Characteristi</b>	cs		•				
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			2.35	Δ	
Pulse Diode Forward Current	I <sub>SM</sub>				24	A	
Body Diode Voltage	$V_{SD}$	I <sub>S</sub> = 2 A, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			11	20	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 5 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		4	8	nC	
Reverse Recovery Fall Time	ta	$_{1F} = 3 \text{ A}$ , $_{10}$ $_$		7			
Reverse Recovery Rise Time	t <sub>b</sub>			4		ns	

#### Notes:

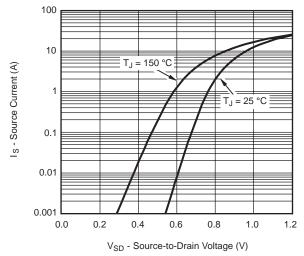
- a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

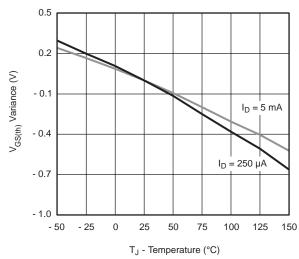




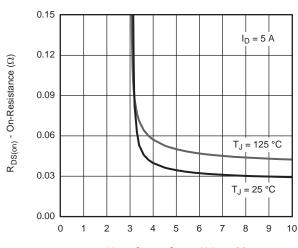




#### Source-Drain Diode Forward Voltage

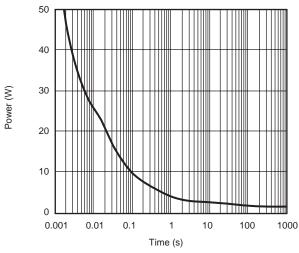


### **Threshold Voltage**

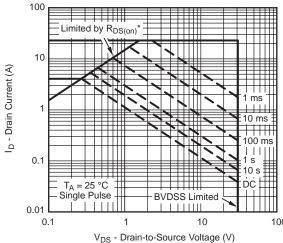


 $V_{\text{GS}}$  - Gate-to-Source Voltage (V)

#### On-Resistance vs. Gate-to-Source Voltage



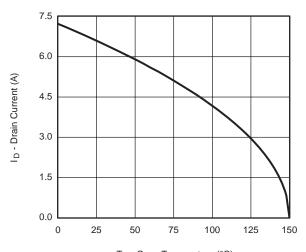
Single Pulse Power



\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

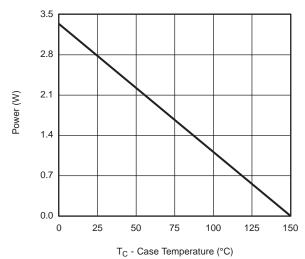
Safe Operating Area, Junction-to-Ambient

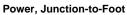


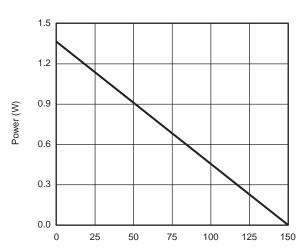


T<sub>C</sub> - Case Temperature (°C)

## **Current Derating\***





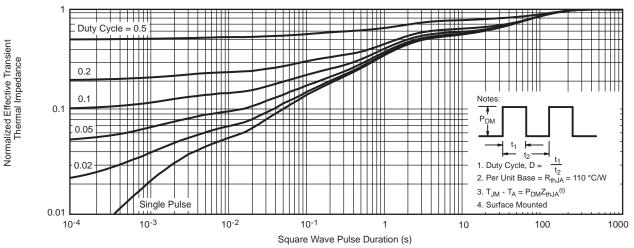


T<sub>A</sub> - Ambient Temperature (°C)

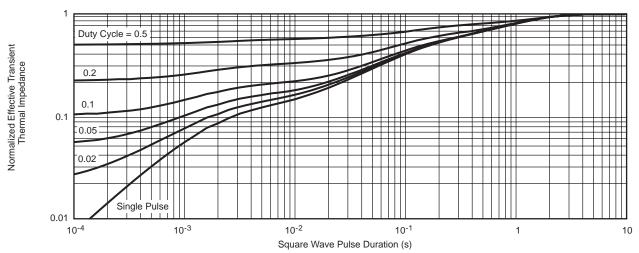
Power, Junction-to-Ambient

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot



SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012







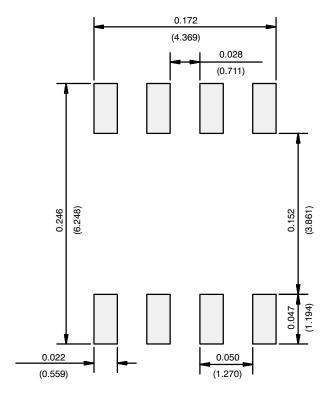
	MILLIM	IETERS	INCHES		
DIM	Min	Max	Min	Max	
Α	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27 BSC		0.050 BSC		
Н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
FCN: C-06527-Rev I 11-Sen-06					

ECN: C-06527-Rev. I, 11-Sep-06

DWG: 5498



## **RECOMMENDED MINIMUM PADS FOR SO-8**



Recommended Minimum Pads Dimensions in Inches/(mm)

Return to Index



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