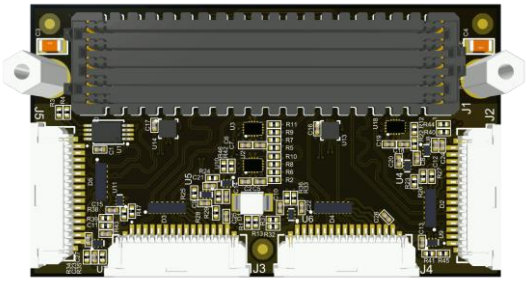
RPi Camera FMC

Overview

Description

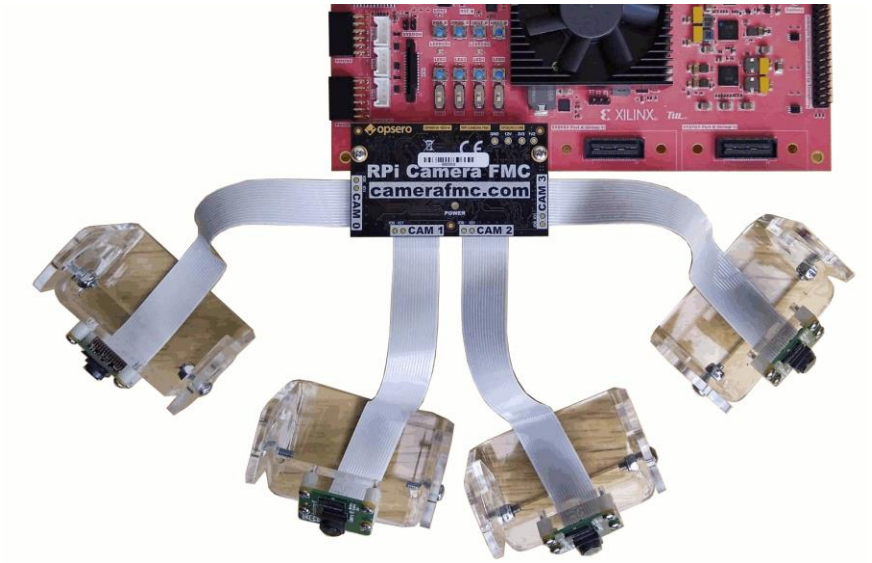
The RPi Camera FMC (FPGA Mezzanine Card) is an add-on/expansion board for FPGA and SoC based development boards. The mezzanine card enables the connection of 4x Raspberry Pi compatible cameras to the carrier development board.

Top view



Bottom view

Application example



Features

- 4x 15-pin FFC connectors for Raspberry Pi cameras
- Support and example designs for multiple development boards
- Direction configurable I/Os for Raspberry Pi camera GPIO (IO0 and IO1)
- ESD protection
- FMC pinout conforms to VITA 57.1 FMC Standard
- Standalone example designs
- PetaLinux example designs coming soon!

Supported development boards

The following development boards are currently supported.

- AMD Xilinx ZCU104 Zynq UltraScale+ Development board
- AMD Xilinx ZCU102 Zynq UltraScale+ Development board
- AMD Xilinx ZCU106 Zynq UltraScale+ Development board
- TUL PYNQ-ZU Zynq UltraScale+ Development board
- Digilent Genesys-ZU Zynq UltraScale+ Development board
- Avnet UltraZed EV Carrier Zynq UltraScale+ Development board

More information on compatibility with the RPi Camera FMC can be found in the compatible boards section.

Supported cameras

The RPi Camera FMC is designed to support all cameras with the standard 15-pin Raspberry Pi camera interface. See the example designs for information on the specific cameras for which we currently have software support.

Ordering

Part name	Part number
RPi Camera FMC	OP068

Pin Configuration

Pinout table

The RPi Camera FMC has a low pin count FPGA Mezzanine Card (FMC) connector, providing the connections to the FPGA on the development board. The following table defines the pinout of the FMC connector and describes each pin's purpose on this mezzanine card.

Pin	Pin name	Net	Description
C1	GND	GND	Ground
C2	DP0_C2M_P	DP0_C2M_P	Not used
C3	DP0_C2M_N	DP0_C2M_N	Not used
C4	GND	GND	Ground
C5	GND	GND	Ground
C6	DP0_M2C_P	DP0_M2C_P	Not used
C7	DP0_M2C_N	DP0_M2C_N	Not used
C8	GND	GND	Ground
C9	GND	GND	Ground
C10	LA06_P	CAM0_DATA0_P	Camera 0 Data lane 0 Positive
C11	LA06_N	CAM0_DATA0_N	Camera 0 Data lane 0 Negative
C12	GND	GND	Ground
C13	GND	GND	Ground
C14	LA10_P	STB_LA10_P	Not connected, reserved for strobe propagation
C15	LA10_N	STB_LA10_N	Not connected, reserved for strobe propagation

C16	GND	GND	Ground
C17	GND	GND	Ground
C18	LA14_P	CAM1_DATA1_P	Camera 1 Data lane 1 Positive
C19	LA14_N	CAM1_DATA1_N	Camera 1 Data lane 1 Negative
C20	GND	GND	Ground
C21	GND	GND	Ground
C22	LA18_P_CC	CAM2_CLK_P	Camera 2 Clock lane Positive
C23	LA18_N_CC	CAM2_CLK_N	Camera 2 Clock lane Negative
C24	GND	GND	Ground
C25	GND	GND	Ground
C26	LA27_P	CAM_IO0_OE_N	Camera IO0 Output enable (active low)
C27	LA27_N	CAM_IO1_OE_N	Camera IO1 Output enable (active low)
C28	GND	GND	Ground
C29	GND	GND	Ground
C30	SCL	I2C_SCL	I2C Clock (FPGA-to-PHY)
C31	SDA	I2C_SDA	I2C Data (bidirectional)
C32	GND	GND	Ground
C33	GND	GND	Ground
C34	GA0	GA0	EEPROM Address Bit 1 (A1)
C35	12P0V_1	12V0	12VDC (Not used)
C36	GND	GND	Ground
C37	12P0V_2	12V0	12VDC (Not used)
C38	GND	GND	Ground

C39	3P3V_1	3V3	3.3VDC
C40	GND	GND	Ground
D1	PG_C2M	PG	Power Good (Driven by carrier)
D2	GND	GND	Ground
D3	GND	GND	Ground
D4	GBTCLK0_M2C_P	N/C	Not used
D5	GBTCLK0_M2C_N	N/C	Not used
D6	GND	GND	Ground
D7	GND	GND	Ground
D8	LA01_P_CC	CAM1_LA01_CLK_P	Camera 1 Clock lane via LA01 Positive
D9	LA01_N_CC	CAM1_LA01_CLK_N	Camera 1 Clock lane via LA01 Negative
D10	GND	GND	Ground
D11	LA05_P	CAM1_SDA	Camera 1 I2C bus data
D12	LA05_N	CAM1_SCL	Camera 1 I2C bus clock
D13	GND	GND	Ground
D14	LA09_P	CAM1_IO1	Camera 1 IO1 (GPIO)
D15	LA09_N	CAM1_IO0	Camera 1 IO0 (GPIO)
D16	GND	GND	Ground
D17	LA13_P	CAM_IO0_DIR	Camera IO0 Direction select
D18	LA13_N	CAM_IO1_DIR	Camera IO1 Direction select
D19	GND	GND	Ground
D20	LA17_P_CC	CAM2_DATA1_P	Camera 2 Data lane 1 Positive
D21	LA17_N_CC	CAM2_DATA1_N	Camera 2 Data lane 1 Negative

D22	GND	GND	Ground
D23	LA23_P	STB_LA23_P	Not connected, reserved for strobe propagation
D24	LA23_N	STB_LA23_N	Not connected, reserved for strobe propagation
D25	GND	GND	Ground
D26	LA26_P	CAM3_LA26_CLK_P	Camera 3 Clock lane via LA26 Positive
D27	LA26_N	CAM3_LA26_CLK_N	Camera 3 Clock lane via LA26 Negative
D28	GND	GND	Ground
D29	TCK	N/C	Not used
D30	TDI	TDI-TDO	JTAG TDI (Connects to TDO to close JTAG chain)
D31	TDO	TDI-TDO	JTAG TDO (Connects to TDI to close JTAG chain)
D32	3P3VAUX	3V3AUX	3.3VDC Power supply for EEPROM
D33	TMS	N/C	Not used
D34	TRST_L	N/C	Not used
D35	GA1	GA1	EEPROM Address Bit 0 (A0)
D36	3P3V_2	3V3	3.3VDC
D37	GND	GND	Ground
D38	3P3V_3	3V3	3.3VDC
D39	GND	GND	Ground
D40	3P3V_4	3V3	3.3VDC
G1	GND	GND	Ground

G2	CLK1_M2C_P	CLK1_M2C_P	Not used
G3	CLK1_M2C_N	CLK1_M2C_N	Not used
G4	GND	GND	Ground
G5	GND	GND	Ground
G6	LA00_P_CC	CAM0_CLK_P	Camera 0 Clock lane Positive
G7	LA00_N_CC	CAM0_CLK_N	Camera 0 Clock lane Negative
G8	GND	GND	Ground
G9	LA03_P	CAM0_SDA	Camera 0 I2C bus data
G10	LA03_N	CAM0_SCL	Camera 0 I2C bus clock
G11	GND	GND	Ground
G12	LA08_P	STB_LA08_P	Not connected, reserved for strobe propagation
G13	LA08_N	STB_LA08_N	Not connected, reserved for strobe propagation
G14	GND	GND	Ground
G15	LA12_P	CAM0_IO1	Camera 0 IO1 (GPIO)
G16	LA12_N	CAM0_IO0	Camera 0 IO0 (GPIO)
G17	GND	GND	Ground
G18	LA16_P	CAM1_LA16_CLK_P	Camera 1 Clock lane via LA16 Positive
G19	LA16_N	CAM1_LA16_CLK_N	Camera 1 Clock lane via LA16 Negative
G20	GND	GND	Ground
G21	LA20_P	CAM3_IO1	Camera 3 IO1 (GPIO)
G22	LA20_N	CAM3_IO0	Camera 3 IO0 (GPIO)
G23	GND	GND	Ground

G24	LA22_P	STB_LA22_P	Not connected, reserved for strobe propagation
G25	LA22_N	STB_LA22_N	Not connected, reserved for strobe propagation
G26	GND	GND	Ground
G27	LA25_P	CAM3_CLK_SEL	Camera 3 Clock select (0=LA26,1=LA31)
G28	LA25_N	CAM1_CLK_SEL	Camera 1 Clock select (0=LA01,1=LA16)
G29	GND	GND	Ground
G30	LA29_P	N/C	Not used
G31	LA29_N	N/C	Not used
G32	GND	GND	Ground
G33	LA31_P	CAM3_LA31_CLK_P	Camera 3 Clock lane via LA31 Positive
G34	LA31_N	CAM3_LA31_CLK_N	Camera 3 Clock lane via LA31 Negative
G35	GND	GND	Ground
G36	LA33_P	CAM3_DATA0_P	Camera 3 Data lane 0 Positive
G37	LA33_N	CAM3_DATA0_N	Camera 3 Data lane 0 Negative
G38	GND	GND	Ground
G39	VADJ_3	VADJ	I/O Supply Voltage (1.2VDC)
G40	GND	GND	Ground
H1	VREF_A_M2C	N/C	Not used
H2	PRSNT_M2C_L	GND	Ground
H3	GND	GND	Ground
H4	CLK0_M2C_P	CLK0_M2C_P	Not used
H5	CLK0_M2C_N	CLK0_M2C_N	Not used

H6	GND	GND	Ground
H7	LA02_P	CAM0_DATA1_P	Camera 0 Data lane 1 Positive
H8	LA02_N	CAM0_DATA1_N	Camera 0 Data lane 1 Negative
H9	GND	GND	Ground
H10	LA04_P	N/C	Not used
H11	LA04_N	N/C	Not used
H12	GND	GND	Ground
H13	LA07_P	N/C	Not used
H14	LA07_N	N/C	Not used
H15	GND	GND	Ground
H16	LA11_P	STB_LA11_P	Not connected, reserved for strobe propagation
H17	LA11_N	STB_LA11_N	Not connected, reserved for strobe propagation
H18	GND	GND	Ground
H19	LA15_P	CAM1_DATA0_P	Camera 1 Data lane 0 Positive
H20	LA15_N	CAM1_DATA0_N	Camera 1 Data lane 0 Negative
H21	GND	GND	Ground
H22	LA19_P	CAM2_IO1	Camera 2 IO1 (GPIO)
H23	LA19_N	CAM2_IO0	Camera 2 IO0 (GPIO)
H24	GND	GND	Ground
H25	LA21_P	STB_LA21_P	Not connected, reserved for strobe propagation

H26	LA21_N	STB_LA21_N	Not connected, reserved for strobe propagation
H27	GND	GND	Ground
H28	LA24_P	CAM2_DATA0_P	Camera 2 Data lane 0 Positive
H29	LA24_N	CAM2_DATA0_N	Camera 2 Data lane 0 Negative
H30	GND	GND	Ground
H31	LA28_P	CAM3_DATA1_P	Camera 3 Data lane 1 Positive
H32	LA28_N	CAM3_DATA1_N	Camera 3 Data lane 1 Negative
H33	GND	GND	Ground
H34	LA30_P	CAM2_SDA	Camera 2 I2C bus data
H35	LA30_N	CAM2_SCL	Camera 2 I2C bus clock
H36	GND	GND	Ground
H37	LA32_P	CAM3_SDA	Camera 3 I2C bus data
H38	LA32_N	CAM3_SCL	Camera 3 I2C bus clock
H39	GND	GND	Ground
H40	VADJ_4	VADJ	I/O Supply Voltage (1.2VDC)

Net lengths

The table below lists the critical trace lengths.

	Net	Length (mils)
Camera 0	CAM0_CLK_N	1506.42
	CAM0_CLK_P	1506.992
	CAM0_DATA0_N	1508.888

	CAM0_DATA0_P	1510.286
	CAM0_DATA1_N	1507.443
	CAM0_DATA1_P	1509.986
Camera 1	CAM1_LA01_CLK_N	1480.268
	CAM1_LA01_CLK_P	1480.153
	CAM1_LA16_CLK_N	1479.618
	CAM1_LA16_CLK_P	1479.503
	CAM1_DATA0_N	1482.367
	CAM1_DATA0_P	1479.931
	CAM1_DATA1_N	1475.515
	CAM1_DATA1_P	1478.691
Camera 2	CAM2_CLK_N	1513.183
	CAM2_CLK_P	1513.034
	CAM2_DATA0_N	1518.514
	CAM2_DATA0_P	1516.078
	CAM2_DATA1_N	1521.252
	CAM2_DATA1_P	1521.171
Camera 3	CAM3_LA26_CLK_N	1625.862
	CAM3_LA26_CLK_P	1622.853
	CAM3_LA31_CLK_N	1624.063
	CAM3_LA31_CLK_P	1621.055
	CAM3_DATA0_N	1627.619
	CAM3_DATA0_P	1623.909

CAM3_DATA1_N	1622.79
CAM3_DATA1_P	1621.035

Specifications

Recommended Operating Conditions

SUPPLY VOLTAGE	MIN	TYP	MAX	UNIT
12 VDC	+11.4	+12	+12.6	V
3.3 VDC	+3.14	+3.3	+3.46	V
VADJ 1.2VDC	+1.14	+1.2	+1.26	V

Note that the 12 VDC power supply is not used by the RPi Camera FMC.

Power Consumption

The specifications below refer to the total current draw on each of the power supplies while the RPi Camera FMC is connected to a development board and has 4x cameras connected and streaming video at 1080p resolution.

SUPPLY	UTILIZATION	MIN	TYP	MAX	UNIT
12 VDC	100%		0		mA
3.3 VDC	100%		(coming soon)		mA
VADJ 1.2 VDC	100%		(coming soon)		mA

- Tests performed at ambient temperature of 25 degrees C
- Tests performed using the ZCU102 development board
- Tests performed using 4x Raspberry Pi camera v2

Note that the RPi Camera FMC example design will also produce an increase in power consumption of the FPGA/MPSoC on the development board due to the use of FPGA and hardware resources.

Thermal Information

We have not performed comprehensive thermal testing on the RPi Camera FMC, however we recommend that it be operated under ambient temperatures between -20 and 60 degrees C. This advice is based on the recommended ambient operating temperatures of the Raspberry Pi camera v2. The critical devices on the mezzanine card have operating ranges that exceed those of the camera and are listed in the table below.

Component Ambient Operating Temperatures

DEVICE	MIN	MAX	UNIT
OnSemi, MIPI Switch, FSA646AUCX	-40	85	C
ST, 2K EEPROM, M24C02-FDW6TP	-40	85	C
TI, Level translator, SN74AVC4T245RSVR	-40	85	C
TI, I2C Level translator, TCA9416DTMR	-40	125	C
ESD Protection	-55	125	C

Components that are not listed in the table above (such as resistors, capacitors) are selected to have minimum operating temperature that is lower than -20 degrees C, and maximum operating temperature that is greater than 60 degrees C.

Reset Timing

The RPi Camera FMC has no special reset requirements, however be aware that Raspberry Pi cameras and compatible cameras typically do have reset requirements. Please refer to the datasheets of the cameras being used for the appropriate reset timing requirements.

I2C (EEPROM) Timing

The serial EEPROM (part number ST, 2K EEPROM, M24C02-FDW6TP) has a maximum operating clock frequency of 400 kHz.

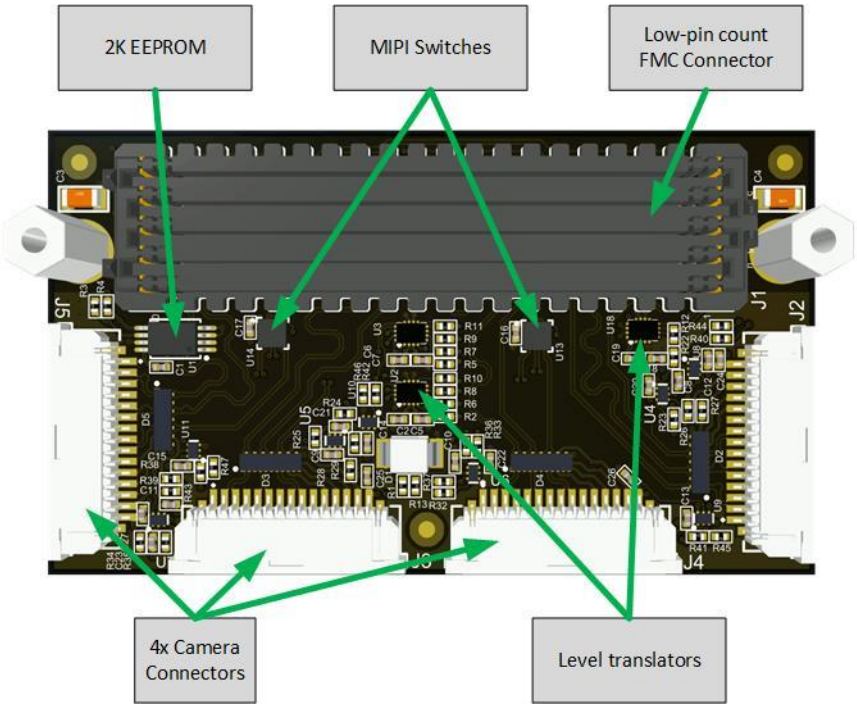
Certifications

- RoHS
- CE
- UKCA

Detailed Description

Hardware Overview

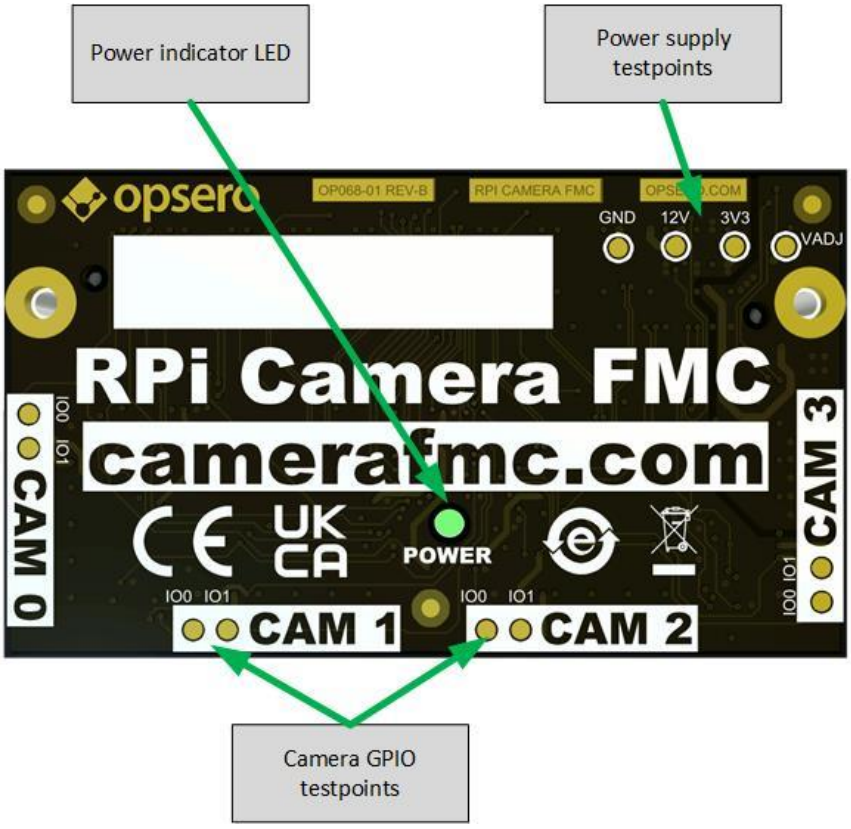
The figure below illustrates the various hardware components that are located on the top-side of the RPi Camera FMC.



The main components on the top-side of the mezzanine card are:

- 4x 15-pin FFC connectors (camera connectors)
- Low Pin Count FMC Connector
- 2K EEPROM
- 2x MIPI switches
- Level translators

The figure below illustrates the various hardware components that are located on the bottom-side of the mezzanine card.



The main components on the bottom-side of the mezzanine card are:

- Power indicator LED
- Test points for power supplies
- Test points for camera GPIOs (IO0 and IO1)

Camera connectors

The Raspberry Pi cameras and compatible cameras connect to the mezzanine card through 4x 15-pin flat flexible cable (FFC) connectors.

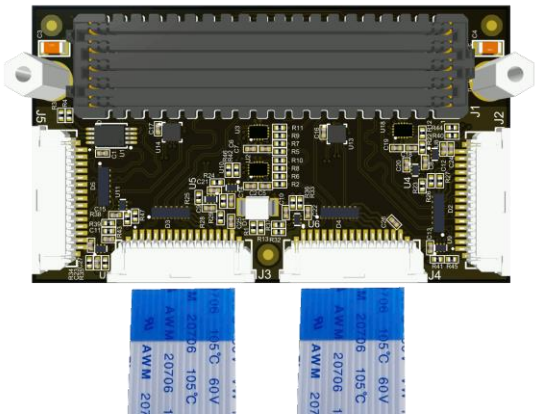
The pinout of the camera connector is shown in the table below:

Pin #	Signal name	Description
1	GND	Ground
2	DATA0_N	Data lane 0 (negative)
3	DATA0_P	Data lane 0 (positive)

4	GND	Ground
5	DATA1_N	Data lane 1 (negative)
6	DATA1_P	Data lane 1 (positive)
7	GND	Ground
8	CLK_N	Clock lane (negative)
9	CLK_P	Clock lane (positive)
10	GND	Ground
11	IO0	General purpose IO 0
12	IO1	General purpose IO 1
13	SCL	I2C bus clock
14	SDA	I2C bus data
15	3V3	3.3VDC power supply

The camera connectors on the mezzanine card are Amphenol ICC, FFC connector, SFW15R-1STE1LF . This is a bottom contact connector, meaning that the flex cable of the camera must be inserted with the contacts facing downwards. The images below illustrate this requirement.

Top view



Bottom view

EEPROM

The EEPROM (ST, 2K EEPROM, M24C02-FDW6TP) stores IPMI FRU data that can be read by the carrier board and contains the following information:

- Manufacturer name (Opsero Electronic Design Inc.)
- Product name
- Product part number
- Serial number
- Power supply requirements

The FRU data is read by some carrier boards to determine the correct VADJ voltage to apply to the mezzanine card. All Opsero FMC products have their EEPROMs programmed with valid FRU data to allow these carrier boards to correctly power them.

Erasing or writing over the contents of the EEPROM can corrupt the IPMI FRU data making the mezzanine card unusable with carrier boards that require the information. We recommend that you do not use the mezzanine card's EEPROM for non-volatile storage but instead use the storage options provided by the carrier board. If you mistakenly erase or corrupt the contents of the EEPROM, you can reprogram it using the Opsero FMC EEPROM Tool. Read more about the FMC EEPROM tool in the User Guide.

Low Pin Count FMC Connector

The RPi Camera FMC has a low pin count FMC (FPGA Mezzanine Card) connector for interfacing with an FPGA or SoC development board. The part number of this connector is Samtec, Low pin count FMC connector, ASP-134604-01 . The pinout of this connector conforms to the VITA 57.1 FPGA Mezzanine Card Standard (for more information, see Pin configuration. For more information on the FMC connector and the VITA 57.1 standard, see the Samtec page on VITA 57.1 .

Level translation

The FPGA I/O voltage (VADJ) is 1.2VDC however the Raspberry Pi camera I2C and GPIO interfaces require 3.3VDC signals. For this reason, the RPi Camera FMC uses bidirectional level translation devices to convert the VADJ voltage levels to 3.3VDC. The RPi Camera FMC uses the two devices listed below:

Device	Purpose
TCA9416DTMR	Level translation of camera I2C buses. Always enabled.
SN74AVC4T245RSVR	Level translation of camera IO0, IO1. Direction and output enable are configurable.

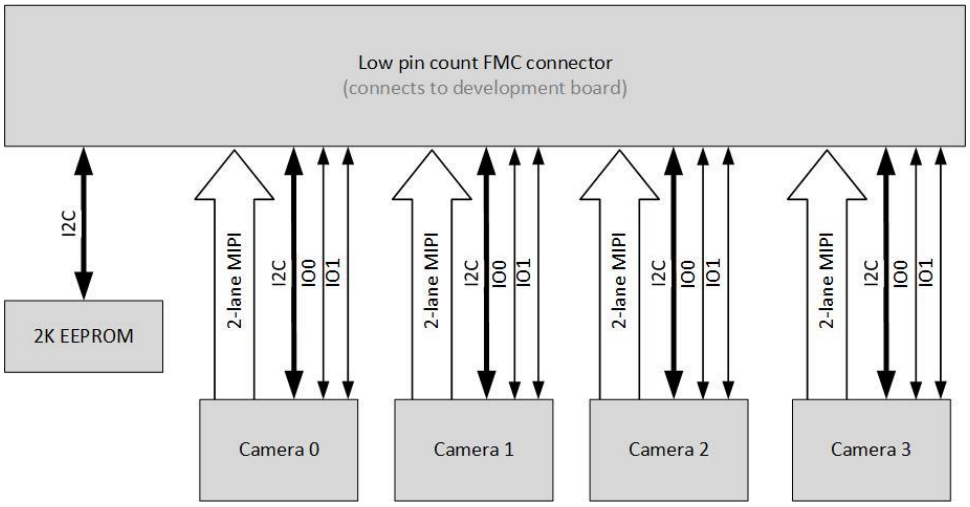
The level translation for the I2C buses is always enabled and cannot be configured. As for the camera GPIO, the user has some control over the direction of IO0 and IO1, as well as whether or not they enabled or disabled (see Camera GPIO for more information).

I/O Interfaces

The FMC connector provides power to the RPi Camera FMC and also presents the following I/O signals to the FPGA fabric of the development board:

- 2-lane MIPI interfaces for each camera
- I2C buses (one for each camera)
- GPIO (IO0 and IO1) for each camera
- I2C for EEPROM R/W access

The MIPI interfaces, I2C buses and camera GPIO are routed to independent pins on the FMC connector. The figure below is a simplified connection diagram for the FMC connector. Note that the MIPI switches and level translation are left out of the diagram for clarity.



I2C Bus Interfaces

The I2C bus interface of each camera is routed independently to the FMC connector. In this configuration, there is no need for an I2C MUX, as the I2C buses are not linked together. Instead, each camera's I2C bus is accessible through dedicated pins on the FMC connector, listed in the table below. This configuration simplifies the I2C interactions with the cameras, but comes at the expense of requiring a dedicated I2C controller for each camera to be implemented in the FPGA fabric.

Camera	I2C signal	Net name	FMC pin

Camera 0	SDA (data)	CAM0_SDA	LA03_P
	SCL (clock)	CAM0_SCL	LA03_N
Camera 1	SDA (data)	CAM1_SDA	LA05_P
	SCL (clock)	CAM1_SCL	LA05_N
Camera 2	SDA (data)	CAM2_SDA	LA30_P
	SCL (clock)	CAM2_SCL	LA30_N
Camera 3	SDA (data)	CAM3_SDA	LA32_P
	SCL (clock)	CAM3_SCL	LA32_N

The I2C buses pass through level translators to convert the VADJ voltage levels to the 3.3VDC levels required by the Raspberry Pi cameras. These level translators are hard wired to be always enabled.

Camera GPIO

Eight FMC pins are dedicated to the control of each camera's GPIO pins IO0 and IO1. These I/Os pass through level translators to convert the VADJ voltage levels to 3.3VDC levels required by the Raspberry Pi cameras.

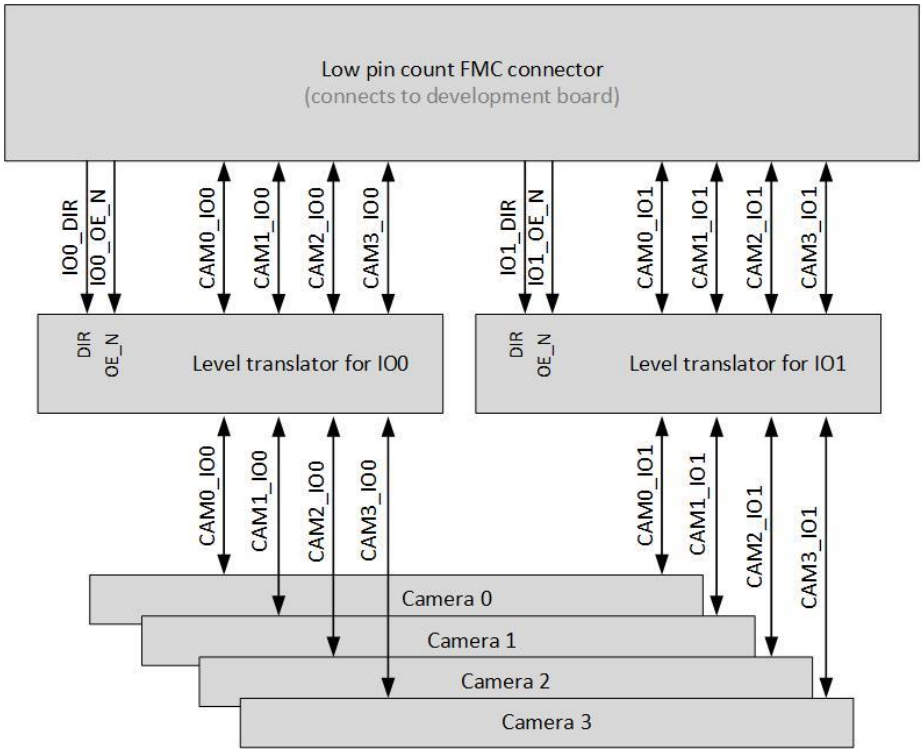
Camera	GPIO	Net name	FMC pin
Camera 0	IO0	CAM0_IO0	LA12_N
	IO1	CAM0_IO1	LA12_P
Camera 1	IO0	CAM1_IO0	LA09_N
	IO1	CAM1_IO1	LA09_P
Camera 2	IO0	CAM2_IO0	LA19_N
	IO1	CAM2_IO1	LA19_P
Camera 3	IO0	CAM3_IO0	LA20_N
	IO1	CAM3_IO1	LA20_P

Direction and output enable

Four FMC pins are dedicated for the configuration of the IO0 and IO1 direction and enabled state. These pins control the direction (camera-to-FPGA or FPGA-to-camera) and output enable for the IO0/IO1 signals, and **the setting applies to all four cameras**.

Net name	FMC Pin	Purpose
CAM_IO0_DIR	LA13_P	IO0 direction (0=Cam-to-FPGA,1=FPGA-to-cam)
CAM_IO1_DIR	LA13_N	IO1 direction (0=Cam-to-FPGA,1=FPGA-to-cam)
CAM_IO0_OE_N	LA27_P	IO0 output enable (0=Enabled,1=Hi-Z output)
CAM_IO1_OE_N	LA27_N	IO1 output enable (0=Enabled,1=Hi-Z output)

The diagram below illustrates the connection of the DIR and OE_N signals of the two level translators, one for IO0 and the other for IO1.



Note that in the case of the Raspberry Pi camera v2 and many of the compatible cameras, the IO0 should be configured as an output (FPGA-to-camera), while the IO1 can be left disabled. The usage of IO0 and IO1 on other cameras may be different and should be verified by the user.

Camera	CAM_IO0_DIR	CAM_IO1_DIR	CAM_IO0_OE_N	CAM_IO1_OE_N
Raspberry Pi camera v2	1	Don’t care	0	Don’t care
Digilent Pcam	1	Don’t care	0	Don’t care

Testpoints

To facilitate debugging, testpoints for the GPIO (IO0 and IO1) of each camera is accessible on the bottom side of the mezzanine card. These testpoints are labelled in the bottom side view above.

MIPI Interfaces

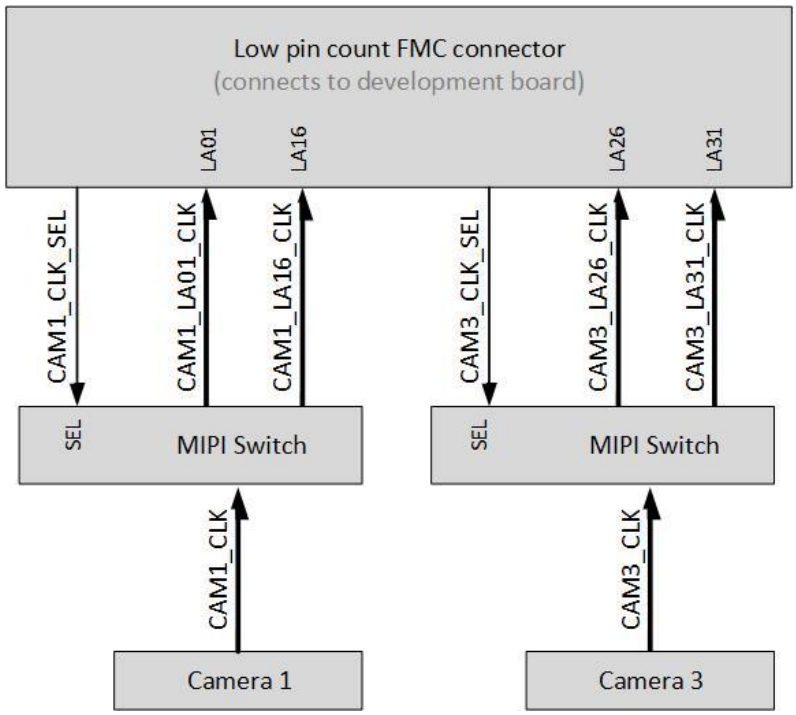
The MIPI CSI interfaces from each camera are routed directly from the camera (FFC) connectors to the FMC connector. This is true for all of the MIPI signals with the exception of the MIPI clocks from cameras 1 and 3, which instead pass through MIPI switches (discussed in the following section). The MIPI CSI signals do not pass through any level translation on the RPi Camera FMC, therefore it is required that the carrier board's FPGA device be able to receive MIPI CSI-2 D-PHY signals directly on it's I/O pins. The AMD Xilinx UltraScale+ and Zynq UltraScale+ devices are capable of receiving MIPI CSI signals in this way.

The MIPI CSI-2 D-PHY interface is a complex inter-chip communication standard that operates at rates of 500-1000 Mbps and uses two transmission modes (low-power mode and high-speed mode) with different voltage levels. For this reason, MIPI D-PHY requires specialized input circuitry which (at the current time) is typically only found on higher end FPGA devices such as the AMD Xilinx UltraScale+ and Zynq UltraScale+ devices.

MIPI Switches

To enable the RPi Camera FMC to support a useful range of carrier boards, it was designed with two MIPI switches (OnSemi, MIPI Switch, FSA646AUCX) that allow the MIPI clocks from cameras 1 and 3 to each be selectively routed to two different pairs on the FMC connector. The ability to redirect these camera clocks to suit the carrier board, allows the mezzanine card to support a wider range of carrier boards than would have otherwise been possible.

The diagram below illustrates the clock connections of cameras 1 and 3 through the MIPI switches. Note that the clock signals (shown as single thick lines for clarity) are actually differential and composed of a positive and negative trace.



It is also important to note that **all of the other MIPI signals**, including the data lanes of cameras 1 and 3, as well as clock and data lanes of cameras 0 and 2, **cannot be selectively routed** as they connect directly from the FMC pins to the camera pins.

Two FMC pins are dedicated to driving the select (SEL) inputs of the MIPI switches; we refer to these signals as the clock select signals and they have the net names CAM1_CLK_SEL and CAM3_CLK_SEL. These signals pass through level converters before driving the MIPI switches which require 3.3VDC inputs. The table below shows the clock select signal locations on the FMC connector, and their effect on the routing of the clocks of cameras 1 and 3.

Net name	FMC pin	Clock routing when CLK_SEL = 0	Clock routing when CLK_SEL = 1
CAM1_CLK_SEL	LA25_N	CAM1_CLK => LA01	CAM1_CLK => LA16
CAM3_CLK_SEL	LA25_P	CAM3_CLK => LA26	CAM3_CLK => LA31

The clock select pins should be driven by the FPGA with constant values, depending on the carrier board that is being used. The table below lists the recommended clock select values for the currently supported carrier boards. Note that these required clock select values are included in the example designs.

Dev board	CAM1_CLK_SEL	CAM3_CLK_SEL
ZCU104	1	0
ZCU102	1	0
ZCU106	1	0
PYNQ-ZU	1	0
Genesys-ZU	0	0
UltraZed EV Carrier	0	1

I/O Expanders

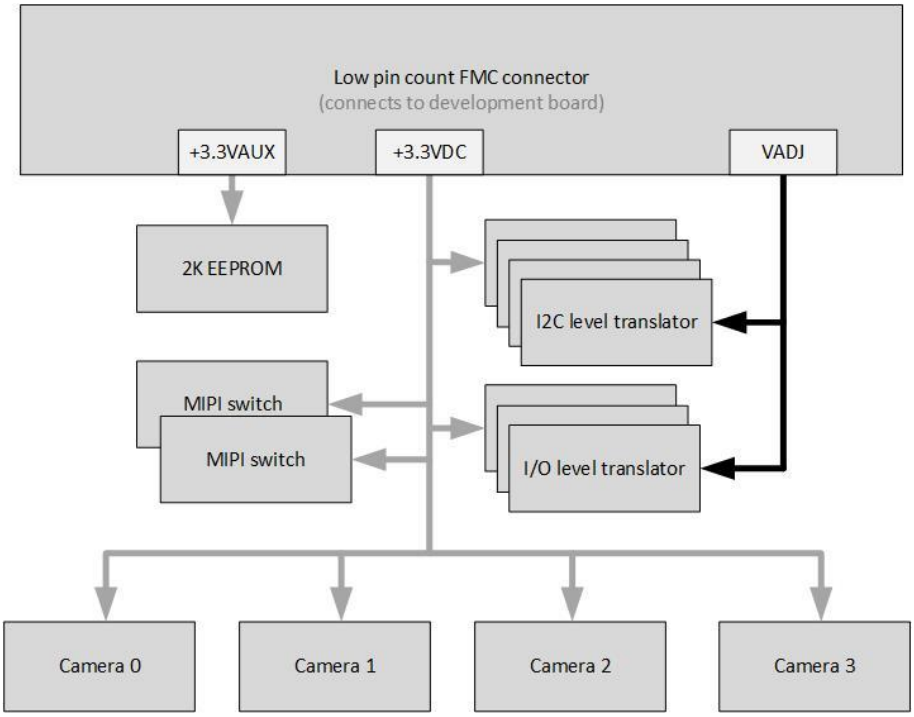
To facilitate production testing of this product, we designed it with 4x I/O expanders (TI, I/O Expander, TCA9536DTMR), one connected to the I2C bus of each camera. The I/O expanders have 4 I/Os, the first two of which are connnected to IO0 and IO1 through 510R resistors for protection in the event of bus contention. More information for using the I/O expanders can be found in the corresponding section of the programming guide.

Power Supplies

All power required by the RPi Camera FMC is supplied by the development board through the FMC connector:

- +12VDC
- +3.3VDC
- +3.3VAUX (for powering EEPROM only)
- VADJ: +1.2VDC

Note that although the FMC standard provides for a 12VDC supply, the RPi Camera FMC does not use or draw current from that supply.



3.3VDC Supply

The 3.3VDC supply provides power for the 4x cameras, but it is also the supply for the MIPI switches and the level translators.

VADJ Supply

As the RPi Camera FMC uses level translators, it can be used with any VADJ voltage level between 1.2VDC and 3.3VDC without risk of damaging any of the components or the cameras. However, we strongly recommend using the RPi Camera FMC at the VADJ voltage level of 1.2VDC if you are using our example designs or other designs that are based on the AMD Xilinx MIPI CSI Controller Subsystem IP core.

The only devices on the RPi Camera FMC that are powered by the VADJ voltage, are the I2C level translators and the I/O level translators.

Power LED and testpoints

A single green LED on the RPi Camera FMC is used to indicate when the required power supplies are active. The LED is controlled by the PG pin of the FMC connector (driven by the carrier board), and driven by one of the I/O level translators.

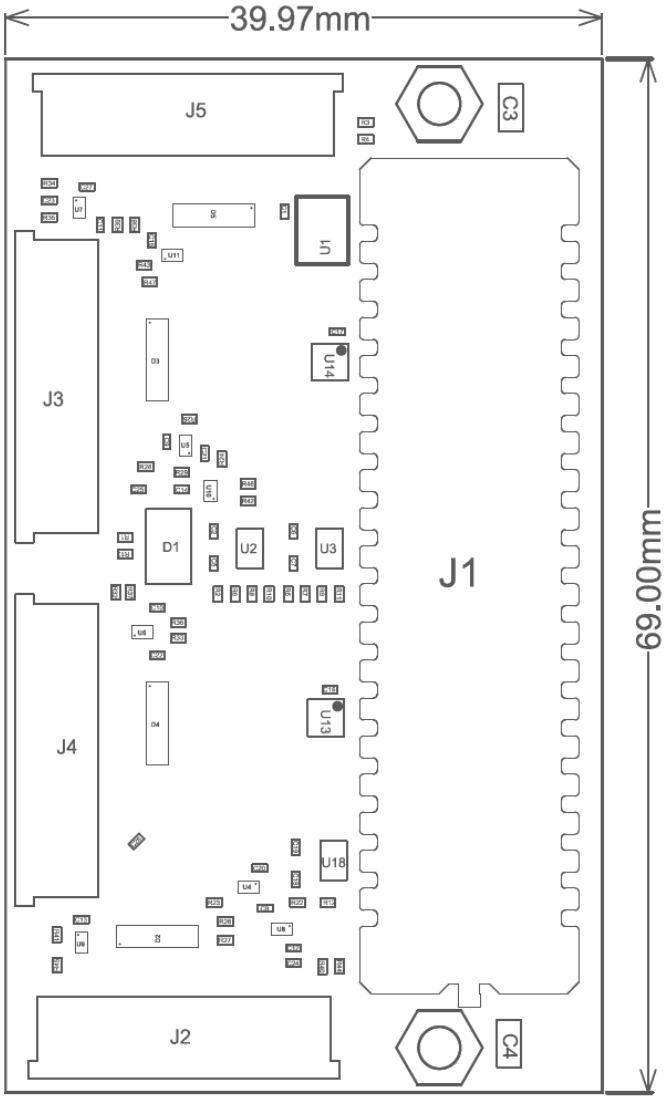
To aid hardware debug, test points are accessible on the bottom side of the mezzanine card for each of the power supplies of the RPi Camera FMC.

Mechanical Information

Dimensions

The mechanical dimensions of the RPi Camera FMC are illustrated in the figures below. All dimensions are in millimeters (mm).

The assembly drawings are also available as PDF files that you can download at the provided links.



- RPi Camera FMC Rev-B Assembly Drawing

3D Model

The 3D model of the board is available as a STEP file at the links below:

- RPi Camera FMC Rev-B 3D STEP model

Mezzanine Fastening Hardware

For mechanical fastening of the mezzanine card to the carrier board, the RPi Camera FMC comes with 2x hex standoffs and the screws to fasten them to the carrier board. We **highly recommend** using the machine screws on each of these standoffs to fix the mezzanine card to the carrier board. If the fastening screws are misplaced, they can be replaced by the ones listed below, or equivalents.

The hex standoff and machine screw part numbers are listed below:

- Hex standoff, Thread M2.5 x 0.45, Brass, Board-to-board length 10mm
  Part number: V6516C
  Manufacturer: Assmann

- Machine screw, Thread M2.5 x 0.45, Length (below head) 4mm, Stainless steel, Phillips head
  Part number: 90116A105
  Supplier: McMaster-Carr

More information

The following online documentation is available for further reference:

- Datasheet
- Getting Started Guide
- Board files and other references
- Reference design documentation

Revision History

Date	Version	Description
2023-05-02	1.0	Initial PDF release.

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