

# UCC21755-Q1 Automotive 10-A Source/Sink Reinforced Isolated Single Channel Gate Driver for SiC/IGBT with Active Protection, Isolated Analog Sensing and High-CMTI

## 1 Features

- 5.7-kV<sub>RMS</sub> single-channel isolated gate driver
- AEC-Q100 Qualified with the following results:
  - Device temperature grade 0: -40°C to +150°C ambient operating temperature range
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- [Functional Safety Quality-Managed](#)
  - [Documentation available to aid functional safety system design](#)
- SiC MOSFETs and IGBTs up to 2121 V<sub>pk</sub>
- 33-V maximum output drive voltage (VDD-VEE)
- ±10-A drive strength and split output
- 150-V/ns minimum CMTI
- 200-ns response time fast DESAT protection with 5-V threshold
- 4-A internal active Miller clamp
- 400-mA soft turn-off when fault happens
- Isolated analog sensor with PWM output for
  - Temperature sensing with NTC, PTC, or thermal diode
  - High voltage DC-link or phase voltage
- Alarm FLT on overcurrent and reset from RST/EN
- Fast enable/disable response on RST/EN
- Reject <40-ns noise transient and pulse on input pins
- 12-V VDD UVLO with power good on RDY
- Inputs/outputs with over- or under-shoot transient voltage immunity up to 5 V
- 130-ns (maximum) propagation delay and 30-ns (maximum) pulse/part skew
- SOIC-16 DW package with creepage and clearance distance > 8mm
- Operating junction temperature -40°C to 150°C

## 2 Applications

- Traction inverter for EVs
- On-board charger and charging pile
- DC/DC converter for HEV/EVs

## 3 Description

The UCC21755-Q1 is a galvanic isolated single channel gate driver designed for SiC MOSFETs and IGBTs up to 2121-V DC operating voltage with advanced protection features, best-in-class dynamic performance, and robustness. UCC21755-Q1 has up to ±10-A peak source and sink current.

The input side is isolated from the output side with SiO<sub>2</sub> capacitive isolation technology, supporting up to 1.5-kV<sub>RMS</sub> working voltage, 12.8-kV<sub>PK</sub> surge immunity with longer than 40-years isolation barrier life, as well as providing low part-to-part skew, and >150-V/ns common mode noise immunity (CMTI).

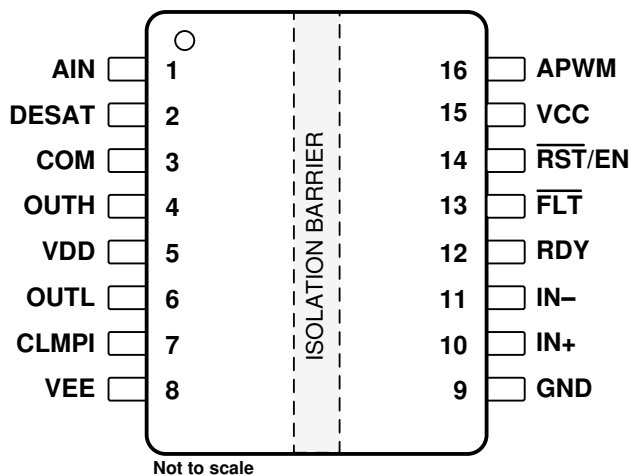
The UCC21755-Q1 includes the state-of-art protection features, such as fast overcurrent and short circuit detection, shunt current sensing support, fault reporting, active Miller clamp, and input and output side power supply UVLO to optimize SiC and IGBT switching behavior and robustness. The isolated analog to PWM sensor can be utilized for easier temperature or voltage sensing, further increasing the drivers' versatility and simplifying the system design effort, size, and cost.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
UCC21755-Q1	SOIC-16	10.3 mm × 7.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Device Pin Configuration



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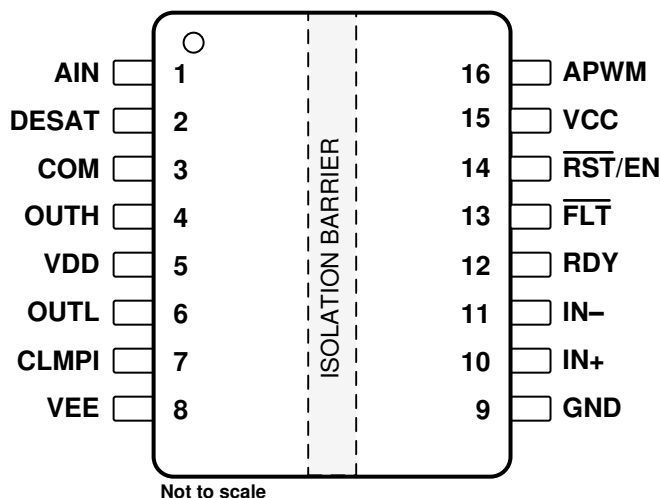
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2022	*	Initial release

## 5 Pin Configuration and Functions



**Figure 5-1. UCC21755-Q1 DW SOIC (16) Top View**

**Table 5-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
AIN	1	I	Isolated analog sensing input, parallel a small capacitor to COM for better noise immunity. Tie to COM if unused.
DESAT	2	I	Desaturation current protection input. Tie to COM if unused.
COM	3	P	Common ground reference, connecting to emitter pin for IGBT and source pin for SiC-MOSFET
OUTH	4	O	Gate driver output pullup
VDD	5	P	Positive supply rail for gate drive voltage. Bypass with a >10-μF capacitor to COM to support specified gate driver source peak current capability. Place decoupling capacitor close to the pin.
OUTL	6	O	Gate driver output pulldown
CLMPI	7	I	Internal Active Miller clamp, connecting this pin directly to the gate of the power transistor. Leave floating or tie to VEE if unused.
VEE	8	P	Negative supply rail for gate drive voltage. Bypass with a >10-μF capacitor to COM to support specified gate driver sink peak current capability. Place decoupling capacitor close to the pin.
GND	9	P	Input power supply and logic ground reference
IN+	10	I	Non-inverting gate driver control input. Tie to VCC if unused.
IN-	11	I	Inverting gate driver control input. Tie to GND if unused.
RDY	12	O	Power good for VCC-GND and VDD-COM. RDY is open-drain configuration and can be paralleled with other RDY signals.
FLT	13	O	Active low fault alarm output upon overcurrent or short circuit. FLT is in open-drain configuration and can be paralleled with other faults.
RST/EN	14	I	The RST/EN serves two purposes: 1) Enables or shuts down the output side. The FET is turned off by a regular turn-off, if pin EN is set to low; 2) Resets the DESAT condition signaled on the FLT pin if the pin RST/EN is set to low for more than 1000 ns. A reset of signal FLT is asserted at the rising edge of pin RST/EN. For automatic RESET function, this pin only serves as an EN pin. Enable or shutdown the output side. The FET is turned off by a regular turn-off, if pin EN is set to low. Tie to IN+ for automatic reset.
VCC	15	P	Input power supply from 3 V to 5.5 V. Bypass with a >1-μF capacitor to GND. Place decoupling capacitor close to the pin.
APWM	16	O	Isolated analog sensing PWM output. Leave floating if unused.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
VCC	VCC - GND	-0.3	6	V
VDD	VDD - COM	-0.3	36	V
VEE	VEE - COM	-17.5	0.3	V
V <sub>MAX</sub>	VDD - VEE	-0.3	36	V
IN+, IN-, RST/EN	DC	GND-0.3	VCC	V
	Transient, less than 100 ns <sup>(2)</sup>	GND-5.0	VCC+5.0	V
DESAT		COM-0.3	VDD+0.3	V
AIN	Reference to COM	-0.3	5	V
OUTH, OUTL, CLMPI	DC	VEE-0.3	VDD	V
	Transient, less than 100 ns <sup>(2)</sup>	VEE-5.0	VDD+5.0	V
RDY, FLT, APWM		GND-0.3	VCC	V
I <sub>FLT</sub> , I <sub>RDY</sub>	FLT and RDY pin input current		20	mA
I <sub>APWM</sub>	APWM pin output current		20	mA
T <sub>J</sub>	Junction Temperature	-40	150	°C
T <sub>stg</sub>	Storage Temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime
- (2) Values are verified by characterization on bench.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	VCC-GND	3	5.5	V
VDD	VDD-COM	13	33	V
VEE	VEE-COM	-16	0	V
V <sub>MAX</sub>	VDD-VEE		33	V
IN+, IN-, RST/EN	Reference to GND, High level input voltage	0.7xVCC	VCC	V
	Reference to GND, Low level input voltage	0	0.3xVCC	V
AIN	Reference to COM	0.6	4.5	V
t <sub>RST/EN</sub>	Minimum pulse width that reset the fault	1000		ns
T <sub>A</sub>	Ambient temperature	-40	125	°C
T <sub>J</sub>	Junction temperature	-40	150	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC21755-Q1	UNIT
		DW (SOIC)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	68.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	27.5	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	32.9	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	14.1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	32.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/- = 5V, 150kHz, 50% Duty Cycle for 10nF load, T <sub>a</sub> = 25°C			985	mW
P <sub>D1</sub>	Maximum power dissipation (side-1)				20	mW
P <sub>D2</sub>	Maximum power dissipation (side-2)				965	mW

## 6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 600 V <sub>RMS</sub>	I-IV	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>	I-III	
DIN V VDE 0884-11 (VDE V 0884-11): 2017-01 <sup>(2)</sup>				
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDb) test	1500	V <sub>RMS</sub>
		DC voltage	2121	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification test)	8000	V <sub>PK</sub>
		V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production test)	8000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(3)</sup>	Test method per IEC 62368-1, 1.2/50 μs waveform, V <sub>TEST</sub> = 1.6 × V <sub>IOSM</sub> = 12800 V <sub>PK</sub> (qualification)	8000	V <sub>PK</sub>

## 6.6 Insulation Specifications (continued)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
q <sub>pd</sub>	Apparent charge <sup>(4)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> = 2545 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> = 3394 V <sub>PK</sub> , t <sub>m</sub> = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> = 3977 V <sub>PK</sub> , t <sub>m</sub> = 1 s	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 0.5 × sin (2πft), f = 1 MHz	~ 1	pF
R <sub>IO</sub>	Insulation resistance, input to output <sup>(5)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	≥ 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	≥ 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	≥ 10 <sup>9</sup>	
	Pollution degree		2	
	Climatic category		40/125/21	
<b>UL 1577</b>				
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> = 5700 V <sub>RMS</sub> , t = 60 s (qualification), V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> = 6840 V <sub>RMS</sub> , t = 1 s (100% production)	5700	V <sub>RMS</sub>

- Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
- This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- Apparent charge is electrical discharge caused by a partial discharge (pd).
- All pins on each side of the barrier tied together creating a two-pin device.

## 6.7 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 68.3°C/W, V <sub>DD</sub> = 15 V, V <sub>EE</sub> = -5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			61	mA
		R <sub>θJA</sub> = 68.3°C/W, V <sub>DD</sub> = 20 V, V <sub>EE</sub> = -5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			49	
P <sub>S</sub>	Safety input, output, or total power	R <sub>θJA</sub> = 68.3°C/W, V <sub>DD</sub> = 20 V, V <sub>EE</sub> = -5V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C			1220	mW
T <sub>S</sub>	Maximum safety temperature				150	°C

- The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>. The junction-to-air thermal resistance, R<sub>qJA</sub>, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: T<sub>J</sub> = T<sub>A</sub> + R<sub>qJA</sub> · P, where P is the power dissipated in the device. T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>qJA</sub> · P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum allowed junction temperature. P<sub>S</sub> = I<sub>S</sub> · V<sub>I</sub>, where V<sub>I</sub> is the maximum supply voltage.

## 6.8 Electrical Characteristics

VCC = 3.3 V or 5.0 V, 1-μF capacitor from VCC to GND, VDD-COM = 20 V, 18 V or 15 V, COM-VEE = 5 V, 8 V or 15 V, C<sub>L</sub> = 100pF, -40°C < T<sub>J</sub> < 150°C (unless otherwise noted)<sup>(1)(2)</sup>.

Parameter		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
VCC UVLO THRESHOLD AND DELAY							
V <sub>VCC_ON</sub>	VCC - GND		2.55	2.7	2.85	V	
V <sub>VCC_OFF</sub>			2.35	2.5	2.65	V	
V <sub>VCC_HYS</sub>			0.2			V	
t <sub>VCCFIL</sub>	VCC UVLO deglitch time		10			μs	
t <sub>VCC+ to OUT</sub>	VCC UVLO on delay to output high	IN+ = VCC, IN– = GND	28	37.8	50	μs	
t <sub>VCC- to OUT</sub>	VCC UVLO off delay to output low		5	10	15	μs	
t <sub>VCC+ to RDY</sub>	VCC UVLO on delay to RDY high	RST/EN = VCC	30	37.8	50	μs	
t <sub>VCC- to RDY</sub>	VCC UVLO off delay to RDY low		5	10	15	μs	
VDD UVLO THRESHOLD AND DELAY							
V <sub>VDD_ON</sub>	VDD - COM		10.5	12	12.8	V	
V <sub>VDD_OFF</sub>			9.9	10.7	11.8	V	
V <sub>VDD_HYS</sub>			0.8			V	
t <sub>VDDFIL</sub>	VDD UVLO deglitch time		5			μs	
t <sub>VDD+ to OUT</sub>	VDD UVLO on delay to output high	IN+ = VCC, IN– = GND	2	5	8	μs	
t <sub>VDD- to OUT</sub>	VDD UVLO off delay to output low		5	10	μs		
t <sub>VDD+ to RDY</sub>	VDD UVLO on delay to RDY high	RST/EN = VCC	10			15	μs
t <sub>VDD- to RDY</sub>	VDD UVLO off delay to RDY low		10			15	μs
VCC, VDD QUIESCENT CURRENT							
I <sub>VCCQ</sub>	VCC quiescent current	OUT(H) = High, f <sub>S</sub> = 0Hz, AIN=2V	2.5	3	4	mA	
		OUT(L) = Low, f <sub>S</sub> = 0Hz, AIN=2V	1.45	2	2.75	mA	
I <sub>VDDQ</sub>	VDD quiescent current	OUT(H) = High, f <sub>S</sub> = 0Hz, AIN=2V	3.6	4	5.9	mA	
		OUT(L) = Low, f <sub>S</sub> = 0Hz, AIN=2V	3.1	3.7	5.3	mA	
LOGIC INPUTS - IN+, IN- and RST/EN							
V <sub>INH</sub>	Input high threshold	VCC=3.3V	1.85			2.31	V
V <sub>INL</sub>	Input low threshold		0.99	1.52	V		
V <sub>INHYS</sub>	Input threshold hysteresis		0.33			V	
I <sub>IH</sub>	Input high level input leakage current	V <sub>IN</sub> = VCC	90			uA	
I <sub>IL</sub>	Input low level input leakage current	V <sub>IN</sub> = GND	-90			uA	
R <sub>IND</sub>	Input pins pull down resistance		55			kΩ	
R <sub>INU</sub>	Input pins pull up resistance		55			kΩ	
T <sub>INFIL</sub>	IN+, IN– and RST/EN deglitch (ON and OFF) filter time	f <sub>S</sub> = 50kHz	28	40	60	ns	
T <sub>RSTFIL</sub>	Deglitch filter time to reset FLT		500	650	800	ns	
GATE DRIVER STAGE							
I <sub>OUTH</sub>	Peak source current	C <sub>L</sub> = 0.18μF, f <sub>S</sub> = 1kHz	10			A	
I <sub>OUTL</sub>	Peak sink current		10			A	
R <sub>OUTH</sub> <sup>(3)</sup>	Output pull-up resistance	I <sub>OUTH</sub> = -0.1A	2.5			Ω	
R <sub>OUTL</sub>	Output pull-down resistance	I <sub>OUTL</sub> = 0.1A	0.3			Ω	
V <sub>OUTH</sub>	High level output voltage	I <sub>OUTH</sub> = -0.2A, VDD = 18V	17.5			V	
V <sub>OUTL</sub>	Low level output voltage	I <sub>OUTL</sub> = 0.2A	60			mV	
ACTIVE PULLDOWN							
V <sub>OUTPD</sub>	Output active pull down on OUTL	I <sub>OUTL(typ)</sub> = 0.1×I <sub>OUTL(typ)</sub> , VDD=OPEN, VEE=COM	1.5	2.0	2.5	V	

## 6.8 Electrical Characteristics (continued)

VCC = 3.3 V or 5.0 V, 1-μF capacitor from VCC to GND, VDD–COM = 20 V, 18 V or 15 V, COM–VEE = 5 V, 8 V or 15 V, C<sub>L</sub> = 100pF, –40°C < T<sub>J</sub> < 150°C (unless otherwise noted)<sup>(1)(2)</sup>.

Parameter	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INTERNAL ACTIVE MILLER CLAMP						
V <sub>CLMPH</sub>	Miller clamp threshold voltage	Reference to VEE	1.5	2.0	2.5	V
V <sub>CLMPI</sub>	Output low clamp voltage	I <sub>CLMPI</sub> = 1 A	VEE + 0.5			V
I <sub>CLMPI</sub>	Output low clamp current	V <sub>CLMPI</sub> = 0V, VEE = –2.5V	4.0			A
R <sub>CLMPI</sub>	Miller clamp pull down resistance	I <sub>CLMPI</sub> = 0.2A	0.6			Ω
t <sub>DCLMPI</sub>	Miller clamp ON delay time	C <sub>L</sub> = 1.8nF	15      50			ns
SHORT CIRCUIT CLAMPING						
V <sub>CLP-OUT(H)</sub>	V <sub>OUTH</sub> –VDD	OUT = High, I <sub>OUT(H)</sub> = 500mA, t <sub>CLP</sub> =10μs	0.9			V
V <sub>CLP-OUT(L)</sub>	V <sub>OUTL</sub> –VDD	OUT = High, I <sub>OUT(L)</sub> = 500mA, t <sub>CLP</sub> =10μs	1.8			V
V <sub>CLP-CLMPI</sub>	V <sub>CLMPI</sub> –VDD	OUT = High, I <sub>CLMPI</sub> = 20mA, t <sub>CLP</sub> =10μs	1.0			V
DESAT PROTECTION						
I <sub>CHG</sub>	Blanking capacitor charge current	V <sub>DESAT</sub> = 2.0V	430	500	570	μA
I <sub>DCHG</sub>	Blanking capacitor discharge current	V <sub>DESAT</sub> = 6.0V	10.0	15.0		mA
V <sub>DESAT</sub>	Detection threshold		4.6	5	5.47	V
t <sub>DESATLEB</sub>	Leading edge blank time		150	200	450	ns
t <sub>DESATFIL</sub>	DESAT deglitch filter		50	140	230	ns
t <sub>DESATOFF</sub>	DESAT propagation delay to OUTL 90%		150	200	300	ns
t <sub>DESATFLT</sub>	DESAT to $\overline{\text{FLT}}$ low delay		400	580	750	ns
INTERNAL SOFT TURN OFF						
I <sub>STO</sub>	Soft turn-off current on fault condition	VDD-VEE = 20 V, OUTL = 8 V	250	400	570	mA
ISOLATED TEMPERATURE SENSE AND MONITOR (AIN–APWM)						
V <sub>AIN</sub>	Analog sensing voltage range		0.6		4.5	V
I <sub>AIN</sub>	Internal current source	V <sub>AIN</sub> =2.5V, -40°C< T <sub>J</sub> < 150°C	196	203	209	uA
f <sub>APWM</sub>	APWM output frequency	V <sub>AIN</sub> =2.5V	380	400	420	kHz
BW <sub>AIN</sub>	AIN-APWM Bandwidth		10			kHz
D <sub>APWM</sub>	APWM Duty Cycle	V <sub>AIN</sub> =0.6V	86.5	88	89.5	%
		V <sub>AIN</sub> =2.5V	48.5	50	51.5	%
		V <sub>AIN</sub> =4.5V	7.5	10	11.5	%
FLT AND RDY REPORTING						
t <sub>RDYHLD</sub>	VDD UVLO RDY low minimum holding time		0.55		1	ms
t <sub>FLTMUTE</sub>	Output mute time on fault	Reset fault through $\overline{\text{RST}}$ /EN	0.55		1	ms
R <sub>ODON</sub>	Open drain output on resistance	I <sub>ODON</sub> = 5mA	30			Ω
V <sub>ODL</sub>	Open drain low output voltage		0.3			V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode transient immunity		150			V/ns

- (1) Currents are positive into and negative out of the specified terminal.
- (2) All voltages are referenced to COM unless otherwise notified.
- (3) For internal PMOS only. Refer to Driver Stage for effective pull-up resistance.



## 6.9 Switching Characteristics

VCC = 5.0 V, 1-μF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 3 V, 5 V or 8 V, C<sub>L</sub> = 100pF, -40°C < T<sub>J</sub> < 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PDLH</sub>	Propagation delay time low-to-high		60	90	130	ns
t <sub>PDHL</sub>	Propagation delay time low-to-high		60	90	130	ns
PWD	Pulse width distortion (t <sub>PDHL</sub> - t <sub>PDLH</sub> )				30	ns
t <sub>sk-pp</sub>	Part to part skew	Rising or falling propagation delay			30	ns
t <sub>r</sub>	Driver output rise time	C <sub>L</sub> = 10nF		33		ns
t <sub>f</sub>	Driver output fall time	C <sub>L</sub> = 10nF		27		ns
f <sub>MAX</sub>	Maximum switching frequency				1	MHz

## 6.10 Insulation Characteristics Curves

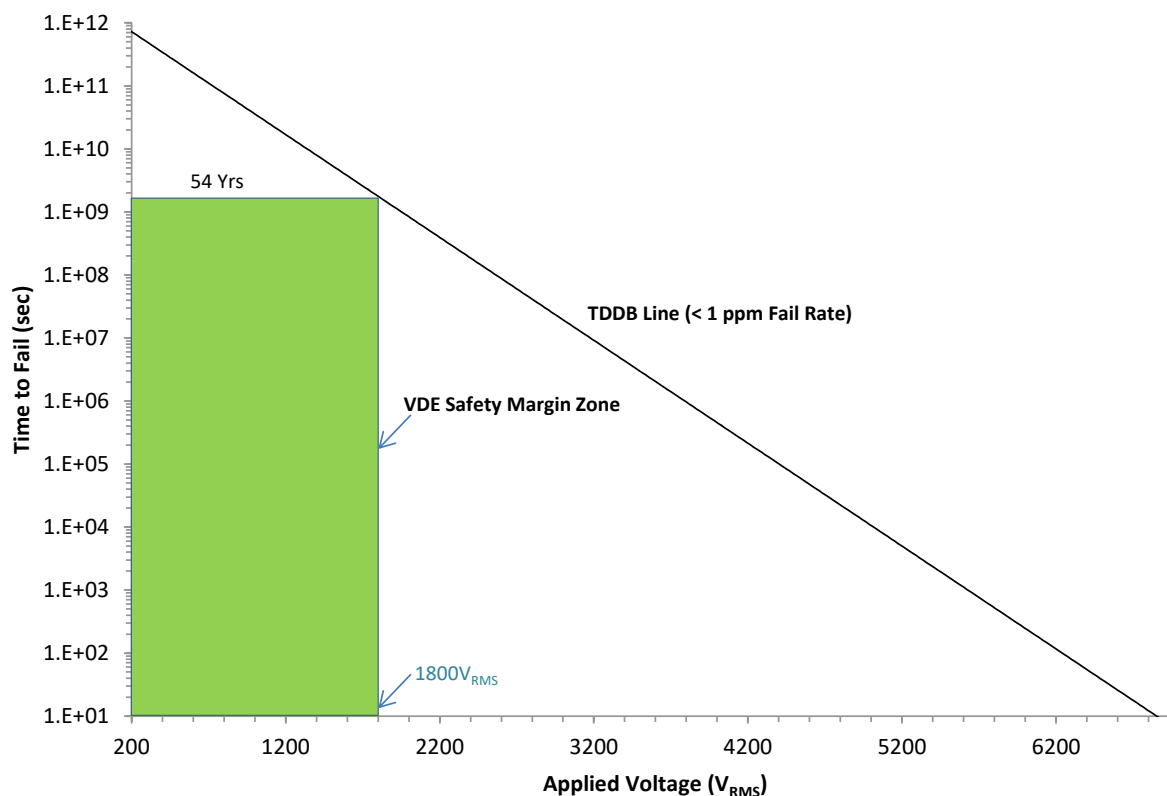


Figure 6-1. Reinforced Isolation Capacitor Life Time Projection

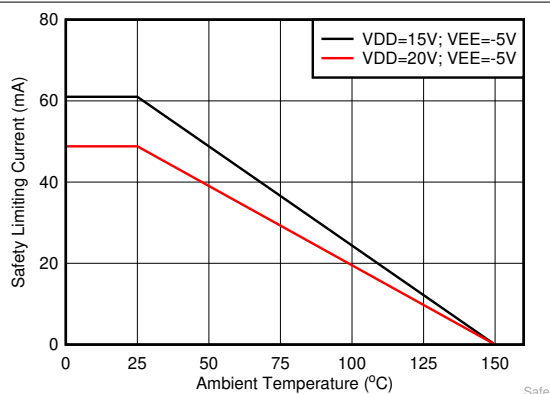


Figure 6-2. Thermal Derating Curve for Limiting Current per VDE

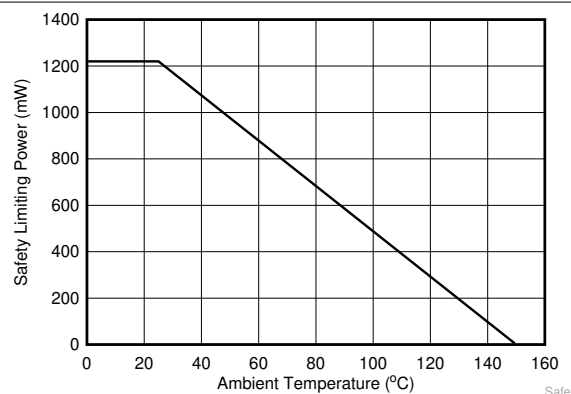


Figure 6-3. Thermal Derating Curve for Limiting Power per VDE

## 6.11 Typical Characteristics

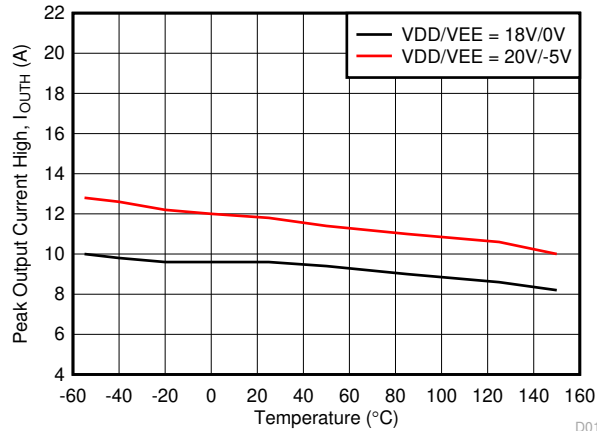


Figure 6-4. Output High Drive Current vs Temperature

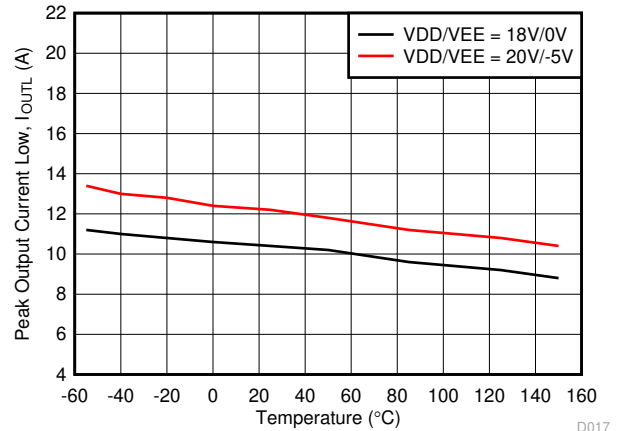


Figure 6-5. Output Low Driver Current vs Temperature

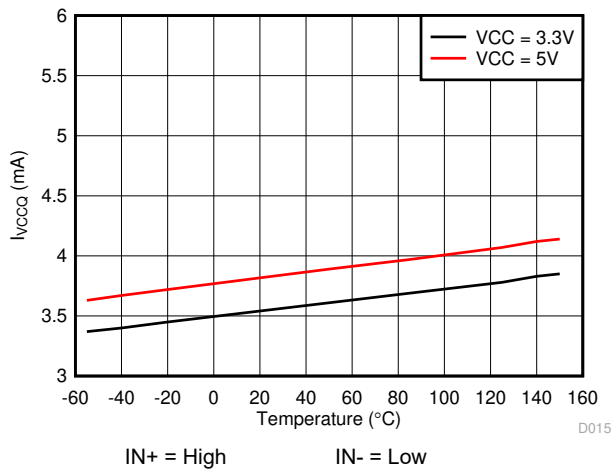


Figure 6-6. I\_VCCQ Supply Current vs Temperature

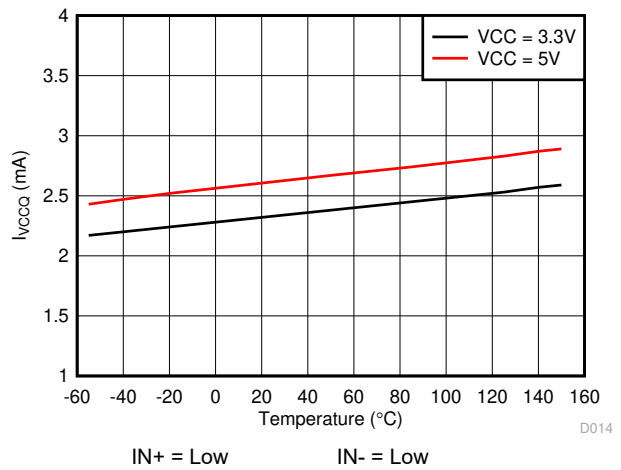


Figure 6-7. I\_VCCQ Supply Current vs Temperature

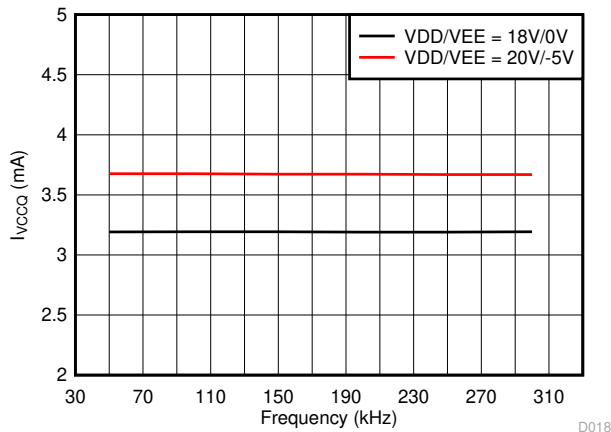


Figure 6-8. I\_VCCQ Supply Current vs Input Frequency

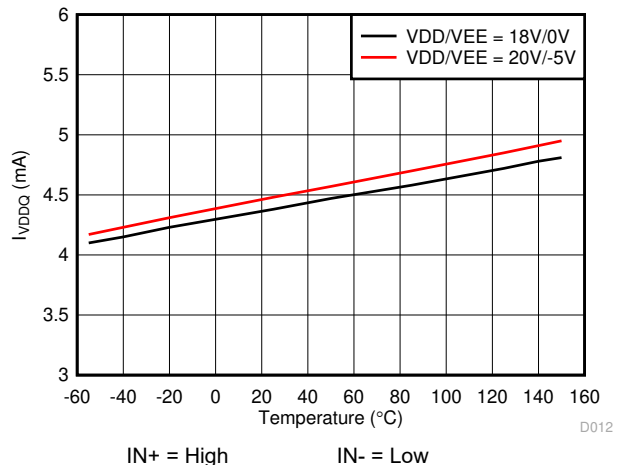


Figure 6-9. I\_VDDQ Supply Current vs Temperature

## 6.11 Typical Characteristics (continued)

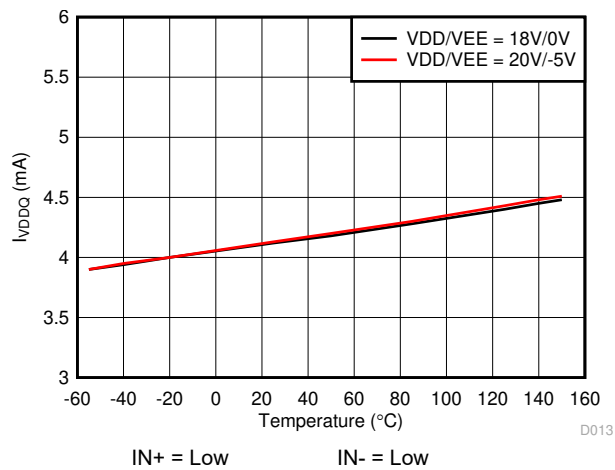


Figure 6-10.  $I_{VDDQ}$  Supply Current vs Temperature

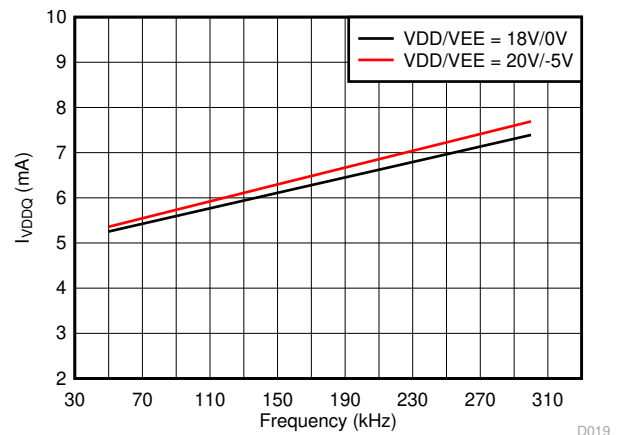


Figure 6-11.  $I_{VDDQ}$  Supply Current vs Input Frequency

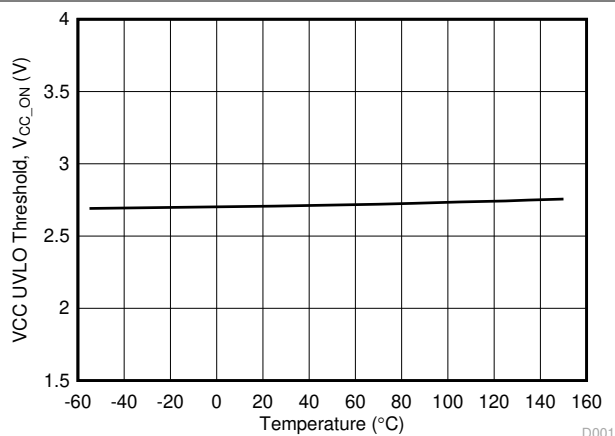


Figure 6-12. VCC UVLO vs Temperature

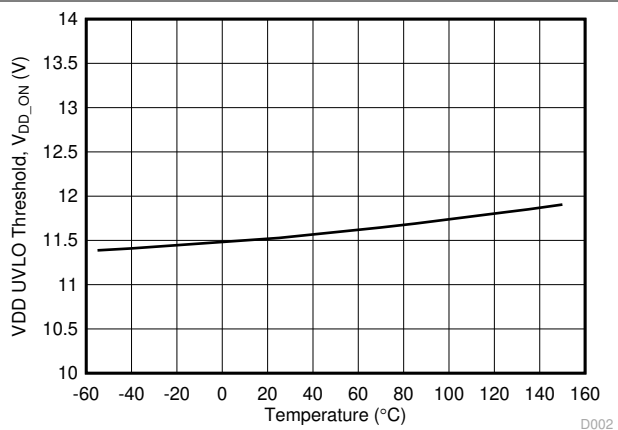


Figure 6-13. VDD UVLO vs Temperature

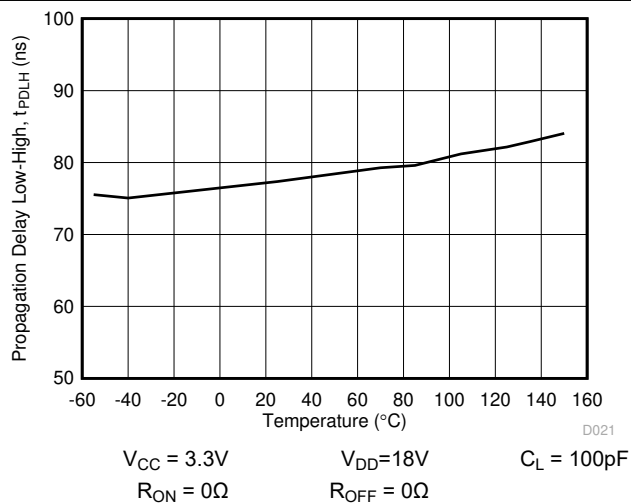


Figure 6-14. Propagation Delay  $t_{PDLH}$  vs Temperature

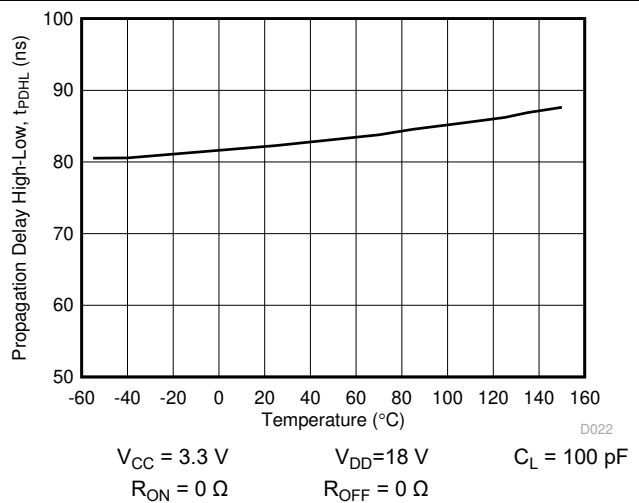


Figure 6-15. Propagation Delay  $t_{PDHL}$  vs Temperature

## 6.11 Typical Characteristics (continued)

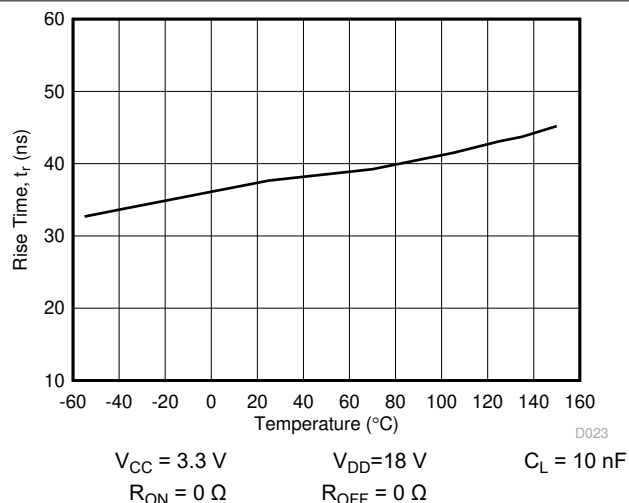


Figure 6-16.  $t_r$  Rise Time vs Temperature

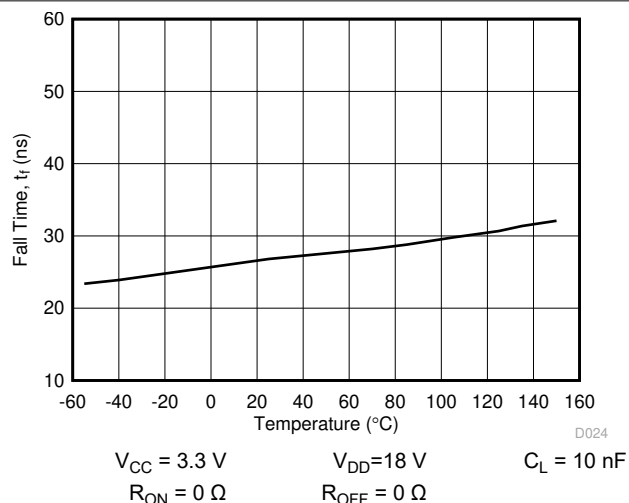


Figure 6-17.  $t_f$  Fall Time vs Temperature

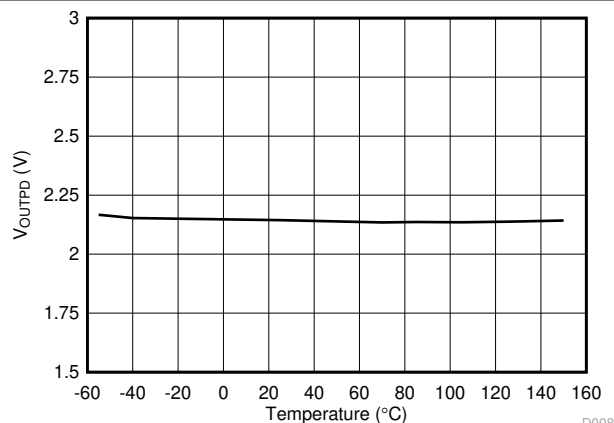


Figure 6-18.  $V_{OUTPD}$  Output Active Pulldown Voltage vs Temperature

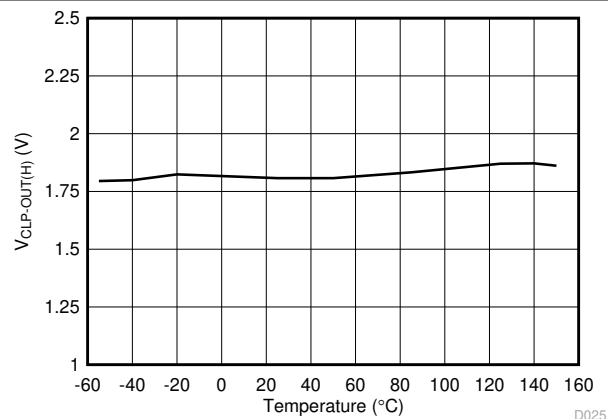


Figure 6-19.  $V_{CLP-OUT(H)}$  Short Circuit Clamping Voltage vs Temperature

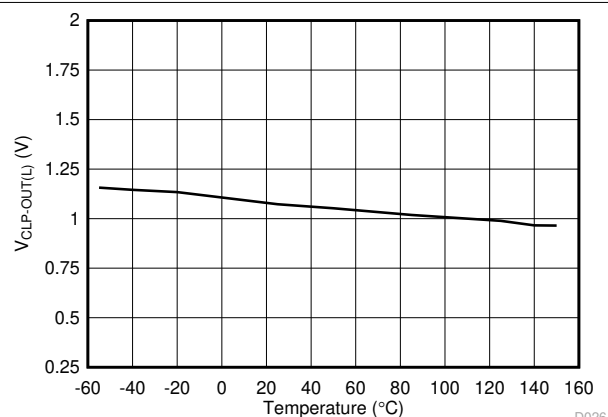


Figure 6-20.  $V_{CLP-OUT(L)}$  Short Circuit Clamping Voltage vs Temperature

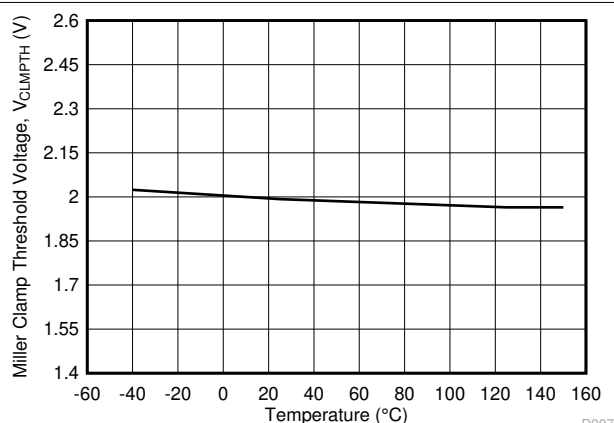


Figure 6-21.  $V_{CLMPH}$  Miller Clamp Threshold Voltage vs Temperature

## 6.11 Typical Characteristics (continued)

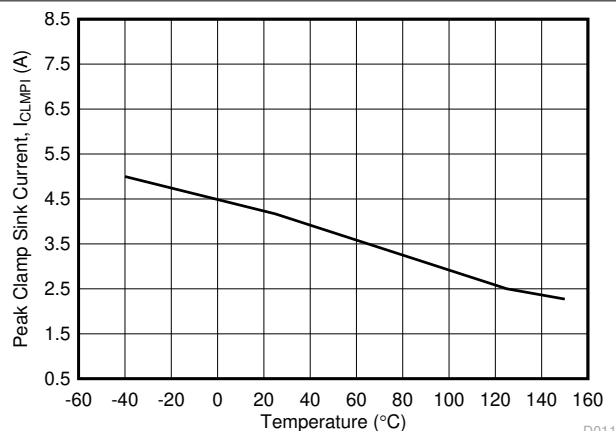


Figure 6-22.  $I_{CLMPI}$  Miller Clamp Sink Current vs Temperature

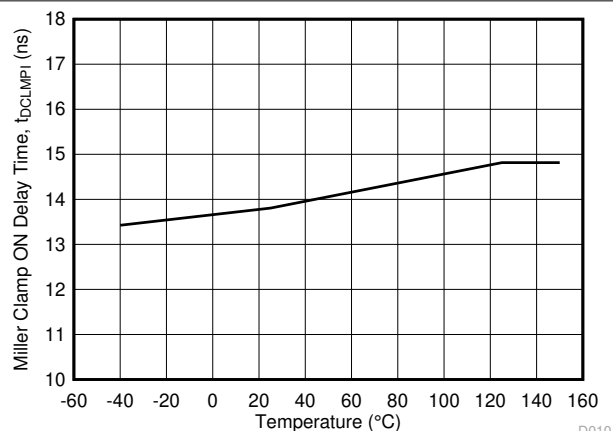


Figure 6-23.  $t_{DCLMPI}$  Miller Clamp ON Delay Time vs Temperature

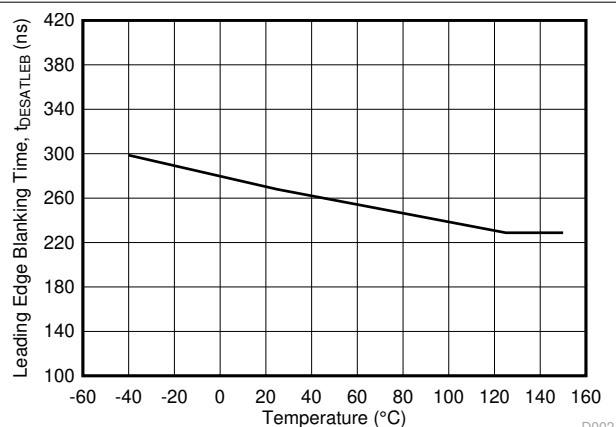


Figure 6-24.  $t_{DESATLEB}$  DESAT Leading Edge Blanking Time vs Temperature

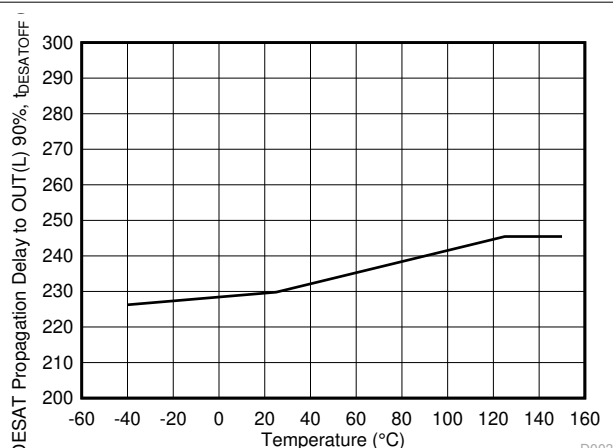


Figure 6-25.  $t_{DESATOFF}$  DESAT Propagation Delay to OUT(L) 90% vs Temperature

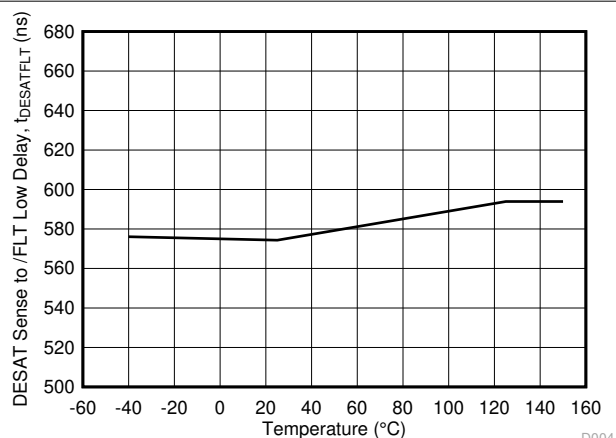


Figure 6-26.  $t_{DESATFLT}$  DESAT Sense to /FLT Low Delay Time vs Temperature

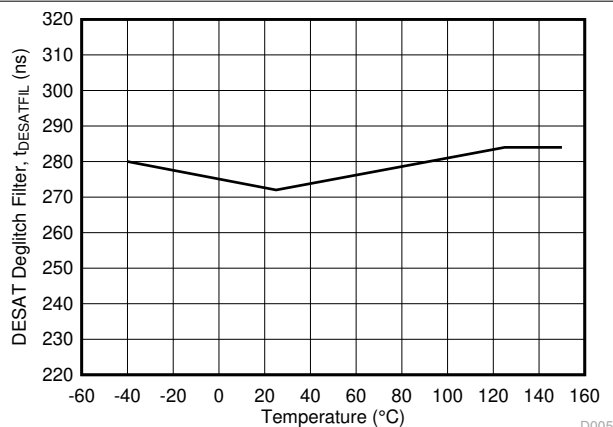


Figure 6-27.  $t_{DESATFIL}$  DESAT Deglitch Filter vs Temperature

## 6.11 Typical Characteristics (continued)

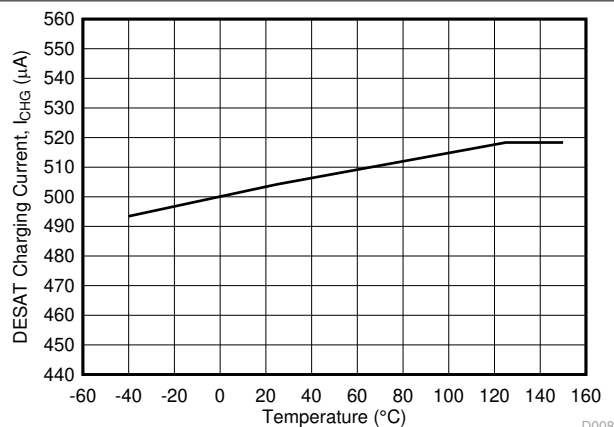


Figure 6-28.  $I_{CHG}$  DESAT Charging Current vs Temperature

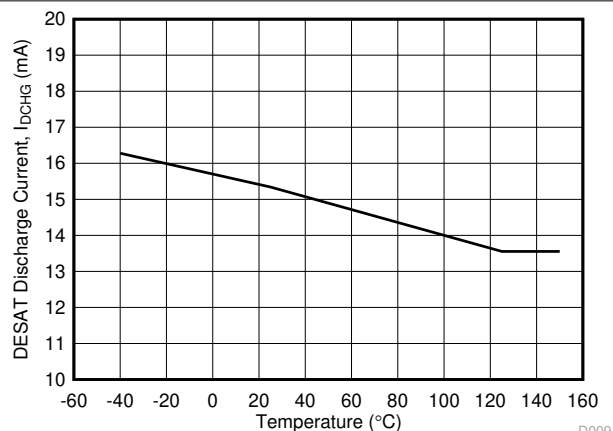


Figure 6-29.  $I_{DCHG}$  DESAT Discharge Current vs Temperature

## 7 Parameter Measurement Information

### 7.1 Propagation Delay

#### 7.1.1 Non-Inverting and Inverting Propagation Delay

Figure 7-1 shows the propagation delay measurement for non-inverting configurations. Figure 7-2 shows the propagation delay measurement with the inverting configurations.

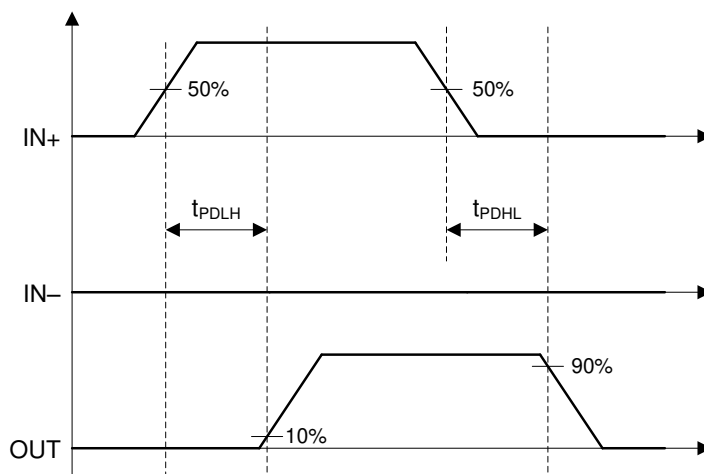


Figure 7-1. Non-Inverting Logic Propagation Delay Measurement

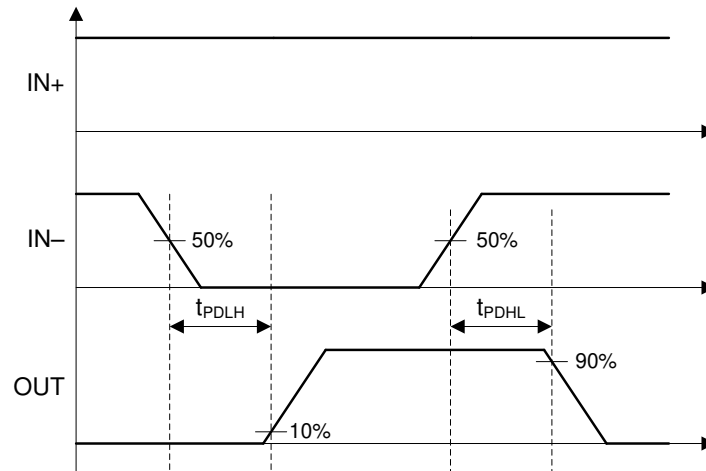


Figure 7-2. Inverting Logic Propagation Delay Measurement

## 7.2 Input Deglitch Filter

To increase the robustness of gate driver over noise transient and accidental small pulses on the input pins, for example, IN+, IN-,  $\overline{\text{RST/EN}}$ , a 40-ns deglitch filter filters out the transients and ensures there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN- PWM pulse is smaller than the input deglitch filter width,  $T_{\text{INFIL}}$ , there are no responses on the OUT drive signal. Figure 7-3 and Figure 7-4 show the IN+ pin ON and OFF pulse deglitch filter effect. Figure 7-5 and Figure 7-6 show the IN- pin ON and OFF pulse deglitch filter effect.

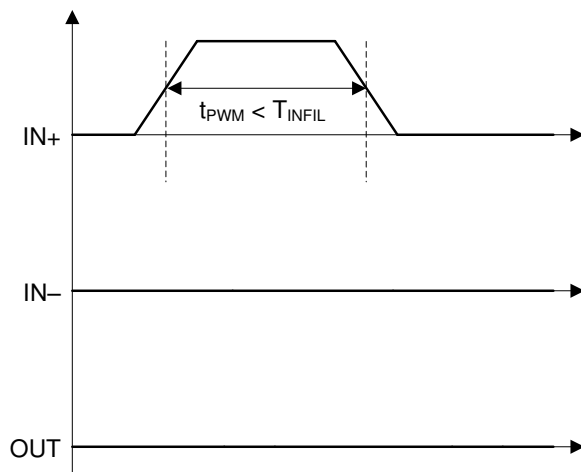


Figure 7-3. IN+ ON Deglitch Filter

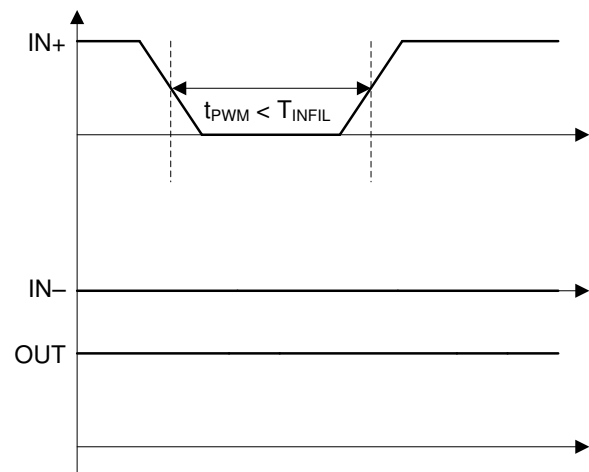
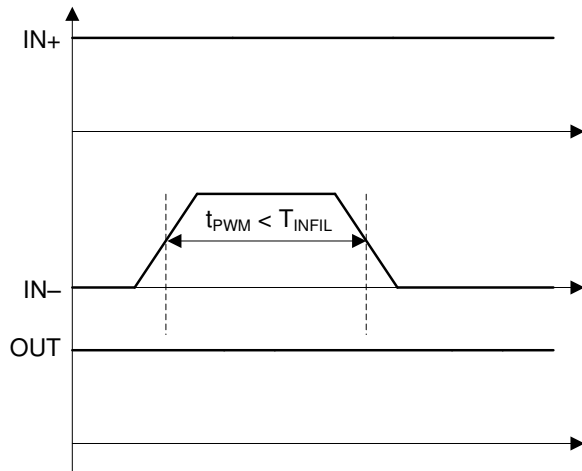
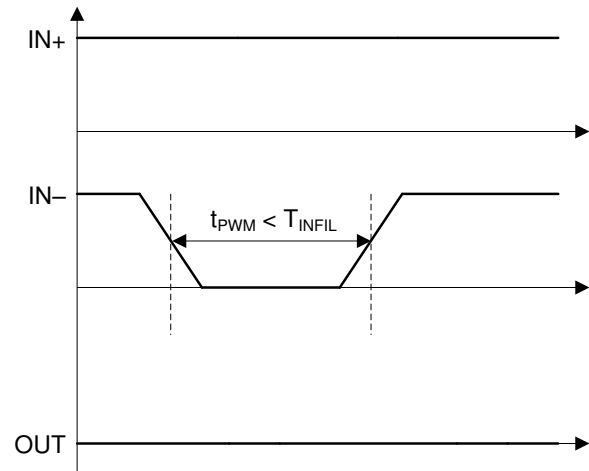


Figure 7-4. IN+ OFF Deglitch Filter





**Figure 7-5. IN- ON Deglitch Filter**

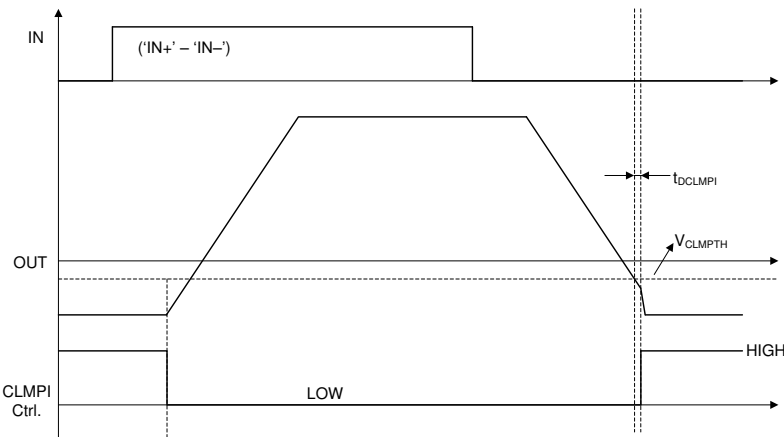


**Figure 7-6. IN- OFF Deglitch Filter**

## 7.3 Active Miller Clamp

### 7.3.1 Internal On-Chip Active Miller Clamp

For a gate driver application with a unipolar bias supply or a bipolar supply with a small negative turn-off voltage, an active Miller clamp can help add a additional low impedance path to bypass the Miller current and prevent the high dV/dt introduced unintentional turn-on through the Miller capacitance. [Figure 7-7](#) shows the timing diagram for an on-chip internal Miller clamp function.



**Figure 7-7. Timing Diagram for Internal Active Miller Clamp Function**

## 7.4 Undervoltage Lockout (UVLO)

Undervoltage lockout (UVLO) is one of the key protection features designed to protect the system in case of bias supply failures on VCC, primary side power supply, and VDD, secondary side power supply.

### 7.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. [Figure 7-8](#) shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN-APWM.

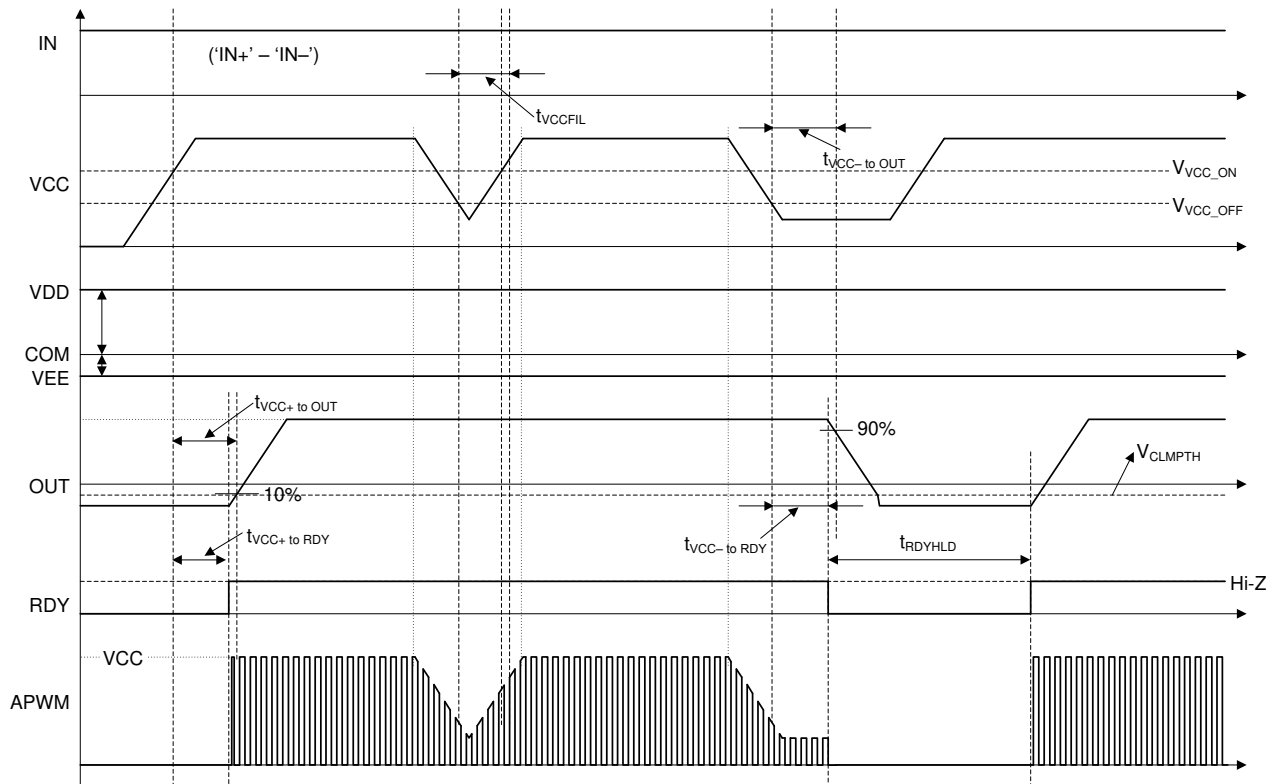
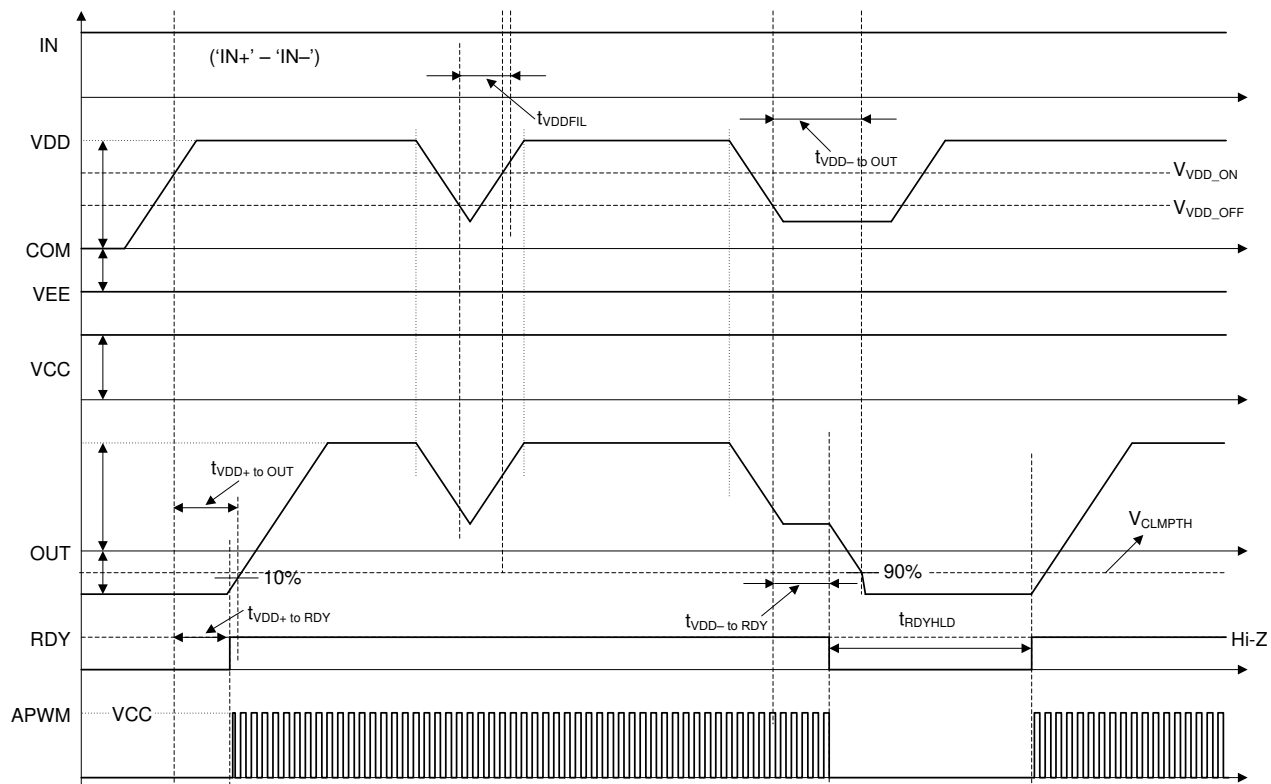


Figure 7-8. VCC UVLO Protection Timing Diagram

### 7.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. [Figure 7-9](#) shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.



**Figure 7-9. VDD UVLO Protection Timing Diagram**

## 7.5 Desaturation (DESAT) Protection

### 7.5.1 DESAT Protection with Soft Turn-OFF

DESAT function is used to detect  $V_{DS}$  for SiC-MOSFETs or  $V_{CE}$  for IGBTs under overcurrent conditions. [Figure 7-10](#) shows the timing diagram of DESAT operation with soft turn-off during the turning on transition.

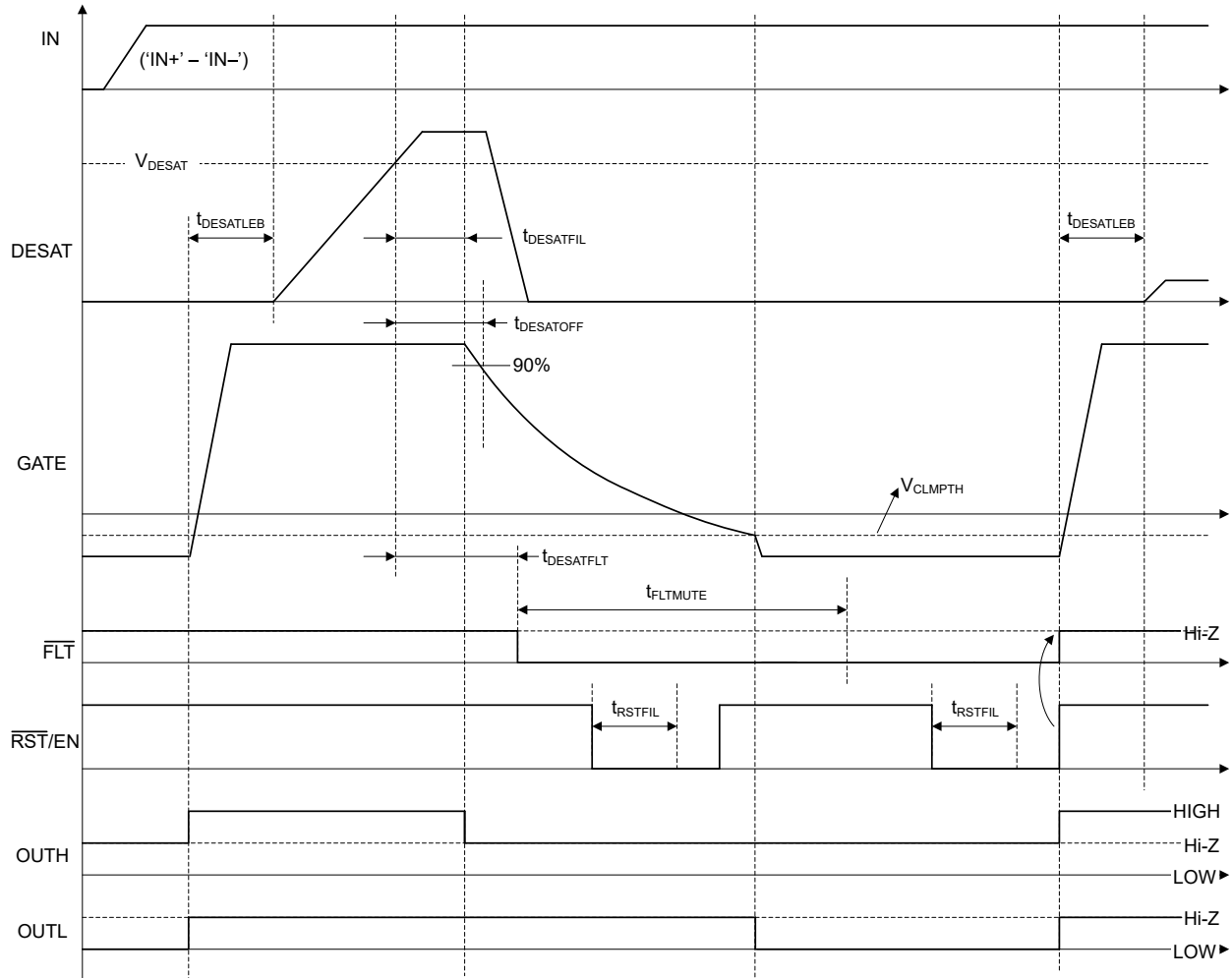
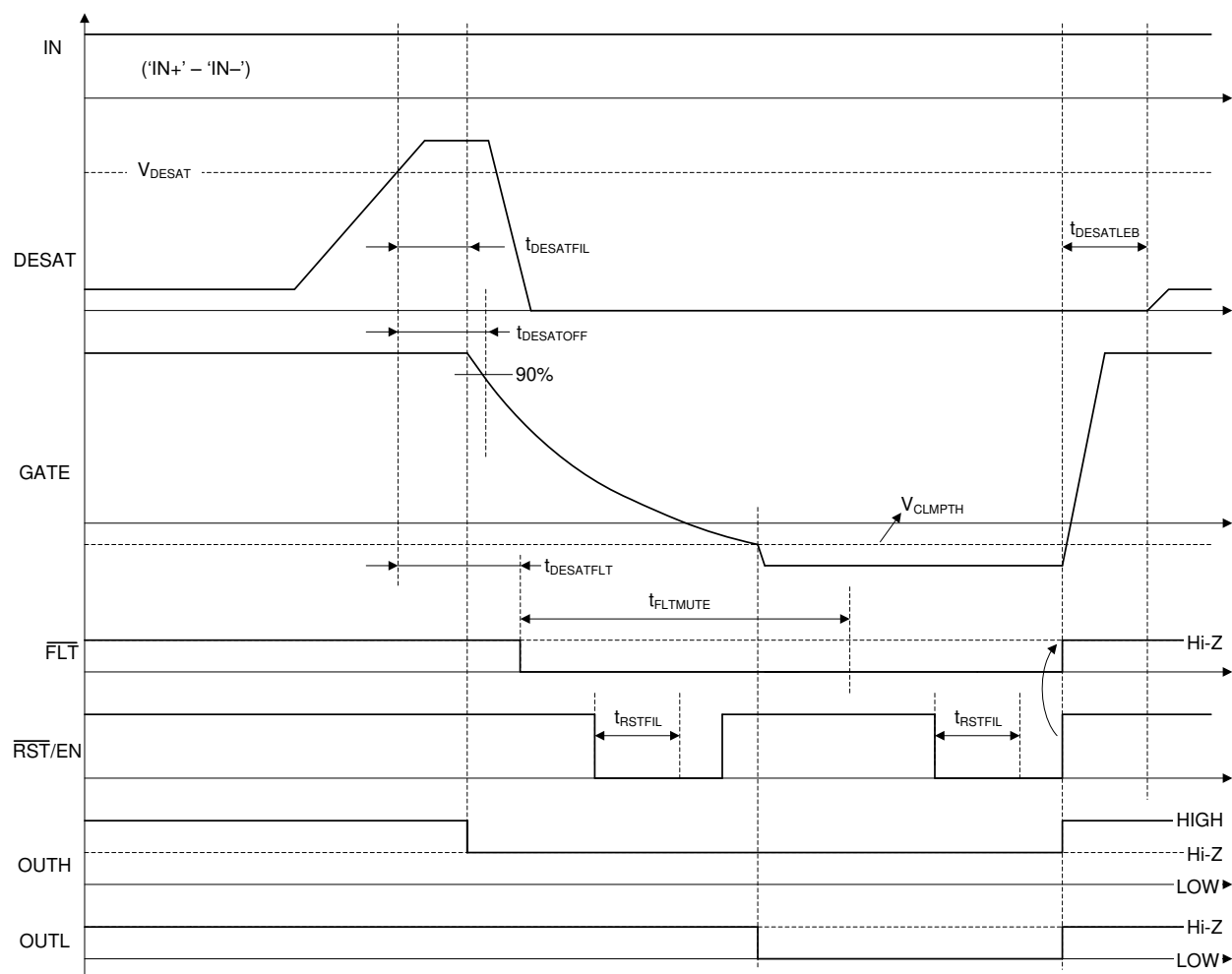


Figure 7-10. DESAT Protection with Soft Turn-OFF During Turn-ON Transition

Figure 7-11 shows the timing diagram of DESAT protection while the power device is already turned on.



**Figure 7-11. DESAT Protection with Soft Turn-OFF While Power Device is ON**

## 8 Detailed Description

### 8.1 Overview

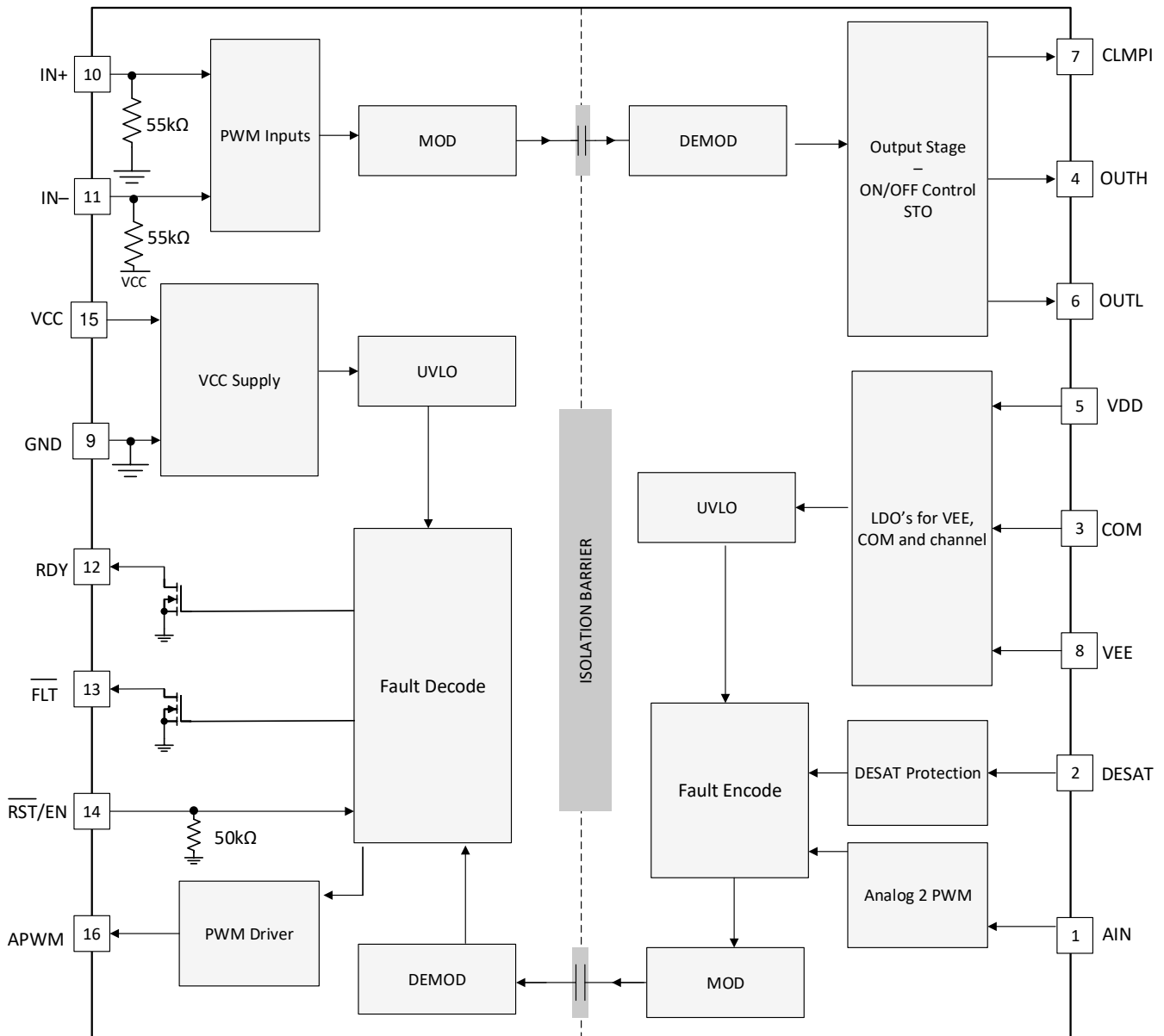
The device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 2121-V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10-kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, etc. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable reinforced isolation between the low voltage DSP/MCU and high voltage side.

The  $\pm 10\text{A}$  peak sink and source current of the device can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The input side is isolated with the output side with a reinforced isolation barrier based on capacitive isolation technology. The device can support up to  $1.5\text{-kV}_{\text{RMS}}$  working voltage,  $12.8\text{-kV}_{\text{PK}}$  surge immunity with longer than 40 years isolation barrier life. The strong drive strength helps to switch the device fast and reduce the switching loss, while the  $150\text{V/ns}$  minimum CMTI guarantees the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12V output side power supply UVLO is suitable for switches with gate voltage  $\geq 15\text{ V}$ . The active Miller clamp feature prevents the false turn on causing by Miller capacitance during fast switching. The device has the state-of-art DESAT detection time, and fault reporting function to the low voltage side DSP/MCU. The soft turn off is triggered when the DESAT fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The isolated analog to PWM sensor can be used as switch temperature sensing, DC bus voltage sensing, auxiliary power supply sensing, and so on. The PWM signal can be fed directly to DSP/MCU or through a low-pass filter as an analog signal.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3 V to 5.5 V. The device supports both unipolar and bipolar power supply on the output side, with a wide range from 13 V to 33 V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed.

### 8.3.2 Driver Stage

The device has  $\pm 10$ -A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. The device can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10 A. The driver features an important safety function wherein, when the input pins are in floating condition, the OUTH/OUTL is held in

LOW state. The split output of the driver stage is depicted in Figure 8-1. The driver has rail-to-rail output by implementing a hybrid pull-up structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pull-up NMOS is the same as the pull down NMOS, so the on resistance  $R_{NMOS}$  is the same as  $R_{OL}$ . The hybrid pull-up structure delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power semiconductor turn-on transient. The  $R_{OH}$  in Figure 8-1 represents the on-resistance of the pull-up P-Channel MOSFET. However, the effective pull-up resistance is much smaller than  $R_{OH}$ . Because the pullup N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pullup N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3 V below VDD voltage. The effective resistance of the hybrid pullup structure during this period is about  $2 \times R_{OL}$ . Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pulldown impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

The pulldown structure of the driver stage is implemented solely by a pulldown N-Channel MOSFET. This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pulldown impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the Miller effect.

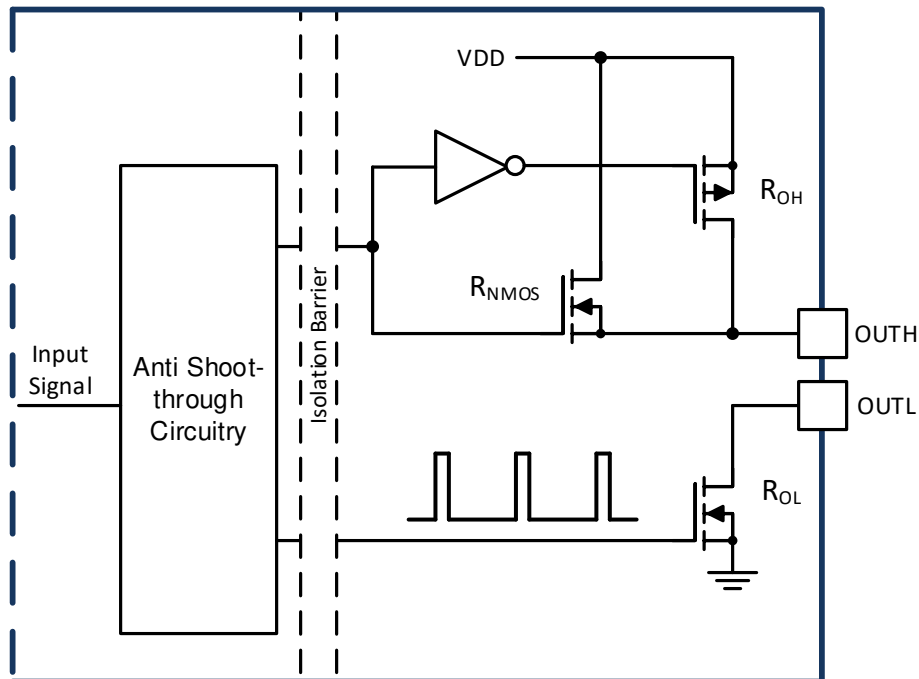


Figure 8-1. Gate Driver Output Stage

### 8.3.3 VCC and VDD Undervoltage Lockout (UVLO)

The device implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. The device implements 12-V threshold voltage of VDD UVLO, with 800-mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn on and turn off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in sudden voltage drop of the power supply. With

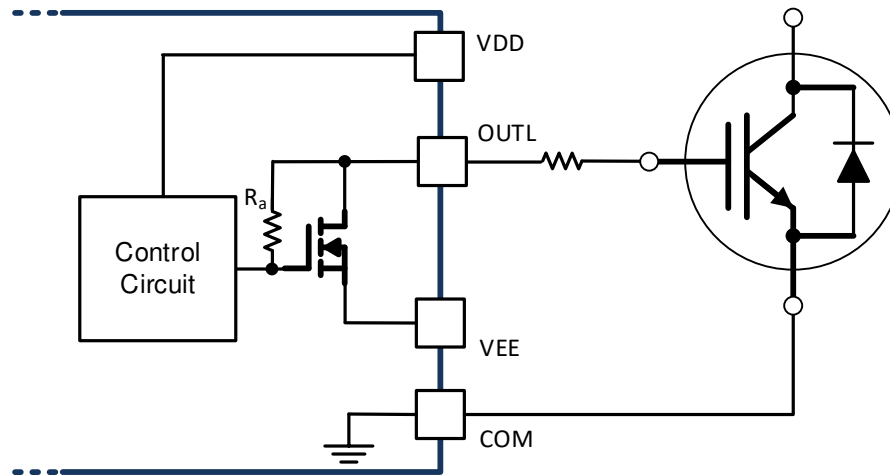


hysteresis and UVLO deglitch filter, the internal UVLO protection block will ignore small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC and VDD are shown in [Figure 7-8](#), and [Figure 7-9](#). The RDY pin on the input side is used to indicate the power good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good. The AIN-APWM function stops working during the UVLO status. The APWM pin on the input side will be held LOW.

### 8.3.4 Active Pulldown

The device implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output be false turned on before the device is back to control.



**Figure 8-2. Active Pulldown**

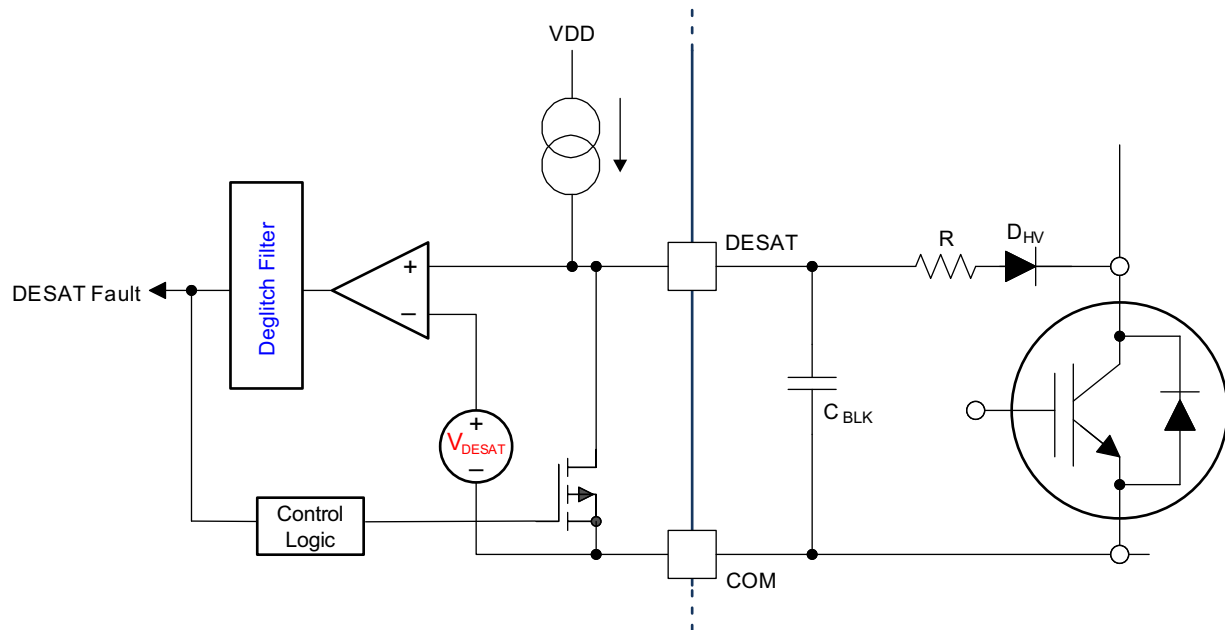
### 8.3.5 Short Circuit Clamping

During short circuit condition, the Miller capacitance can cause a current sinking to the OUTH/OUTL/CLMPI pin due to the high  $dV/dt$  and boost the OUTH/OUTL/CLMPI voltage. The short circuit clamping feature of the device can clamp the OUTH/OUTL/CLMPI pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL/CLMPI to VDD.



### 8.3.7 Desaturation (DESAT) Protection

The UCC21755-Q1 implements a fast overcurrent and short circuit protection feature to protect the IGBT module from catastrophic breakdown during fault. The DESAT pin has a typical 5V threshold with respect to COM, the source or emitter of the power semiconductor. When the input is in a floating condition or the output is held in low state, the DESAT pin is pulled down by an internal MOSFET and held in the LOW state, which prevents the overcurrent and short circuit fault from false triggering. The internal current source of the DESAT pin is activated only during the driver ON state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in the ON state. The internal pulldown MOSFET helps to discharge the voltage of the DESAT pin when the power semiconductor is turned off. The UCC21755-Q1 features a 200-ns internal leading edge blanking time after the OUTH switches to high state. The internal current source is activated to charge the external blanking capacitor after the internal leading edge blanking time. The typical value of the internal current source is 500  $\mu$ A.



**Figure 8-5. DESAT Protection**

### 8.3.8 Soft Turn-Off

The device initiates a soft turn-off when the overcurrent and short circuit protection are triggered. When the overcurrent and short circuit faults occur, the IGBT transits from the active region to the desaturation region very quickly. The channel current is controlled by the gate voltage and decreases softly; thus, the overshoot of the IGBT is limited and prevents the overvoltage breakdown. There is a tradeoff between the overshoot voltage and short circuit energy. The turn-off speed should be slow to limit the overshoot-voltage, but the shutdown time should not be too long that the large energy dissipation can breakdown the device. The 400-mA soft turn-off current of the device ensures the power switches are safely turned off during short circuit events. [Figure 7-10](#) shows the soft turn-off timing diagram.

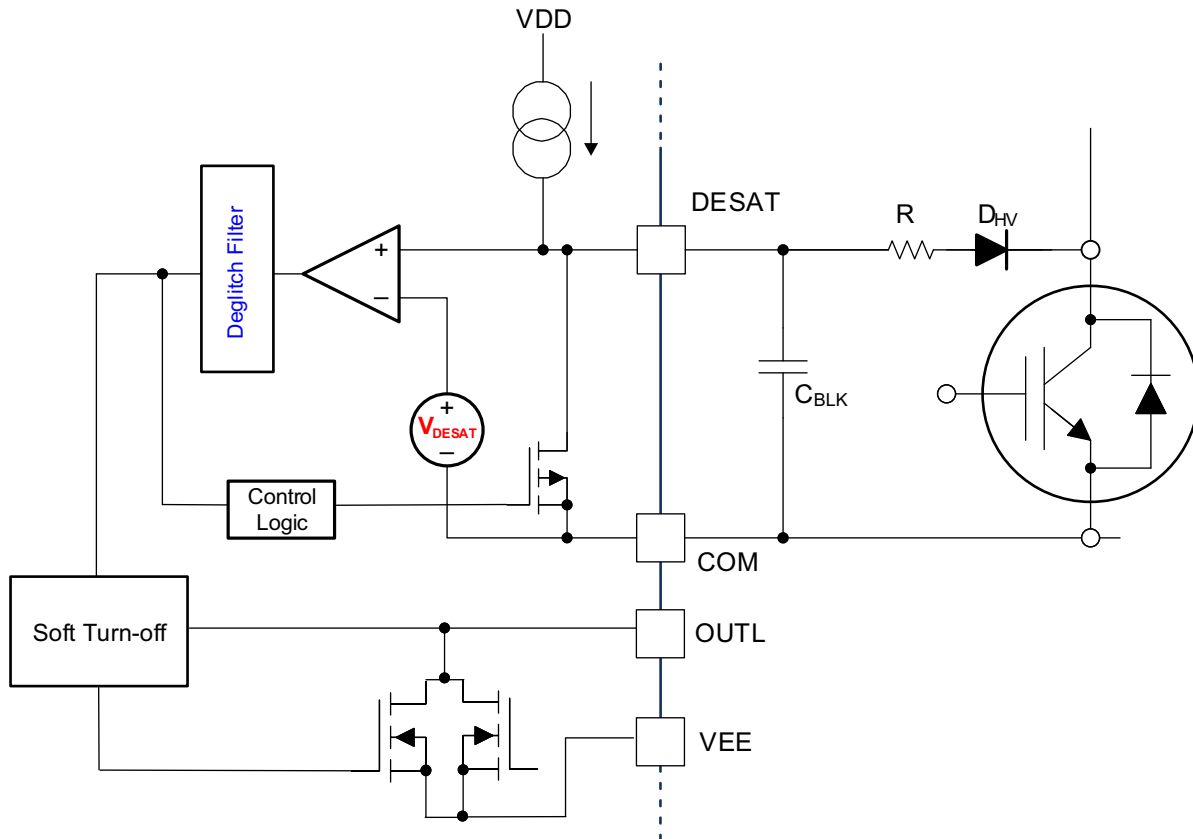


Figure 8-6. Soft Turn-Off

### 8.3.9 Fault ( $\overline{\text{FLT}}$ ), Reset and Enable ( $\overline{\text{RST/EN}}$ )

The  $\overline{\text{FLT}}$  pin of UCC21755-Q1 is open drain and can report a fault signal to the DSP/MCU when the fault is detected through the DESAT pin. The  $\overline{\text{FLT}}$  pin is pulled down to GND after the fault is detected, and is held low until a reset signal is received from  $\overline{\text{RST/EN}}$ . The device has a fault mute time  $t_{\text{FLTMUTE}}$ , within which the device ignores any reset signal.

The  $\overline{\text{RST/EN}}$  is pulled down internally by a 50-k $\Omega$  resistor, and is thus disabled by default when this pin is floating. It must be pulled up externally to enable the driver. The pin has two purposes:

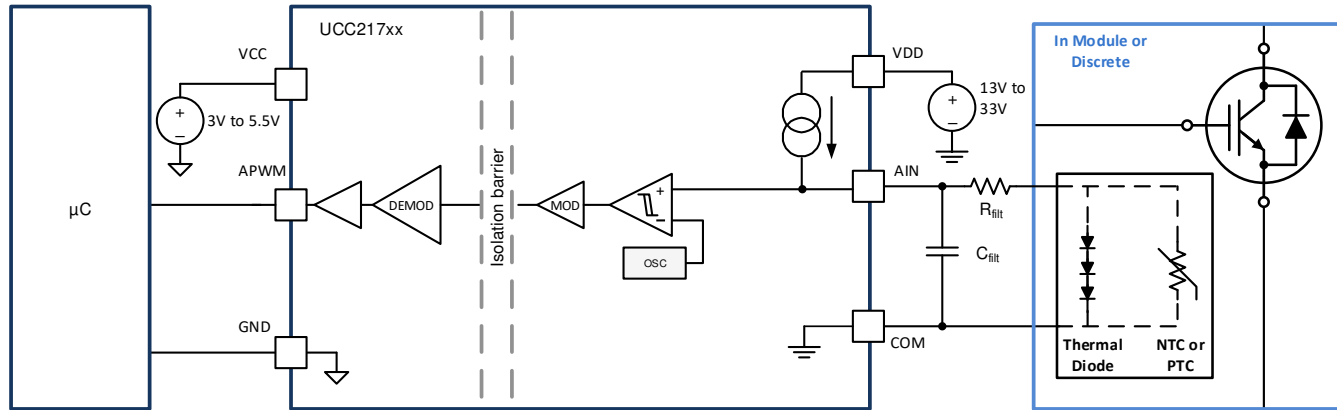
- To reset the  $\overline{\text{FLT}}$  pin. If the  $\overline{\text{RST/EN}}$  pin is pulled low for more than  $t_{\text{RSTFIL}}$  after the mute time  $t_{\text{FLTMUTE}}$ , then the fault signal is reset and  $\overline{\text{FLT}}$  returns to a high impedance state upon the next rising edge applied to the  $\overline{\text{RST/EN}}$  pin.
- To enable and shut down the device. If the  $\overline{\text{RST/EN}}$  pin is pulled low for longer than  $t_{\text{RSTFIL}}$ , the driver is disabled and OUTL is activated to pull down the gate of the IGBT or SiC MOSFET. The pin must be pulled up externally to enable the part; otherwise, the device is disabled by default.

### 8.3.10 Isolated Analog to PWM Signal Function

The device features an isolated analog to PWM signal function from AIN to APWM pin, which allows the isolated temperature sensing, high voltage dc bus voltage sensing, etc. An internal current source  $I_{\text{AIN}}$  in AIN pin is implemented in the device to bias an external thermal diode or temperature sensing resistor. The device encodes the voltage signal  $V_{\text{AIN}}$  to a PWM signal, passing through the reinforced isolation barrier, and output to APWM pin on the input side. The PWM signal can either be transferred directly to DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The AIN voltage input range is from 0.6 V to 4.5 V, and the corresponding duty cycle of the APWM output ranges from 88% to 10%. The duty cycle increases linearly from 10% to 88% while the AIN voltage decreases from 4.5 V to 0.6 V. This corresponds to the temperature coefficient of the negative temperature coefficient (NTC) resistor and thermal diode. When AIN is floating, the AIN voltage is 5 V and the APWM operates at 400 kHz with approximately 10% duty cycle.

The accuracy of the duty cycle is  $\pm 3\%$  across temperature without one time calibration. The accuracy can be improved using calibration. The accuracy of the internal current source  $I_{AIN}$  is  $\pm 3\%$  across temperature.

The isolated analog to PWM signal feature can also support other analog signal sensing, such as the high voltage DC bus voltage, and so on. The internal current source  $I_{AIN}$  should be taken into account when designing the potential divider if sensing a high voltage.



**Figure 8-7. Isolated Analog to PWM Signal**

## 8.4 Device Functional Modes

Table 8-1 lists the device function.

**Table 8-1. Function Table**

INPUT							OUTPUT				
VCC	VDD	VEE	IN+	IN-	RST/EN	AIN	RDY	FLT	OUTH/OUTL	CLMPI	APWM
PU	PD	PU	X	X	X	X	Low	HiZ	Low	Low	Low
PD	PU	PU	X	X	X	X	Low	HiZ	Low	Low	Low
PU	PU	PU	X	X	Low	X	HiZ	HiZ	Low	Low	Low
PU	Open	PU	X	X	X	X	Low	HiZ	HiZ	HiZ	HiZ
PU	PU	Open	X	X	X	X	Low	HiZ	Low	Low	Low
PU	PU	PU	Low	X	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	X	High	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	High	High	High	X	HiZ	HiZ	Low	Low	P*
PU	PU	PU	High	Low	High	X	HiZ	HiZ	High	HiZ	P*

PU: Power Up ( $V_{CC} \geq 2.85$  V,  $V_{DD} \geq 13.1$  V,  $V_{EE} \leq 0$  V); PD: Power Down ( $V_{CC} \leq 2.35$  V,  $V_{DD} \leq 9.9$  V); X: Irrelevant; P\*: PWM Pulse; HiZ: High Impedance

## 9 Applications and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

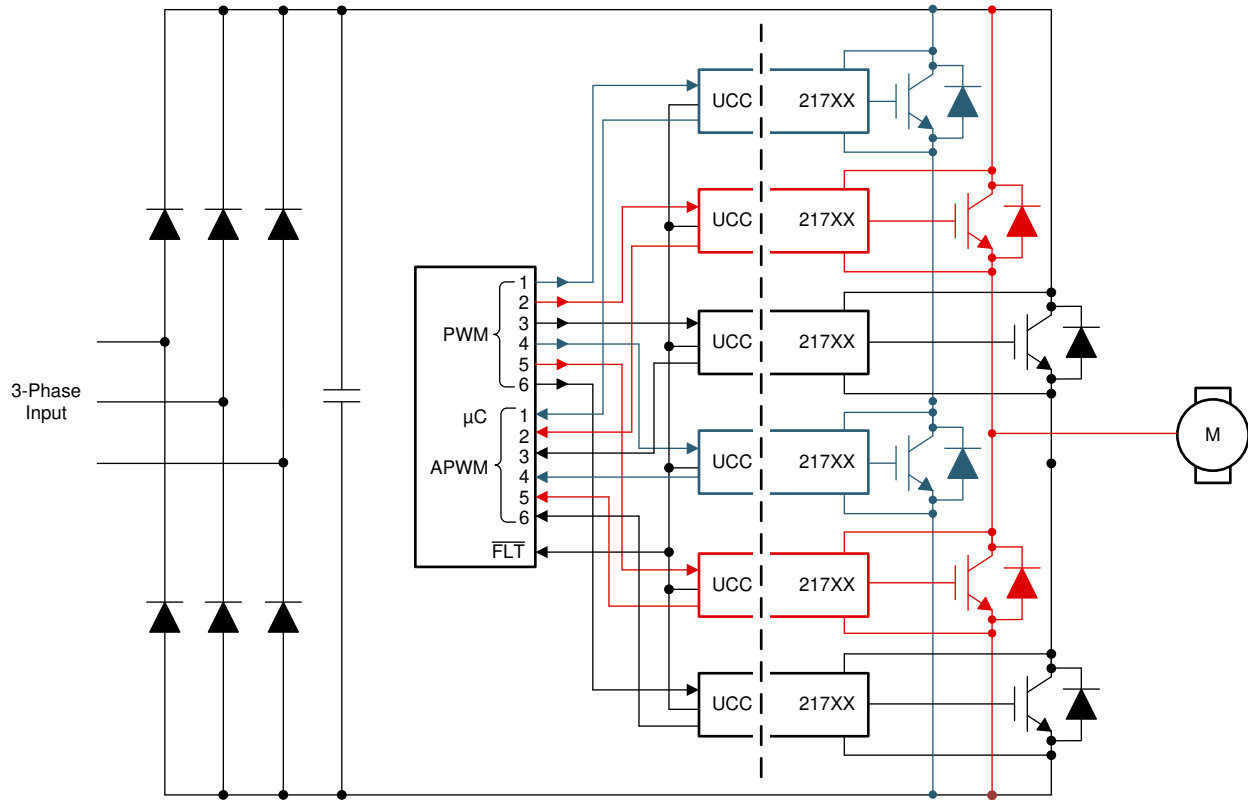
The device is very versatile because of the strong drive strength, wide range of output power supply, high isolation ratings, high CMTI and superior protection and sensing features. The 1.5-kVRMS working voltage and 12.8-kVPK surge immunity can support up both SiC MOSFET and IGBT modules with DC bus voltage up to 2121 V. The device can be used in both low power and high power applications such as the traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies and etc. The device can drive the high power SiC MOSFET module, IGBT module or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves the cost and space of the board design. The device can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signal from 3.3 V to 5 V, and the device level shifts the signal to output side through reinforced isolation barrier. The device has wide output power supply range from 13 V to 33 V and support wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT application and many others. The 12-V UVLO benefits the power semiconductor with lower conduction loss and improves the system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

The device features extensive protection and monitoring features, which can monitor, report and protect the system from various fault conditions.

- Fast detection and protection for the overcurrent and short circuit fault. The semiconductor is shutdown when the fault is detected and  $\overline{\text{FLT}}$  pin is pulled down to indicate the fault detection. The device is latched unless reset signal is received from the  $\overline{\text{RST/EN}}$  pin.
- Soft turn-off feature to protect the power semiconductor from catastrophic breakdown during overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power good status can be monitored from the RDY pin.
- Analog signal sensing with isolated analog to PWM signal feature. This feature allows the device to sense the temperature of the semiconductor from the thermal diode or temperature sensing resistor, or dc bus voltage with resistor divider. A PWM signal is generated on the low voltage side with reinforced isolated from the high voltage side. The signal can be fed back to the microcontroller for the temperature monitoring, voltage monitoring and etc.
- The active Miller clamp feature protects the power semiconductor from false turn on.
- Enable and disable function through the  $\overline{\text{RST/EN}}$  pin
- Short circuit clamping
- Active pulldown

### 9.2 Typical Application

Figure 9-1 shows the typical application of a half bridge using two UCC21755-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications such as traction inverter in HEV/EV to convert the DC current of the electric vehicle's battery to the AC current to drive the electric motor in the propulsion system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.



**Figure 9-1. Typical Application Schematic**

### 9.2.1 Design Requirements

The design of the power system for end equipment should consider some design requirements to ensure the reliable operation of the device through the load range. The design considerations include the peak source and sink current, power dissipation, overcurrent and short circuit protection, AIN-APWM function for analog signal sensing, etc.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are shown in [Table 9-1](#).

**Table 9-1. Design Parameters**

PARAMETER	VALUE
Input Supply Voltage	5 V
IN-OUT Configuration	Non-inverting
Positive Output Voltage VDD	15 V
Negative Output Voltage VEE	-5 V
DC Bus Voltage	800 V
Peak Drain Current	300 A
Switching Frequency	50 kHz
Switch Type	IGBT Module

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Input Filters for IN+, IN- and $\overline{RST/EN}$

In the applications of traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong drive strength of the device, the  $dV/dt$  can be high, especially for SiC MOSFET. Noise can not only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the non-ideal PCB layout and coupled capacitance.

The device features a 40-ns internal deglitch filter to IN+, IN- and  $\overline{\text{RST/EN}}$  pin. Any signal less than 40ns can be filtered out from the input pins. For noisy systems, external low pass filter can be added externally to the input pins. Adding low pass filters to IN+, IN- and  $\overline{\text{RST/EN}}$  pins can effectively increase the noise immunity and increase the signal integrity. When not in use, the IN+, IN- and  $\overline{\text{RST/EN}}$  pins should not be floating. IN- should be tied to GND if only IN+ is used for non-inverting input to output configuration. The purpose of the low pass filter is to filter out the high frequency noise generated by the layout parasitics. While choosing the low pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

### 9.2.2.2 PWM Interlock of IN+ and IN-

The device features the PWM interlock for IN+ and IN- pins, which can be used to prevent the phase leg shoot through issue. As shown in Table 8-1, the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in Figure 9-2, the PWM\_T is the PWM signal to top side switch, the PWM\_B is the PWM signal to bottom side switch. For the top side gate driver, the PWM\_T signal is given to the IN+ pin, while the PWM\_B signal is given to the IN- pin; for the bottom side gate driver, the PWM\_B signal is given to the IN+ pin, while PWM\_T signal is given to the IN- pin. When both PWM\_T and PWM\_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot through condition.

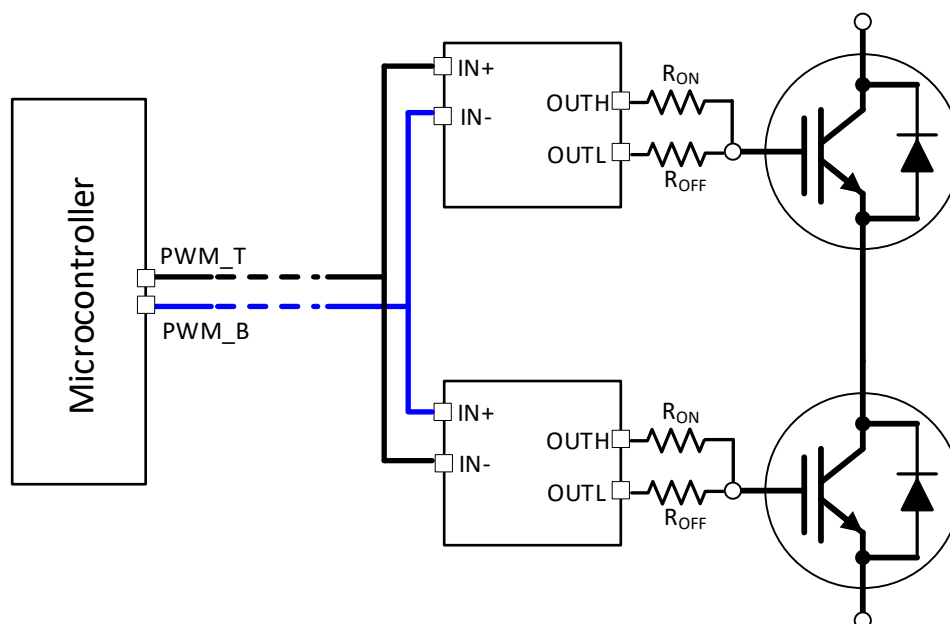


Figure 9-2. PWM Interlock for a Half Bridge

### 9.2.2.3 $\overline{\text{FLT}}$ , RDY, and $\overline{\text{RST/EN}}$ Pin Circuitry

Both  $\overline{\text{FLT}}$  and RDY pin are open-drain output. The  $\overline{\text{RST/EN}}$  pin has 50-k $\Omega$  internal pulldown resistor, so the driver is in OFF status if the  $\overline{\text{RST/EN}}$  pin is not pulled up externally. A 5-k $\Omega$  resistor can be used as pullup resistor for the  $\overline{\text{FLT}}$ , RDY, and  $\overline{\text{RST/EN}}$  pins.

To improve the noise immunity due to the parasitic coupling and common mode noise, low pass filters can be added between the  $\overline{\text{FLT}}$ , RDY, and  $\overline{\text{RST/EN}}$  pins and the microcontroller. A filter capacitor between 100 pF to 300 pF can be added.



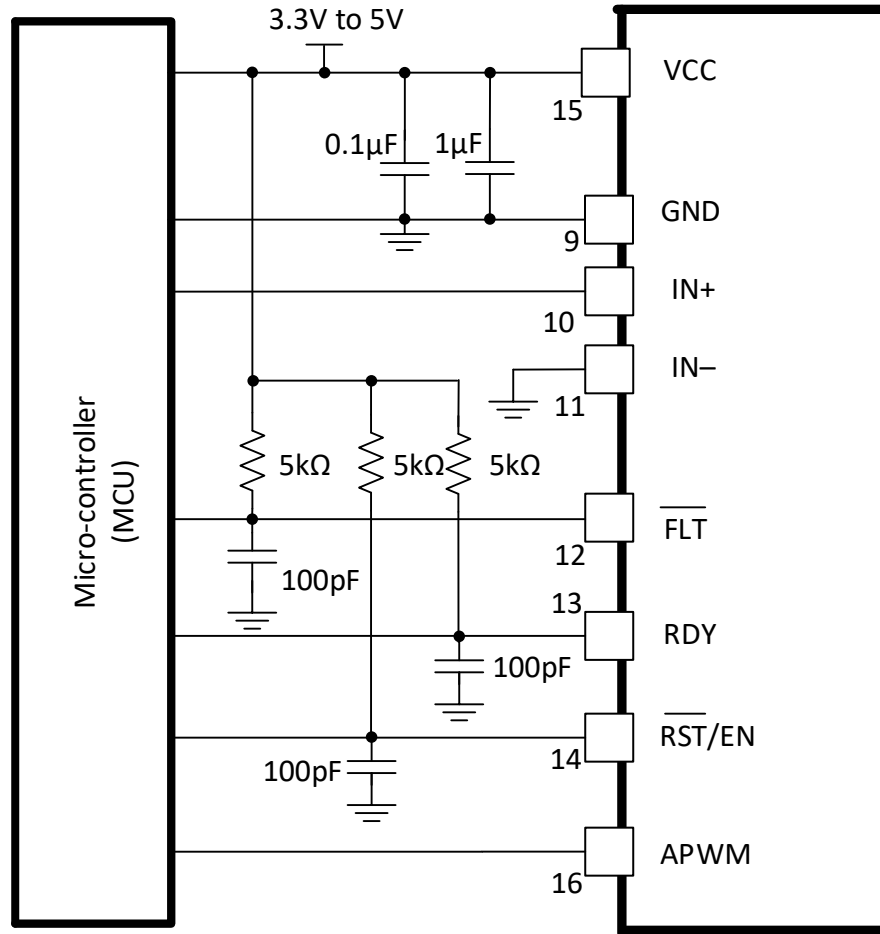


Figure 9-3.  $\overline{\text{FLT}}$ , RDY and  $\overline{\text{RST/EN}}$  Pins Circuitry

#### 9.2.2.4 $\overline{\text{RST/EN}}$ Pin Control

$\overline{\text{RST/EN}}$  pin has two functions. It is used to enable or shutdown the outputs of the driver and to reset the fault signaled on the  $\overline{\text{FLT}}$  pin after DESAT is detected.  $\overline{\text{RST/EN}}$  pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. By default the driver is disabled with the internal 50k $\Omega$  pulldown resistor at this pin.

When the driver is latched after DESAT is detected, the  $\overline{\text{FLT}}$  pin and output are latched low and need to be reset by the  $\overline{\text{RST/EN}}$  pin. The microcontroller must send a signal to  $\overline{\text{RST/EN}}$  pin after the fault to reset the driver. The driver will not respond until after the mute time  $t_{\text{FLTMUTE}}$ . The reset signal must be held low for at least  $t_{\text{RSTFIL}}$  after the mute time.

This pin can also be used to automatically reset the driver. The continuous input signal IN+ or IN- can be applied to  $\overline{\text{RST/EN}}$  pin. There is no separate reset signal from the microcontroller when configuring the driver this way. If the PWM is applied to the non-inverting input IN+, then IN+ can also be tied to  $\overline{\text{RST/EN}}$  pin. If the PWM is applied to the inverting input IN-, then a NOT logic is needed between the PWM signal from the microcontroller and the  $\overline{\text{RST/EN}}$  pin. Using either configuration results in the driver being reset in every switching cycle without an extra control signal from microcontroller tied to  $\overline{\text{RST/EN}}$  pin. One must ensure the PWM off-time is greater than  $t_{\text{RSTFIL}}$  in order to reset the driver in cause of a DESAT fault.

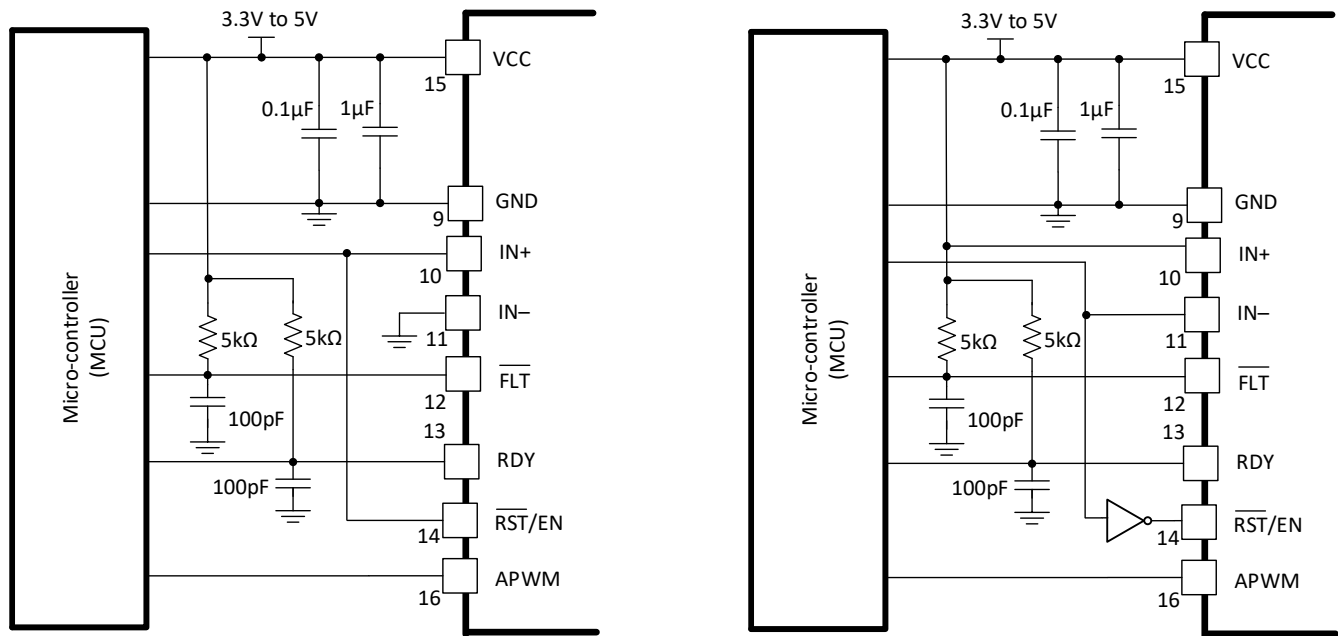


Figure 9-4. Automatic Reset Control

### 9.2.2.5 Turn-On and Turn-Off Gate Resistors

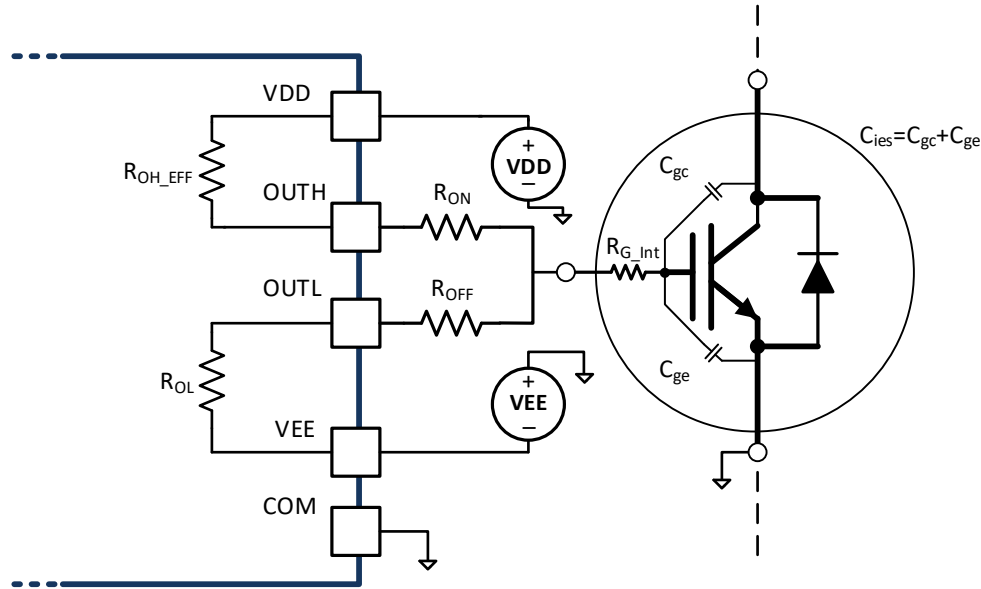
The device features split outputs OUTH and OUTL, which enables the independent control of the turn-on and turn-off switching speeds. The turn-on and turn-off resistances determine the peak source and sink current, which control the switching speed. Meanwhile, the power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. At first, the peak source and sink current are calculated as:

$$I_{\text{source\_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{EE}}}{R_{\text{OH\_EFF}} + R_{\text{ON}} + R_{\text{G\_Int}}}\right)$$

$$I_{\text{sink\_pk}} = \min\left(10\text{A}, \frac{V_{\text{DD}} - V_{\text{EE}}}{R_{\text{OL}} + R_{\text{OFF}} + R_{\text{G\_Int}}}\right) \quad (1)$$

Where

- $R_{\text{OH\_EFF}}$  is the effective internal pullup resistance of the hybrid pullup structure, shown in Figure 8-1, which is approximately  $2 \times R_{\text{OL}}$ , about  $0.7 \Omega$ . This is the dominant resistance during the switching transient of the pull up structure.
- $R_{\text{OL}}$  is the internal pulldown resistance, about  $0.3 \Omega$ .
- $R_{\text{ON}}$  is the external turn on gate resistance.
- $R_{\text{OFF}}$  is the external turn off gate resistance.
- $R_{\text{G\_Int}}$  is the internal resistance of the SiC MOSFET or IGBT module.



**Figure 9-5. Output Model for Calculating Peak Gate Current**

For example, for an IGBT module based system with the following parameters:

- $Q_g = 3300 \text{ nC}$
- $R_{G\_Int} = 1.7 \Omega$
- $R_{ON}=R_{OFF}= 1 \Omega$

The peak source and sink current in this case are:

$$I_{\text{source\_pk}} = \min(10\text{A}, \frac{V_{DD} - V_{EE}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}}) \approx 5.9\text{A}$$

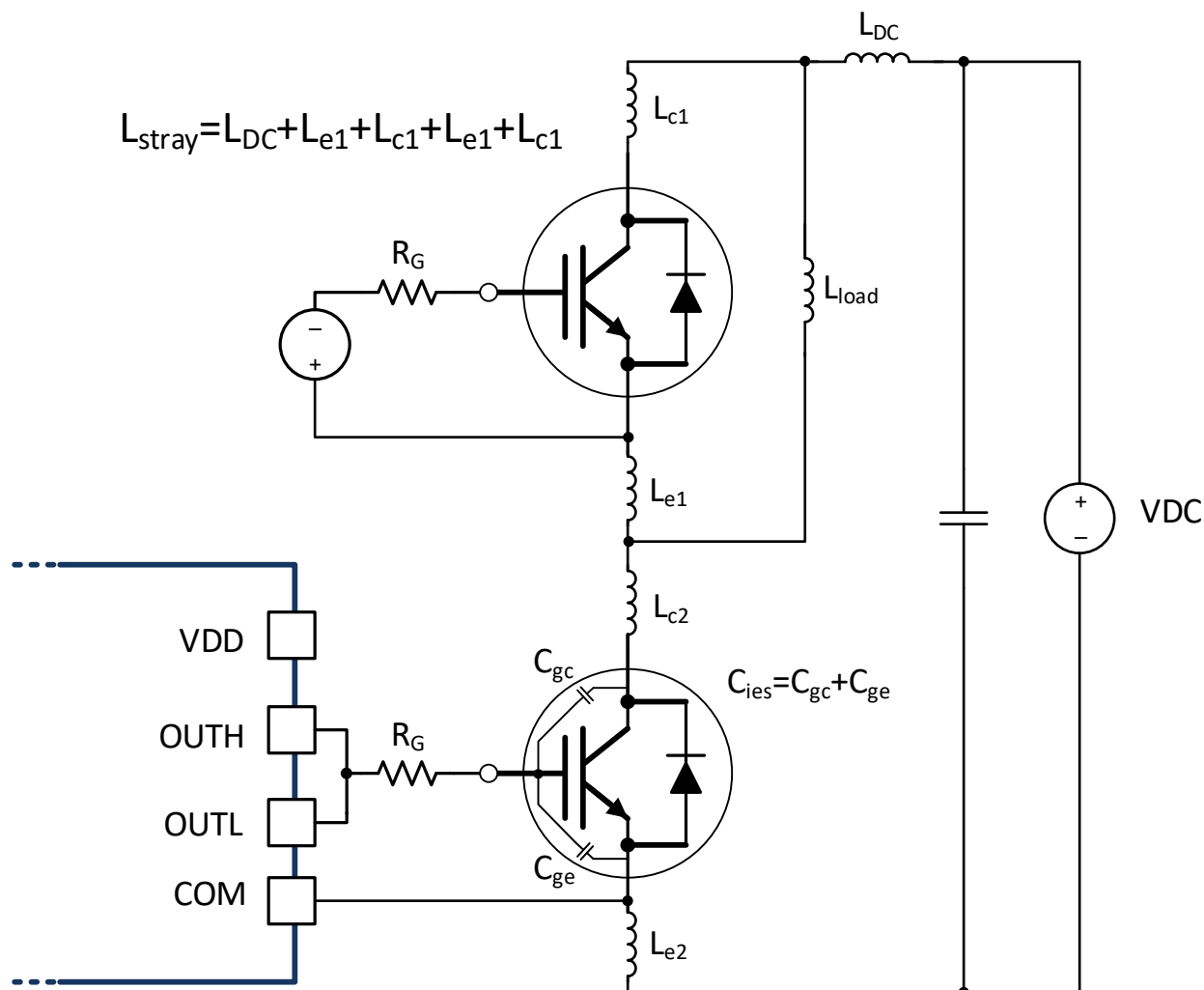
$$I_{\text{sink\_pk}} = \min(10\text{A}, \frac{V_{DD} - V_{EE}}{R_{OL} + R_{OFF} + R_{G\_Int}}) \approx 6.7\text{A} \quad (2)$$

Using 1-Ω external gate resistance, the peak source current is 5.9 A, the peak sink current is 6.7 A. The collector-to-emitter  $dV/dt$  during the turn-on switching transient is dominated by the gate current at the Miller plateau voltage. The hybrid pullup structure ensures the peak source current at the Miller plateau voltage, unless the turn-on gate resistor is too high. The faster the collector-to-emitter,  $V_{ce}$ , voltage rises to  $V_{DC}$ , the smaller the turn-on switching loss. The  $dV/dt$  can be estimated as  $Q_{gc}/I_{\text{source\_pk}}$ . For the turn off switching transient, the drain-to-source  $dV/dt$  is dominated by the load current, unless the turn-off gate resistor is too high. After  $V_{ce}$  reaches the DC bus voltage, the power semiconductor is in SATURATION mode and the channel current is controlled by  $V_{ge}$ . The peak sink current determines the  $dI/dt$ , which dominates the  $V_{ce}$  voltage overshoot accordingly. If using relatively large turn-off gate resistance, the  $V_{ce}$  overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{ce} = L_{\text{stray}} \cdot I_{\text{load}} / ((R_{OFF} + R_{OL} + R_{G\_Int}) \cdot C_{ies} \cdot \ln(V_{\text{plat}} / V_{th})) \quad (3)$$

Where

- $L_{\text{stray}}$  is the stray inductance in power switching loop, as shown in [Figure 9-6](#).
- $I_{\text{load}}$  is the load current, which is the turn off current of the power semiconductor.
- $C_{ies}$  is the input capacitance of the power semiconductor.
- $V_{\text{plat}}$  is the plateau voltage of the power semiconductor.
- $V_{th}$  is the threshold voltage of the power semiconductor.



**Figure 9-6. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration**

The power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \quad (4)$$

$P_Q$  is the quiescent power loss for the driver, which is  $I_q \times (V_{DD} - V_{EE}) = 5 \text{ mA} \times 20 \text{ V} = 0.100 \text{ W}$ . The quiescent power loss is the power consumed by the internal circuits, such as the input stage, reference voltage, logic circuits, and protection circuits when the driver is switching, when the driver is biased with  $V_{DD}$  and  $V_{EE}$ , and the charging and discharging current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left( \frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}} \right) \cdot (V_{DD} - V_{EE}) \cdot f_{sw} \cdot Q_g \quad (5)$$

Where

- $Q_g$  is the gate charge required at the operation point to fully charge the gate voltage from  $V_{EE}$  to  $V_{DD}$ .
- $f_{sw}$  is the switching frequency.

In this example, the  $P_{SW}$  can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left( \frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}} \right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g = 0.505W \quad (6)$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150^\circ C \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50 kHz to keep the gate driver in the thermal limit. By using a lower switching frequency or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

#### 9.2.2.6 Overcurrent and Short Circuit Protection

A standard desaturation circuit can be applied to the DESAT pin. If the voltage of the DESAT pin is higher than the threshold  $V_{DESAT}$ , the soft turn-off is initiated. A fault will be reported to the input side to DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the RST/EN pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for SiC MOSFET and IGBT.

If DESAT pin is not in use, it must be tied to COM to avoid overcurrent fault false triggering.

- Fast reverse recovery high voltage diode is recommended in the desaturation circuit. A resistor is recommended in series with the high voltage diode to limit the inrush current.
- A Schottky diode is recommended from COM to DESAT to prevent driver damage caused by negative voltage.
- A Zener diode is recommended from COM to DESAT to prevent driver damage caused by positive voltage.

#### 9.2.2.7 Isolated Analog Signal Sensing

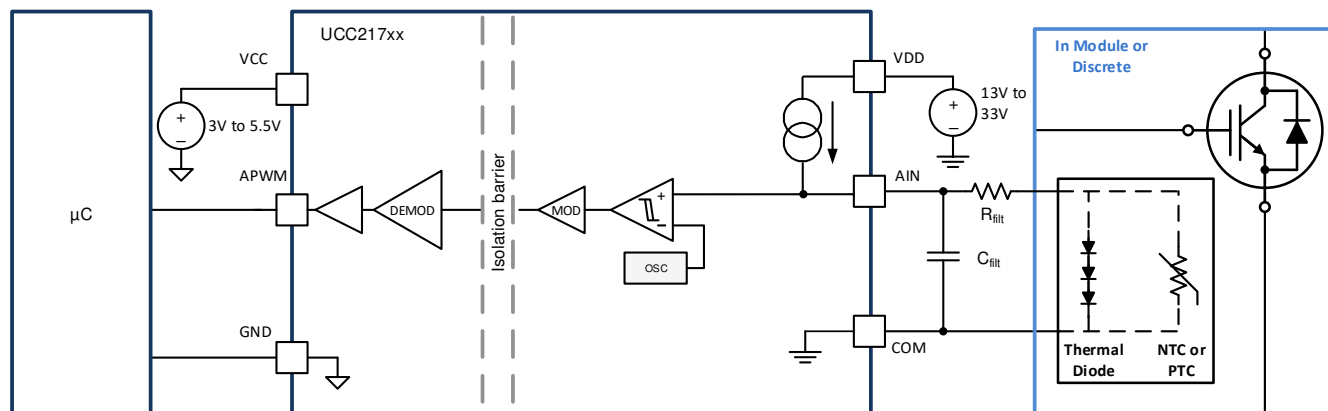
The isolated analog signal sensing feature provides a simple isolated channel for the isolated temperature detection, voltage sensing and etc. One typical application of this function is the temperature monitor of the power semiconductor. Thermal diodes or temperature sensing resistors are integrated in the SiC MOSFET or IGBT module close to the dies to monitor the junction temperature. The device has an internal 200-μA current source with ±3% accuracy across temperature, which can forward bias the thermal diodes or create a voltage drop on the temperature sensing resistors. The sensed voltage from the AIN pin is passed through the isolation barrier to the input side and transformed to a PWM signal. The duty cycle of the PWM changes linearly from 10% to 88% when the AIN voltage changes from 4.5 V to 0.6 V and can be represented using Equation 9.

$$D_{APWM}(\%) = -20 * V_{AIN} + 100 \quad (9)$$

##### 9.2.2.7.1 Isolated Temperature Sensing

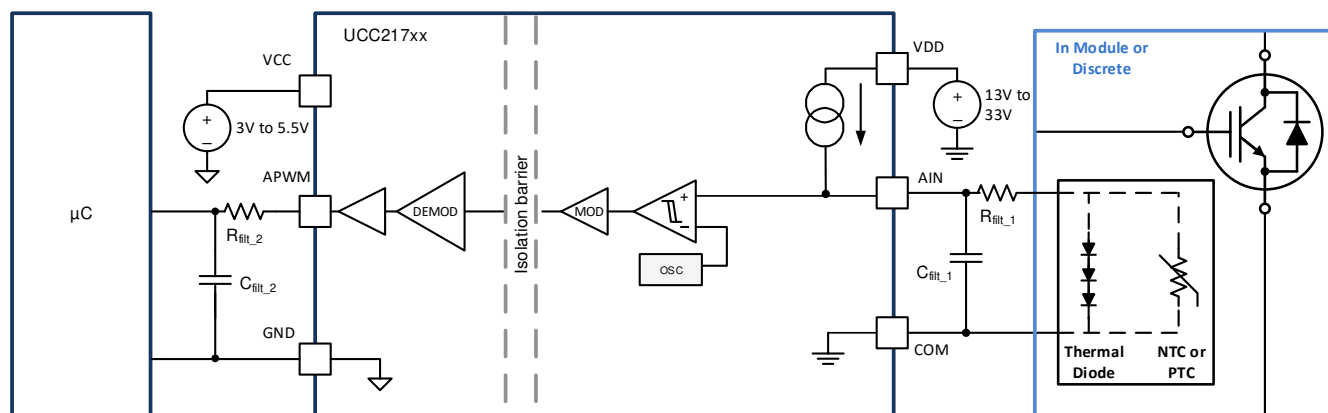
A typical application circuit is shown in Figure 9-7. To sense temperature, the AIN pin is connected to the thermal diode or thermistor which can be discrete or integrated within the power module. A low-pass filter is recommended for the AIN input. Since the temperature signal does not have a high bandwidth, the low-pass filter is mainly used for filtering the noise introduced by the switching of the power device, which does not require stringent control for propagation delay. The filter capacitance for  $C_{filt}$  can be chosen between 1 nF to 100 nF and the filter resistance  $R_{filt}$  between 1 Ω to 10 Ω according to the noise level.

The output of APWM is directly connected to the microcontroller to measure the duty cycle dependent on the voltage input at AIN, using Equation 9.



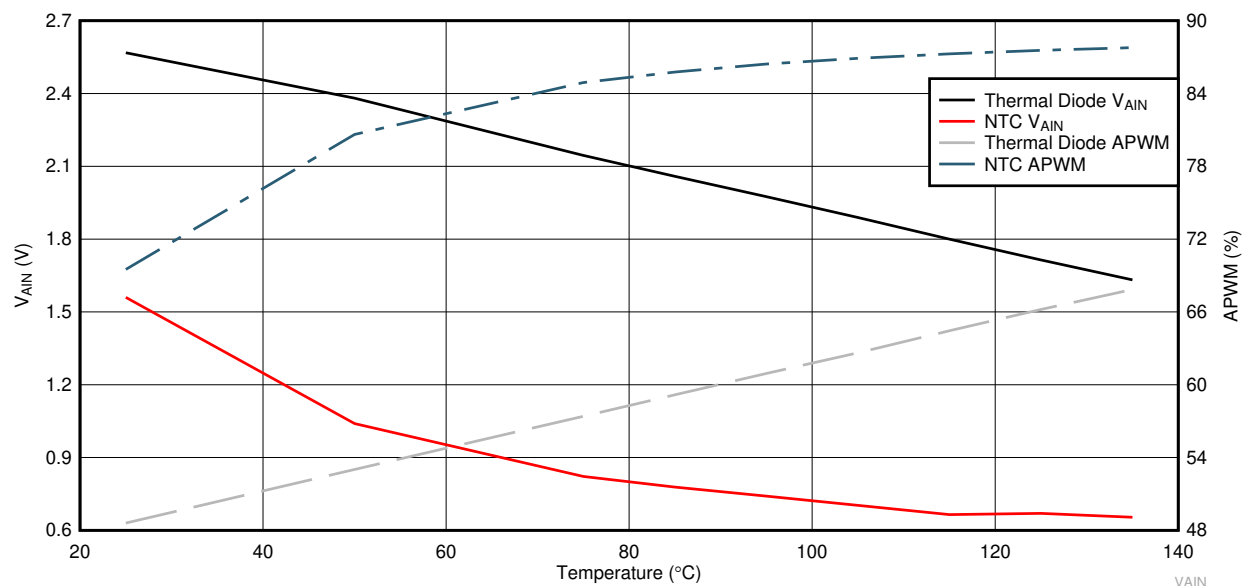
**Figure 9-7. Thermal Diode or Thermistor Temperature Sensing Configuration**

When a high-precision voltage supply for VCC is used on the primary side of the device's the duty cycle output of APWM may also be filtered and the voltage measured using the microcontroller's ADC input pin, as shown in [Figure 9-8](#). The frequency of APWM is 400 kHz, so the value for  $R_{\text{filt}_2}$  and  $C_{\text{filt}_2}$  should be such that the cutoff frequency is below 400 kHz. Temperature does not change rapidly, thus the rise time due to the RC constant of the filter is not under a strict requirement.



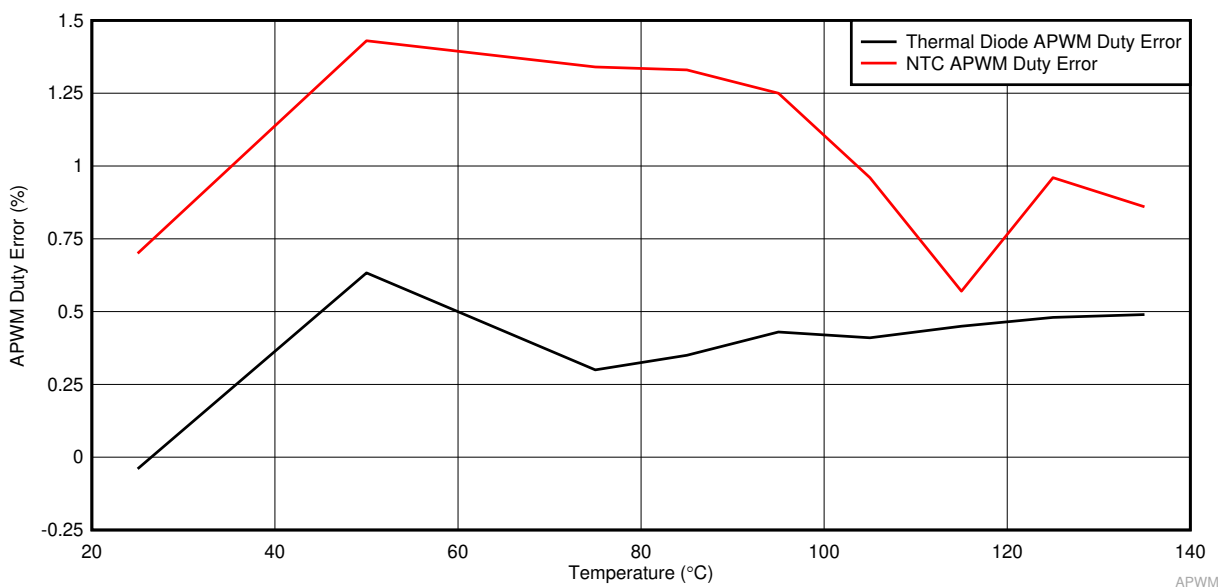
**Figure 9-8. APWM Channel with Filtered Output**

The example below shows the results using a 4.7-k $\Omega$  NTC, NTCS0805E3472FMT, in series with a 3-k $\Omega$  resistor and also the thermal diode using four diode-connected MMBT3904 NPN transistors. The sensed voltage of the 4 MMBT3904 thermal diodes connected in series ranges from about 2.5 V to 1.6 V from 25°C to 135°C, corresponding to 50% to 68% duty cycle. The sensed voltage of the NTC thermistor connected in series with the 3-k $\Omega$  resistor ranges from about 1.5 V to 0.6 V from 25°C to 135°C, corresponding to 70% to 88% duty cycle. The voltage at VAIN of both sensors and the corresponding measured duty cycle at APWM is shown in [Figure 9-9](#).

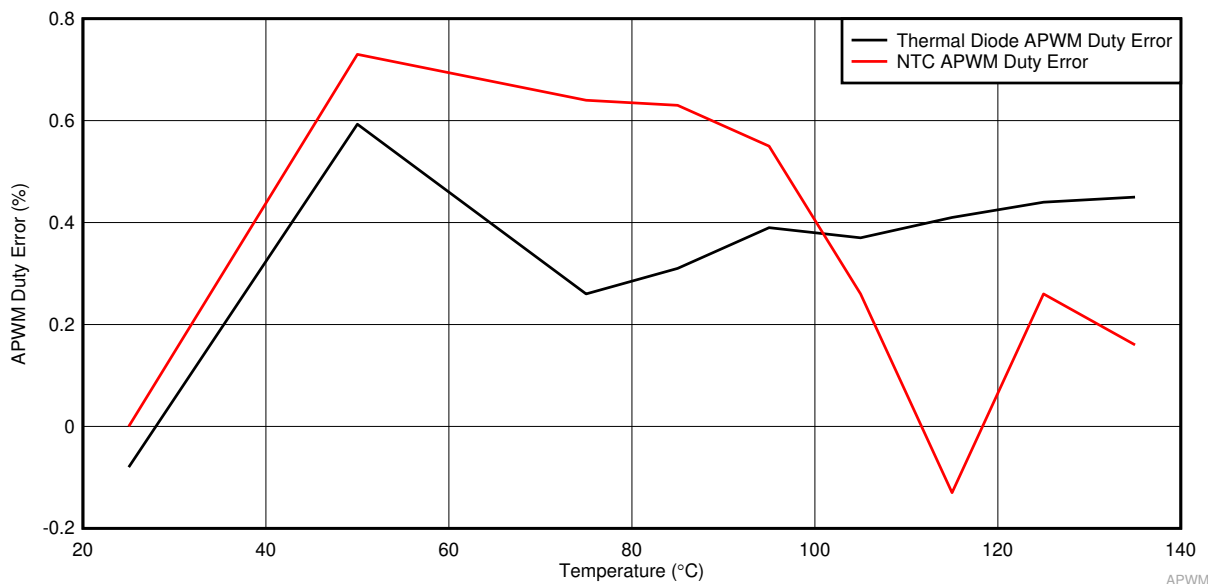


**Figure 9-9. Thermal Diode and NTC  $V_{AIN}$  and Corresponding Duty Cycle at APWM**

The duty cycle output has an accuracy of  $\pm 3\%$  throughout temperature without any calibration, as shown in Figure 9-10 but with single-point calibration at 25°C, the duty accuracy can be improved to  $\pm 1\%$ , as shown in Figure 9-11.



**Figure 9-10. APWM Duty Error Without Calibration**

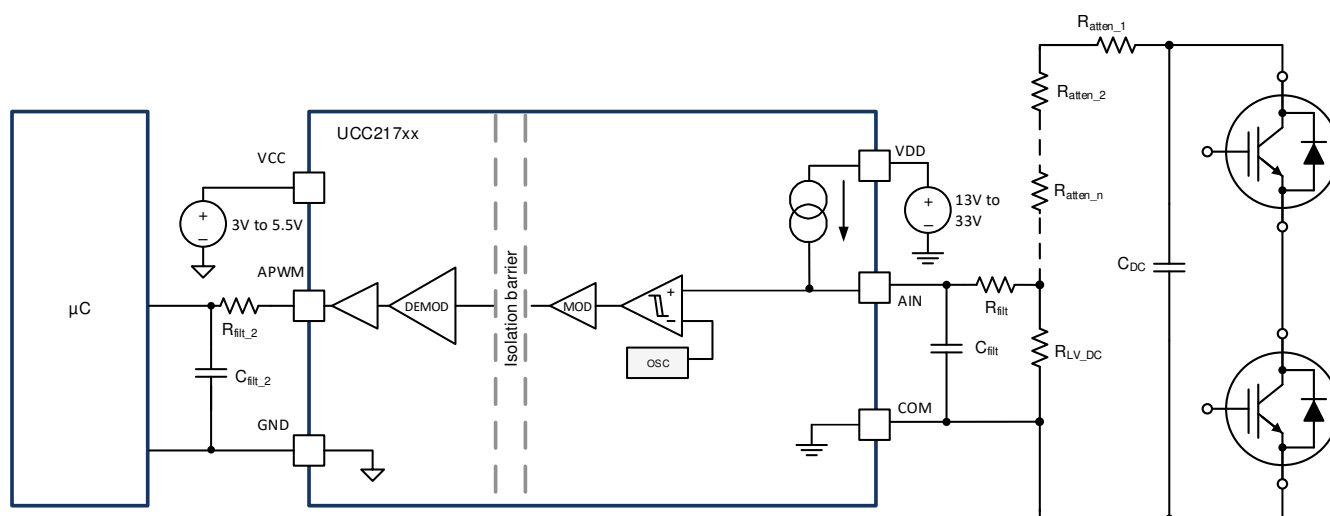


**Figure 9-11. APWM Duty Error with Single-Point Calibration**

#### 9.2.2.7.2 Isolated DC Bus Voltage Sensing

The AIN to APWM channel may be used for other applications such as the DC-link voltage sensing, as shown in Figure 9-12. The same filtering requirements as given above may be used in this case, as well. The number of attenuation resistors,  $R_{atten\_1}$  through  $R_{atten\_n}$ , is dependent on the voltage level and power rating of the resistor. The voltage is finally measured across  $R_{LV\_DC}$  to monitor the stepped-down voltage of the HV DC-link which must fall within the voltage range of AIN from 0.6V to 4.5V. The driver should be referenced to the same point as the measurement reference; thus, in the case shown below, the UCC21755-Q1 is driving the lower IGBT in the half-bridge and the DC-link voltage measurement is referenced to COM. The internal current source  $I_{AIN}$  should be taken into account when designing the resistor divider. The AIN pin voltage is:

$$V_{AIN} = \frac{R_{LV\_DC}}{R_{LV\_DC} + \sum_{i=1}^n R_{atten\_i}} \cdot V_{DC} + R_{LV\_DC} \cdot I_{AIN} \quad (10)$$



**Figure 9-12. DC-Link Voltage Sensing Configuration**

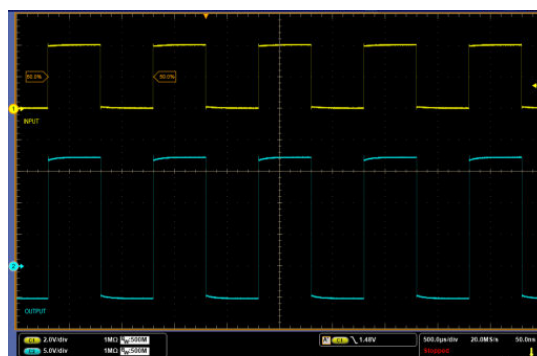


To increase the IGBT gate drive current, a non-inverting current buffer (such as the NPN/PNP buffer shown in [Figure 9-13](#)) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/D45VH10 pair is up to 20-A peak.

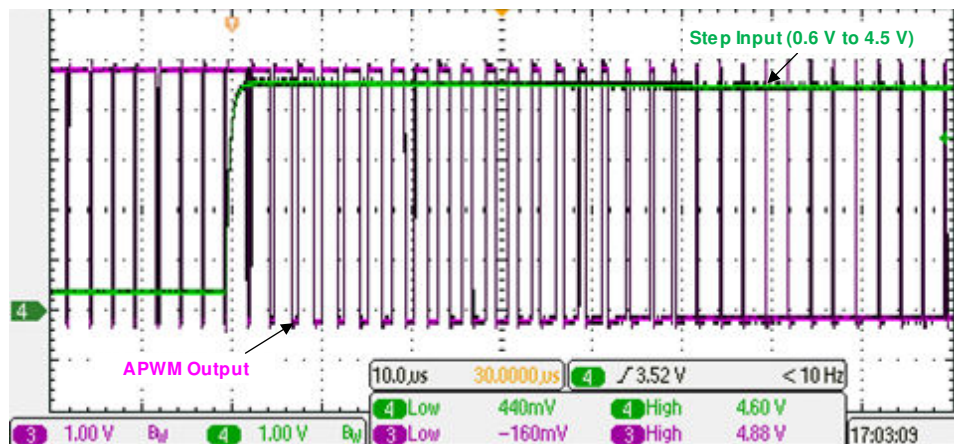
$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \quad (11)$$

- 
- The schematic diagram illustrates a two-stage CMOS differential amplifier. The first stage is a differential pair with NMOS tail current source and PMOS load, biased by a current mirror. The second stage is a differential pair with NMOS load and PMOS tail current source, biased by a current mirror. The output is taken differentially from the second stage.

### 9.2.3 Application Curves



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**Figure 9-15. AIN Step Input (green) and APWM Output (pink)**

## 10 Power Supply Recommendations

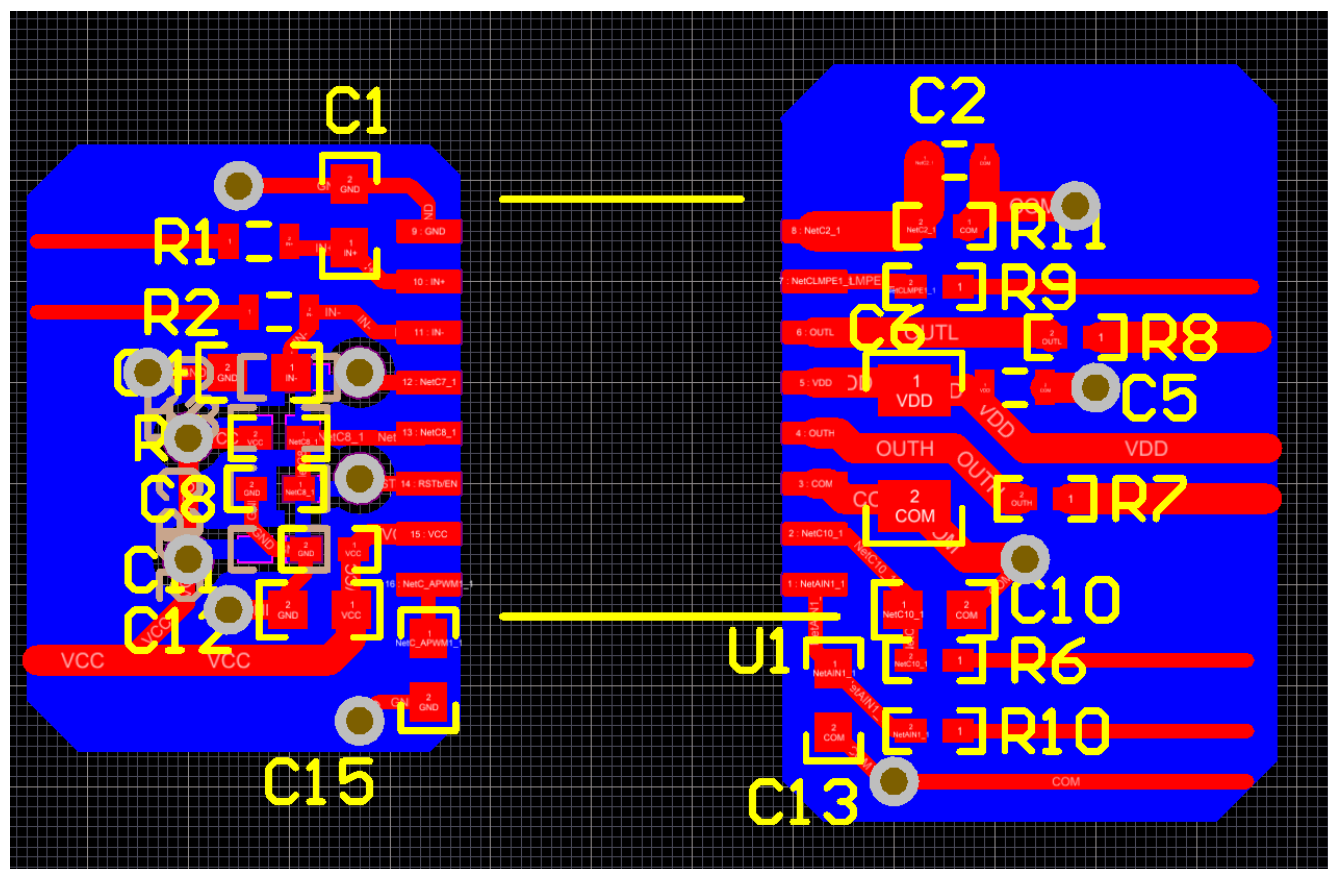
During the turn on and turn off switching transient, the peak source and sink current is provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize the power supply and ensure a reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering the device has  $\pm 10\text{-A}$  peak drive strength and can generate high  $dV/dt$ , a  $10\text{-}\mu\text{F}$  bypass cap is recommended between VDD and COM, VEE and COM. A  $1\text{-}\mu\text{F}$  bypass cap is recommended between VCC and GND due to less current comparing with output side power supplies. A  $0.1\text{-}\mu\text{F}$  decoupling cap is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

## 11 Layout

### 11.1 Layout Guidelines

Due to the strong drive strength of the device, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high  $dI/dt$  and voltage spike on the parasitic inductance of PCB traces.
- The driver COM pin should be connected to the Kelvin connection of SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow.
- If the gate driver is used for the low side switch which the COM pin connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high side switch, which the COM pin is connected to the switch node, ground plane is not recommended.
- If ground plane is not used on the output side, separate the return path of the DESAT and AIN ground loop from the gate loop ground which has large peak source and sink current.
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier.



## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

For related documentation see the following:

- [Isolation Glossary](#)

### 12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21755QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21755Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC21755QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UCC21755QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC21755QDWRQ1	SOIC	DW	16	2000	356.0	356.0	35.0
UCC21755QDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0



## GENERIC PACKAGE VIEW

**DW 16**

**SOIC - 2.65 mm max height**

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224780/A



DW0016B

# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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