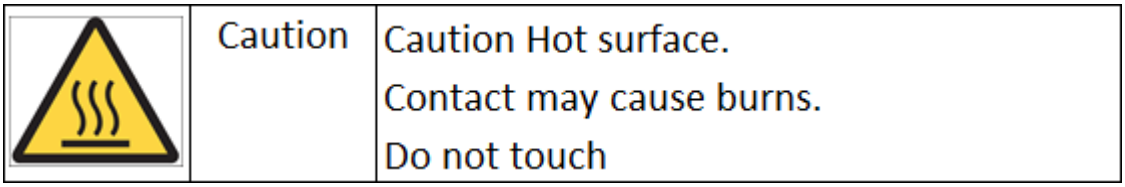
The LP8756xQ1EVM (SV601325) Evaluation Module

This user's guide describes the operation of the SV601325 revision of the evaluation module for the LP8756xQ1 multi-phase 4-core step-down converter from Texas Instruments (TI). If the board you have has BMC031 in the upper-left corner, please reference The LP8756xQ1EVM (BMC031) Evaluation Module document instead. The LP8756xQ1 can be used in five different output configurations, and this user's guide includes all these five variants (see Table 1). The user's guide also provides design information including the schematic and bill of materials (BOM).



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1 Overview

The LP8756xQ1EVM customer evaluation module demonstrates the integrated circuit LP8756xQ1 from TI. The LP8756xQ1 is a high-performance, multi-phase step-down converter designed to meet the power management requirements of the latest applications processors and platform needs in automotive infotainment and cluster applications and also in automotive camera power applications. The device contains four step-down converter cores, which are bundled together in all possible configurations between single 4-phase buck converter and four single-phase buck converters. This document covers user software provided with the EVM and design documentation that includes schematics and parts list.

Table 1. LP8756xQ1 Configurations

PART NUMBER	OUTPUT CONFIGURATION	NUMBER OF OUTPUTS	EVM NUMBER
LP87561Q1	4-phase	1	LP87561Q1EVM
LP87562Q1	3-phase + 1-phase	2	LP87562Q1EVM
LP87563Q1	2-phase + 1-phase + 1-phase	3	LP87563Q1EVM
LP87564Q1	4 × 1-phase	4	LP87564Q1EVM
LP87565Q1	2-phase + 2-phase	2	LP87565Q1EVM

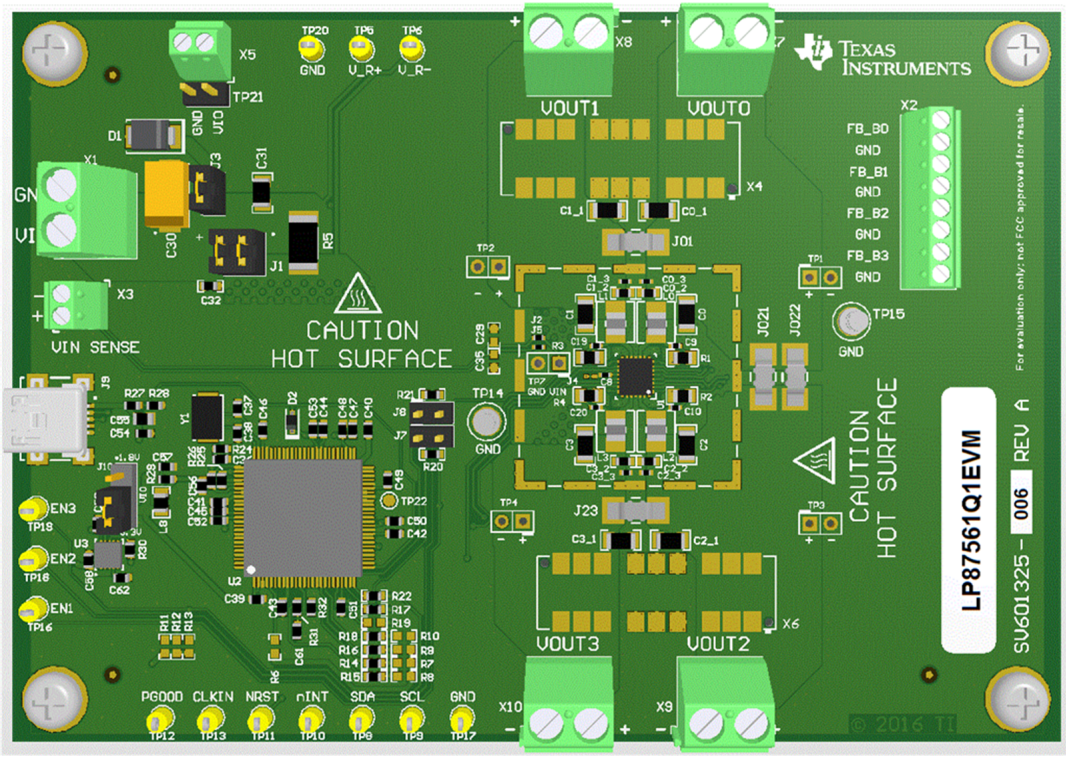


Figure 1. LP8756xQ1EVM

2 Quick Setup Guide

Many of the components on the LP8756xQ1 are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

Upon opening the LP8756xQ1EVM package, ensure that the following items are included:

- LP8756xQ1 Evaluation Board
- USB Cable

If any of the items are missing, contact the closest Texas Instruments Product Information Center to inquire about a replacement.

2.1 Installing/Opening the Software

The EVM software is controlled through a graphical user interface (GUI). The software communicates with the EVM through an available USB port. The minimum hardware requirements for the EVM software are:

- IBM PC-compatible computer running a Microsoft Windows® XP or newer operating system
- Available USB port
- Mouse

Software installation

1. Open the LP8756_installer.exe
2. Installer prompts to accept the license agreement (see Figure 2).
3. Installer prompts to choose which features of LP8756x Installer you want to install (see Figure 3).
4. Installer prompts to select Destination Folder (see Figure 4).
5. Press Install and the installation starts.
6. Installer prompts when installation is complete (see Figure 5).

Open the LP8756x GUI. Connect the EVM to the PC with the USB cable.

1. With the power supply disconnected from the unit under test (UUT), open LP8756EVM.exe located in the directory selected during installation.
2. On the Evaluation SW window bottom right corner you should see text “Hardware connected.”. Refer to Figure 6.

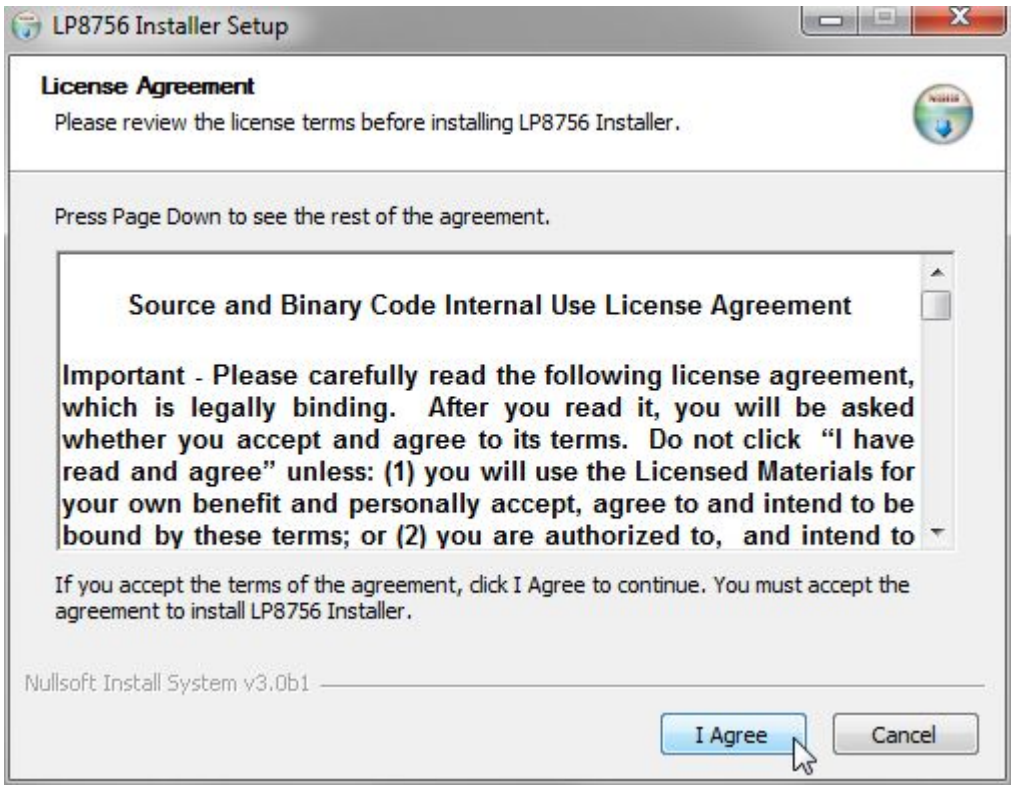


Figure 2. LP8756 Installer License Agreement

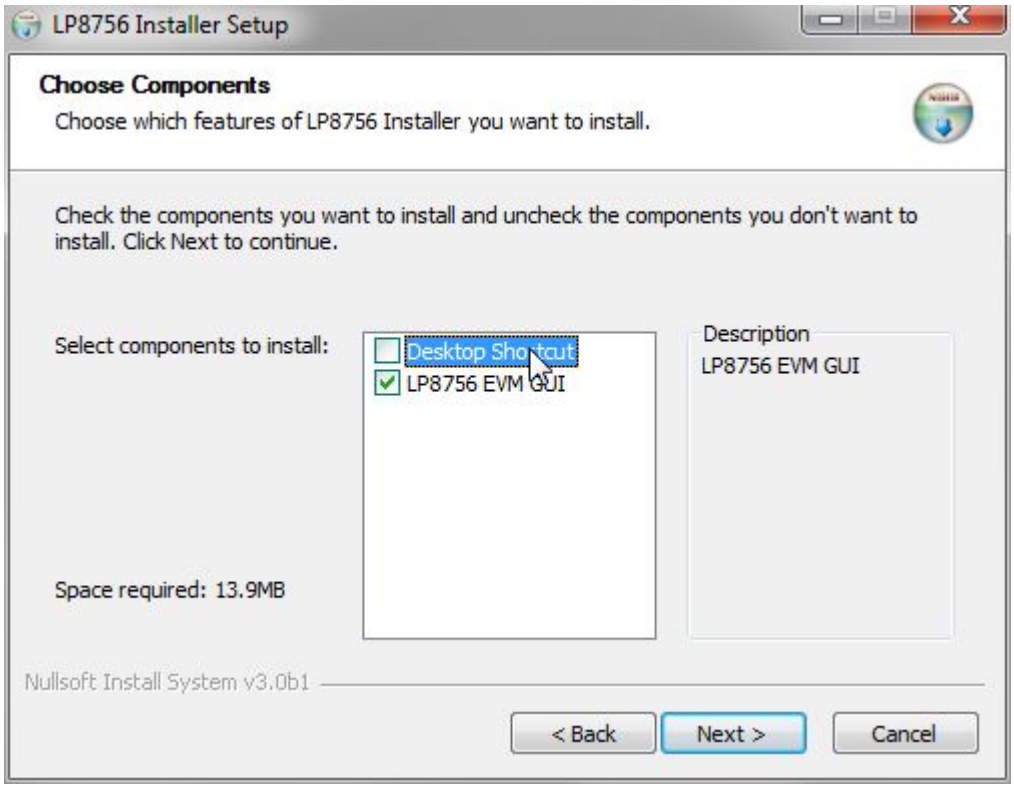


Figure 3. Features of LP8756 Installation

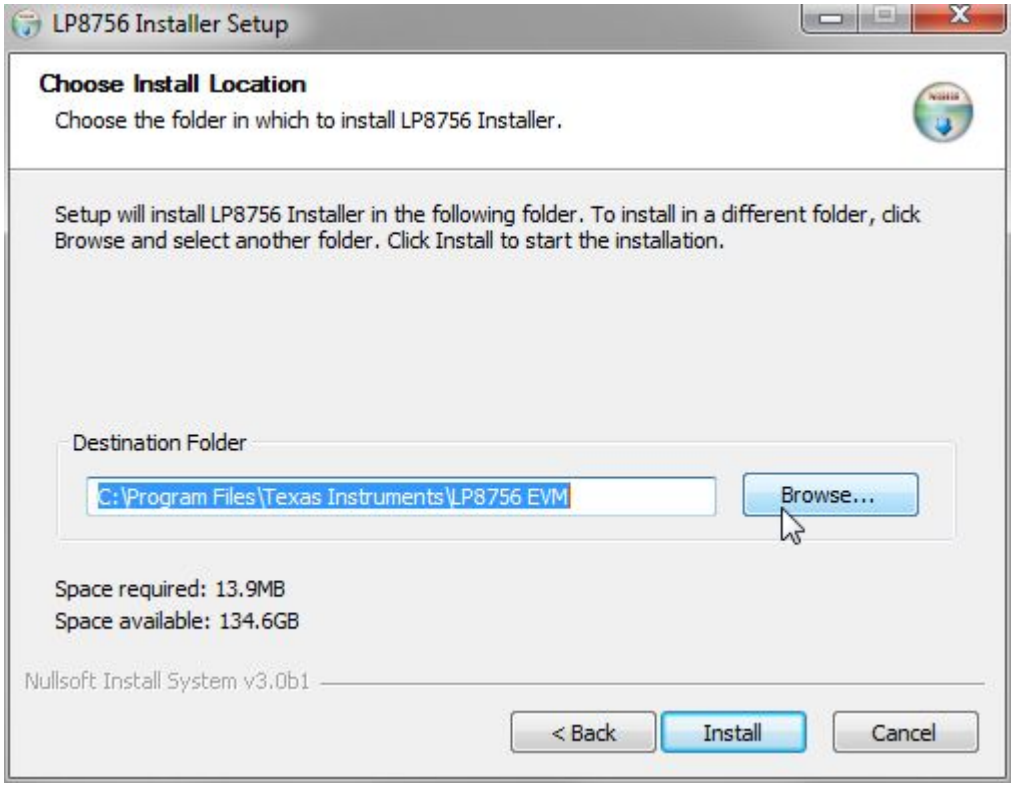


Figure 4. LP8756 Destination Folder

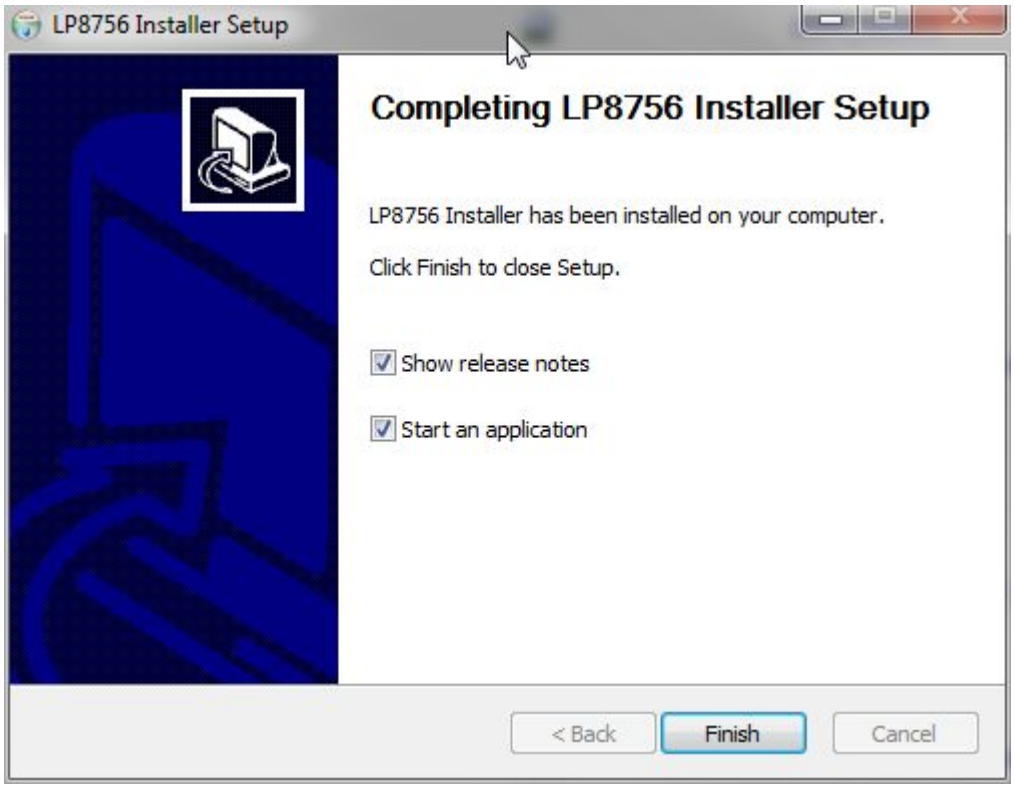


Figure 5. LP8756 Installation Complete

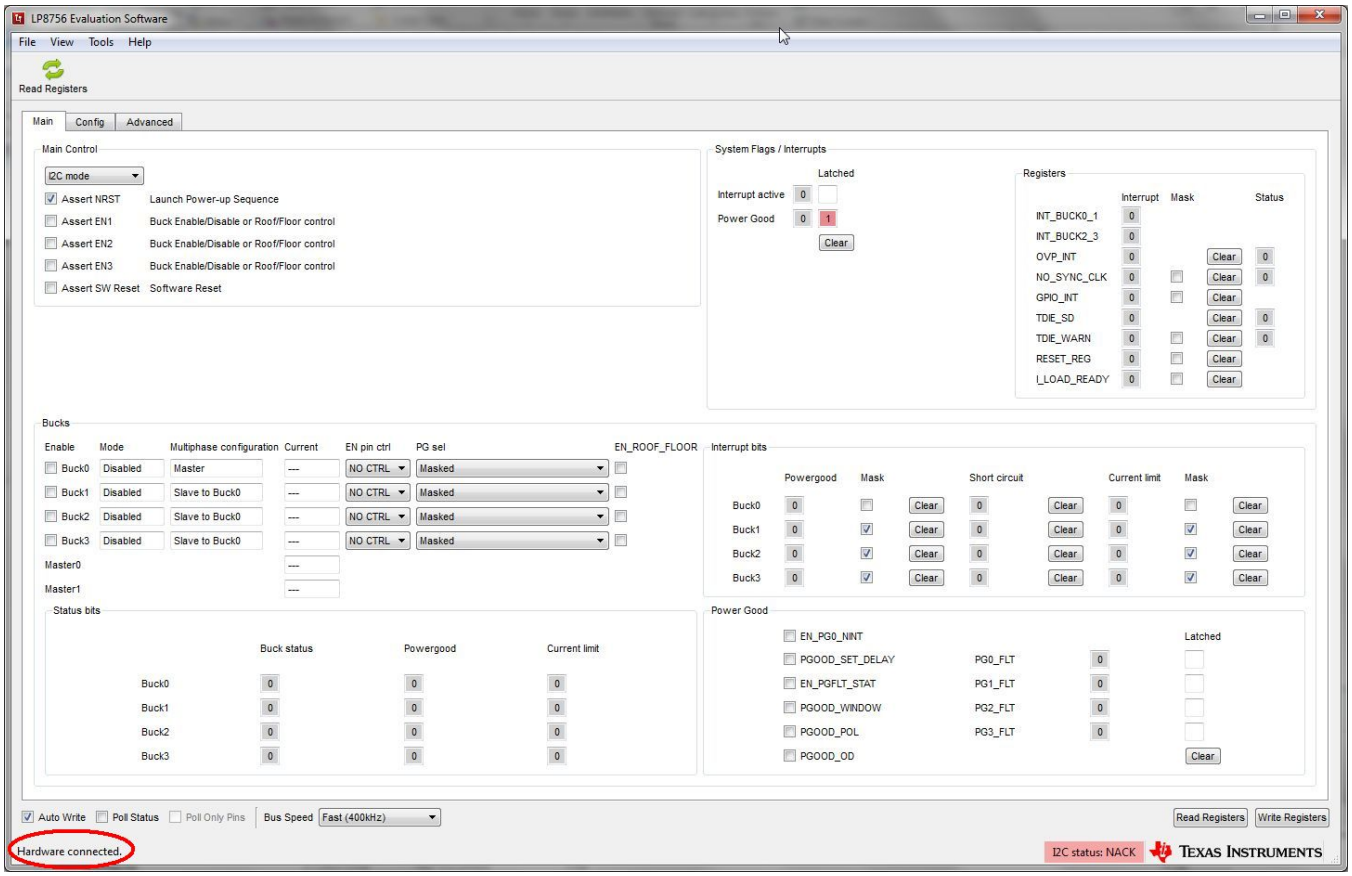


Figure 6. Evaluation Software Graphical User Interface (GUI) When Board Connected

2.2 Power Supply Setup

To power up the EVM, one power supply is needed. For full-load testing of the LP8756xQ1EVM, a DC-power supply capable of at least 10 A and 4 V is required. 5 A is suggested as a practical minimum for partial load. The power supply is connected to the EVM using connector X1. The power supply and cabling must present low impedance to the UUT; the length of power supply cables must be minimized. Remote sense, using connector X3, can be used to compensate for voltage drops in the cabling.

With the power supply disconnected from the UUT, set the supply to 3.7 V DC and the current limit to 5 A minimum. Set the power supply output OFF. Connect the power supply's positive terminal (+) to VIN and negative terminal (–) to GND on UUT (X1 power-in terminal block). Check that jumpers on the boards are set as shown in Figure 1 (factory default jumper configuration).

Set power supply output ON, and then continue with the following steps. Note that following steps are only an example. Register values, enable control, mode and multiphase status may differ depending on the LP8756xQ1EVM configuration.

1. On Evaluation software GUI, click on Assert NRST (see Figure 7).
2. Click on either of the two Read Registers buttons. You should see ready message on green background next to the Read Registers button (see Figure 8).
3. Check that Buck0 is enabled (see Figure 9).
4. Click on Assert EN1 (see Figure 10).
5. Click on either of the two Read Registers buttons.
6. In this example case the GUI indicates "Disabled" under "Mode" until EN1 is asserted. After EN1 is asserted "Mode" is changed to "Enabled". In case BUCKx is enabled or disabled with bit instead of ENx pin, the "Mode" can be checked by reading registers. GUI indicates also "Master" under "Multiphase status" of Buck 0. Mode of other bucks are "Disabled" and Multiphase status is "Slave to Buck0". The EVM is now ready for testing with default register settings loaded.

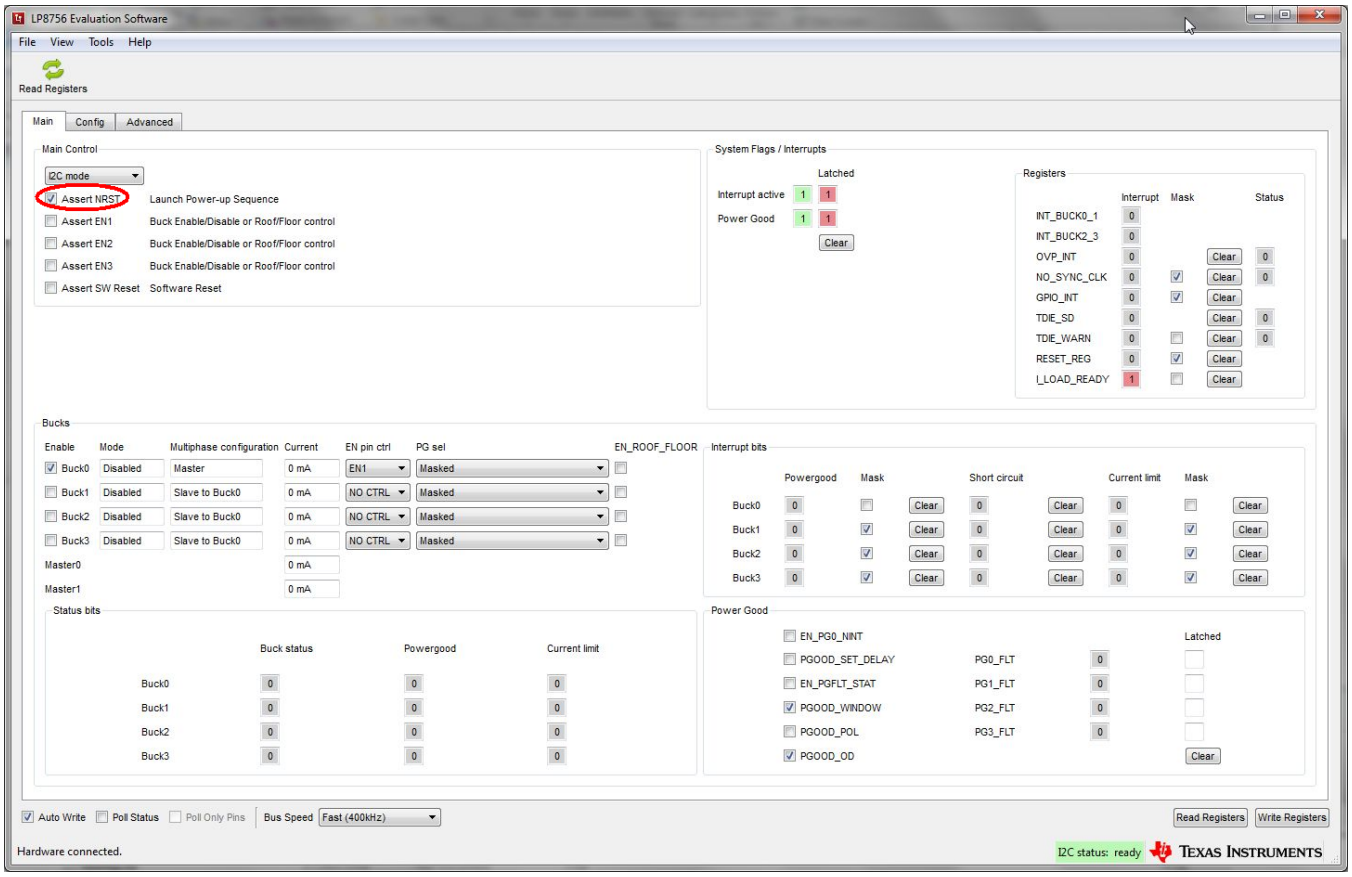


Figure 7. Assert nRST

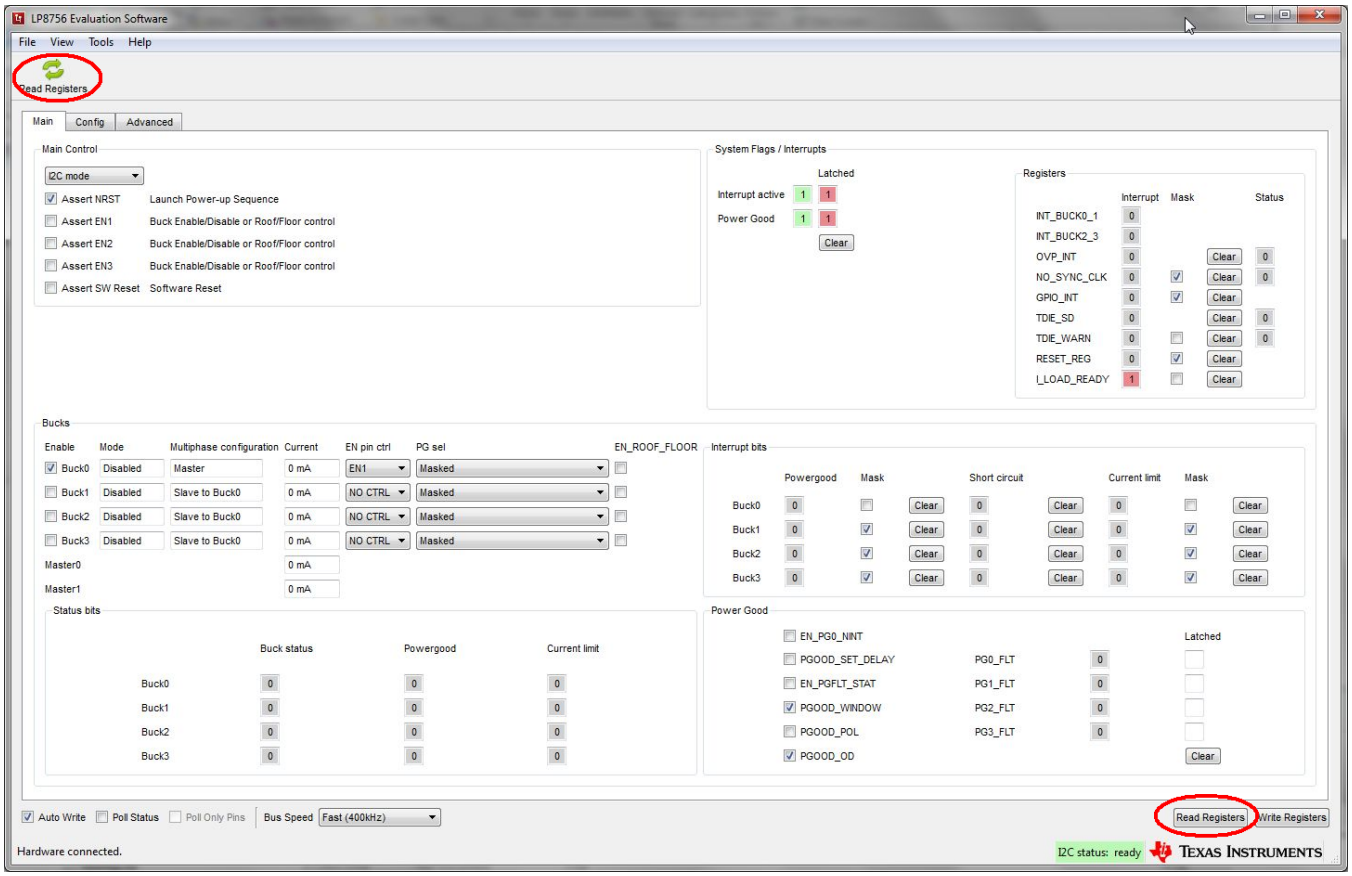


Figure 8. Read Registers Buttons

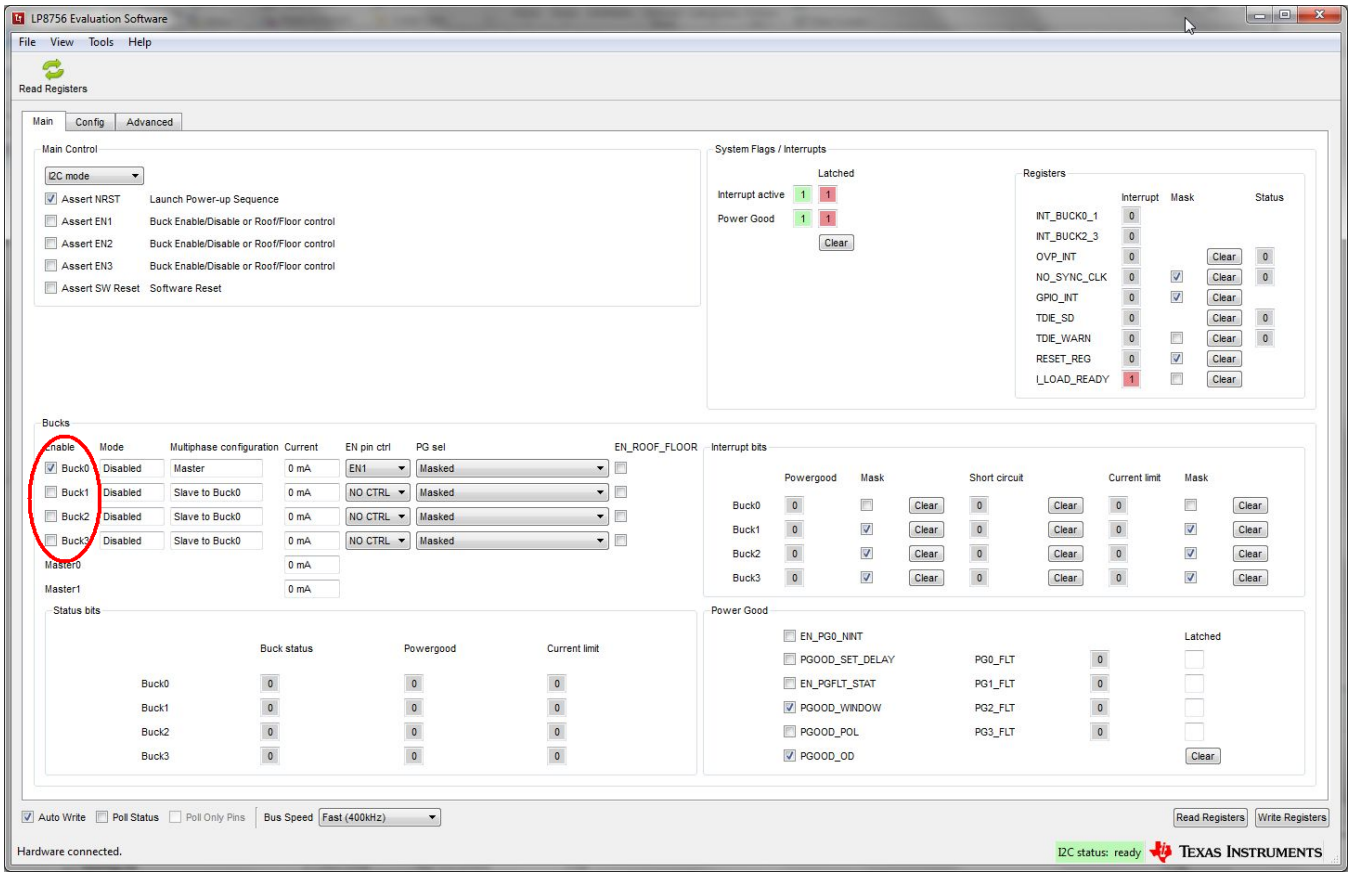


Figure 9. BUCK0 Enabled

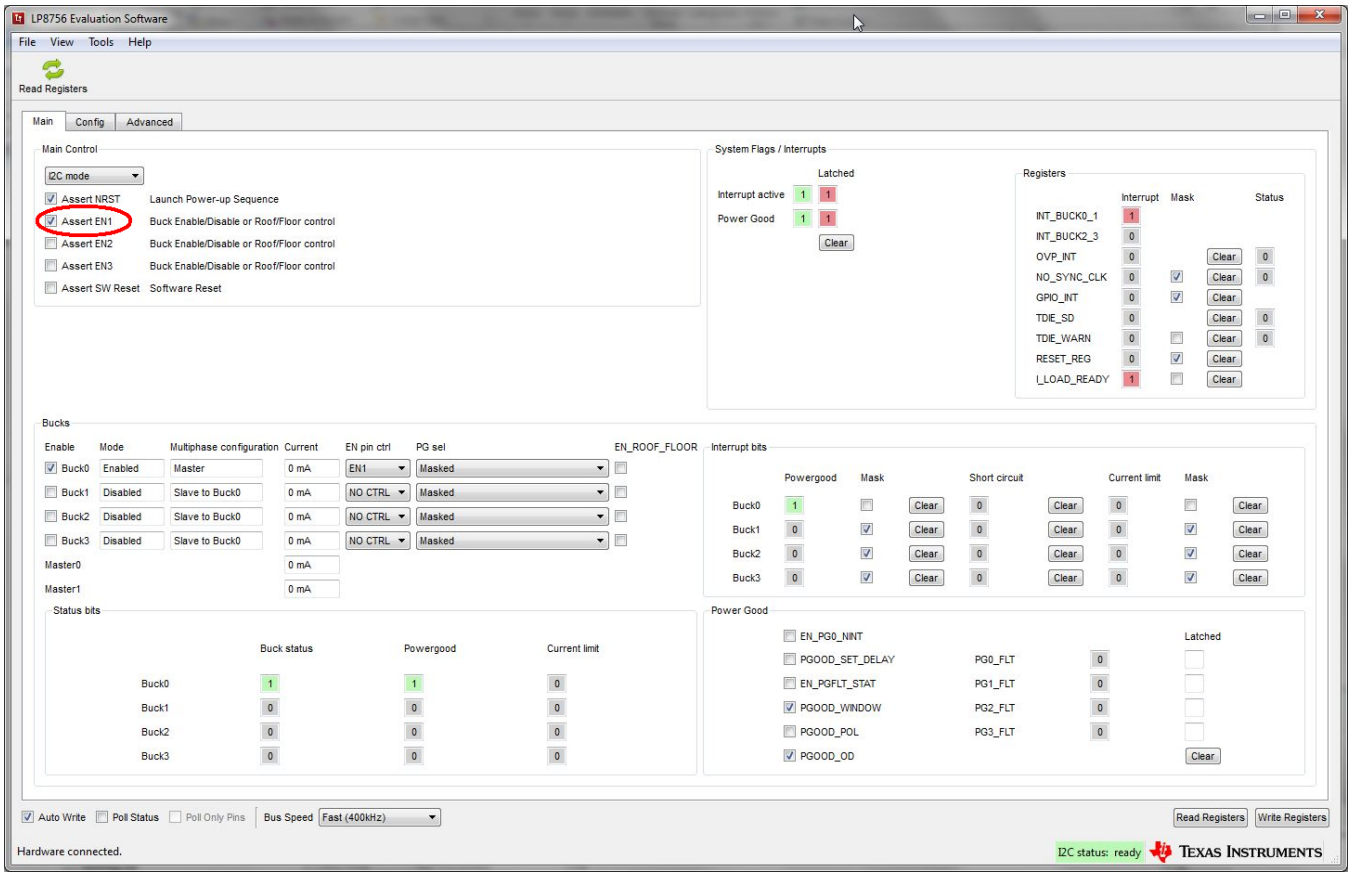


Figure 10. Assert EN1

2.3 Notes on Efficiency Measurement Procedure

Output Connections: An appropriate electronic load or high-power system source meter instrument, specified for operation down to 500 mV, is desirable for loading the UUT. The maximum load current is specified as 4 A per phase. Be sure to choose the correct wire size when attaching the electronic load. A wire resistance that is too high will cause a voltage drop in the power distribution path which becomes significant compared to the absolute value of the output voltage. Connect an electric load to any combination of X7, X8, X9, or X10.. It is advised that, prior to connecting the load, it be set to sink 0 A to avoid power surges or possible shocks.

Voltage drop across the PCB traces will yield inaccurate efficiency measurements. For the most accurate voltage measurement at the EVM, use TP7 to measure the input voltage and X2 to measure the output voltage.

To measure the current flowing to/from the UUT, use the current meter of the DC power supply/electric load as long as it is accurate. Some power source ammeters may show offset of several milliamps and thus will yield inaccurate efficiency measurements. In order to perform very accurate I_q measurements on the UUT, disconnect input protective Zener diode D1 by removing the shunt J3 from the board. When connected, this diode will cause some leakage, especially on high VIN voltages.

3 GUI Overview

The evaluation software has the following tabs: Main, Config, and Advanced. The three tabs together provide the user access to the whole register map of the LP8756x. Additional register control can be obtained from Tools --> Direct Register Access.

3.1 Main Tab

The Main tab (see for example Figure 10) has the elemental controls for the EVM and provides a view to the chip status. Starting from top, the main controls are:

- I2C mode or 4 Enable mode. If this states I2C mode, device is controlled with I2C. When this states 4EN mode, bucks are controlled with ENx pins.
- Assert NRST: This checkbox will assert high level to LP8756xQ1 NRST pin. This pin enables the chip internal voltage reference and bias circuitry.
- Assert EN1: This checkbox will assert high level to LP8756xQ1 EN1 pin. Asserting EN1 may enable the buck regulator(s) or switch to different output voltage level, depending on the register settings.
- Assert EN2: This checkbox will assert high level to LP8756xQ1 EN2 pin. Asserting EN2 may enable the buck regulator(s) or switch to different output voltage level, depending on the register settings.
- Assert EN3: This checkbox will assert high level to LP8756xQ1 EN3 pin. Asserting EN3 may enable the buck regulator(s) or switch to different output voltage level, depending on the register settings.
- Assert EN4: In 4 Enable mode, this checkbox will assert high level to LP8756x SCL pin, (alternative function is EN4). Asserting EN4 may enable the buck regulator(s), depending on the register settings. This checkbox is visible only when device is configured to 4 Enable Signal Mode.
- Assert SW Reset: To perform a complete SW reset to the chip, assert this checkbox. See the LP8756 datasheet for explanation of LP8756 reset scenarios.

NOTE: The recommended start-up sequence for LP8756xQ1 is to first assert NRST, then write all needed configuration bits by using the GUI, and then enable buck regulator(s) by ENx pin or EN_BUCKx bit.

The "Bucks" section provides status information and enable controls for all the 4 buck cores. On the left of the section are the check-boxes for the buck enable bits. The "Mode" field provides information on each of the buck core and can have any of the values given in Table 2:

Table 2. Mode Information

BUCK MODE	
Disabled	Buck state machine in 'disable'
Enabled	Buck state machine in 'enable'

The "Multiphase status" info field tells whether a buck core is configured as a master or a slave. The "Current" field gives the result of the buck converter load current measurement operation. Output currents of each buck core and total output current of master(s) are shown on the fields.

The "System Flags / Interrupts" section as well as the "Interrupt bits" and the "Status bits" sections give data on system faults and warnings. If the interrupt is set for any reason the Interrupt active field shall show ‘1’ on red background. The flag causing the interrupt will also be set on the Main tab. Interrupts on LP8756xQ1 can only be cleared by writing '1’ to associated registers. Any individual flag can be cleared by clicking the "Clear" button next to each flag field. Some of the flags also have a mask bits. If "Mask" check-box of certain flag is checked, the interrupt is not generated. The "Status" bits will show the current status of the faults.

The "Power Good" section is for Power Good pin control and indication. It includes the latched values of buck Power Good Faults. These can be cleared with the Clear -button.

At the bottom of the GUI window is the "Auto Write" checkbox. If "Auto Write" is checked (default) any checking, un-checking or pulldown menu selections will immediately launch I^2C writes to the chip register(s). If not checked, the user can update the chip registers to correspond the configuration selected on the GUI by clicking "Write Registers".

If "Poll Status" is selected the software sends a query to the LP8756 at a fixed interval in order to detect the status of the chip, including operation mode, multi-phase status, and output current. If also the "Poll Only Pins" is selected the software is monitoring only the state of Interrupt and Powergood pins. If "Poll Status" is not selected or if "Poll Only Pins" is selected, user can read the registers by applying "Read Registers". "Bus Speed" pulldown menu selections are given in Table 3 below and is instantly applied for System I^2C.

Table 3. I^2C-Compatible Bus Support

BUS SPEED SELECTION	EXPLANATION
Fast (400 kHz)	Fast I^2C-compliant operation at 400 kHz
High-Speed (3.4 MHz)	HS I^2C-compliant data transfer with master codes.

3.2 Other Tabs and Menus

The "Tools" pulldown menu hosts another way of accessing the LP8756xQ1 registers (see Figure 11). The "Direct Register Access" tool can be used to read or write any register (see Figure 12). Selecting a register, the bits appear on the right side Field View (see Figure 13). When moving mouse over bits in Field View, bits are highlighted in the register view. Bits can be controlled either from register view or field view. Register settings can also be saved to a file or pre-made register file can be loaded in the Direct Register Access tool. Registers can be updated immediately or manually (see Figure 14).

When using direct register access, TI recommends un-checking the poll status check-box. This way the GUI will only do the reads and writes commanded from the direct access dialog.

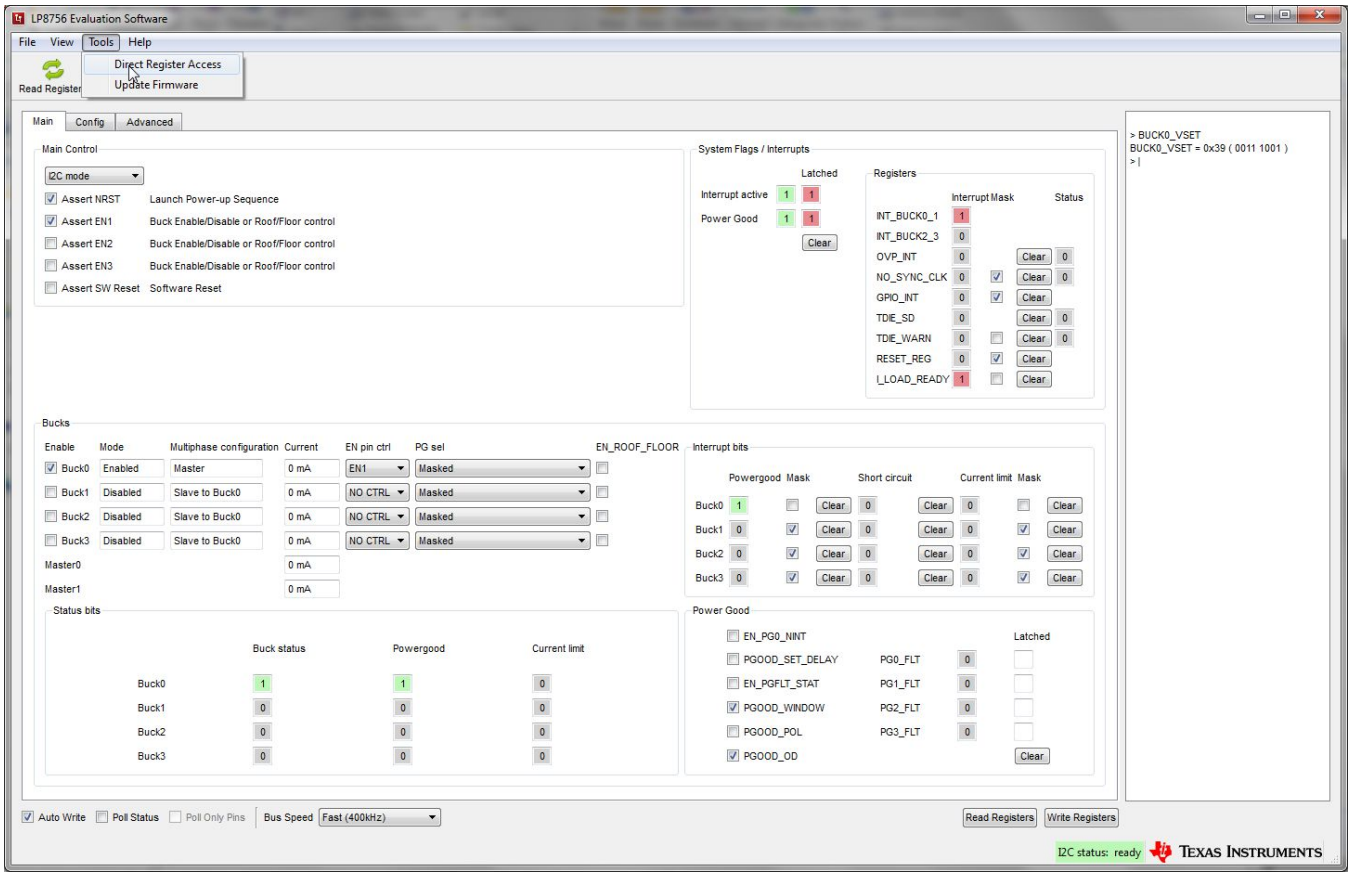
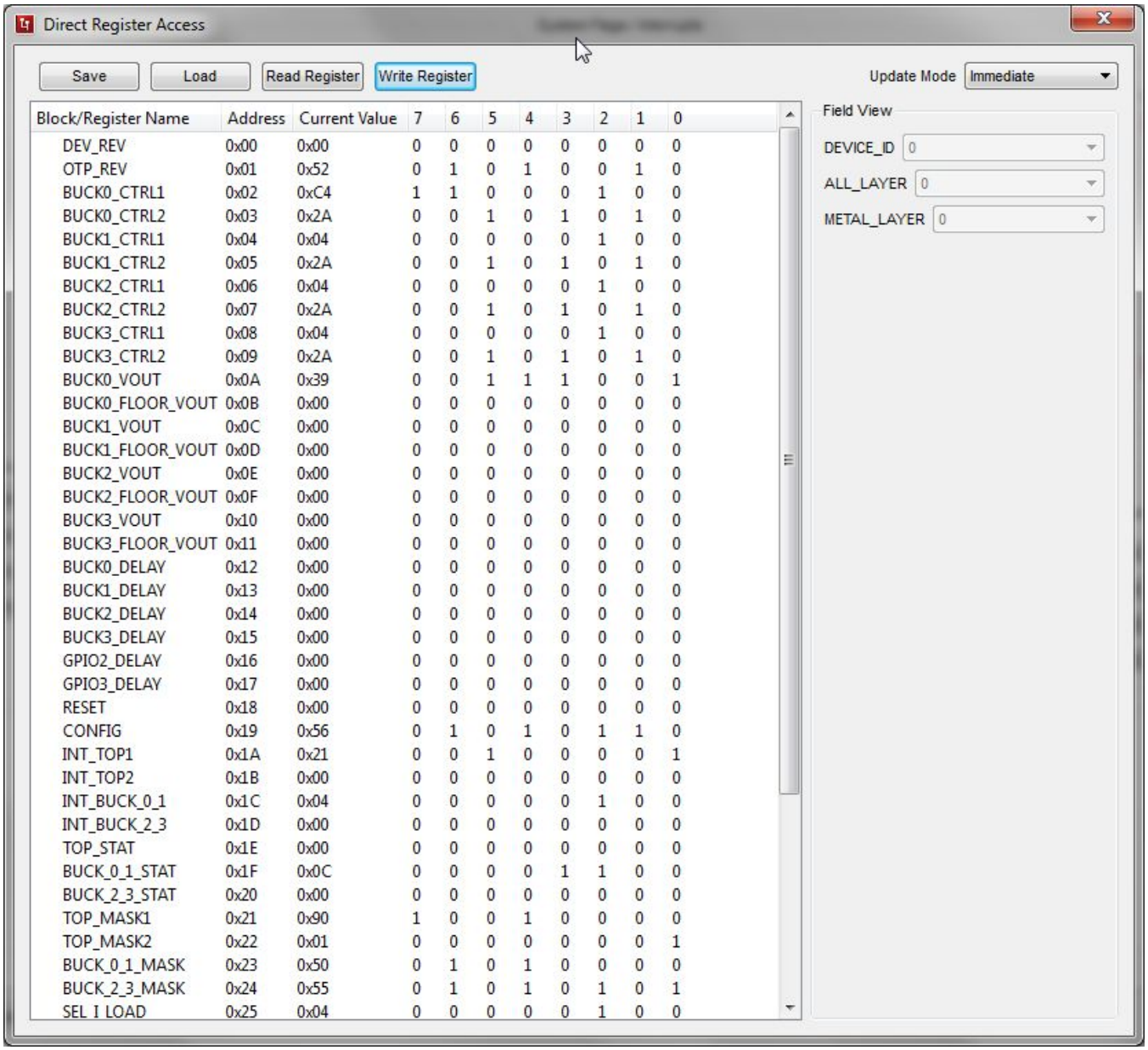


Figure 11. Accessing Direct Register Write



Block/Register Name	Address	Current Value	7	6	5	4	3	2	1	0
DEV_REV	0x00	0x00	0	0	0	0	0	0	0	0
OTP_REV	0x01	0x52	0	1	0	1	0	0	1	0
BUCK0_CTRL1	0x02	0xC4	1	1	0	0	0	1	0	0
BUCK0_CTRL2	0x03	0x2A	0	0	1	0	1	0	1	0
BUCK1_CTRL1	0x04	0x04	0	0	0	0	0	1	0	0
BUCK1_CTRL2	0x05	0x2A	0	0	1	0	1	0	1	0
BUCK2_CTRL1	0x06	0x04	0	0	0	0	0	1	0	0
BUCK2_CTRL2	0x07	0x2A	0	0	1	0	1	0	1	0
BUCK3_CTRL1	0x08	0x04	0	0	0	0	0	1	0	0
BUCK3_CTRL2	0x09	0x2A	0	0	1	0	1	0	1	0
BUCK0_VOUT	0x0A	0x39	0	0	1	1	1	0	0	1
BUCK0_FLOOR_VOUT	0x0B	0x00	0	0	0	0	0	0	0	0
BUCK1_VOUT	0x0C	0x00	0	0	0	0	0	0	0	0
BUCK1_FLOOR_VOUT	0x0D	0x00	0	0	0	0	0	0	0	0
BUCK2_VOUT	0x0E	0x00	0	0	0	0	0	0	0	0
BUCK2_FLOOR_VOUT	0x0F	0x00	0	0	0	0	0	0	0	0
BUCK3_VOUT	0x10	0x00	0	0	0	0	0	0	0	0
BUCK3_FLOOR_VOUT	0x11	0x00	0	0	0	0	0	0	0	0
BUCK0_DELAY	0x12	0x00	0	0	0	0	0	0	0	0
BUCK1_DELAY	0x13	0x00	0	0	0	0	0	0	0	0
BUCK2_DELAY	0x14	0x00	0	0	0	0	0	0	0	0
BUCK3_DELAY	0x15	0x00	0	0	0	0	0	0	0	0
GPIO2_DELAY	0x16	0x00	0	0	0	0	0	0	0	0
GPIO3_DELAY	0x17	0x00	0	0	0	0	0	0	0	0
RESET	0x18	0x00	0	0	0	0	0	0	0	0
CONFIG	0x19	0x56	0	1	0	1	0	1	1	0
INT_TOP1	0x1A	0x21	0	0	1	0	0	0	0	1
INT_TOP2	0x1B	0x00	0	0	0	0	0	0	0	0
INT_BUCK_0_1	0x1C	0x04	0	0	0	0	0	1	0	0
INT_BUCK_2_3	0x1D	0x00	0	0	0	0	0	0	0	0
TOP_STAT	0x1E	0x00	0	0	0	0	0	0	0	0
BUCK_0_1_STAT	0x1F	0x0C	0	0	0	0	1	1	0	0
BUCK_2_3_STAT	0x20	0x00	0	0	0	0	0	0	0	0
TOP_MASK1	0x21	0x90	1	0	0	1	0	0	0	0
TOP_MASK2	0x22	0x01	0	0	0	0	0	0	0	1
BUCK_0_1_MASK	0x23	0x50	0	1	0	1	0	0	0	0
BUCK_2_3_MASK	0x24	0x55	0	1	0	1	0	1	0	1
SEL_I_LOAD	0x25	0x04	0	0	0	0	0	1	0	0

Figure 12. Direct Register Access View

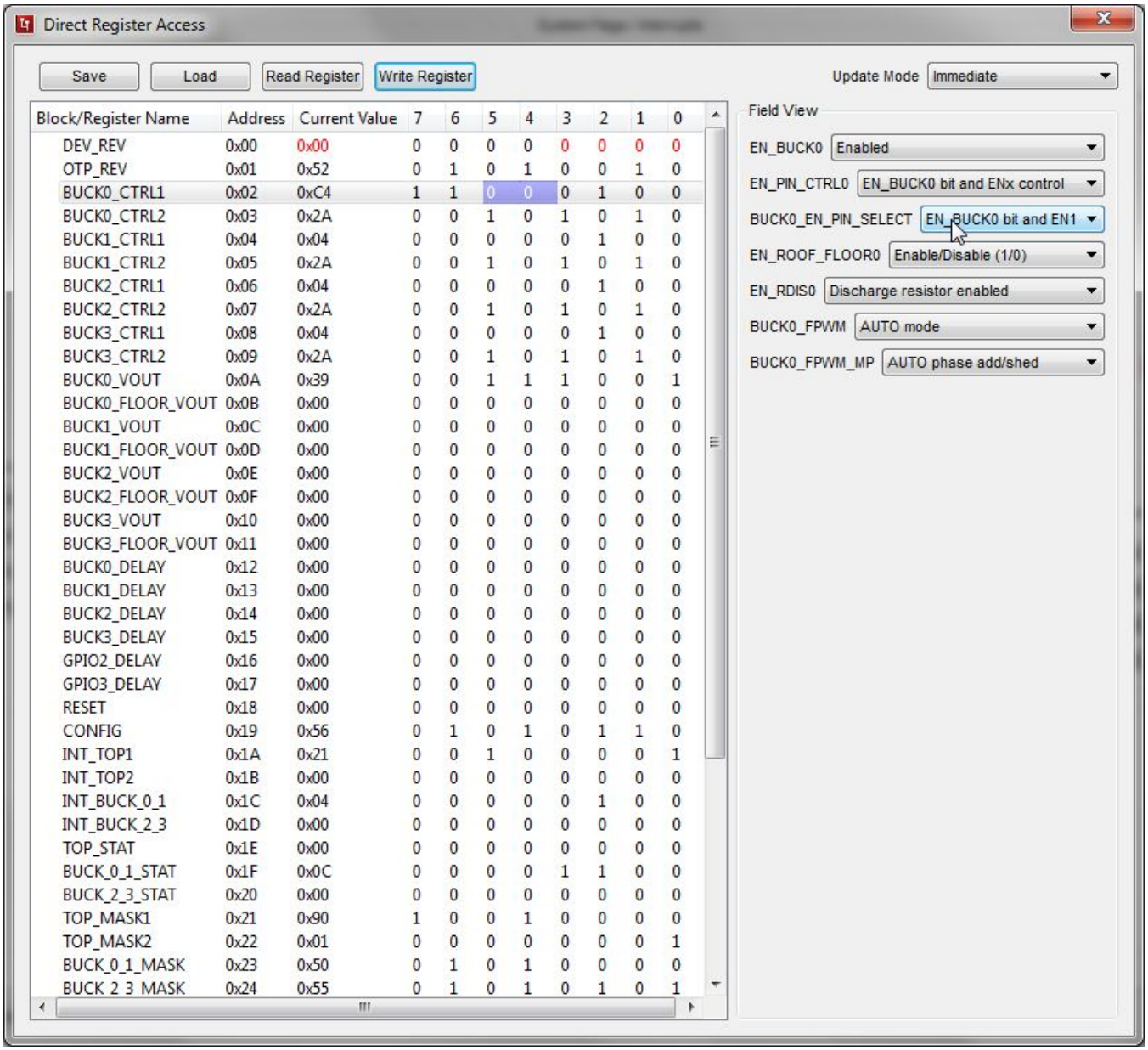


Figure 13. Selecting Register Values

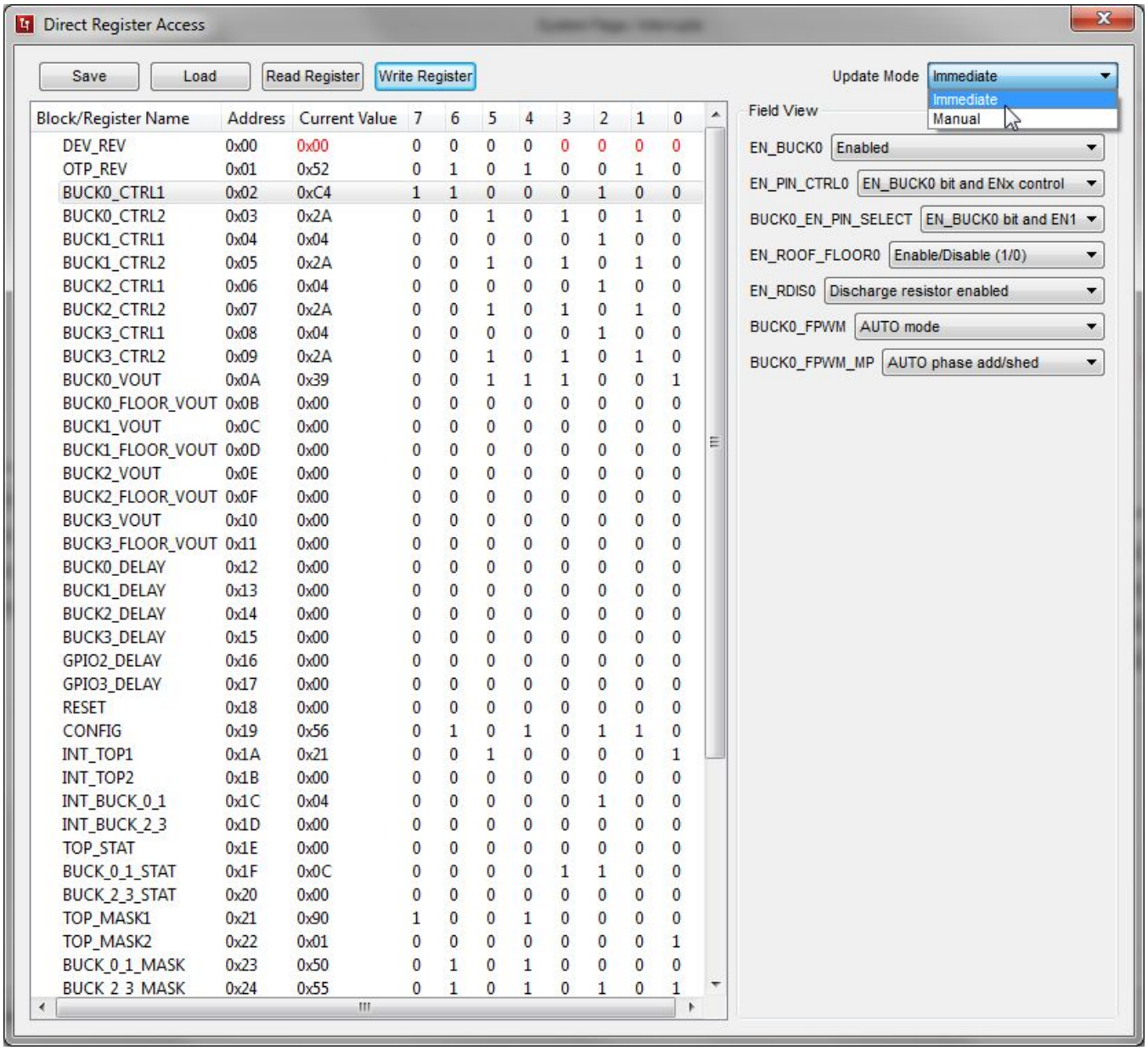


Figure 14. Register Update Mode

The "Config" and "Advanced" tabs provide the user with pulldown menus and check-boxes for the part of the register space that is not covered by the Main tab, such as output voltage control. These controls are self-explanatory. Refer to the LP8756xQ1 data sheet for explanation of the functions. See following images for reference of the Config and Advanced tabs.

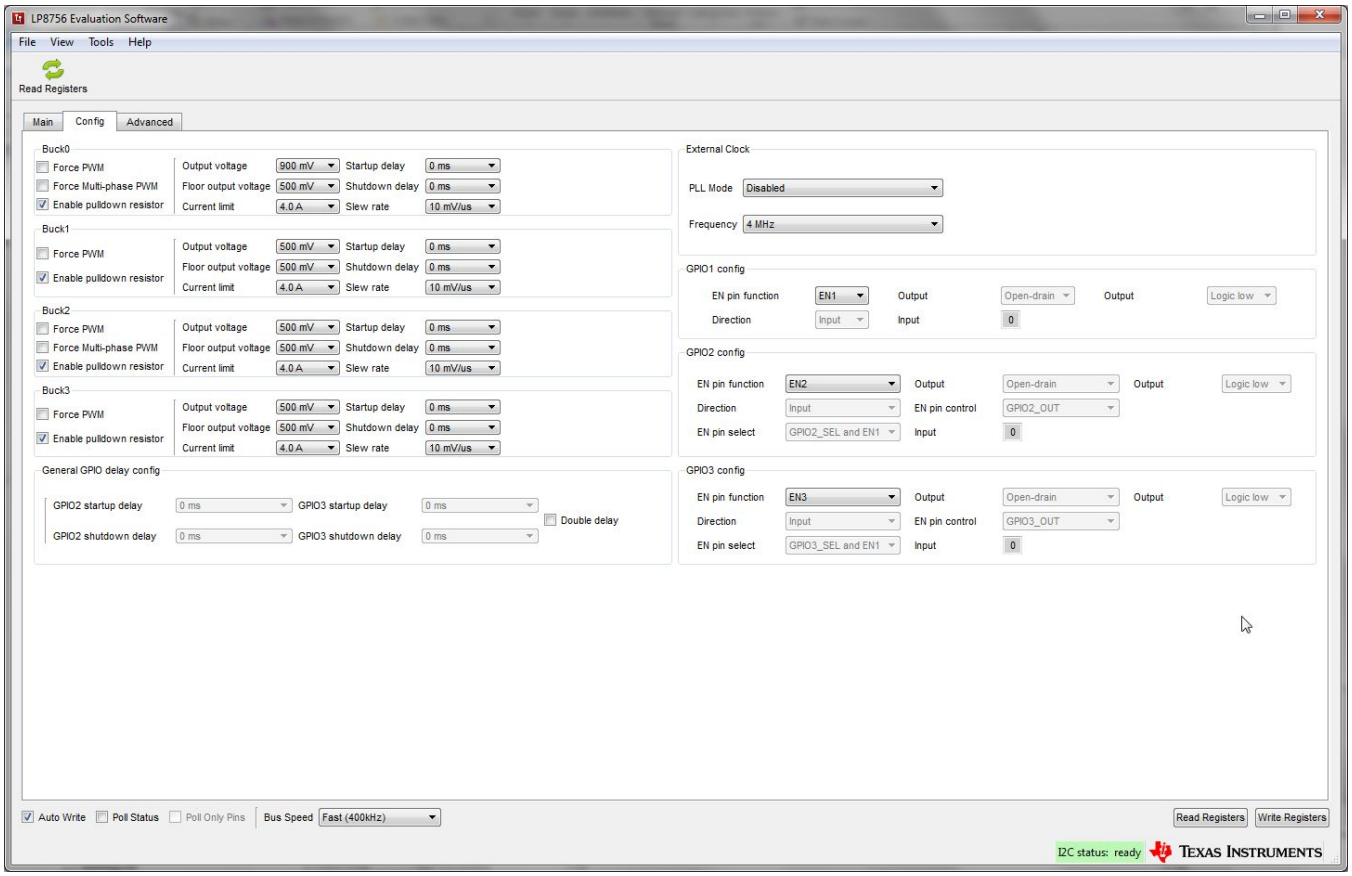


Figure 15. Config Tab of the LP8756 GUI

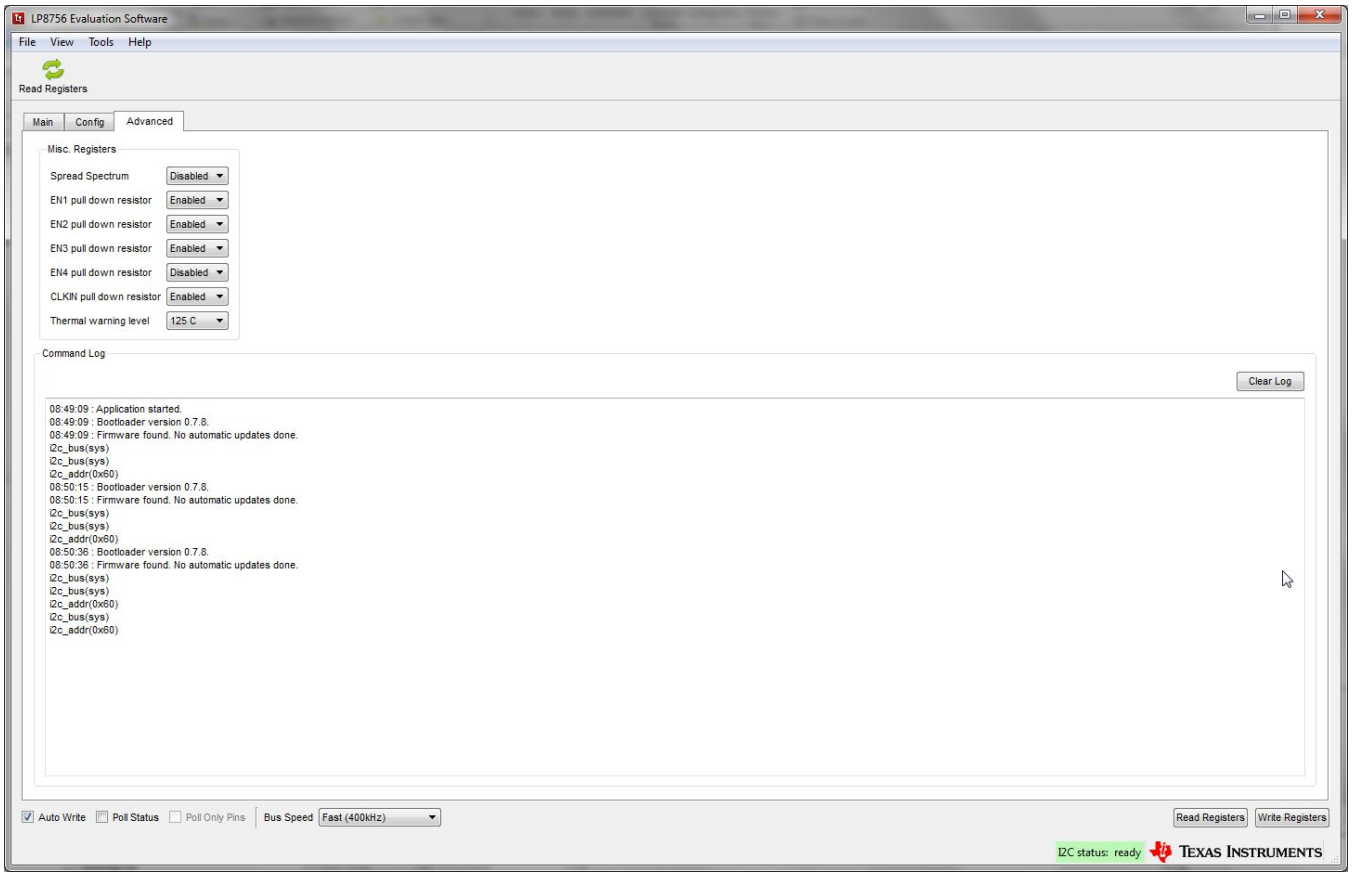


Figure 16. Advanced Tab of LP8756 GUI

3.3 Console

To show or hide the console, toggle the option in the View pulldown menu (see Figure 17). The console can be used to access the LP8756 registers. Registers can be read or written simply by referring to the logical registers by their name. See an example Figure 18. The console has a number of integrated macros that are listed in Table 4.

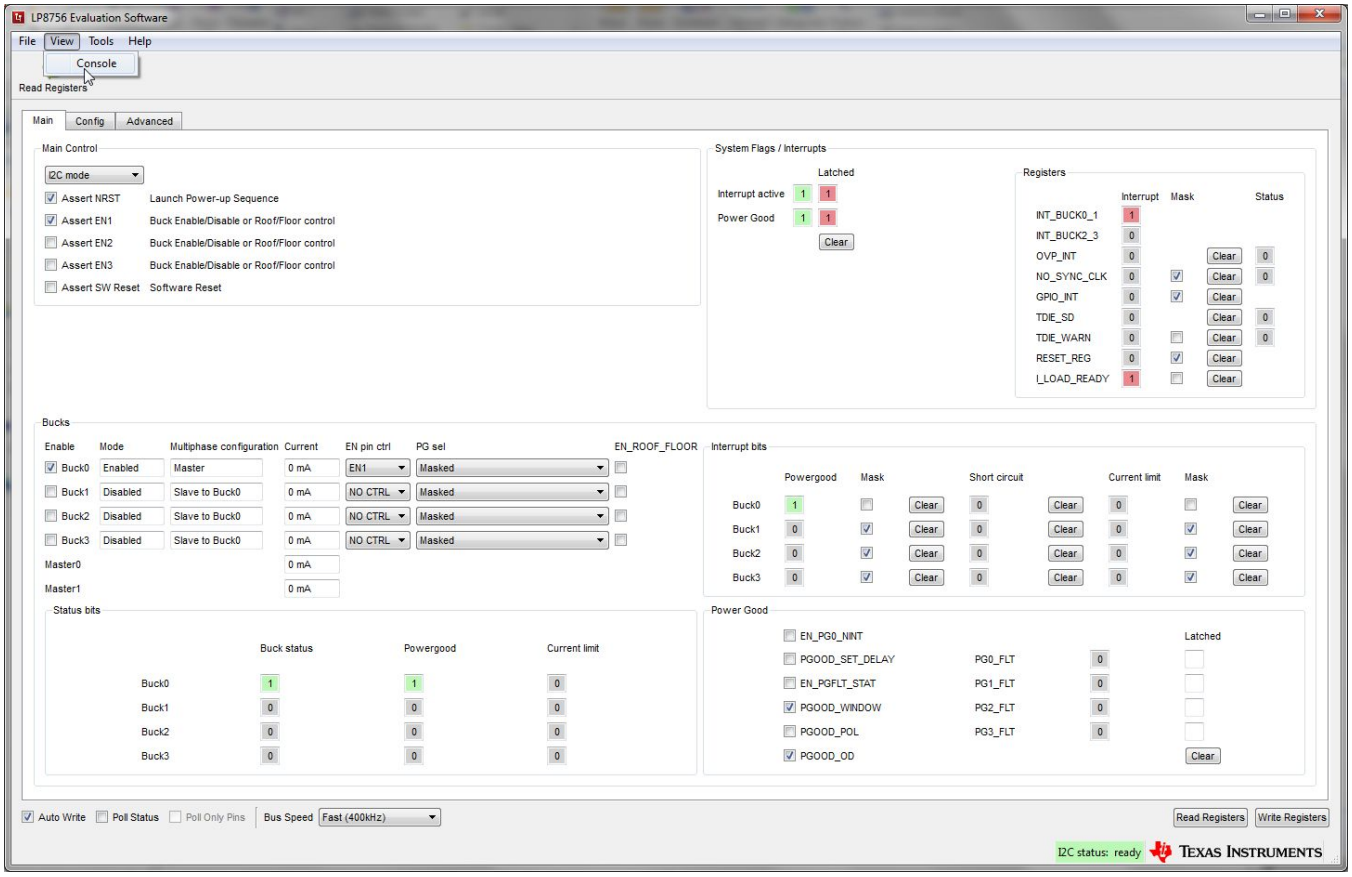


Figure 17. Opening Console

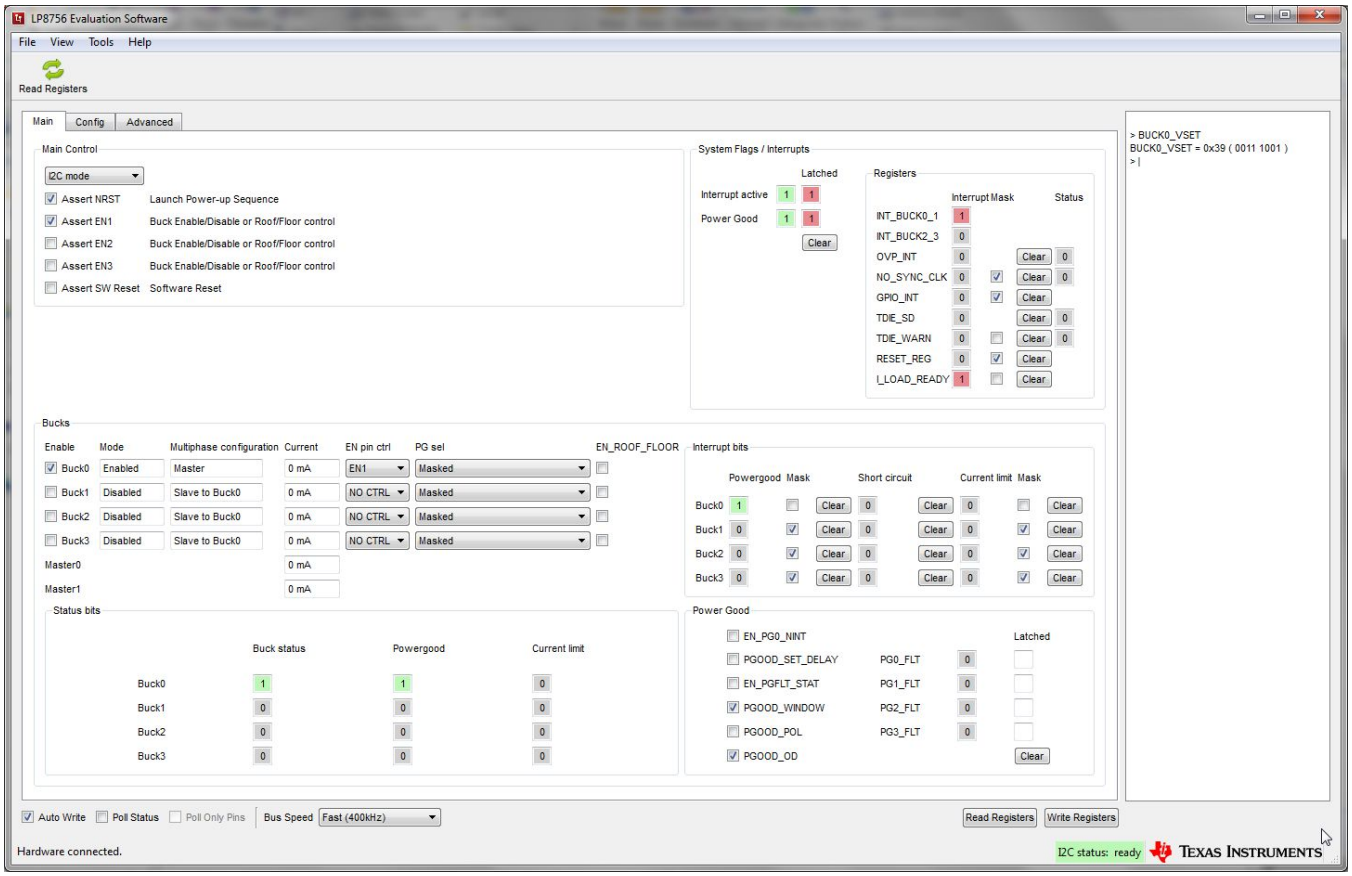


Figure 18. Example of Command Use in Console

Table 4. Console Macros

Command	Parameters	Explanation
register_name	= register value | -	Write a value to writable I²C register or logical register. If no parameter given, will return the current register value. The logical register names are the same as given in the data sheet, and must be in uppercase. Example: BUCK0_VSET = 40
wait	(time)	Wait for time given in ms. Useful in loops.
iout	(buck number)	Returns the measured load current of the chosen buck core.
0x	address = data or address[bits] = data	I²C read or write command. addr = value examples: 0x12 = 0xaa 0x12[7] = 1 0x12[3:0] = 15

The console supports use of scripts. If a text file containing commands supported by the console is stored in the same folder with the evaluation software executable, then the script can be launched from the console by typing the text file name, like script.txt.

4 Bill of Materials

Table 5 lists EVM bill of materials. This includes all output configurations listed in Table 1. Differences are in device settings, placement of the output shunts (J01, J021, J022, J23) and the feedback connections. See Section 6 for these configuration specific assembly details.

NOTE: The LP8756xQ1 I/O lines are connected to the microcontroller through 0-Ω resistors. These resistors are assembled to match the default I/O configuration of the LP8756xQ1. If ENx/GPIOx or PGOOD pins are configured as push-pull outputs, corresponding 0-Ω resistors (R18, R20, R21, R22) must be removed to prevent possible damage to the microcontroller I/O pins. In open-drain configuration the microcontroller internal pullups are enabled by the GUI and pullup resistors R7 to R13 are not needed. See also for reference.

Table 5. Bill of Materials for LP8756xQ1EVM

Designator	Description	Manufacturer	Part Number	Qty.
PCB	Printed Circuit Board	Any	SV601325	1
C0, C0_1, C1, C1_1, C2, C2_1, C3, C3_1, C33, C34	CAP, CERM, 22uF, 10V, X7R, 10%, 1206	MuRata	GCM31CR71A226KE02	10
C0_2, C1_2, C2_2, C3_2, C32	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C104KA01D	5
C0_3, C1_3, C2_3, C3_3	CAP, CERM, 3300 pF, 50 V, +/- 10%, X7R, 0402	MuRata	GRM155R71H332KA01D	4
C4, C5, C6, C7	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805_140	MuRata	GCM21BR71A106KE22L	4
C8, C14, C18, C24, C28	CAP, CERM, 0.1 µF, 16 V, +/- 5%, X7R, 0402	MuRata	GRM155R71C104JA88D	5
C9, C10, C19, C20	CAP, CERM, 390 pF, 50 V, +/- 10%, X7R, 0402	MuRata	GRM155R71H391KA01D	4
C11, C15, C21, C25	CAP, CERM, 6800 pF, 50 V, +/- 10%, X7R, 0402	MuRata	GRM155R71H682KA88D	4
C12, C13, C16, C17, C22, C23, C26, C27	CAP, CERM, 100 µF, 6.3 V, +/- 20%, X5R, 0805	MuRata	GRM21BR60J107M	8
C30	CAP, TA, 220 µF, 10 V, +/- 10%, 0.05 ohm, SMD	AVX	TPSD227K010R0050	1
C31	CAP, CERM, 100 µF, 6.3 V, +/- 20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	1
C36, C54	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H100JA01D	2
C37, C38	CAP, CERM, 15 pF, 100 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C2A150JA01D	2
C39, C41, C42, C43, C44, C45, C46, C48, C50, C51, C52, C53, C56	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	MuRata	GRM188R71E104KA01D	13
C40, C47, C49, C57	CAP, CERM, 10 µF, 16 V, +/- 20%, X5R, 0603	Taiyo Yuden	EMK107BBJ106MA-T	4
C55	CAP, CERM, 10 µF, 16 V, +/- 10%, X5R, 0805	Taiyo Yuden	EMK212BJ106KG-T	1
C58, C59, C60, C61	CAP, CERM, 1 µF, 25 V, +/- 10%, X5R, 0603	MuRata	GRM188R61E105KA12D	4
C62	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X5R, 0603	MuRata	GRM188R61H103KA01D	1
D1	Diode, Zener, 5.6V, 5W, SMB	Micro Commercial Components	SMBJ5339B-TP	1
D2	Diode, Schottky, 30 V, 0.2 A, SOD-323	Diodes Inc.	BAT42WS-7-F	1
FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	3
H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead		NY PMS 440 0025 PH	4

Table 5. Bill of Materials for LP8756xQ1EVM (continued)

Designator	Description	Manufacturer	Part Number	Qty.
H7, H8, H9, H10	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
J0A, J1B, J2, J2B, J3B, J5	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	1 - 6
J01, J021, J022, J23	JUMPER TIN SMD	Harwin	S1911-46R	0 - 4
J1	Header, 100mil, 2x2, Gold, TH	Samtec	TSW-102-07-G-D	1
J3, J7, J8, TP21	Header, 100mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	4
J9	Connector, Receptacle, Mini-USB Type B, R/A, Top Mount SMT	TE Connectivity	1734035-2	1
J10	Header, 100mil, 3x1, Gold, TH	Samtec	HTSW-103-07-G-S	1
L0, L1, L2, L3	Inductor, Shielded, 470 nH, 4.7 A, 0.021 ohm, SMD	MuRata Toko	DFE252012PD-R47M	4
L4, L5, L6, L7	Ferrite Bead, 30 ohm @ 100 MHz, 4 A, 0805	MuRata	BLM21PG300SH1D	4
L8	Inductor, Wirewound, Ferrite, 10 µH, 0.12 A, 0.5 ohm, SMD	Taiyo Yuden	LB2012T100KR	1
LBL1	Thermal Transfer Printable Labels, 1.250" W x 0.250" H - 10,000 per roll	Brady	THT-13-457-10	1
R1, R2, R3, R4	RES, 3.9, 5%, 0.125 W, 0805	Vishay-Dale	CRCW08053R90JNEA	4
R5	RES, 0.01, 1%, 3 W, 2512	Bourns	CRA2512-FZ-R010ELF	1
R14, R15, R16, R17, R18, R20, R21, R22	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	8
R24	RES, 6.80 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-076K8L	1
R25, R26	RES, 39.0, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0739RL	2
R27	RES, 68.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0768KL	1
R28	RES, 33.0 k, 1%, 0.1 W, 0603	Yageo America	RC0603FR-0733KL	1
R29	RES, 1.00, 1%, 0.1 W, 0603	Yageo America	RC0603FR-071RL	1
R30	RES, 470 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW0603470KJNEA	1
R31, R32	RES, 1.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	2
SH-J1, SH-J2, SH-J3, SH-J4	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA	4
TP5, TP6, TP8, TP9, TP10, TP11, TP12, TP13, TP16, TP17, TP18, TP19, TP20	Test Point, TH, Miniature, Yellow	Keystone	5004	13
TP14, TP15	Terminal, Turret, TH, Double	Keystone	1502-2	2
U1	Four-Phase Buck Converter Up to 16-A Total Current With Integrated Switches, RNF0026C	Texas Instruments	LP87561DRNFRQ1 (4-ph) LP87562ARNFRQ1 (3+1) LP87563BRNFRQ1 (2+1+1) LP87564FRNFRQ1 (4 x 1) LP87565ARNFRQ1 (2 + 2)	1
U2	AT91SAM ARM-based Flash MCU, LQFP100	Atmel	ATSAM3U2CA-AU	1
U3	Dual Linear Regulator with 300mA and 150mA Outputs and Power-On-Reset, 10-pin WSON, Pb-Free	Texas Instruments	LP3996SD-1833/NOPB	1
X1, X7, X8, X9, X10	Terminal Block, 5.08 mm, 2x1, TH	Phoenix Contact	1715721	5
X2	Terminal Block, 8x1, 2.54 mm, TH	Phoenix Contact	1725711	1
X3, X5	Terminal Block, 100mil, 2x1, 6A, 63V, TH	Phoenix Contact	1725656	2
Y1	Crystal, 12Mhz, 18pF, SMD	AVX	CX5032GB12000H0PESZZ	1
C29, C35	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	MuRata	GRM188R71C104KA01D	0
H5, H6	Standard Shield Cover, 26.67 x 26.67 mm	Laird-Signal Integrity Products	BMI-S-203-C	0
H11, H12	Standard Surface Mount Shield , 26.21 x 26.21 mm, Height 5.08mm	Laird-Signal Integrity Products	BMI-S-203-F	0

Table 5. Bill of Materials for LP8756xQ1EVM (continued)

Designator	Description	Manufacturer	Part Number	Qty.
J1A, J2A, J3A, J4	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0 - 4
R6, R19	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0
R7, R8, R9, R10, R11, R12, R13	RES, 1.8 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06031K80JNEA	0
R23	RES, 50, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060350R0FKEA	0
TP1, TP2, TP3, TP4, TP7	Header, 100mil, 2x1, Gold, TH	Samtec	TSW-102-07-G-S	0
X4, X6	Receptacle, 2.5mm, 3x2, Gold, SMT	TE Connectivity	6651712-1	0

5 Board Layout

This section describes the board layout of the LP8756xQ1EVM. See the LP8756xQ1 data sheet for specific PCB layout recommendations.

The board is constructed on a 6-layer PCB. using 60-µm copper on top and bottom layers to reduce resistance and improve heat transfer. Similar layout can be done as a 4-layer board but 6 layers were chosen to improve grounding and reduce DC resistance.

Board stack-up is shown in Figure 19. Figure 20 shows the top view of the entire board and Figure 21 through Figure 28 show the component placement, layout, and 3D view close to the LP8756 device.

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.020mm	3.5	
3	Top Layer	Copper	0.060mm		
4	Dielectric1	FR-4	0.063mm	4.2	
5	MidLayer1	Copper	0.035mm		
6	Dielectric2	FR-4	0.254mm	4.2	
7	Midlayer2	Copper	0.035mm		
8	Dielectric3	FR-4	0.127mm	4.2	
9	MidLayer3	Copper	0.036mm		
10	Dielectric4	FR-4	0.254mm	4.2	
11	Midlayer4	Copper	0.036mm		
12	Dielectric5	FR-4	0.063mm	4.2	
13	Bottom Layer	Copper	0.060mm		
14	Bottom Solder	Solder Resist	0.020mm	3.5	
15	Bottom Overlay				

Figure 19. Board Stack-Up

The design utilizes dual side placement of the components. This allows placement of the inductors next to the LP8756xQ1 device for reducing SW node area for improved efficiency and reduced EMI. SW nets have also snubber components to reduce SW pin spiking and EMI. The input capacitors can be placed very close to the LP8756xQ1 device, to bottom side, to keep parasitic inductances low, and there is also space for input filters for further EMI reduction. With these modifications, the EVMs can pass CISPR25 radiated and conducted EMI test without (optional) EMI shields H5 and H6.

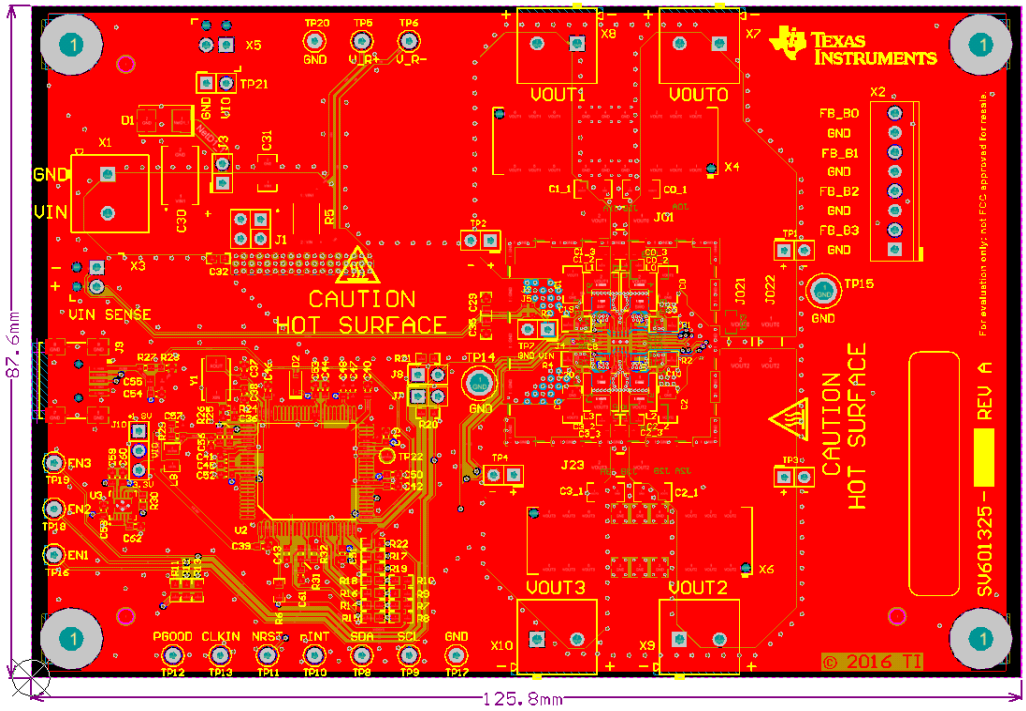


Figure 20. Top View of the LP8756xQ1EVM

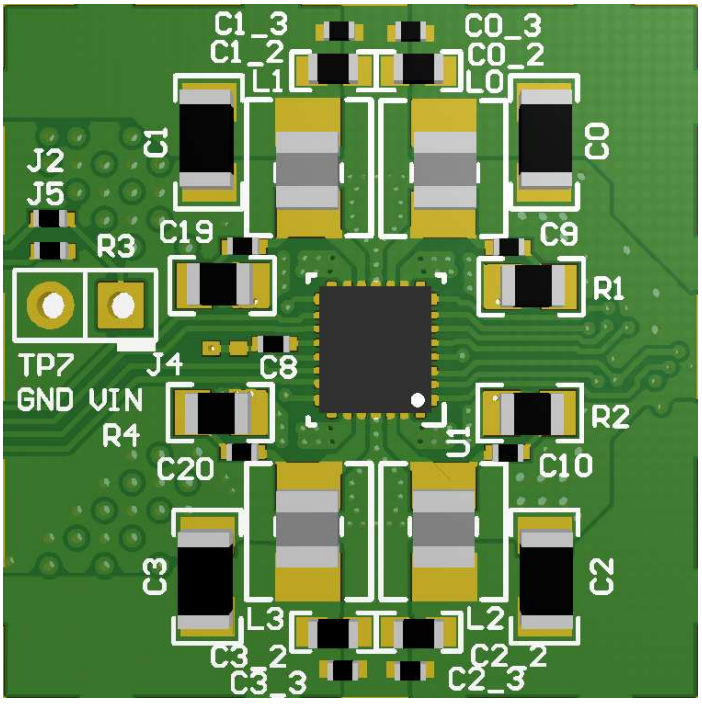


Figure 21. Component Placement Top Layer

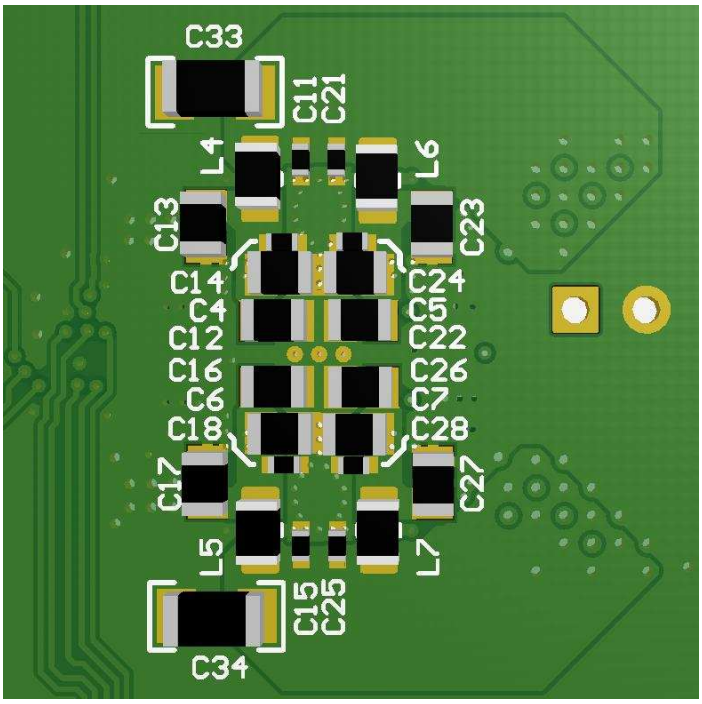
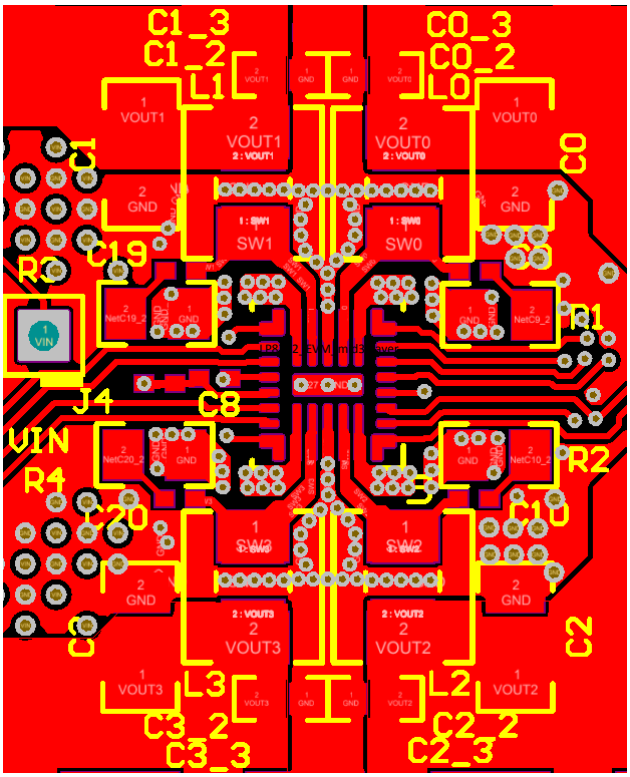
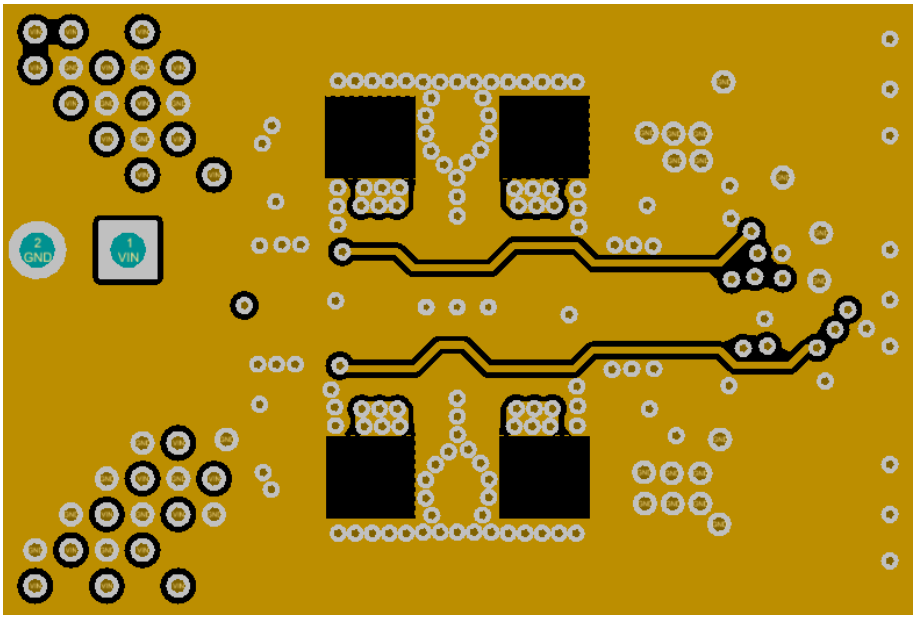


Figure 22. Component Placement Bottom Layer



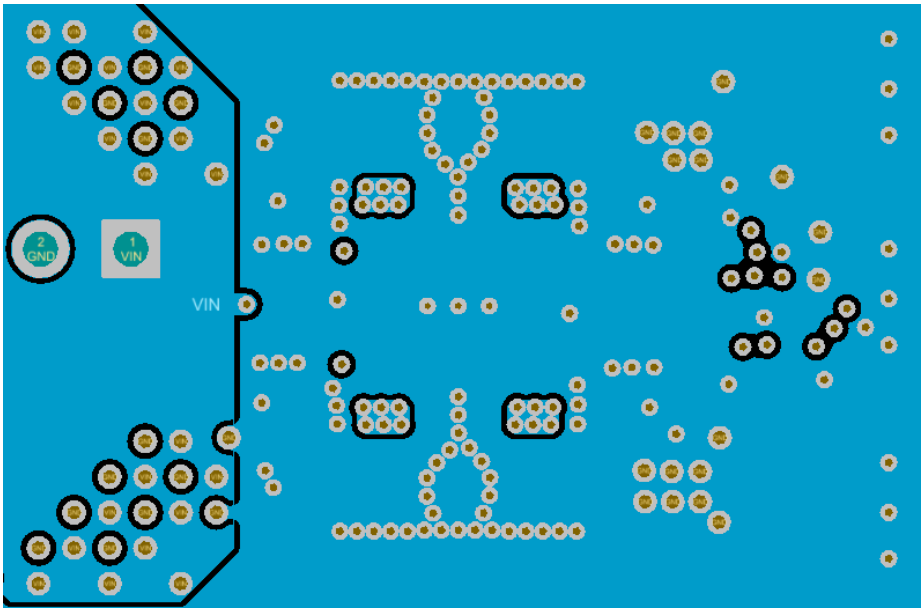
VIN nets are connected to bottom layer with multiple vias. This allows closer placement of the inductors, thus reducing SW node size and EMI. Also snubber circuits are placed next to SW nets for EMI reduction. Multiple GND vias are used to provide solid ground around the LP8756xQ1 device.

Figure 23. Top Layer



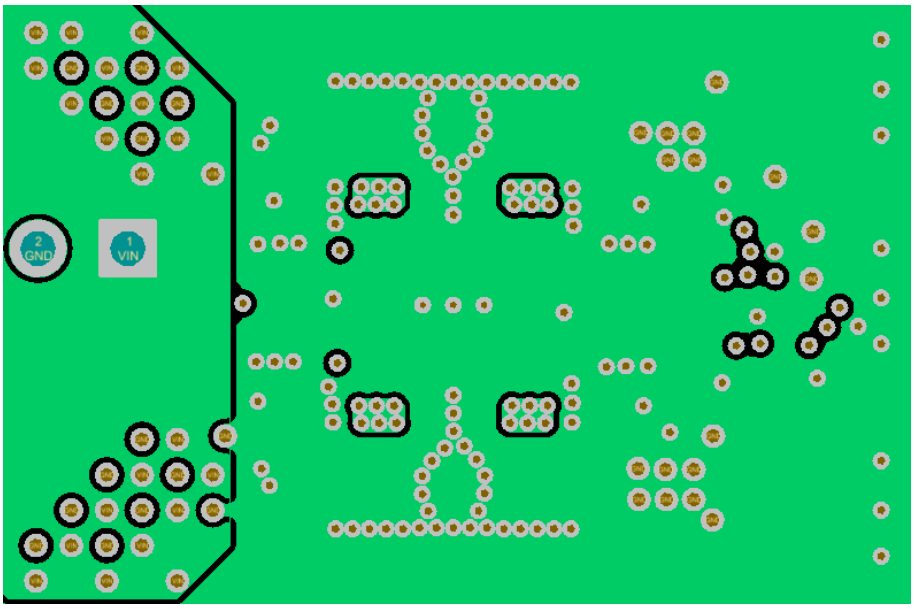
GND plane close to top layer (0.063 mm) helps to reduce parasitic inductance. Holes in the plane are under inductor footprint (SW node) to reduce parasitic capacitance of the SW node, thus reducing noise coupling and improving efficiency.

Figure 24. Mid-Layer1



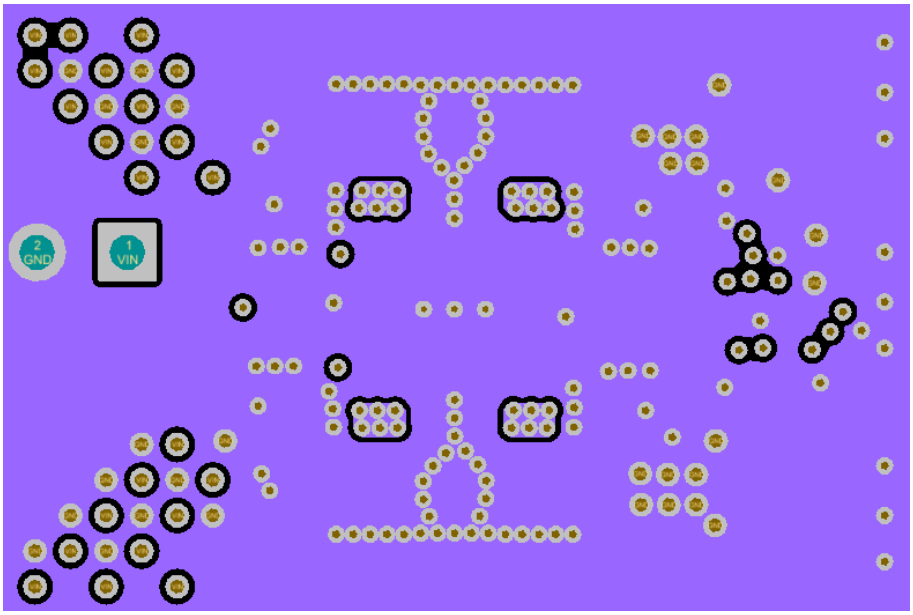
VIN supply is routed in this layer between the ground planes to reduce radiated emissions. VIN and GND vias are placed in hatched pattern to avoid large gaps in these planes.

Figure 25. Mid-Layer2



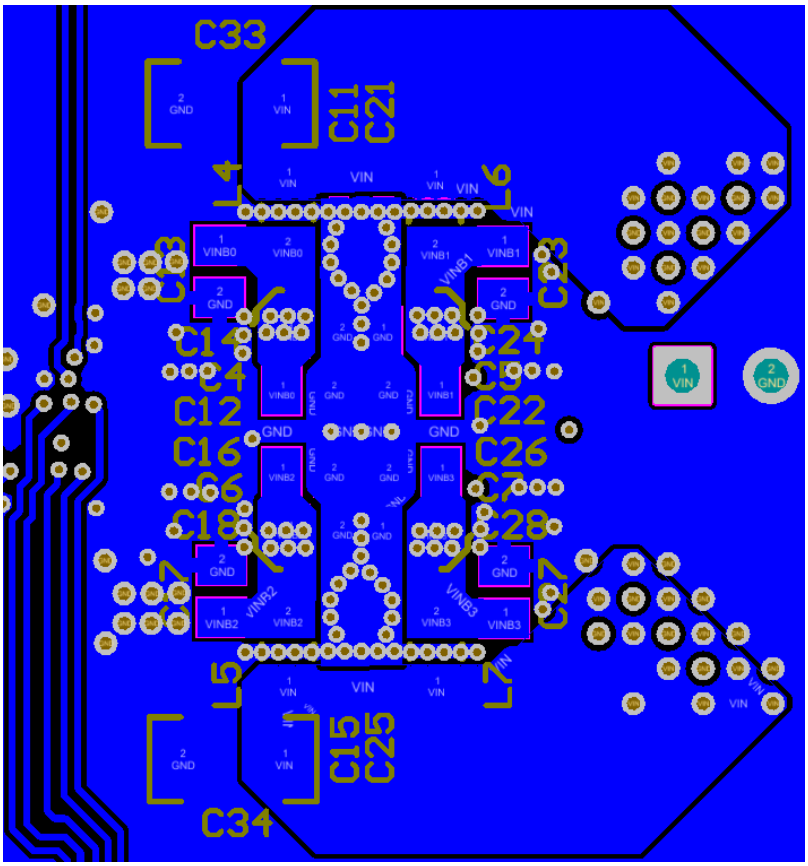
This layer is similar to mid-layer2 to reduce resistance of the VIN net.

Figure 26. Mid-Layer3



Placed close to bottom layer (0.063 mm) to reduce parasitic inductance.

Figure 27. Mid-Layer4, GND Plane



Input capacitors and filters are placed under the LP8756xQ1 into bottom layer. This allows closer placement of the inductors and input components reducing SW and VIN net areas and improving EMI.

Figure 28. Bottom Layer (note mirror view)

6 LP8756xQ1EVM Schematics

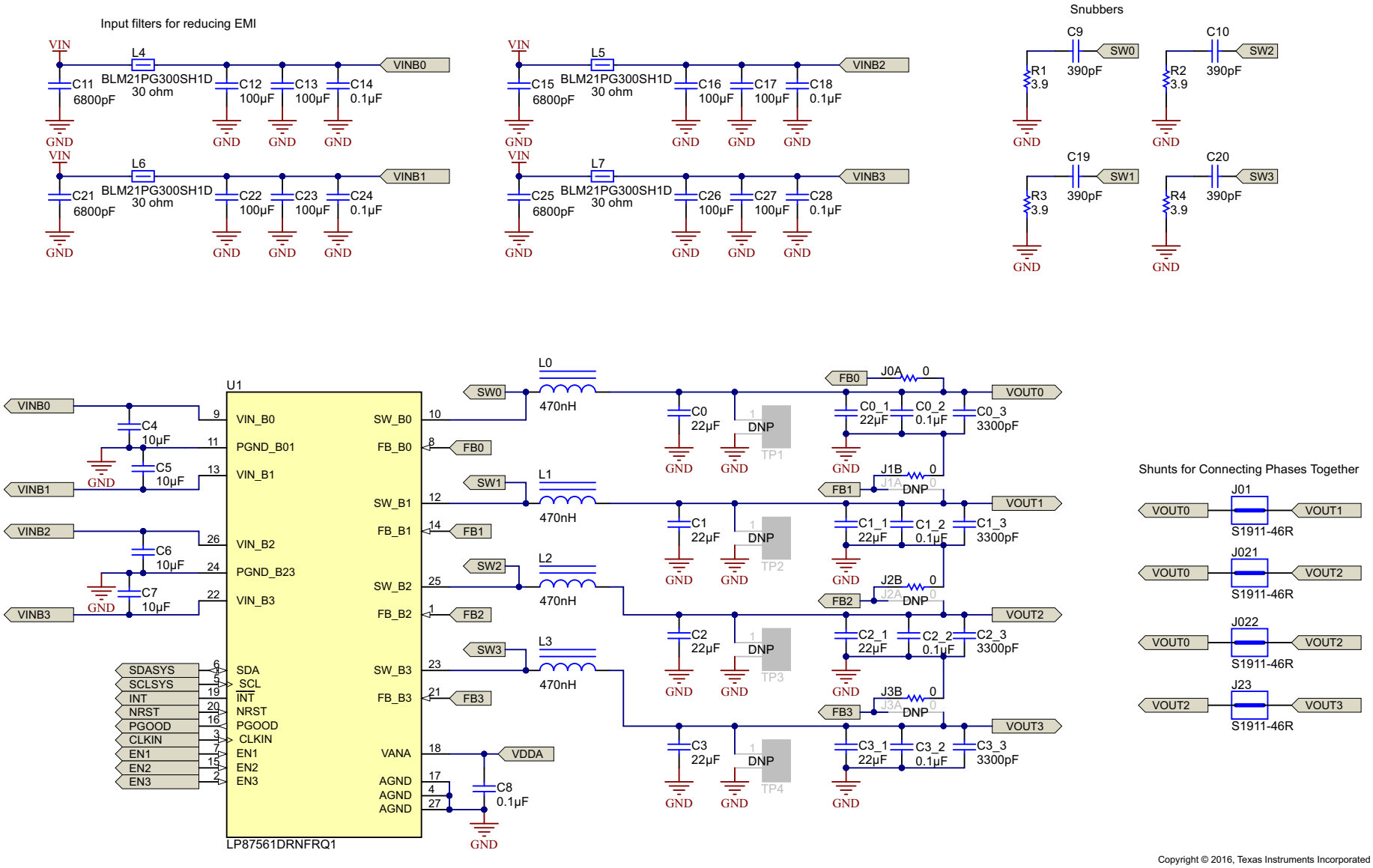


Figure 29. LP87561Q1EVM Schematic

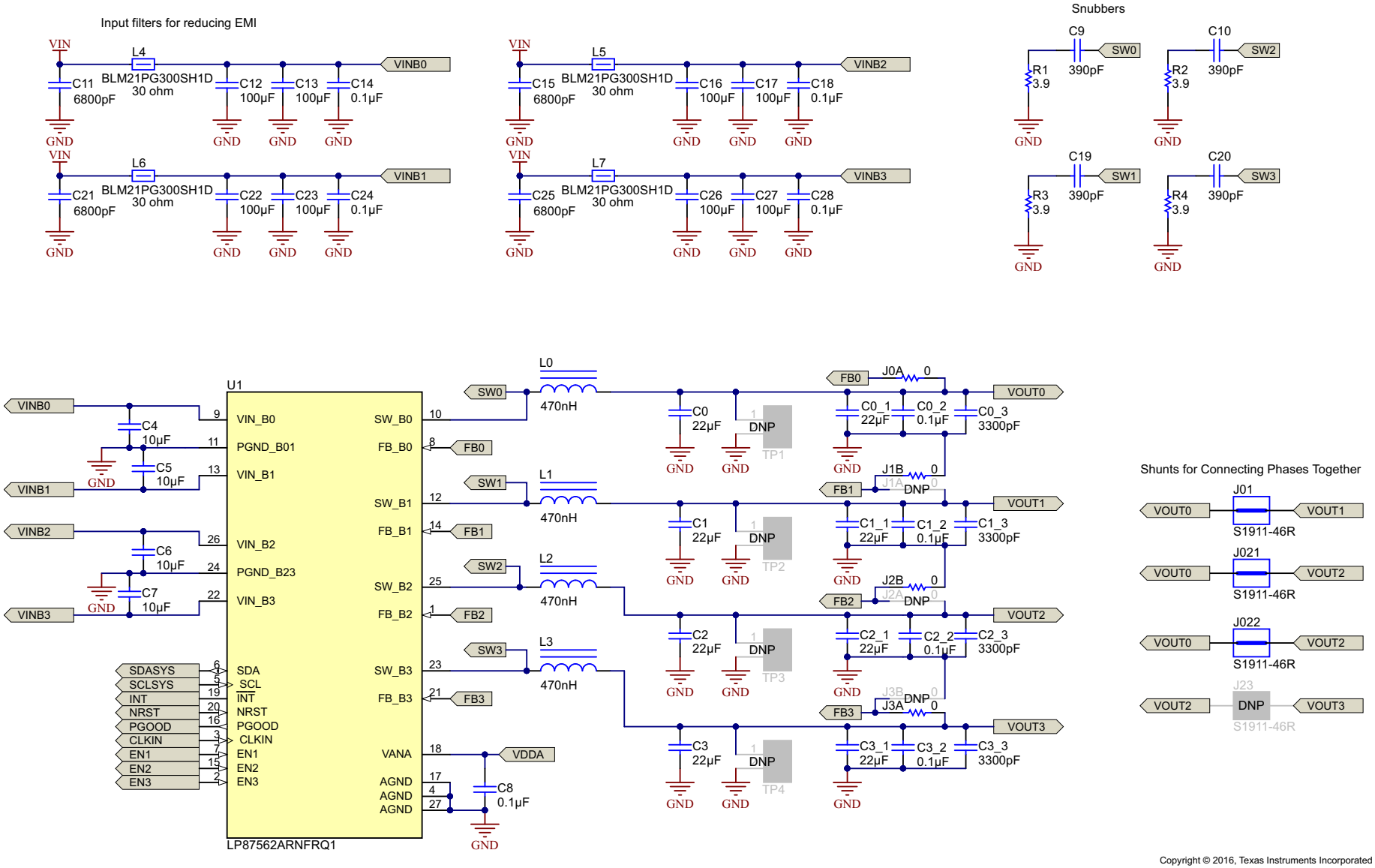


Figure 30. LP87562Q1EVM Schematic

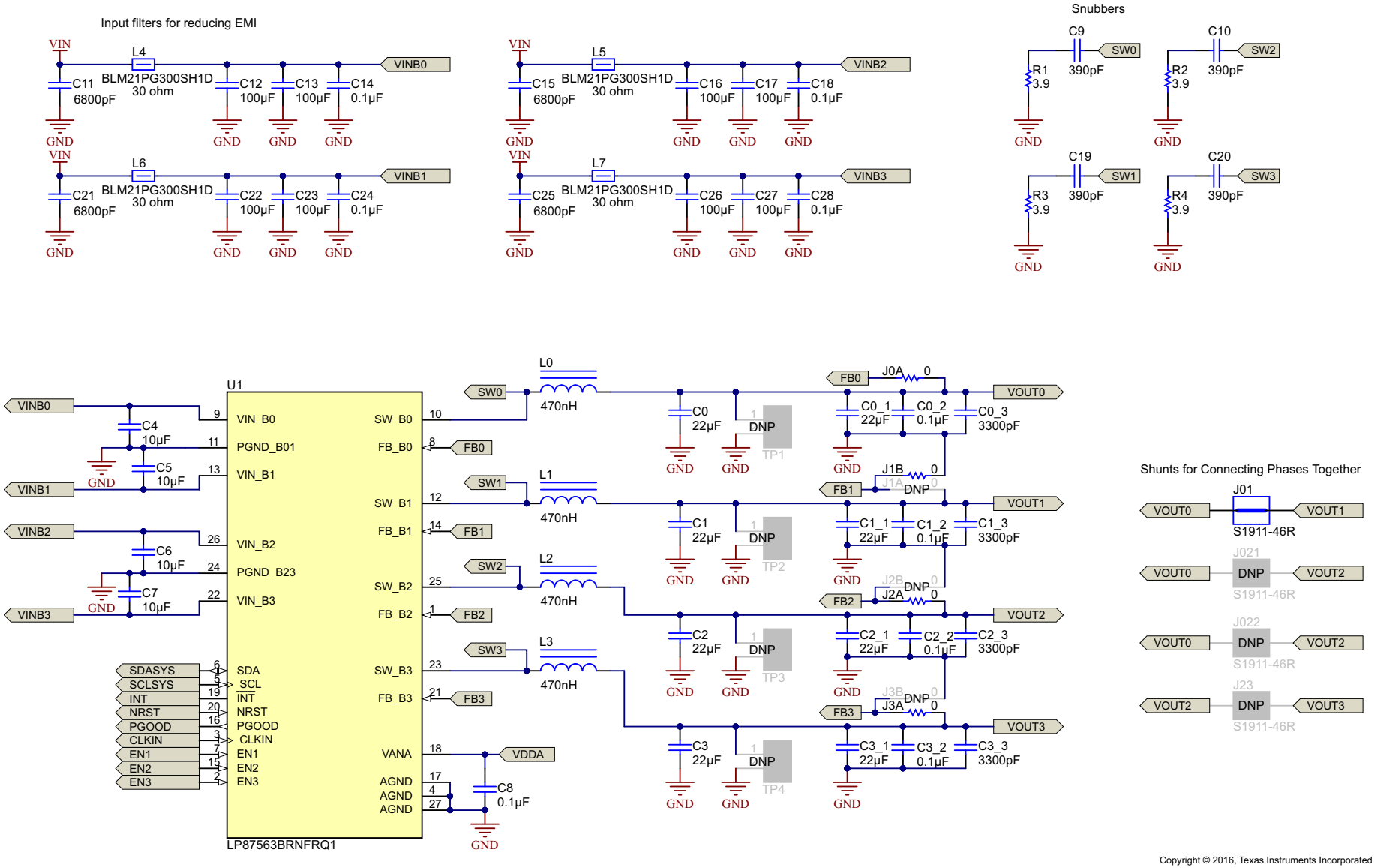


Figure 31. LP87563Q1EVM

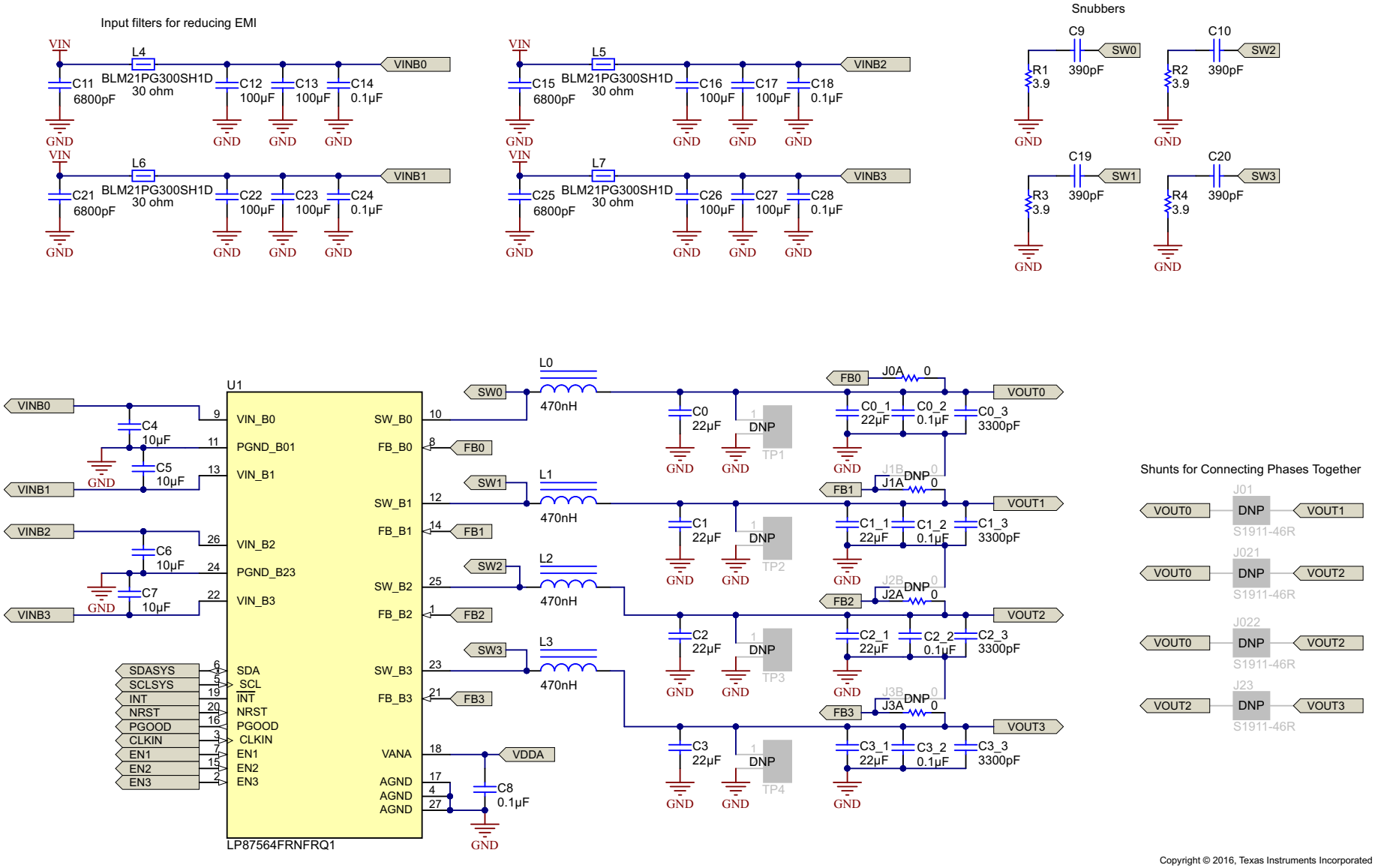


Figure 32. LP87564Q1EVM Schematic

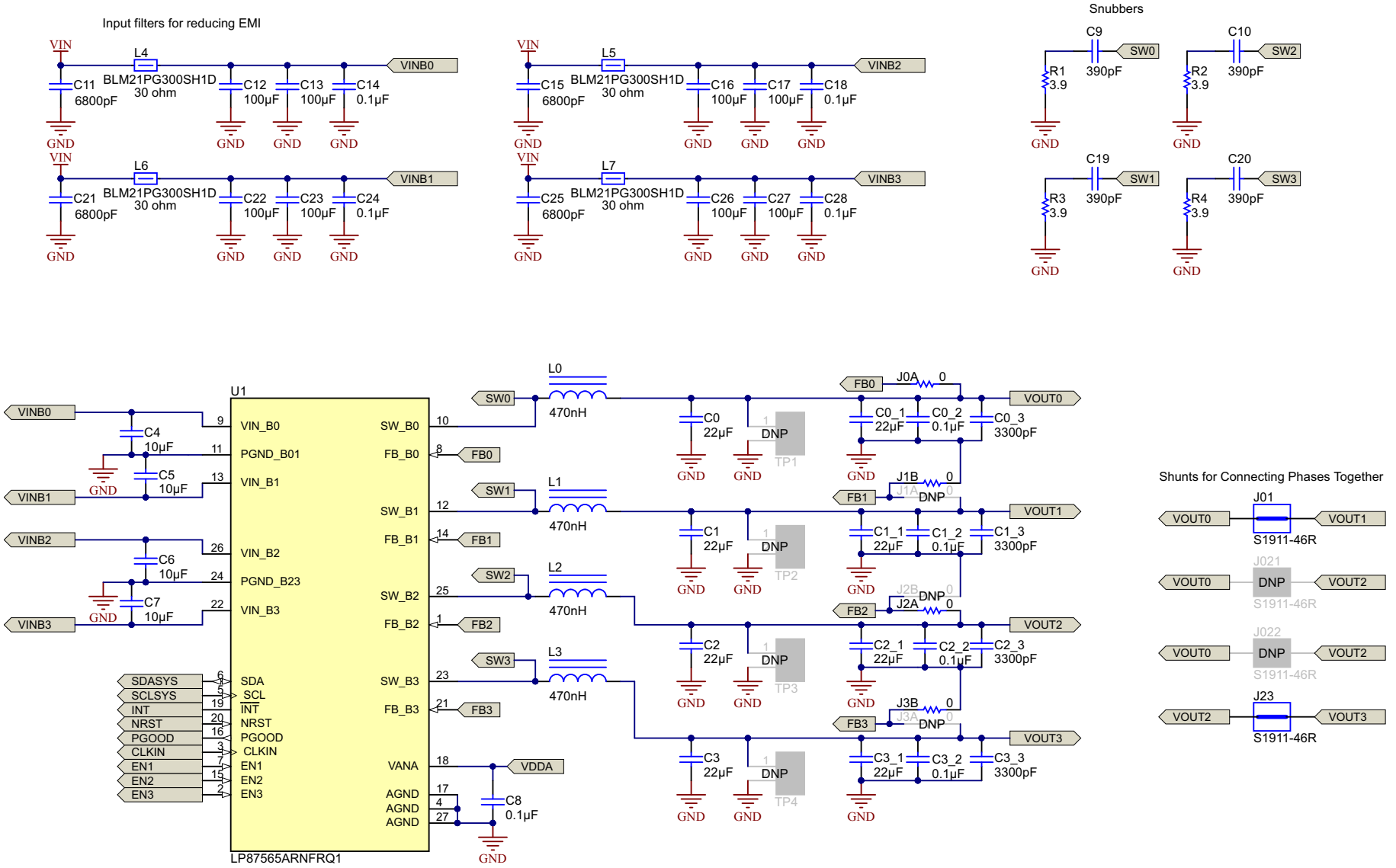


Figure 33. LP87565Q1EVM Schematic

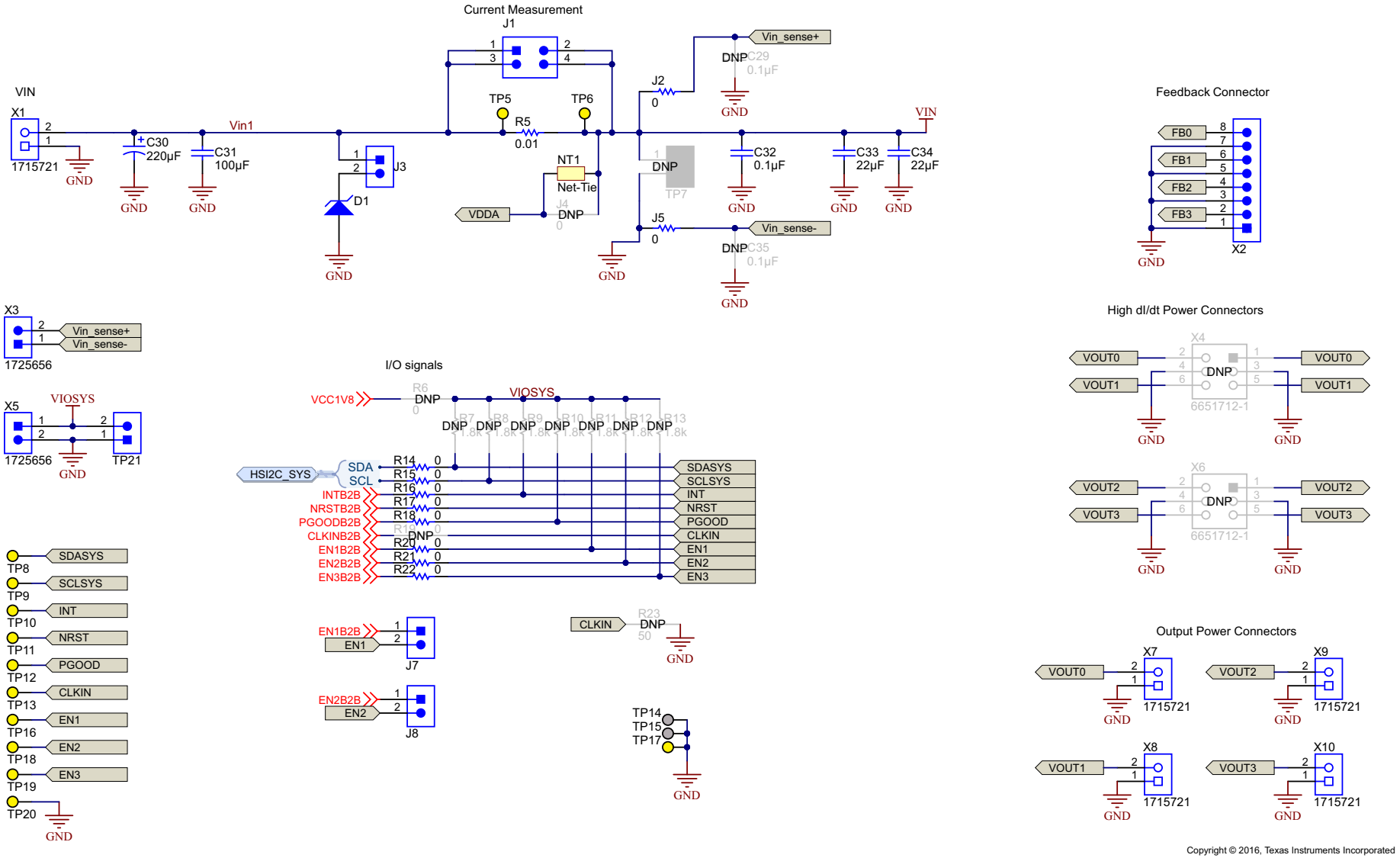


Figure 34. EVM Connectors

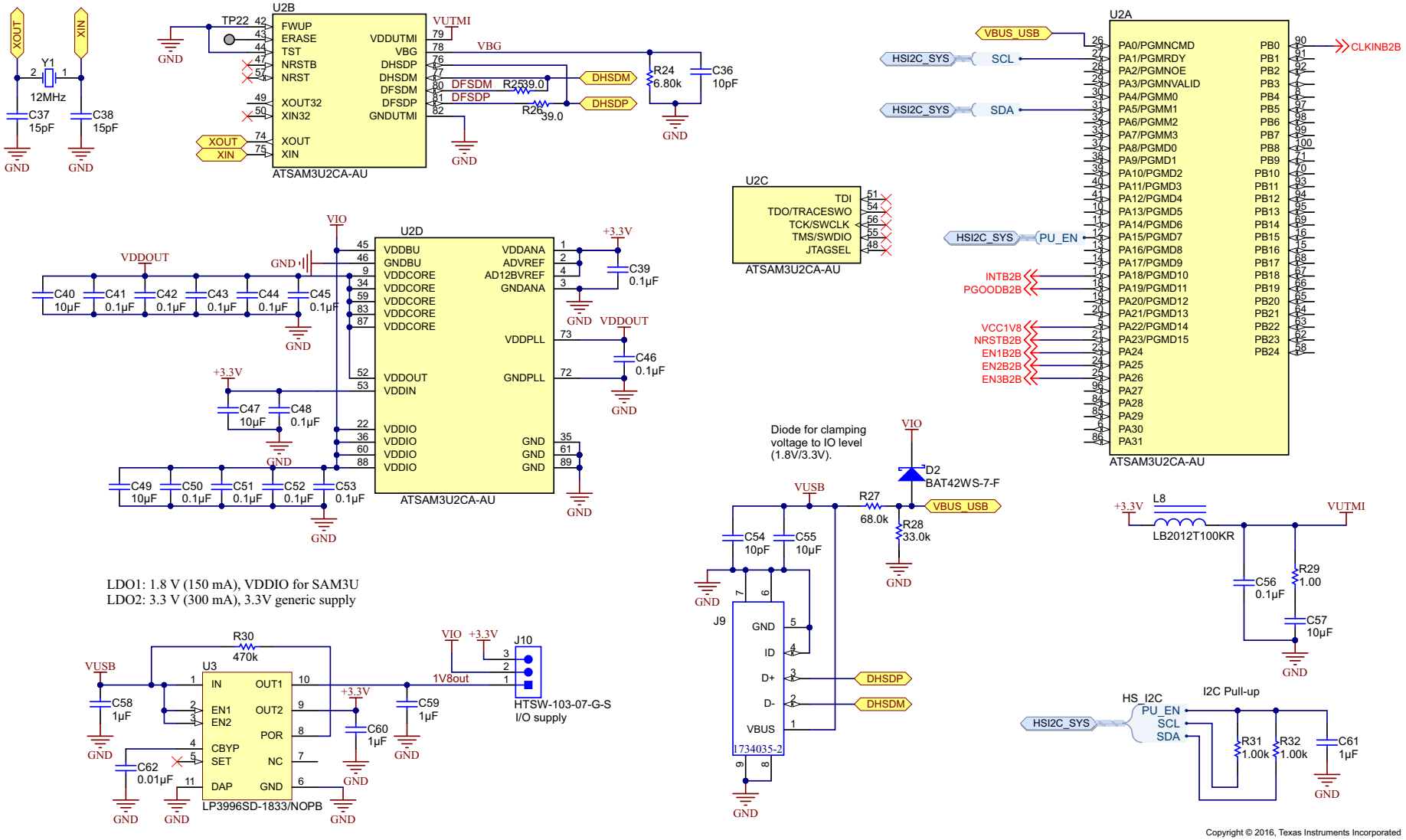


Figure 35. EVM I²C Interface

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2016) to A Revision	Page
• Added caution graphic	1
• Changed Changed number of outputs for LP87525Q1 from "5" to "2"	3

Revision History

Changes from A Revision (February 2017) to B Revision	Page
• Added (SV601325) to the title to indicate which EVM version it applies to	1
• Added link to the newer BMC031 version of this document	1
• Added hyperlink for the GUI installer	4

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   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
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なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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