ESD Protection Diode
Micro–Packaged Diodes for ESD Protection

ESD7551, SZESD7551

The ESD7551 is designed to protect voltage sensitive components that require ultra–low capacitance from ESD and transient voltage events. Excellent clamping capability, low capacitance, low leakage, and fast response time, make these parts ideal for ESD protection on designs where board space is at a premium. Because of its low capacitance, the part is well suited for use in high frequency designs such as USB 2.0 high speed and antenna line applications.

Features

- Ultra–Low Capacitance (0.35 pF Max)
- Low Clamping Voltage
- Stand–off Voltage: 3.3 V
- Low Leakage
- Response Time is < 1 ns
- Low Dynamic Resistance < 1 Ω
- Protection for the Following Standards: IEC 61000–4–2 (Level 4) & ISO 10605
- SZESD7551MXWT5G – Wettable Flank Package for Optimal Automated Optical Inspection (AOI)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- RF Signal ESD Protection
- RF Switching, PA, and Antenna ESD Protection
- Near Field Communications

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Total Power Dissipation on FR–5 Board (Note 1) @ T_A = 25°C Thermal Resistance, Junction–to–Ambient	P_D $R_{\theta JA}$	250 400	mW °C/W
Junction and Storage Temperature Range	T_J, T_{stg}	–55 to +150	°C
Lead Solder Temperature – Maximum (10 Second Duration)	T_L	260	°C
IEC 61000–4–2 Contact IEC 61000–4–2 Air ISO 10605 150 pF/2 kΩ ISO 10605 330 pF/2 kΩ ISO 10605 330 pF/330 Ω	ESD	±25 ±25 ±30 ±30 ±20	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR–5 = 1.0 x 0.75 x 0.62 in.

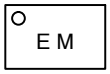
See Application Note AND8308/D for further description of survivability specs.

ON Semiconductor®

www.onsemi.com

MARKING DIAGRAM

X2DFN2
CASE 714AB



E = Specific Device Code
M = Date Code

X2DFNW2
CASE 711BG

F = Specific Device Code
M = Date Code

ORDERING INFORMATION

Device	Package	Shipping†
ESD7551N2T5G	X2DFN2 (Pb–Free)	8000 / Tape & Reel
SZESD7551N2T5G	X2DFN2 (Pb–Free)	8000 / Tape & Reel
SZESD7551MXWT5G	X2DFNW2 (Pb–Free)	8000 / Tape & Reel

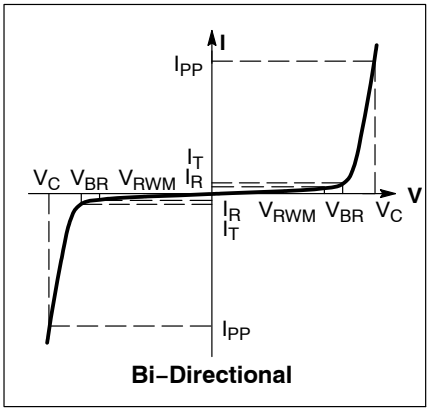
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				3.3	V
Breakdown Voltage (Note 2)	V_{BR}	I_T = 1 mA	5.0	6.0	7.5	V
Reverse Leakage Current	I_R	V_{RWM} = 3.3 V		< 1.0	50	nA
Clamping Voltage (Note 3)	V_C	I_{PP} = 1 A			10	V
Clamping Voltage (Note 3)	V_C	I_{PP} = 3 A			13	V
ESD Clamping Voltage	V_C	Per IEC61000−4−2				
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz V_R = 0 V, f = 1 GHz		0.25 0.22	0.35 0.35	pF
Dynamic Resistance	R_{DYN}	TLP Pulse		0.55		Ω

2. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.
3. Non−repetitive current pulse at T_A = 25°C, per IEC61000−4−5 waveform.

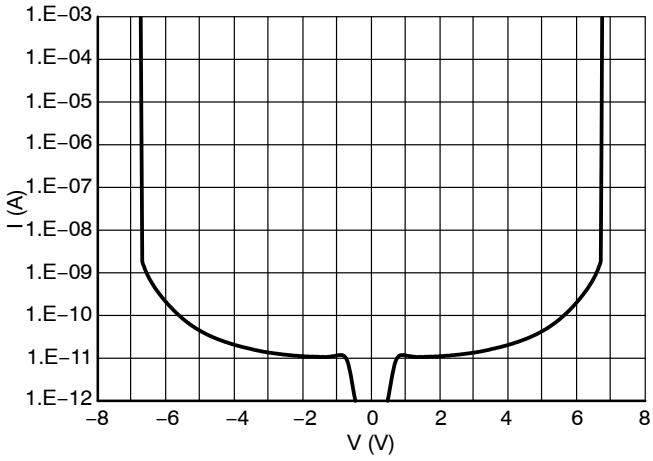


Figure 1. IV Characteristics

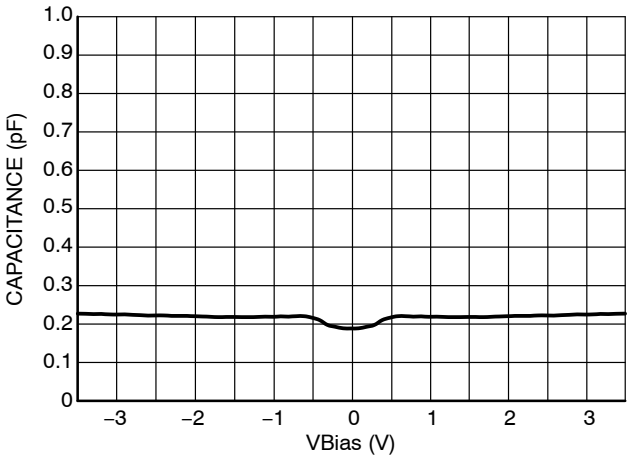


Figure 2. CV Characteristics

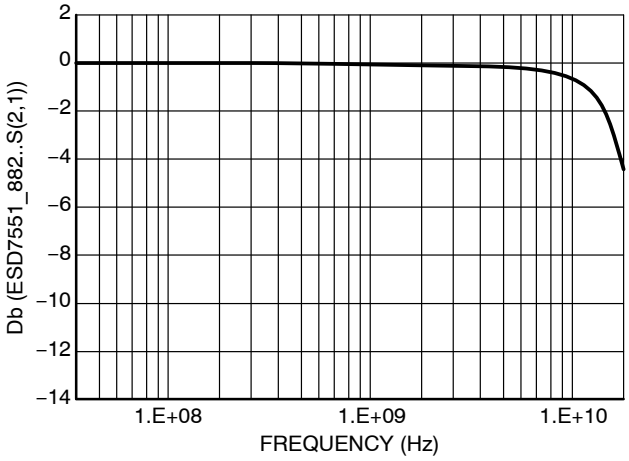


Figure 3. RF Insertion Loss

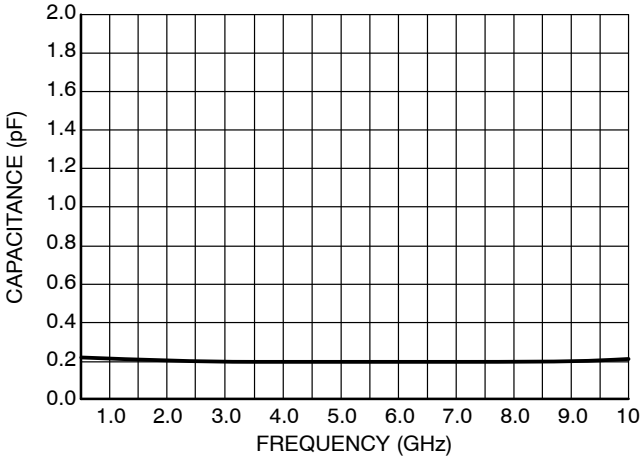


Figure 4. Capacitance over Frequency

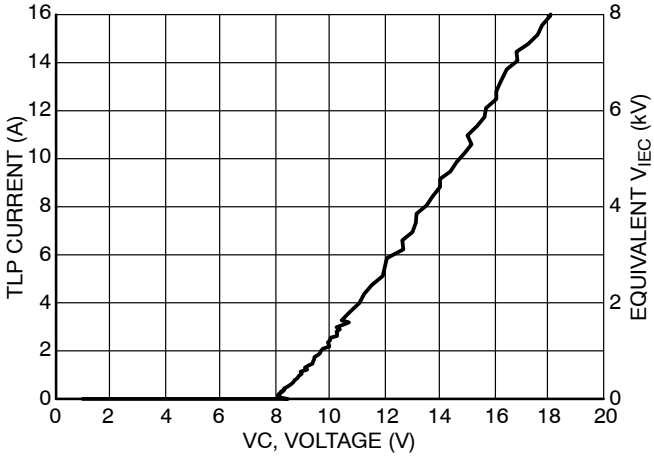


Figure 5. Positive TLP I−V Curve

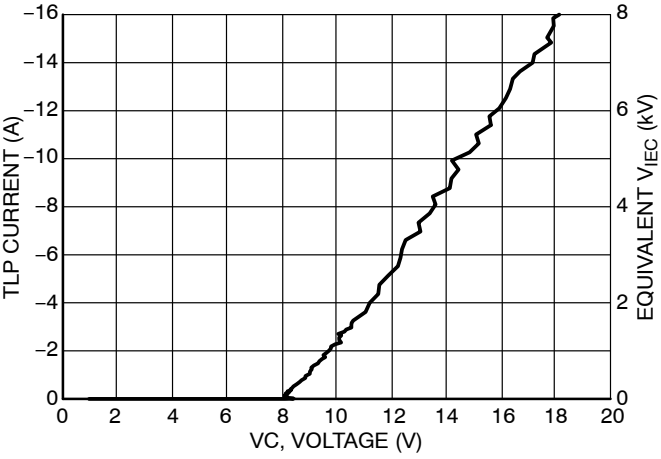


Figure 6. Negative TLP I−V Curve

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

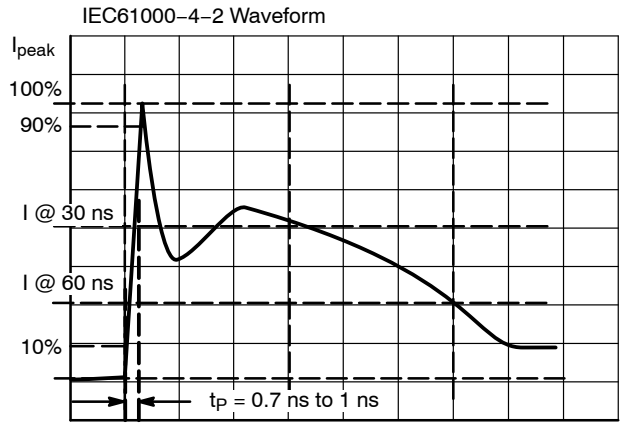


Figure 7. IEC61000−4−2 Spec

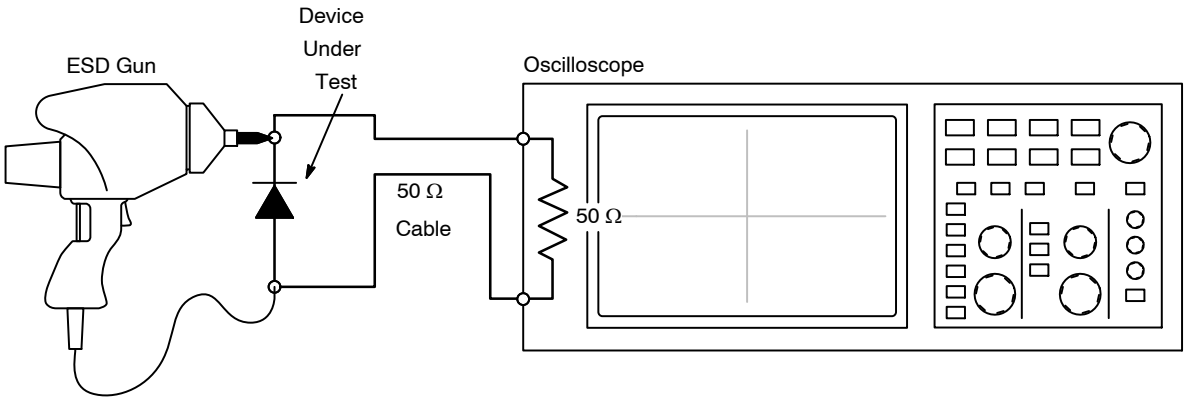


Figure 8. Diagram of ESD Test Setup

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

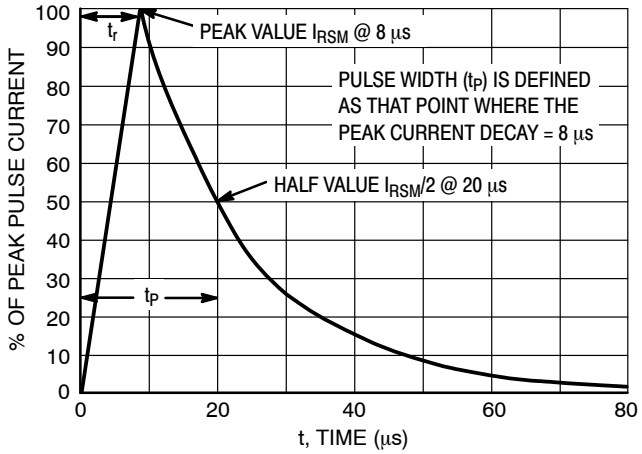


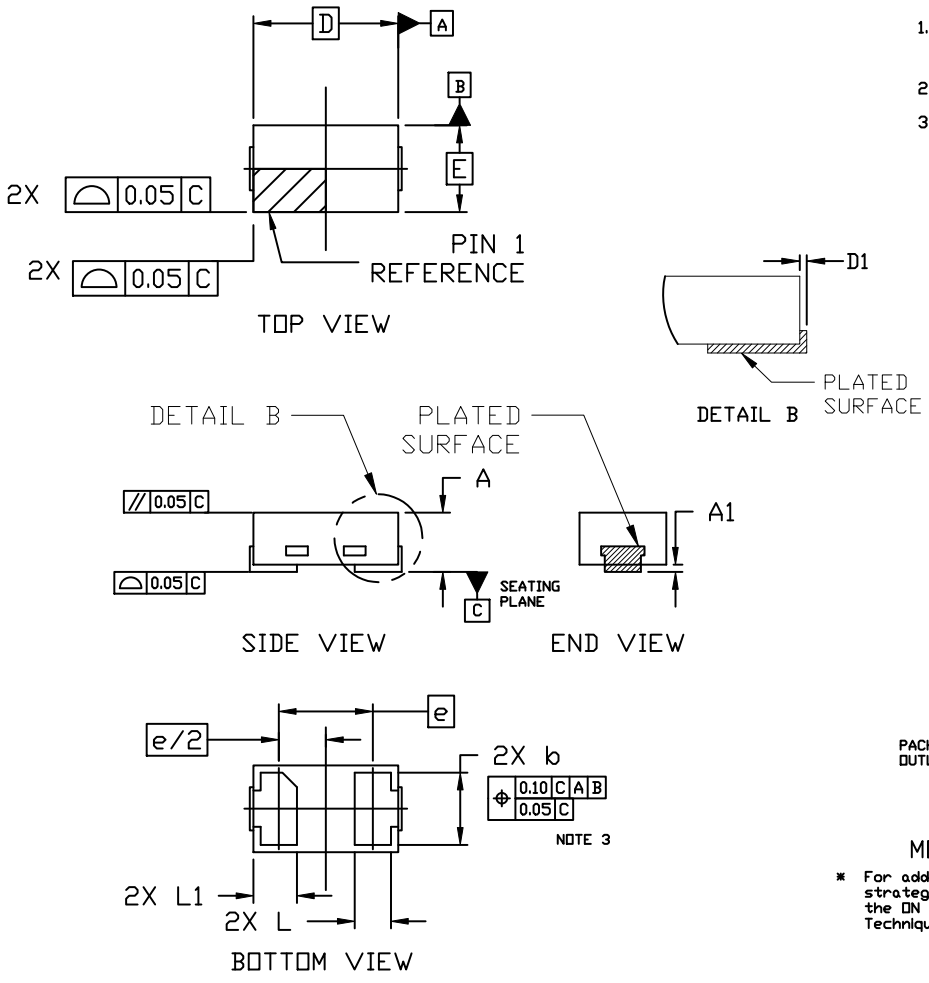
Figure 9. 8 x 20 μs Pulse Waveform

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

X2DFNW2 1.0x0.6, 0.65P
CASE 711BG
ISSUE C

SCALE 8:1

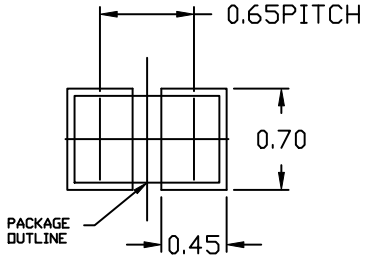
DATE 13 SEP 2019



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
A1	---	---	0.05
b	0.45	0.50	0.55
D	0.90	1.00	1.10
D1	---	---	0.05
E	0.50	0.60	0.70
e	0.65 BSC		
L	0.22 REF		
L1	0.24	0.285	0.34



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present. Some products may not follow the Generic Marking.

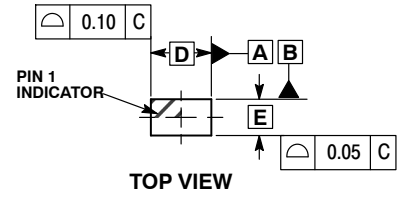
DOCUMENT NUMBER:	**98AON15241G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**X2DFNW2 1.0X0.6, 0.65P**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

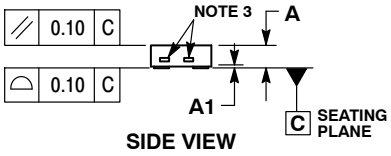
X2DFN2 1.0x0.6, 0.65P
CASE 714AB
ISSUE B

SCALE 8:1

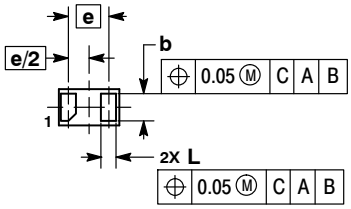
DATE 21 NOV 2017



TOP VIEW



SIDE VIEW

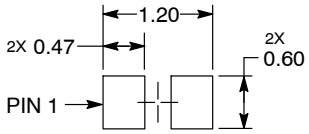


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
A1	---	0.03	0.05
b	0.45	0.50	0.55
D	0.95	1.00	1.05
E	0.55	0.60	0.65
e	0.65 BSC		
L	0.20	0.25	0.30

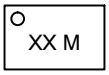
RECOMMENDED SOLDER FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**X2DFN2 1.0X0.6, 0.65P**	**PAGE 1 OF 1**

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