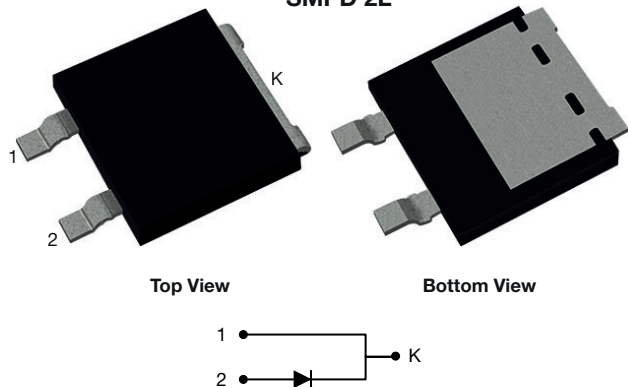


Surface-Mount Low V_F Standard Rectifiers

eSMP® Series SMPD 2L



LINKS TO ADDITIONAL RESOURCES



PRIMARY CHARACTERISTICS	
$I_{F(AV)}$	12 A
V_{RRM}	400 V, 600 V
I_{FSM}	165 A
V_F at $I_F = 12$ A ($T_J = 125$ °C)	0.83 V
T_J max.	175 °C
Package	SMPD 2L
Circuit configuration	Single

FEATURES

- Creepage and clearance distance 3.7 mm typical
- Very low profile - typical height of 1.7 mm
- Low forward voltage drop
- Ideal for automated placement
- Oxide planar chip junction
- AEC-Q101 qualified available
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Material categorization: for definitions of compliance please see www.vishay.com/doc299912



RoHS
COMPLIANT
HALOGEN
FREE

TYPICAL APPLICATIONS

General purpose, power line polarity protection, in both consumer and automotive on board charger (OBC) applications.

MECHANICAL DATA

Case: SMPD 2L

Molding compound meets UL 94 V-0 flammability rating
Base P/N-M3 - halogen-free, RoHS-compliant, and commercial grade

Base P/NHM3 - halogen-free, RoHS-compliant, and AEC-Q101 qualified

Terminals: matte tin plated leads, solderable per J-STD-002 and JESD 22-B102

M3 and HM3 suffix meet JESD 201 class 2 whisker test

Polarity: as marked

MAXIMUM RATINGS (T _A = 25 °C unless otherwise noted)				
PARAMETER	SYMBOL	SE12DTLG	SE12DTLJ	UNIT
Device marking code		SE12DTLG	SE12DTLJ	
Maximum repetitive peak reverse voltage	V _{RRM}	400	600	V
Maximum DC forward current	I _F ⁽¹⁾	12		A
	I _F ⁽²⁾	3.6		
Peak forward surge current 10 ms single half sine-wave superimposed on rated load	I _{FSM}	165		A
Operating junction and storage temperature range	T _J , T _{STG} ⁽³⁾	-55 to +175		°C

Notes

(1) Mounted on infinite heatsink

(2) Free air, mounted on recommended copper pad area

(3) The heat generated must be less than the thermal conductivity from junction to ambient $dP_D/dT_J < R_{thJA}$



ELECTRICAL CHARACTERISTICS (T _J = 25 °C unless otherwise noted)						
PARAMETER	TEST CONDITIONS		SYMBOL	TYP.	MAX.	UNIT
Instantaneous forward voltage	I _F = 6 A	T _J = 25 °C	V _F ⁽¹⁾	0.86	-	V
	I _F = 12 A			0.93	1	
	I _F = 6 A	T _J = 125 °C		0.72	-	
	I _F = 12 A			0.83	0.9	
Reverse current	Rated V _R	T _J = 25 °C	I _R ⁽²⁾	-	5	μA
		T _J = 125 °C		12	70	
Typical reverse recovery time	I _F = 0.5 A, I _R = 1.0 A, I _{rr} = 0.25 A		t _{rr}	300	-	ns
Typical junction capacitance	4.0 V, 1 MHz		C _J	96	-	pF

Notes(1) Pulse test: 300 μs pulse width, 1 % duty cycle(2) Pulse test: Pulse width $\leq 40\text{ ms}$

THERMAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Typical thermal resistance	$R_{\theta JA}^{(1)(2)}$	57	71	$^{\circ}\text{C/W}$
	$R_{\theta JM}^{(3)}$	1.5	1.8	

Notes(1) The heat generated must be less than the thermal conductivity from junction-to-ambient: $dP_D/dT_J < 1/R_{\theta JA}$ (2) Free air, mounted on recommended PCB, 2 oz. pad area; thermal resistance $R_{\theta JA}$ - junction to ambient to follow JEDEC® 51-2A(3) Mounted on infinite heatsink thermal resistance $R_{\theta JM}$ - junction to mount to follow JEDEC® 51-14 transient dual interface test method (TDIM)

ORDERING INFORMATION (Example)				
PREFERRED P/N	UNIT WEIGHT (g)	PREFERRED PACKAGE CODE	BASE QUANTITY	DELIVERY MODE
SE12DTLJ-M3/I	0.51	I	2000/reel	13" diameter plastic tape and reel
SE12DTLJHM3/I ⁽¹⁾	0.51	I	2000/reel	13" diameter plastic tape and reel

Note

(1) AEC-Q101 qualified

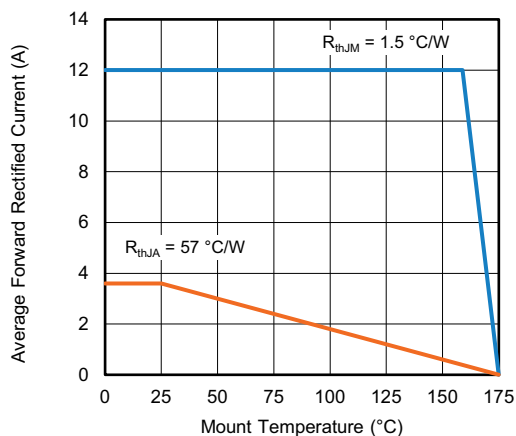
RATINGS AND CHARACTERISTICS CURVES ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)


Fig. 1 - Forward Current Derating Curve

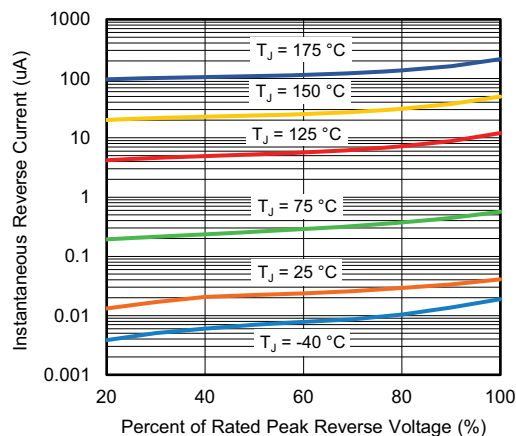


Fig. 4 - Typical Reverse Leakage Characteristics

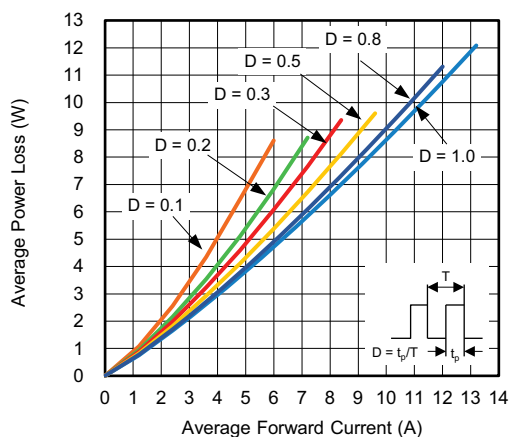


Fig. 2 - Forward Power Loss Characteristics

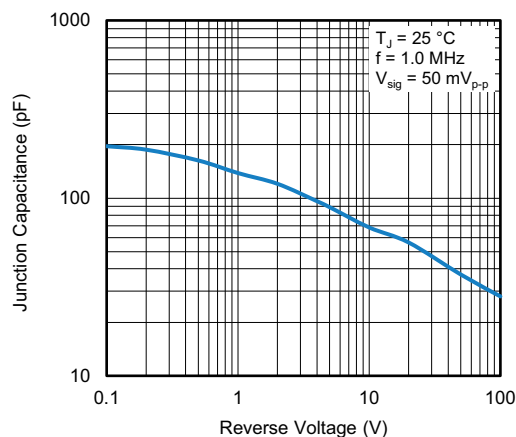


Fig. 5 - Typical Junction Capacitance

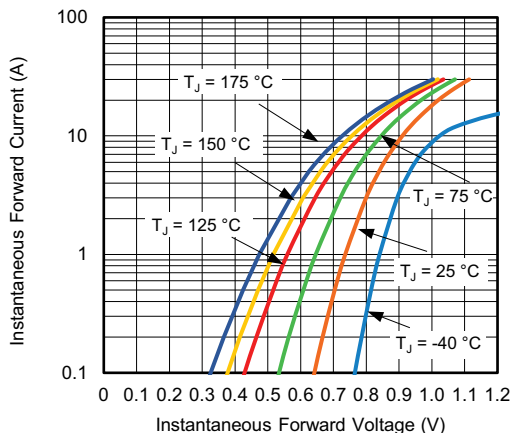


Fig. 3 - Typical Instantaneous Forward Characteristics

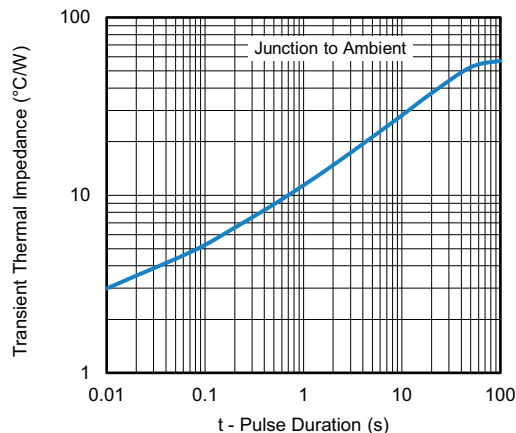
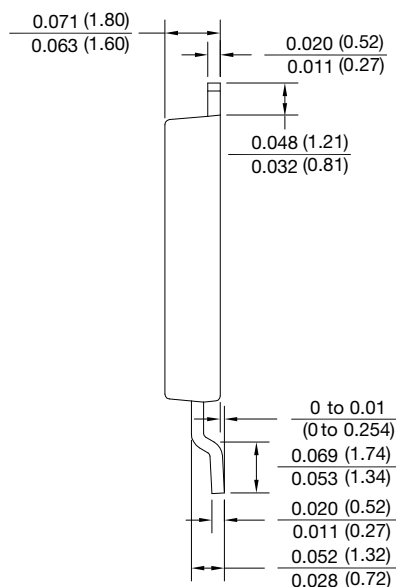
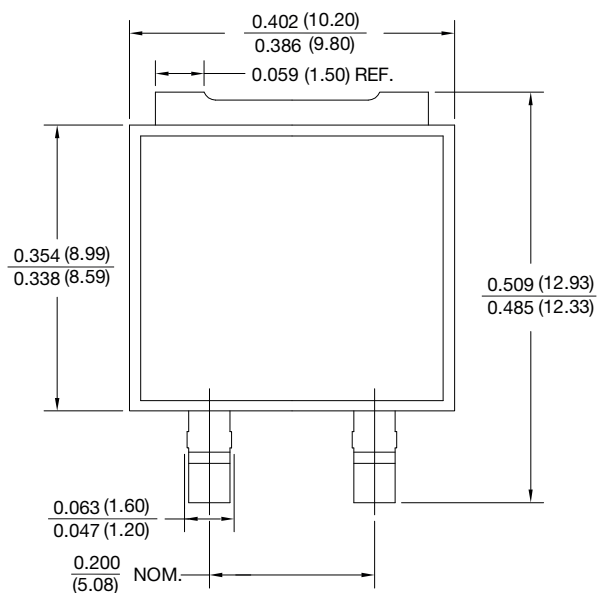


Fig. 6 - Typical Transient Thermal Impedance

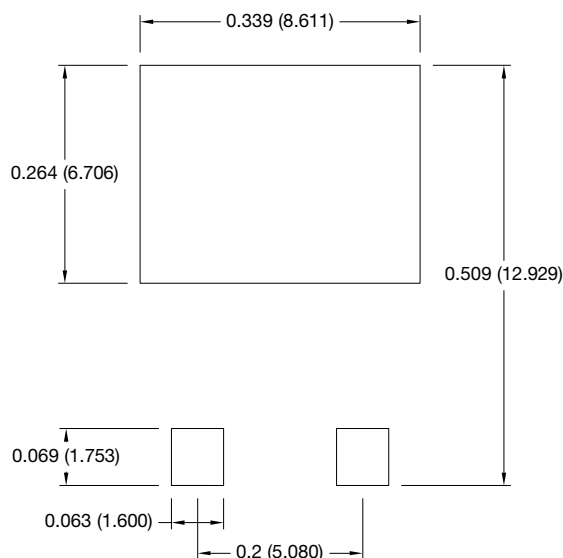
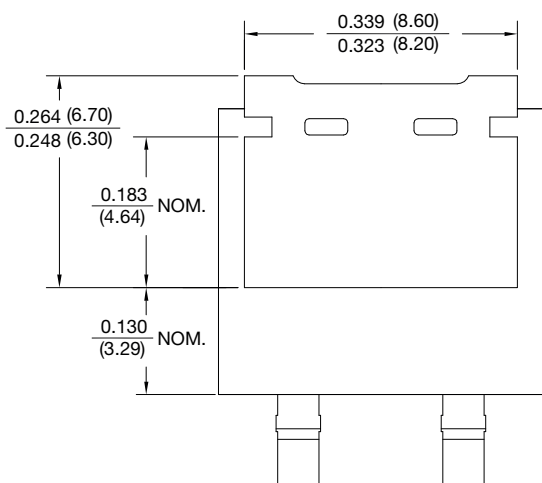


PACKAGE OUTLINE DIMENSIONS in inches (millimeters)

SMPD 2L



Mounting Pad Layout



Note

- The suggested mounting pad layout is provided for reference only, as actual pad layouts may vary depending on application



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