

MOSFET - Power, Single N-Channel

80 V, 1.5 mΩ, 255 A

NTMTS1D5N08H

Features

- Small Footprint (8x8 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	80	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	A
		$T_C = 100^\circ\text{C}$	162	
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^\circ\text{C}$	P_D	W
		$T_C = 100^\circ\text{C}$	83	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	A
		$T_A = 100^\circ\text{C}$	23	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25^\circ\text{C}$	P_D	W
		$T_A = 100^\circ\text{C}$	1.7	
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10\ \mu\text{s}$	I_{DM}	900	A
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Source Current (Body Diode)		I_S	173	A
Single Pulse Drain-to-Source Avalanche Energy ($L = 3\ \text{mH}$, $I_{L(pk)} = 32\ \text{A}$)		E_{AS}	1536	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	°C

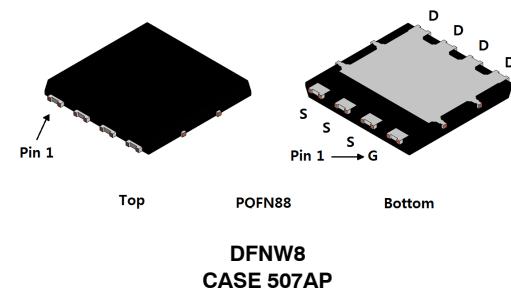
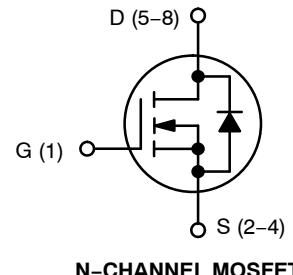
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

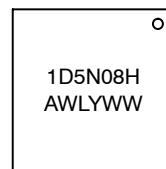
Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.6	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	30	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(\text{BR})DSS}$	$R_{DS(\text{ON}) \text{ MAX}}$	$I_D \text{ MAX}$
80 V	1.5 mΩ @ 10 V	255 A



MARKING DIAGRAM



A = Assembly Location

WL = 2-digit Wafer Lot Code

Y = Year Code

WW = Work Week Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NTMTS1D5N08H

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}}/T_J$				59		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0 \text{ V}$, $V_{\text{DS}} = 80 \text{ V}$	$T_J = 25^\circ\text{C}$		10		μA
			$T_J = 125^\circ\text{C}$			250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}$, $V_{\text{GS}} = 20 \text{ V}$				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}$, $I_D = 490 \mu\text{A}$		2.0	3.0	4.0	V
Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})}/T_J$				-6.9		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}$	$I_D = 90 \text{ A}$		1.16	1.5	$\text{m}\Omega$
		$V_{\text{GS}} = 6 \text{ V}$	$I_D = 49 \text{ A}$		1.68	2.0	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 5 \text{ V}$, $I_D = 90 \text{ A}$			294		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	$V_{\text{GS}} = 0 \text{ V}$, $f = 1 \text{ MHz}$, $V_{\text{DS}} = 40 \text{ V}$			8220		pF
Output Capacitance	C_{OSS}				1190		
Reverse Transfer Capacitance	C_{RSS}				31		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 10 \text{ V}$, $V_{\text{DS}} = 64 \text{ V}$; $I_D = 90 \text{ A}$			125		nC
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$				21		
Gate-to-Source Charge	Q_{GS}				34		
Gate-to-Drain Charge	Q_{GD}				29		
Plateau Voltage	V_{GP}				4.5		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{\text{d}(\text{ON})}$	$V_{\text{GS}} = 10 \text{ V}$, $V_{\text{DS}} = 64 \text{ V}$, $I_D = 90 \text{ A}$, $R_G = 6 \Omega$			33		ns
Rise Time	t_r				23		
Turn-Off Delay Time	$t_{\text{d}(\text{OFF})}$				100		
Fall Time	t_f				30		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0 \text{ V}$, $I_S = 90 \text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 125^\circ\text{C}$		0.7		
Reverse Recovery Time	t_{RR}	$V_{\text{GS}} = 0 \text{ V}$, $dI_S/dt = 100 \text{ A}/\mu\text{s}$, $I_S = 90 \text{ A}$			75		ns
Reverse Recovery Charge	Q_{RR}				146		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

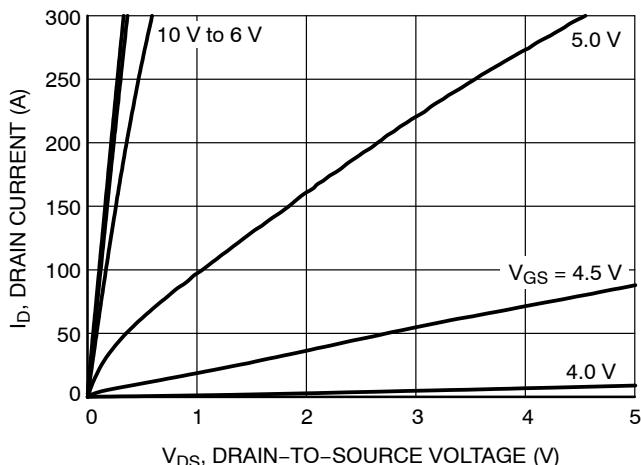


Figure 1. On-Region Characteristics

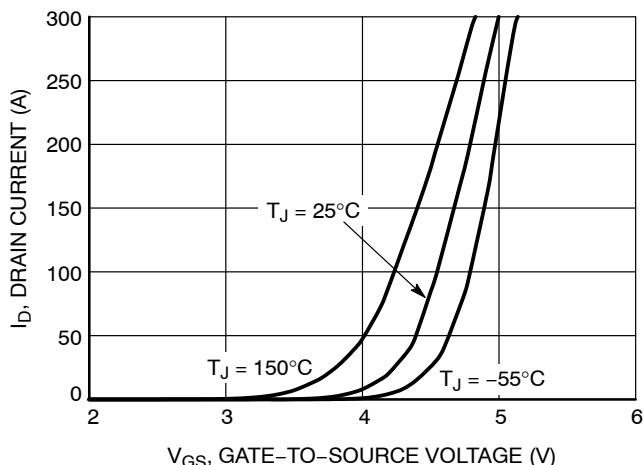


Figure 2. Transfer Characteristics

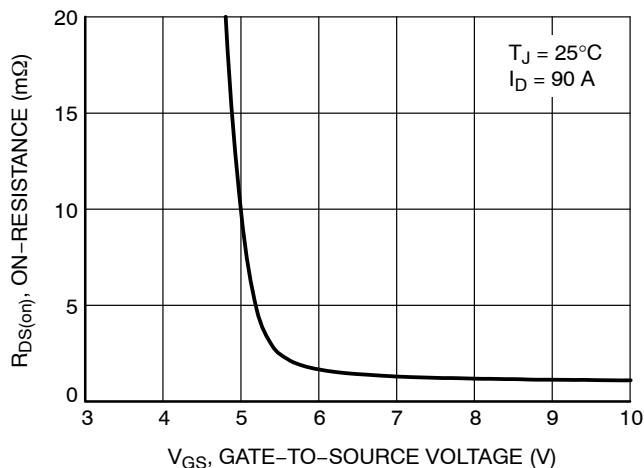


Figure 3. On-Resistance vs. Gate-to-Source Voltage

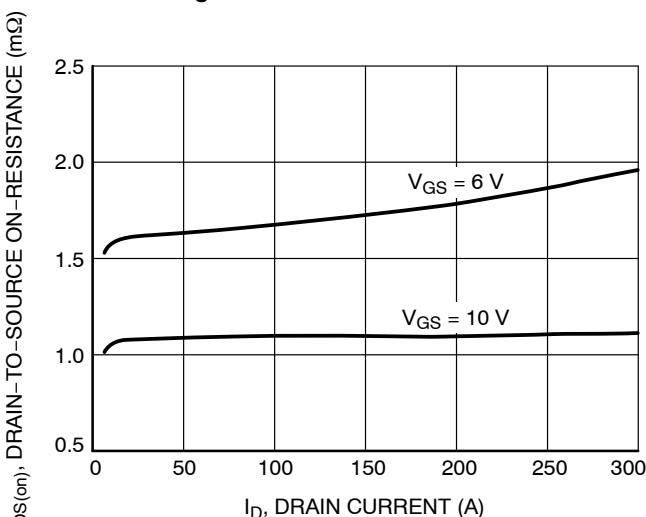


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

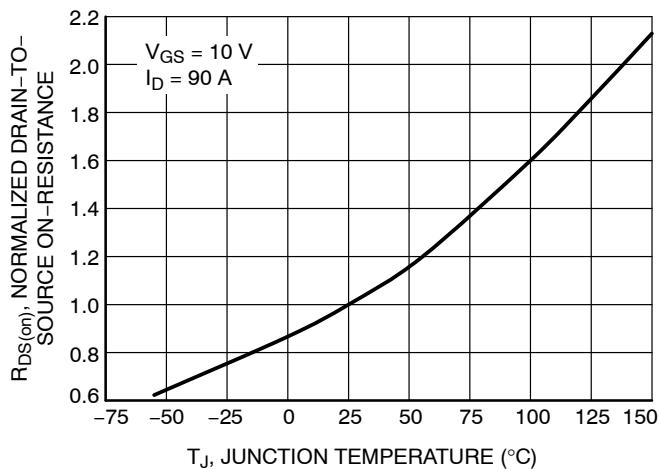


Figure 5. On-Resistance Variation with Temperature

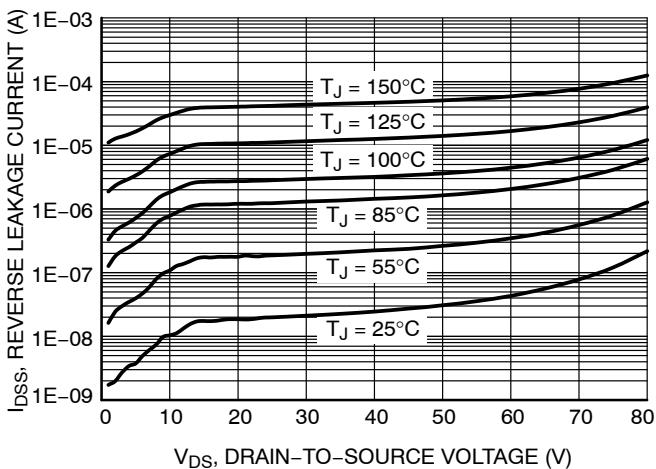


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

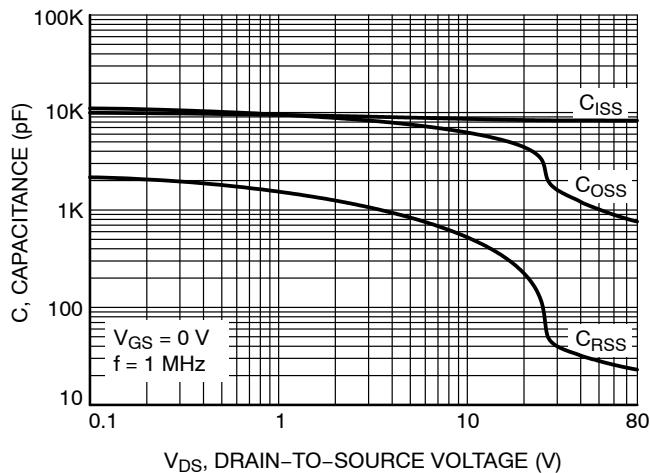


Figure 7. Capacitance Variation

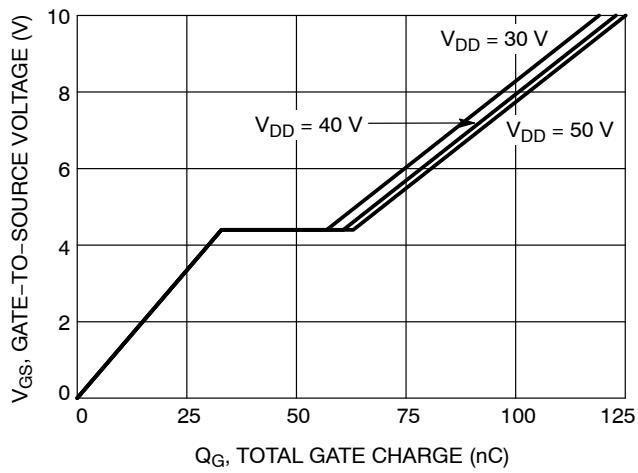


Figure 8. Gate-to-Source Voltage vs. Total Charge

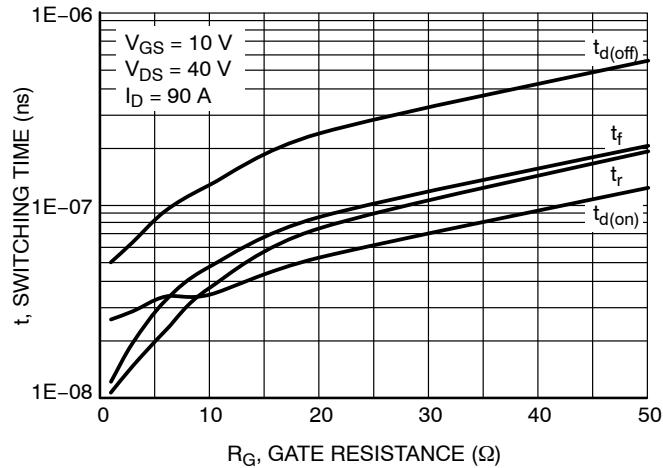


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

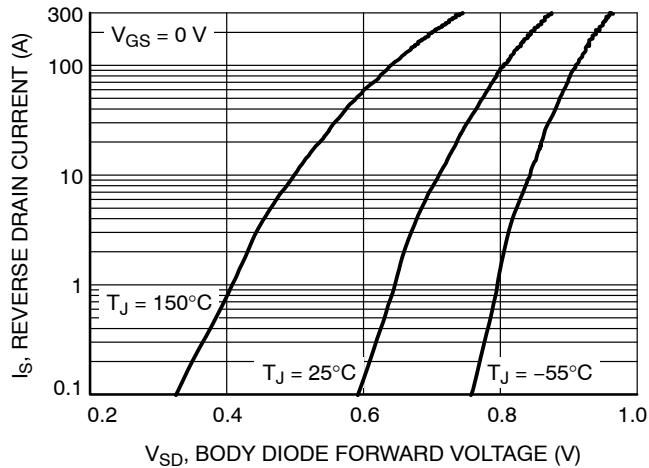


Figure 10. Diode Forward Voltage vs. Current

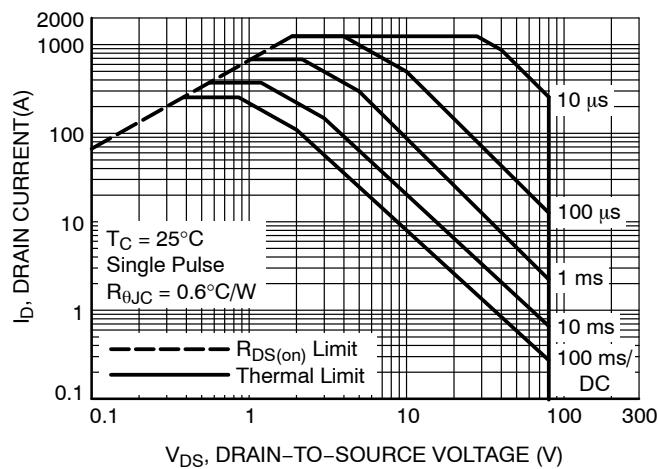


Figure 11. Maximum Rated Forward Biased Safe Operating Area

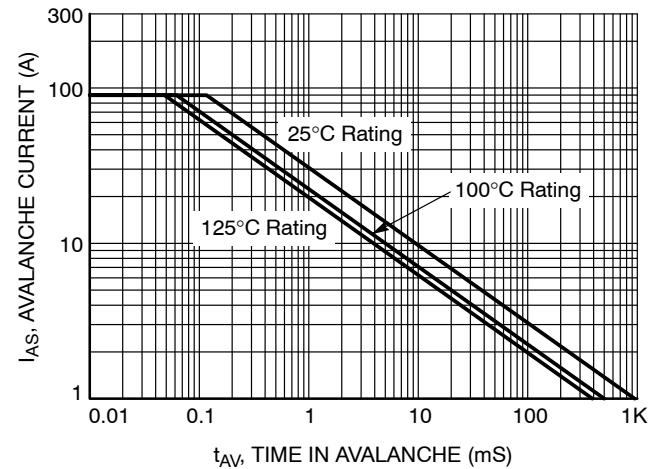


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

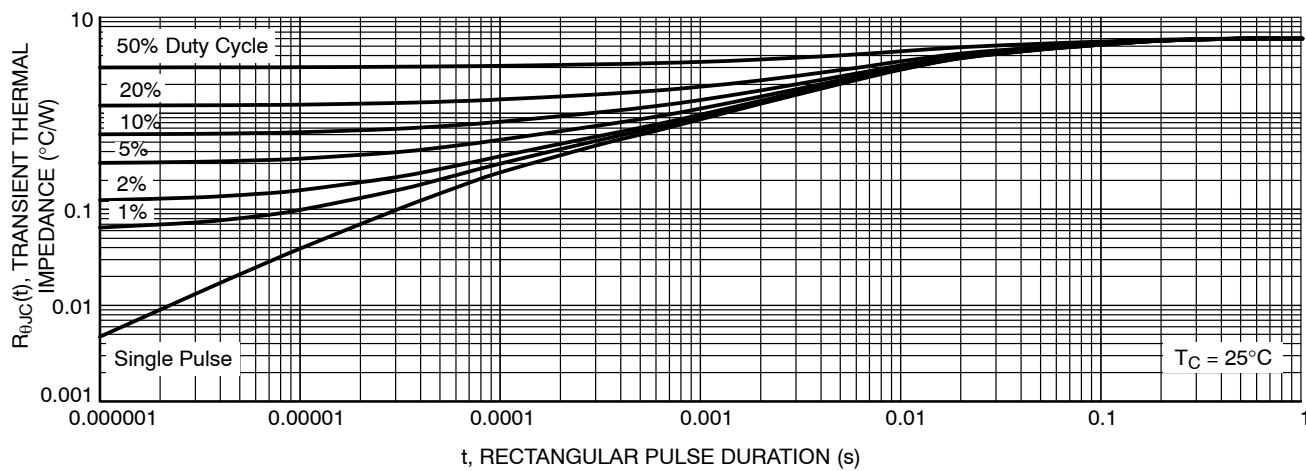


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

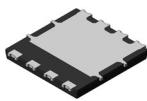
Device	Marking	Package	Shipping [†]
NTMTS1D5N08H	NTMTS1D5N08H	POWER 88 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

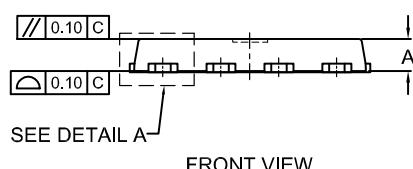
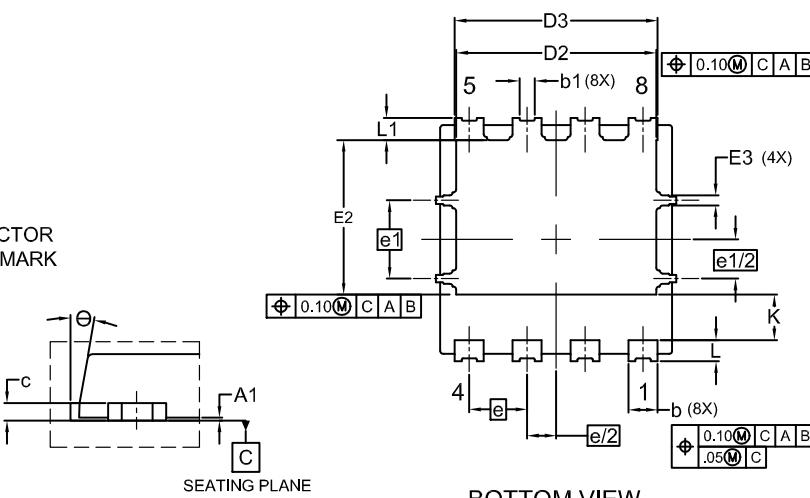
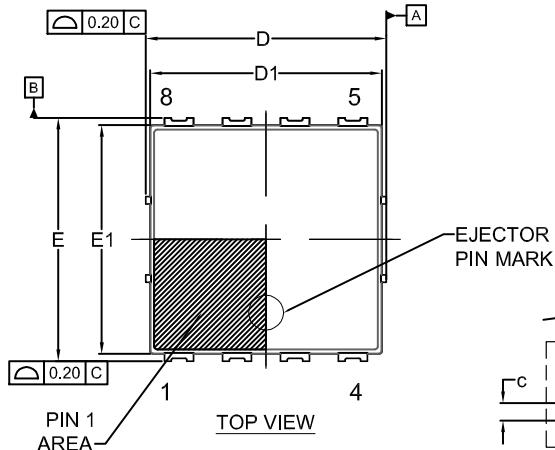
PACKAGE DIMENSIONS

ON Semiconductor®

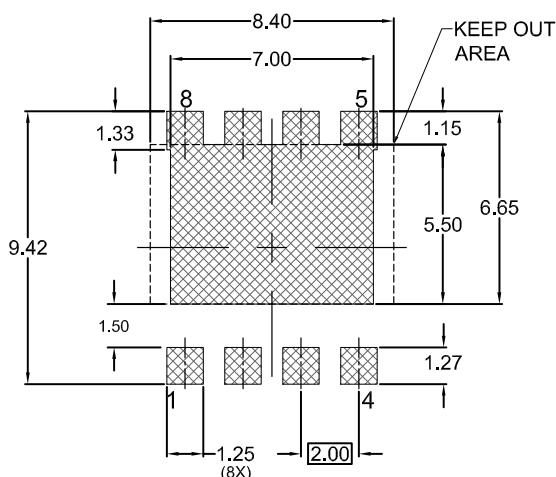


TDFNW8 8.3x8.4, 2.0P, SINGLE COOL
CASE 507AP
ISSUE D

DATE 29 MAR 2021



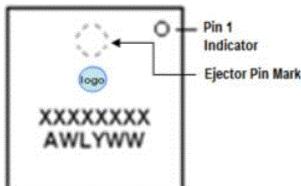
DETAIL A
SCALE: 2X



RECOMMENDED LAND PATTERN*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SODERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot Code
Y = Year Code
WW = Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	--	0.05
b	0.90	1.00	1.10
b1	0.35	0.45	0.55
c	0.23	0.28	0.33
D	8.20	8.30	8.40
D1	7.90	8.00	8.10
D2	6.80	6.90	7.00
D3	6.90	7.00	7.10
E	8.30	8.40	8.50
E1	7.80	7.90	8.00
E2	5.24	5.34	5.44
E3	0.25	0.35	0.45
e	2.00	BSC	
e/2	1.00	BSC	
e1	2.70	BSC	
e1/2	1.35	BSC	
K	1.50	1.57	1.70
L	0.64	0.74	0.84
L1	0.67	0.77	0.87
Θ	0°	--	12°

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