

# LDO Regulator, 300 mA, Low Dropout Voltage, Ultra Low Noise, High PSRR with Power Good

## NCV8164

The NCV8164 is a 300 mA LDO, next generation of high PSRR, ultra-low noise and low dropout regulators with Power Good open collector output. Designed to meet the requirements of RF and sensitive analog circuits, the NCV8164 device provides ultra-low noise, high PSRR and low quiescent current. The device also offers excellent load/line transients. The NCV8164 is designed to work with a 1  $\mu$ F input and a 1  $\mu$ F output ceramic capacitor. It is available in industry standard TSOP-5, WDFNW6 0.65P, 2 mm x 2 mm and DFNW8 0.65P, 3 mm x 3 mm.

### Features

- Operating Input Voltage Range: 1.6 V to 5.5 V
- Available in Fixed Voltage Option: 1.2 V to 5.0 V
- Adjustable Version Reference Voltage: 1.2 V
- $\pm 2\%$  Accuracy Over Load and Temperature
- Ultra Low Quiescent Current Typ. 30  $\mu$ A
- Standby Current: Typ. 0.1  $\mu$ A
- Very Low Dropout: 110 mV at 300 mA for 3.3 V Variant
- Ultra High PSRR: Typ. 85 dB at 10 mA,  $f = 1$  kHz
- Ultra Low Noise: 9  $\mu$ V<sub>RMS</sub> (Fixed Version)
- Stable with a 1  $\mu$ F Small Case Size Ceramic Capacitors
- Available in – TSOP-5 3 mm x 1.5 mm x 1 mm CASE 483
  - ◆ WDFNW6 2 mm x 2 mm x 0.75 mm CASE 511DW
  - ◆ DFNW8 3 mm x 3 mm x 0.9 mm CASE 507AD
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Communication Systems
- In-Vehicle Networking
- Telematics, Infotainment and Clusters
- General Purpose Automotive

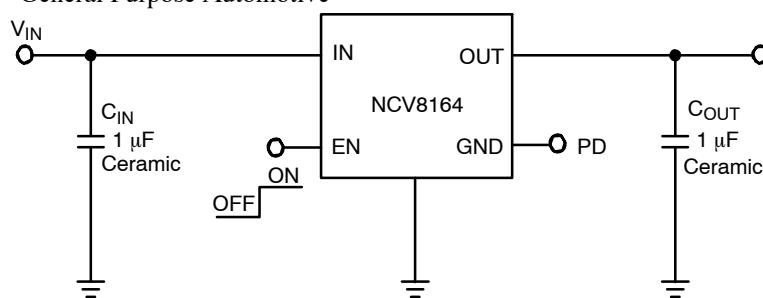
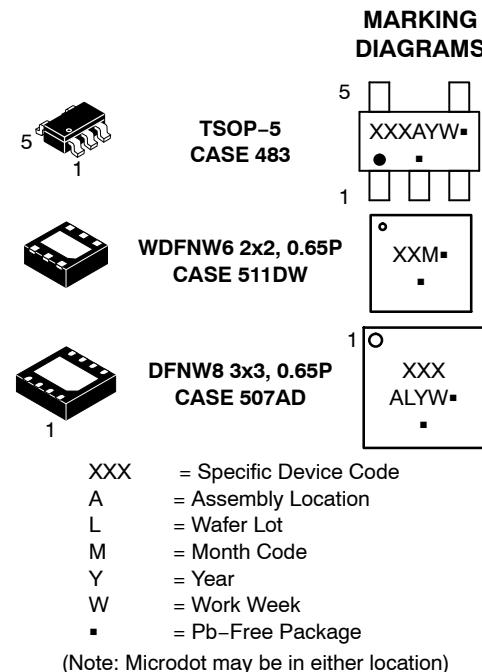
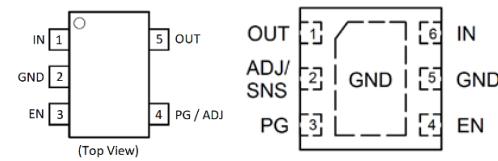


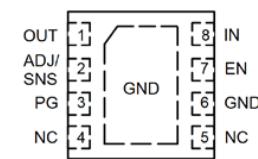
Figure 1. Typical Application Schematics



### PIN CONNECTIONS



WDFNW6 2x2 mm  
(Top View)



DFNW8 3x3 mm  
(Top View)

### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 10 of this data sheet.

## PIN FUNCTION DESCRIPTION

Pin No. TSOP-5	Pin No. WDFNW6	Pin No. DFNW8	Pin Name	Description
1	6	8	IN	Input voltage supply pin
5	1	1	OUT	Regulated output voltage. The output should be bypassed with small 1 $\mu$ F ceramic capacitor
3	4	7	EN	Chip enable: Applying $V_{EN} < 0.25$ V disables the regulator, Pulling $V_{EN} > 0.7$ V enables the LDO
4 / –	3	3	PG	Power Good, open collector. Use 10 k $\Omega$ to 100 k $\Omega$ pull-up resistor connected to output or input voltage
2	5	6	GND	Common ground connection
– / 4	2	2	ADJ	Adjustable output feedback pin (for adjustable version only)
–	2	2	SNS	Sense feedback pin. Must be connected to OUT pin on PCB (for fixed versions only)
–	–	4, 5	N/C	Not connected, pin can be tied to ground plane for better power dissipation
–	EPAD	EPAD	EPAD	Expose pad should be tied to ground plane for better power dissipation

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	$V_{IN}$	–0.3 to 6	V
Output Voltage	$V_{OUT}$	–0.3 to $V_{IN}+0.3$ , max. 6	V
Chip Enable Input	$V_{CE}$	–0.3 to 6	V
Power Good Voltage	$V_{PG}$	–0.3 to 6	V
Power Good Current	$I_{PG}$	30	mA
Output Short Circuit Duration	$t_{SC}$	unlimited	s
Maximum Junction Temperature	$T_J$	150	°C
Storage Temperature	$T_{STG}$	–55 to 150	°C
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2000	V
ESD Capability, Charged Device Model (Note 2)	$ESD_{CDM}$	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

2. This device series incorporates ESD protection and is tested by the following methods:

ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)

ESD Charged Device Model tested per EIA/JESD22-C101, Field Induced Charge Model

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
<b>THERMAL CHARACTERISTICS, TSOP-5 PACKAGE</b>			
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	158	°C/W
Thermal Resistance, Junction-to-Case (top)	$R_{\theta JC(\text{top})}$	155	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	$R_{\theta JC(\text{bot})}$	102	°C/W
Thermal Resistance, Junction-to-Board	$R_{\theta JB}$	197	°C/W
Characterization Parameter, Junction-to-Top	$\Psi_{JT}$	40	°C/W
Characterization Parameter, Junction-to-Board	$\Psi_{JB}$	82	°C/W

## THERMAL CHARACTERISTICS, WDFNW6-2X2, 0.65 PITCH PACKAGE

Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	51	°C/W
Thermal Resistance, Junction-to-Case (top)	$R_{\theta JC(\text{top})}$	142	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	$R_{\theta JC(\text{bot})}$	2.0	°C/W
Thermal Resistance, Junction-to-Board	$R_{\theta JB}$	117	°C/W
Characterization Parameter, Junction-to-Top	$\Psi_{JT}$	1.9	°C/W
Characterization Parameter, Junction-to-Board	$\Psi_{JB}$	7.7	°C/W

## THERMAL CHARACTERISTICS, DFNW8-3X3, 0.65 PITCH PACKAGE

Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	50	°C/W
Thermal Resistance, Junction-to-Case (top)	$R_{\theta JC(\text{top})}$	142	°C/W
Thermal Resistance, Junction-to-Case (bottom) (Note 4)	$R_{\theta JC(\text{bot})}$	7.9	°C/W
Thermal Resistance, Junction-to-Board	$R_{\theta JB}$	125	°C/W
Characterization Parameter, Junction-to-Top	$\Psi_{JT}$	2.0	°C/W
Characterization Parameter, Junction-to-Board	$\Psi_{JB}$	7.5	°C/W

3. The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a high-K board, following the JEDEC51.7 guidelines with assumptions as above, in an environment described in JESD51-2a.
4. The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the IC exposed pad. Test description can be found in the ANSI SEMI standard G30-88.

## ELECTRICAL CHARACTERISTICS

( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ;  $V_{\text{IN}} = V_{\text{OUT}(\text{NOM})} + 0.5 \text{ V}$ ;  $I_{\text{OUT}} = 1 \text{ mA}$ ,  $C_{\text{IN}} = C_{\text{OUT}} = 1 \mu\text{F}$ ,  $V_{\text{EN}} = V_{\text{IN}}$ , unless otherwise noted.  
Typical values are at  $T_J = +25^{\circ}\text{C}$  (Note 5))

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage		$V_{\text{IN}}$	1.6		5.5	V
Output Voltage Accuracy	$V_{\text{IN}} = V_{\text{OUT}(\text{NOM})} + 0.5 \text{ V}$ to $5.5 \text{ V}$ , $0.1 \text{ mA} \leq I_{\text{OUT}} \leq 300 \text{ mA}$	$V_{\text{OUT}}$	-2		+2	%
Reference Voltage (Adjustable Ver. ADJ pin connected to OUT)	$V_{\text{IN}} = 1.6 \text{ V}$ to $5.5 \text{ V}$ , $0.1 \text{ mA} \leq I_{\text{OUT}} \leq 300 \text{ mA}$	$V_{\text{ADJ}}$	1.176	1.2	1.224	V
Line Regulation	$V_{\text{OUT}(\text{NOM})} + 0.5 \text{ V} \leq V_{\text{IN}} \leq 5.5 \text{ V}$	$\text{Line}_{\text{Reg}}$		0.5		mV/V
Load Regulation	$I_{\text{OUT}} = 1 \text{ mA}$ to $300 \text{ mA}$	$\text{Load}_{\text{Reg}}$		2		mV
Dropout Voltage (Note 6) TSOP-5, WDFNW6	$I_{\text{OUT}} = 300 \text{ mA}$	$V_{\text{OUT}(\text{NOM})} = 1.5 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 1.8 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 2.5 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 2.8 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 3.0 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 3.3 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 5.0 \text{ V}$	$V_{\text{DO}}$	170 155 125 115 113 110 95	295 255 200 185 177 170 135	mV
Dropout Voltage (Note 6) DFNW8	$I_{\text{OUT}} = 300 \text{ mA}$	$V_{\text{OUT}(\text{NOM})} = 1.5 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 1.8 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 2.5 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 2.8 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 3.0 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 3.3 \text{ V}$ $V_{\text{OUT}(\text{NOM})} = 5.0 \text{ V}$	$V_{\text{DO}}$	180 165 140 130 127 125 112	315 275 220 205 197 190 170	mV
Output Current Limit	$V_{\text{OUT}} = 90\% V_{\text{OUT}(\text{NOM})}$	$I_{\text{CL}}$	350	560		mA
Short Circuit Current	$V_{\text{OUT}} = 0 \text{ V}$	$I_{\text{SC}}$		580		
Quiescent Current	$I_{\text{OUT}} = 0 \text{ mA}$	$I_{\text{Q}}$		30	40	$\mu\text{A}$
Shutdown Current	$V_{\text{EN}} \leq 0.25 \text{ V}$	$I_{\text{DIS}}$		0.01	1.5	$\mu\text{A}$
EN Pin Threshold Voltage	EN Input Voltage "H" EN Input Voltage "L"	$V_{\text{ENH}}$ $V_{\text{ENL}}$	0.7		0.25	V
EN Pull Down Current	$V_{\text{EN}} = 5.5 \text{ V}$	$I_{\text{EN}}$		0.2	0.6	$\mu\text{A}$
Power Good Threshold Voltage	Output Voltage Raising Output Voltage Falling	$V_{\text{PGUP}}$ $V_{\text{PGDW}}$		95 90		%
Power Good Output Voltage Low	$\text{IPG} = 5 \text{ mA}$ , Open drain	$V_{\text{PGLO}}$			0.3	V
Turn-On Time (Note 7)	$C_{\text{OUT}} = 1 \mu\text{F}$ , From assertion of $V_{\text{EN}}$ to $V_{\text{OUT}} = 95\% V_{\text{OUT}(\text{NOM})}$			120		$\mu\text{s}$

**ELECTRICAL CHARACTERISTICS** (continued)

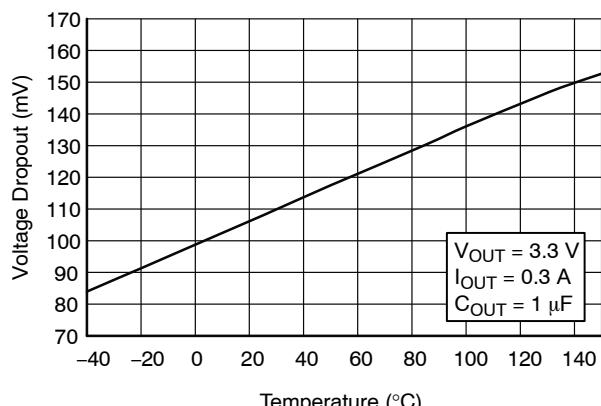
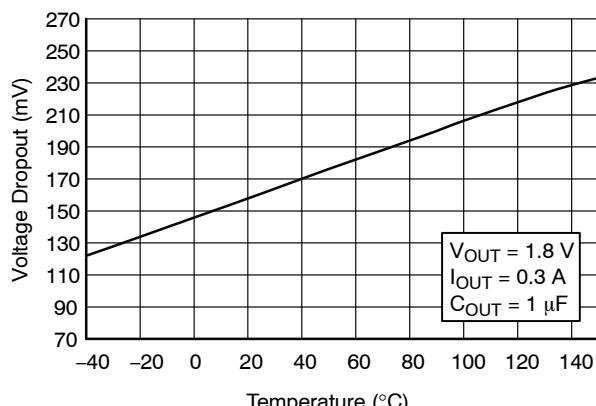
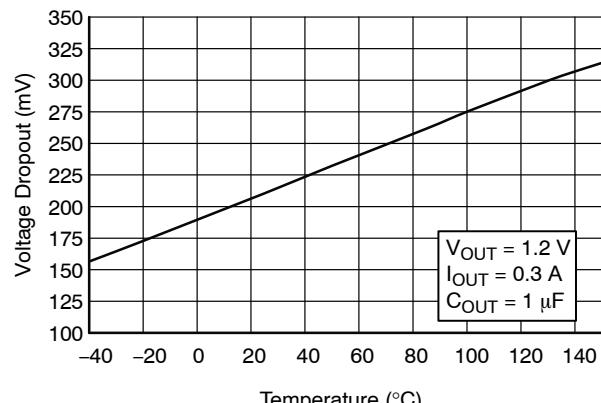
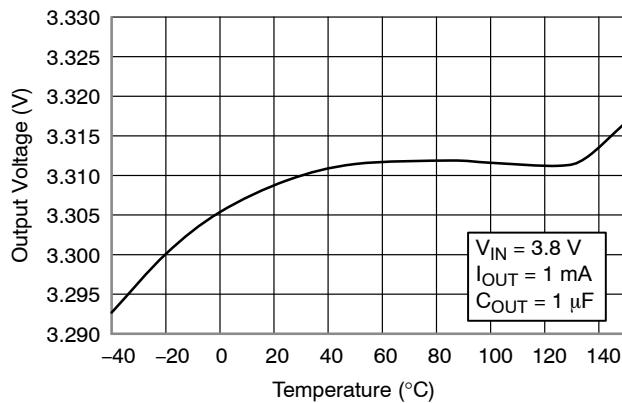
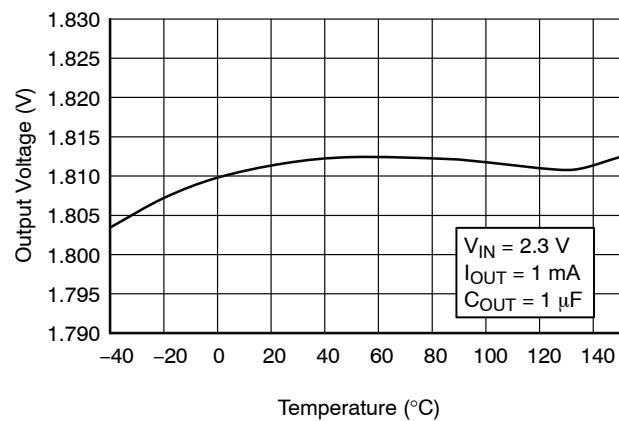
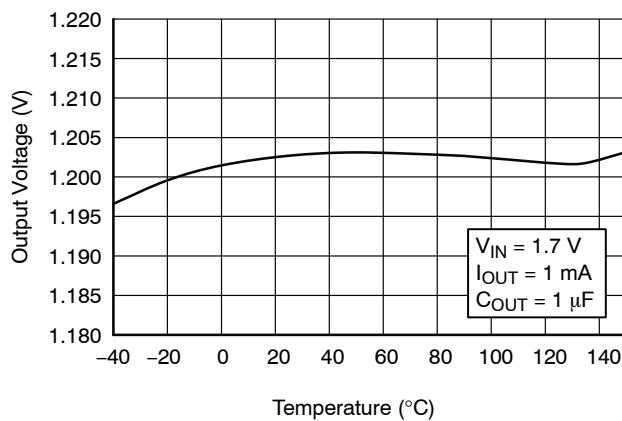
( $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$ ;  $V_{\text{IN}} = V_{\text{OUT}(\text{NOM})} + 0.5 \text{ V}$ ;  $I_{\text{OUT}} = 1 \text{ mA}$ ,  $C_{\text{IN}} = C_{\text{OUT}} = 1 \mu\text{F}$ ,  $V_{\text{EN}} = V_{\text{IN}}$ , unless otherwise noted.  
Typical values are at  $T_J = +25^{\circ}\text{C}$  (Note 5))

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Power Supply Rejection Ratio (Note 7)	$V_{\text{OUT}(\text{NOM})} = 3.3 \text{ V}$ , $I_{\text{OUT}} = 10 \text{ mA}$	$f = 100 \text{ Hz}$	P <sub>SRR</sub>	83 85 80 61			dB
		$f = 1 \text{ kHz}$					
		$f = 10 \text{ kHz}$					
		$f = 100 \text{ kHz}$					
Output Voltage Noise (Fixed Ver.)	$f = 10 \text{ Hz to } 100 \text{ kHz}$	$I_{\text{OUT}} = 10 \text{ mA}$	V <sub>N</sub>		9		$\mu\text{V}_{\text{RMS}}$
Thermal Shutdown Threshold (Note 7)	Temperature rising		T <sub>SDH</sub>		165		$^{\circ}\text{C}$
	Temperature hysteresis		T <sub>HYST</sub>		15		$^{\circ}\text{C}$
Active output discharge resistance	$V_{\text{EN}} < 0.25 \text{ V}$ , Version A only		R <sub>DIS</sub>		260		$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization.  
Production tested at  $T_J = T_A = 25^{\circ}\text{C}$ .
6. Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible. Dropout voltage is characterized when  $V_{\text{OUT}}$  falls 3% below  $V_{\text{OUT}(\text{NOM})}$ .
7. Guaranteed by design and characterization.

## TYPICAL CHARACTERISTICS



## TYPICAL CHARACTERISTICS (continued)

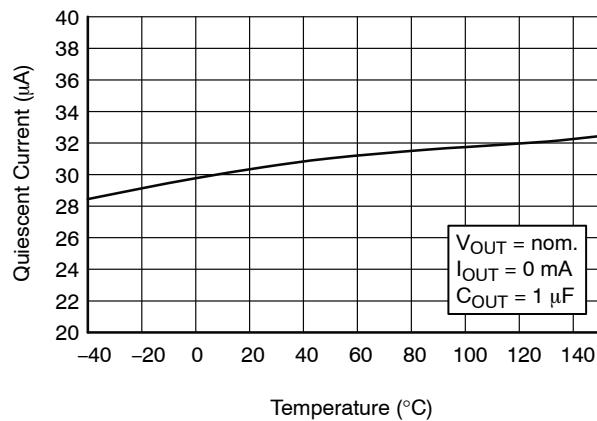


Figure 8. Quiescent Current vs. Temperature

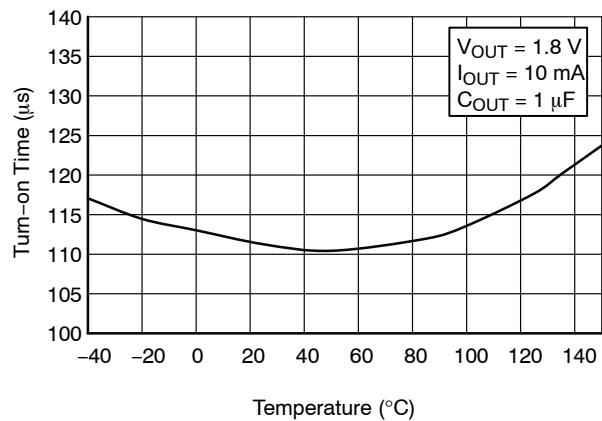


Figure 9. Turn-on Time vs. Temperature

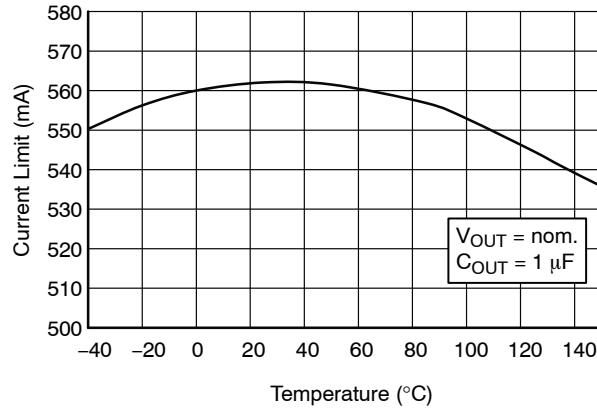


Figure 10. Current Limit vs. Temperature

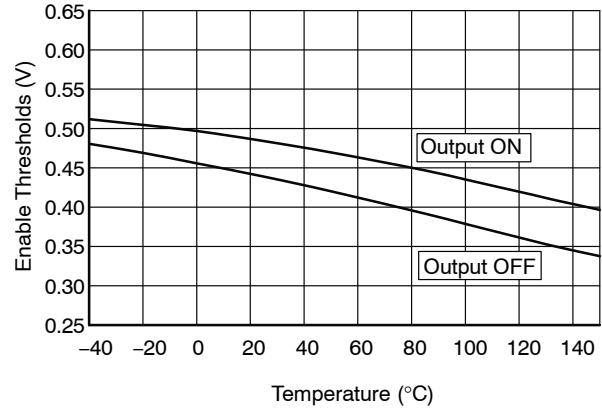


Figure 11. Enable Thresholds vs. Temperature

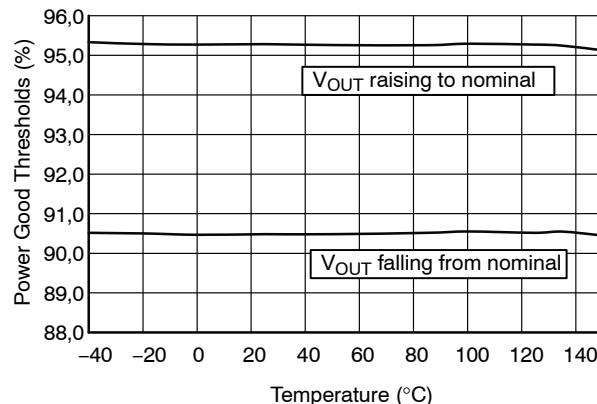


Figure 12. Power Good Threshold vs. Temperature

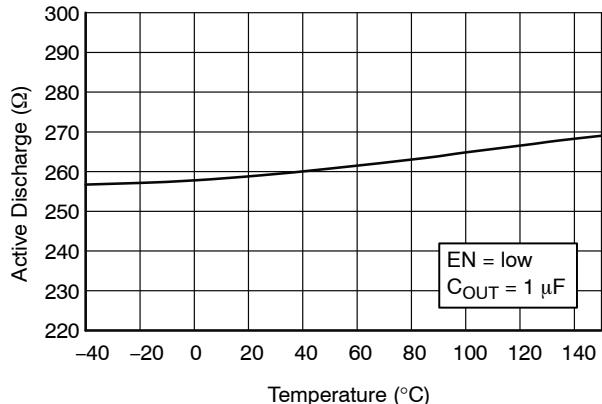
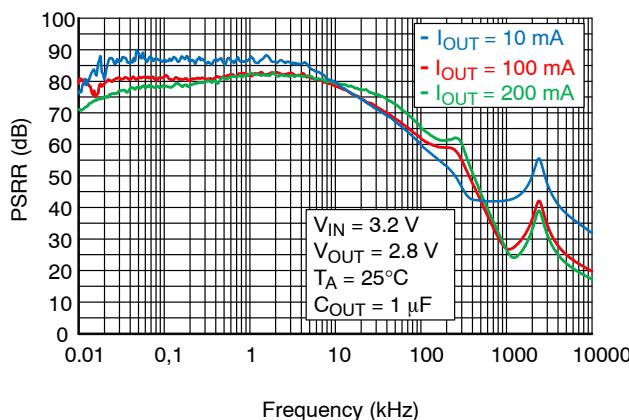
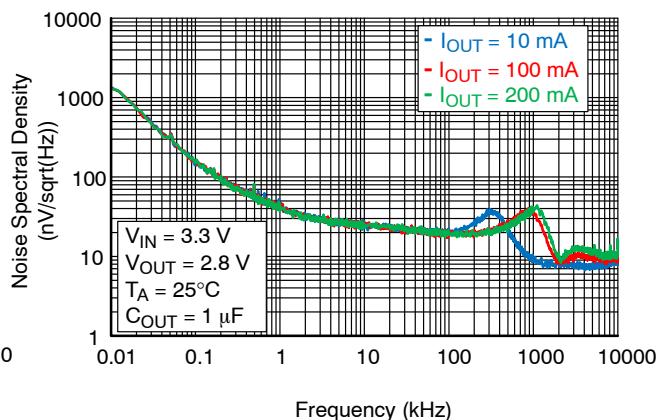


Figure 13. Active Discharge Resistance vs. Temperature

## TYPICAL CHARACTERISTICS (continued)



**Figure 14. Power Supply Rejection Ratio for  $V_{OUT} = 2.8\text{ V}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$**



**Figure 15. Output Voltage Noise Spectral Density for  $V_{OUT} = 2.8\text{ V}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$**

## APPLICATIONS INFORMATION

The NCV8164 is the member of new family of high output current and low dropout regulators which delivers low quiescent and ground current consumption, good noise and power supply ripple rejection ratio performance. The NCV8164 incorporates EN pin and power good output for simple controlling by MCU or logic. Standard features include current limiting, soft-start feature and thermal protection.

**Input Decoupling ( $C_{IN}$ )**

It is recommended to connect at least  $1\text{ }\mu\text{F}$  ceramic X5R or X7R capacitor between IN and GND pin of the device. This capacitor will provide a low impedance path for any unwanted AC signals or noise superimposed onto constant input voltage. The good input capacitor will limit the influence of input trace inductances and source resistance during sudden load current changes. Higher capacitance and lower ESR capacitors will improve the overall line transient response.

**Output Decoupling ( $C_{OUT}$ )**

The NCV8164 does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. The device is designed to be stable with standard ceramics capacitors with values of  $1\text{ }\mu\text{F}$  or greater. The X5R and X7R types have the lowest capacitance variations over temperature thus they are recommended.

**Power Good Output Connection**

The NCV8164 include Power Good functionality for better interfacing to MCU system. Power Good output is open collector type, capable to sink up to  $10\text{ mA}$ . Recommended operating current is between  $10\text{ }\mu\text{A}$  and

$1\text{ mA}$  to obtain low saturation voltage. External pull-up resistor can be connected to any voltage up to  $5.5\text{ V}$  (please see Absolute Maximum Ratings table above).

**Power Dissipation and Heat Sinking**

The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to  $+125^\circ\text{C}$ , however device is capable to work up to junction temperature  $+150^\circ\text{C}$ . The maximum power dissipation the NCV8164 can handle is given by:

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{QJA}} \quad (\text{eq. 1})$$

The power dissipated by the NCV8164 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND}(I_{OUT})) + I_{OUT}(V_{IN} - V_{OUT}) \quad (\text{eq. 2})$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + (V_{OUT} \times I_{OUT})}{I_{OUT} + I_{GND}} \quad (\text{eq. 3})$$

**Hints**

$V_{IN}$  and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8164, and make traces as short as possible.

**Adjustable Version**

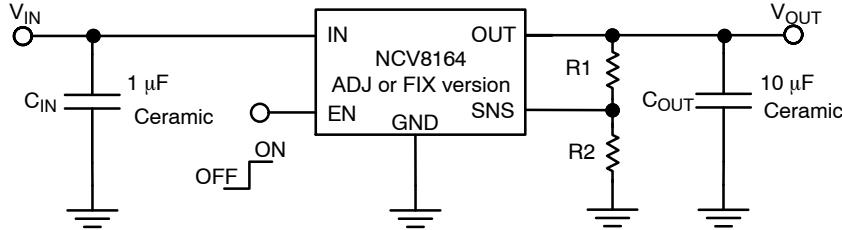
Not only adjustable version, but also any fixed version can be used to create adjustable voltage, where original fixed voltage becomes reference voltage for resistor divider and feedback loop. Output voltage can be equal or higher than original fixed option, while possible range is from 1.2 V up to 5.0 V. Figure 16 shows how to add external resistors to increase output voltage above fixed value.

Output voltage is then given by equation

$$V_{\text{OUT}} = V_{\text{FIX}} \times (1 + R1/R2) \quad (\text{eq. 4})$$

where  $V_{\text{FIX}}$  is voltage of original fixed version (from 1.2 V up to 5.0 V) or adjustable version (1.2 V). Do not operate the device at output voltage about 5.2 V, as device can be damaged.

In order to avoid influence of current flowing into SNS pin to output voltage accuracy (SNS current varies with voltage option and temperature, typical value is 300 nA) it is recommended to use values of R1 and R2 below 500 k $\Omega$ .



**Figure 16. Adjustable Variant Application**

Please note that output noise is amplified by  $V_{\text{OUT}} / V_{\text{FIX}}$  ratio. For example, if original 1.2 V fixed variant is used to create 3.6 V output voltage, output noise is increased  $3.6 / 1.2 = 3$  times and real value will be  $3 \times 9 \mu\text{V}_{\text{rms}} = 27 \mu\text{V}_{\text{rms}}$ . For noise sensitive applications it is

recommended to use as high fixed variant as possible – for example in case above it is better to use 3.3 V fixed variant to create 3.6 V output voltage, as output noise will be amplified only  $3.6 / 3.3 = 1.09 \times (9.8 \mu\text{V}_{\text{rms}})$ .

# NCV8164

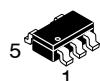
## ORDERING INFORMATION

Device part no.	Voltage Option	Marking	Option	Package	Shipping †
NCV8164ASNADJT1G	ADJ	M2	With Active Output Discharge	TSOP-5 (Pb-Free)	3000 / Tape & Reel
NCV8164ASN120T1G	1.2 V	MA	With Active Output Discharge		
NCV8164ASN150T1G	1.5 V	MN	With Active Output Discharge		
NCV8164ASN180T1G	1.8 V	MJ	With Active Output Discharge		
NCV8164ASN250T1G	2.5 V	MP	With Active Output Discharge		
NCV8164ASN280T1G	2.8 V	MK	With Active Output Discharge		
NCV8164ASN300T1G	3.0 V	MQ	With Active Output Discharge		
NCV8164ASN330T1G	3.3 V	ML	With Active Output Discharge		
NCV8164AMTWADJTAG	ADJ	L3	With Active Output Discharge	WDFNW6 (WF, Pb-Free)	3000 / Tape & Reel
NCV8164AMTW110TAG	1.1 V	LC	With Active Output Discharge		
NCV8164AMTW120TAG	1.2 V	LA	With Active Output Discharge		
NCV8164AMTW180TAG	1.8 V	LJ	With Active Output Discharge		
NCV8164AMTW280TAG	2.8 V	LK	With Active Output Discharge		
NCV8164AMTW290TAG	2.9 V	LH	With Active Output Discharge		
NCV8164AMLADJTCG	ADJ	K2	With Active Output Discharge	DFNW8 (WF, Pb-Free)	3000 / Tape & Reel
NCV8164AML120TCG	1.2 V	KA	With Active Output Discharge		
NCV8164AML150TCG	1.5 V	KN	With Active Output Discharge		
NCV8164AML180TCG	1.8 V	KJ	With Active Output Discharge		
NCV8164AML250TCG	2.5 V	KP	With Active Output Discharge		
NCV8164AML280TCG	2.8 V	KK	With Active Output Discharge		
NCV8164AML300TCG	3.0 V	KQ	With Active Output Discharge		
NCV8164AML330TCG	3.3 V	KL	With Active Output Discharge		

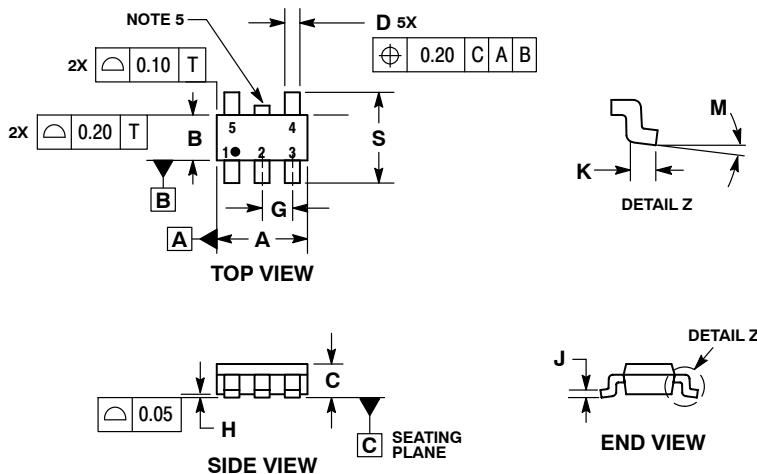
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**MECHANICAL CASE OUTLINE**  
PACKAGE DIMENSIONS

**onsemi**<sup>TM</sup>



SCALE 2:1



**TSOP-5**  
CASE 483  
ISSUE N

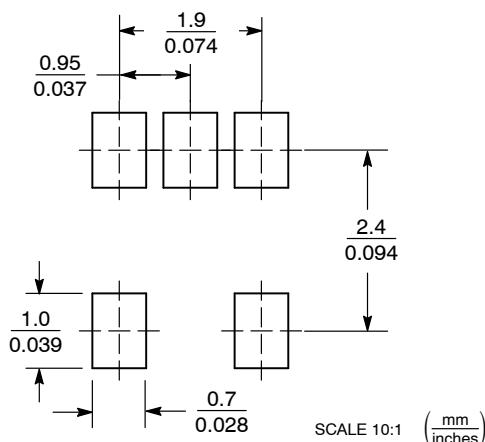
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

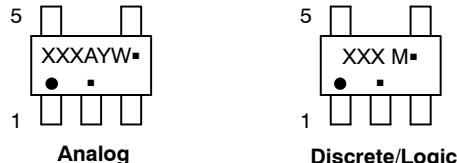
MILLIMETERS		
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0°	10°
S	2.50	3.00

**SOLDERING FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***



XXX = Specific Device Code    XXX = Specific Device Code  
 A = Assembly Location    M = Date Code  
 Y = Year    □ = Pb-Free Package  
 W = Work Week  
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

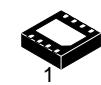
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DESCRIPTION:	TSOP-5	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

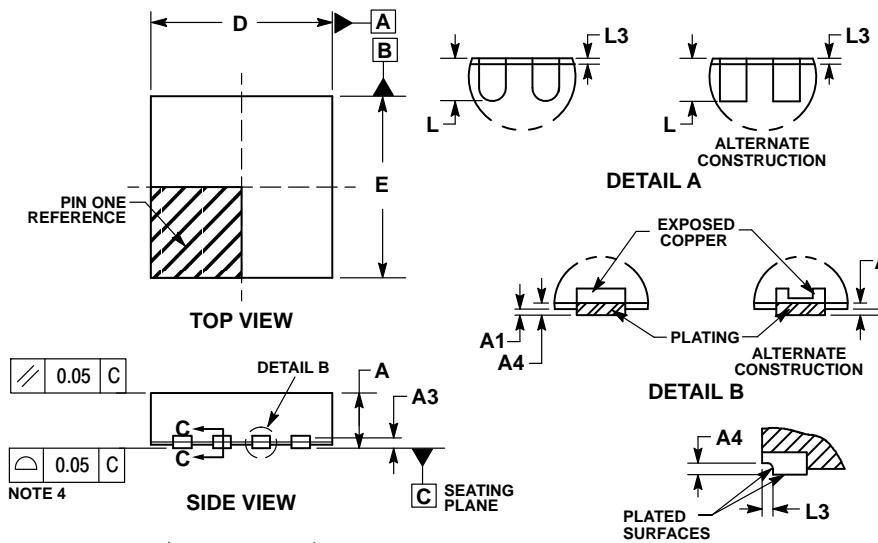
ON Semiconductor®



SCALE 2:1

DFNW8 3x3, 0.65P  
CASE 507AD  
ISSUE A

DATE 15 JUN 2018

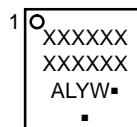


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION *b* APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURE TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3	0.20	REF	
A4	0.10	---	---
<i>b</i>	0.25	0.30	0.35
D	2.90	3.00	3.10
D2	2.30	2.40	2.50
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
e	0.65	BSC	
K	0.28	REF	
L	0.30	0.40	0.50
L3	0.05	REF	

### GENERIC MARKING DIAGRAM\*



XXXXXX = Specific Device Code

A = Assembly Location

L = Wafer Lot

Y = Year

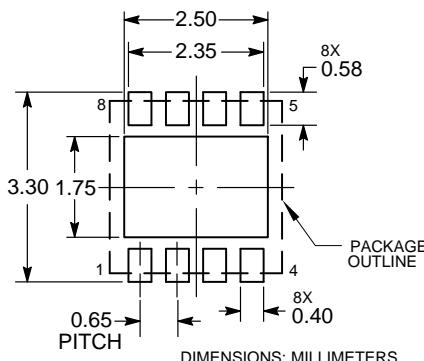
W = Work Week

■ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

### RECOMMENDED SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERMM/D.

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DESCRIPTION:	DFNW8 3x3, 0.65P	PAGE 1 OF 1

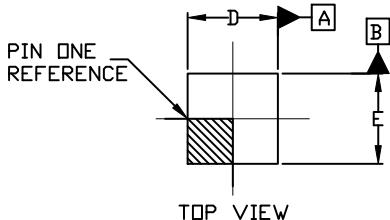
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# **MECHANICAL CASE OUTLINE**

## **PACKAGE DIMENSIONS**

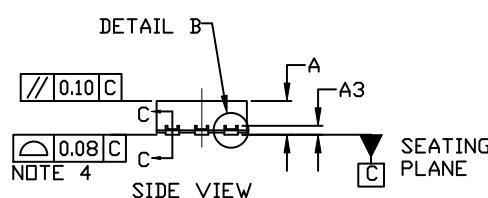


SCALE 4:1

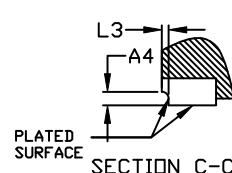


**WDFNW6 2x2, 0.65P**  
**CASE 511DW**  
**ISSUE B**

DATE 15 JUN 2018

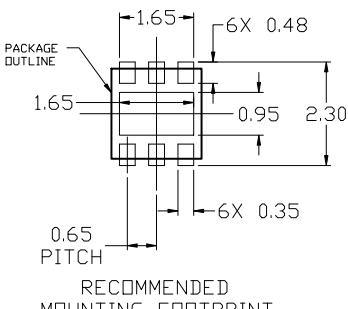


DETAIL A



The diagram illustrates a cross-section of a printed circuit board. A horizontal line represents the 'PLATED SURFACE'. A vertical line labeled 'A1' extends from the surface. A diagonal line labeled 'A4' extends from the surface. A shaded rectangular area, representing 'EXPOSED COPPER', is located at the intersection of A1 and A4. A second shaded rectangular area, representing 'ALTERNATE', is located further down the A4 line, below the first shaded area. Dashed arcs above the lines A1 and A4 indicate the continuation of the plated surface.

## DETAILS



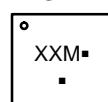
RECOMMENDED  
MOUNTING FOOTPRINT

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.80	0.90	1.00
e	0.65 BSC		
K	0.25 REF		
L	0.25	0.30	0.35
L3	0.05 REF		

## GENERIC MARKING DIAGRAM\*



M = Month Code

- M = Month Code
- ▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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<b>DESCRIPTION:</b>	<b>WDFNW6 2x2, 0.65P</b>	<b>PAGE 1 OF 1</b>

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