60V DUAL N-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_C = +25°C
60V	12.5mΩ @ V_{GS} = 10V	44A
	16.8mΩ @ V_{GS} = 4.5V	38A

Features

- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- Low Input Capacitance
- Fast Switching Speed
- Wettable Flank for Improved Optical Inspection
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Description and Applications

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

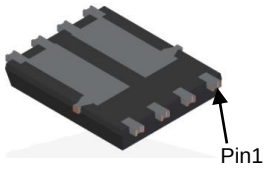
- Wireless Charging
- DC-DC Converters
- Power Management

Mechanical Data

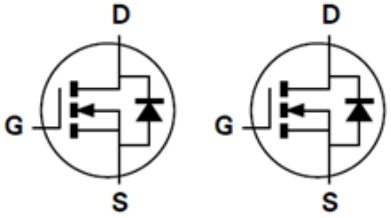
- Case: PowerDI®5060-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish – Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

PowerDI5060-8/SWP (Type UXD)

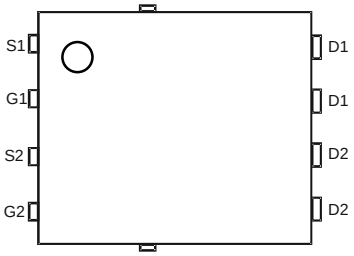
Top View



Bottom View



Internal Schematic



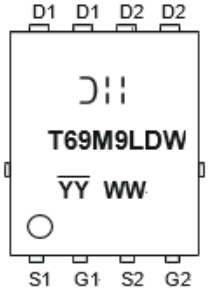
Top View
Pin Configuration

Ordering Information (Note 4)

Part Number	Case	Packaging
DMT69M9LPDW-13	PowerDI5060-8/SWP (Type UXD)	2500/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
T69M9LDW = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 21 = 2021)
WW = Week Code (01 to 53)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	60	V
Gate-Source Voltage			V_{GSS}	±16	V
Continuous Drain Current, V_{GS} = 10V (Note 6)		T_C = +25°C T_C = +70°C	I_D	44.0 35.5	A
Continuous Drain Current, V_{GS} = 10V (Note 5)	Steady State	T_A = +25°C T_A = +70°C	I_D	11.0 8.8	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I_{DM}	176	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	44	A
Pulsed Body Diode Forward Current (10µs Pulse, Duty Cycle = 1%)			I_{SM}	176	A
Avalanche Current, L = 0.1mH			I_{AS}	30	A
Avalanche Energy, L = 0.1mH			E_{AS}	45	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	2.5	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	50	°C/W
Total Power Dissipation (Note 6)	T_C = +25°C	P_D	40.3	W
Thermal Resistance, Junction to Case (Note 6)		$R_{\theta JC}$	3.1	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 48V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±16V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.7	—	2	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	9.9	12.5	mΩ	V_{GS} = 10V, I_D = 20A
		—	11.9	16.8		V_{GS} = 4.5V, I_D = 15A
Diode Forward Voltage	V_{SD}	—	0.9	1.2	V	V_{GS} = 0V, I_S = 20A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	—	2212	—	pF	V_{DS} = 30V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	495	—		
Reverse Transfer Capacitance	C_{rss}	—	46	—		
Gate Resistance	R_G	—	1.7	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 10V)	Q_g	—	33.5	—	nC	V_{DS} = 30V, I_D = 13.5A
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	15.6	—		
Gate-Source Charge	Q_{gs}	—	4.7	—		
Gate-Drain Charge	Q_{gd}	—	5.3	—		
Turn-On Delay Time	$t_{D(ON)}$	—	4.5	—	ns	V_{GS} = 10V, V_{DD} = 30V, R_G = 6Ω, I_D = 13.5A
Turn-On Rise Time	t_R	—	8.6	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	35.9	—		
Turn-Off Fall Time	t_F	—	15.7	—		
Reverse Recovery Time	t_{RR}	—	18.2	—	ns	I_F = 13.5A, di/dt = 400A/µs
Reverse Recovery Charge	Q_{RR}	—	33.1	—	nC	

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz. copper, with thermal bias to bottom layer 1inch square copper plate.
6. Thermal resistance from junction to soldering point (on the exposed drain pad).
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

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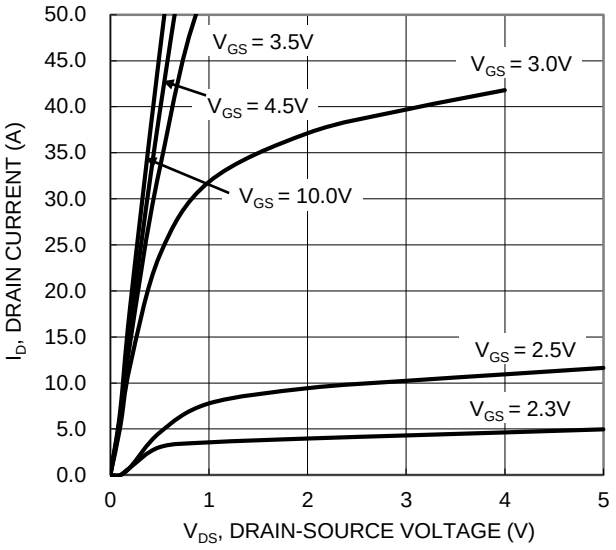

Figure 1. Typical Output Characteristic

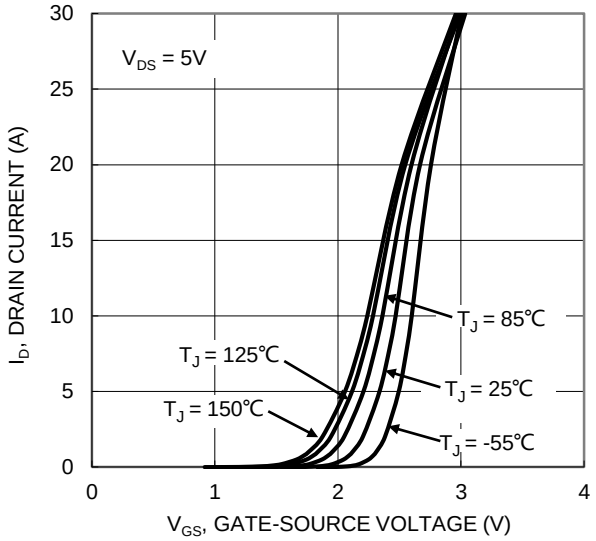

Figure 2. Typical Transfer Characteristic

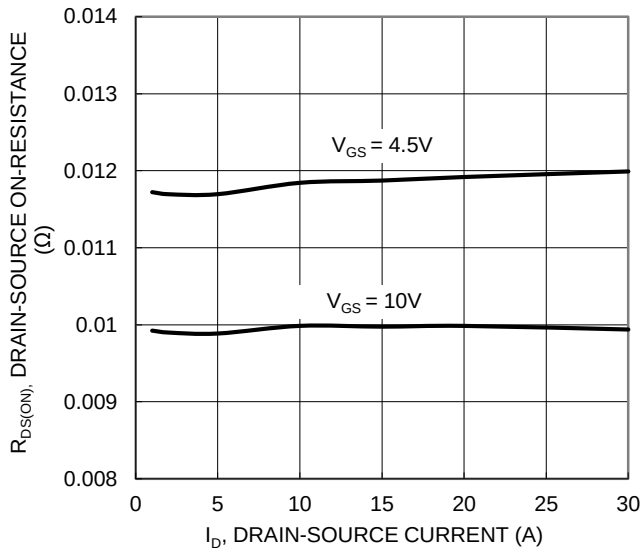

Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

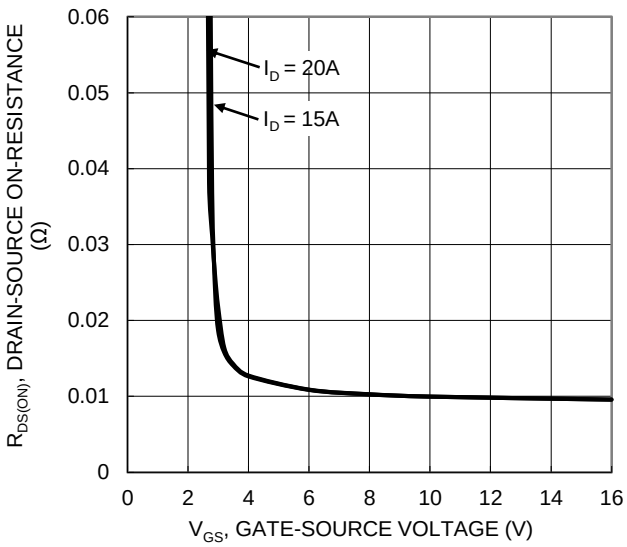

Figure 4. Typical Transfer Characteristic

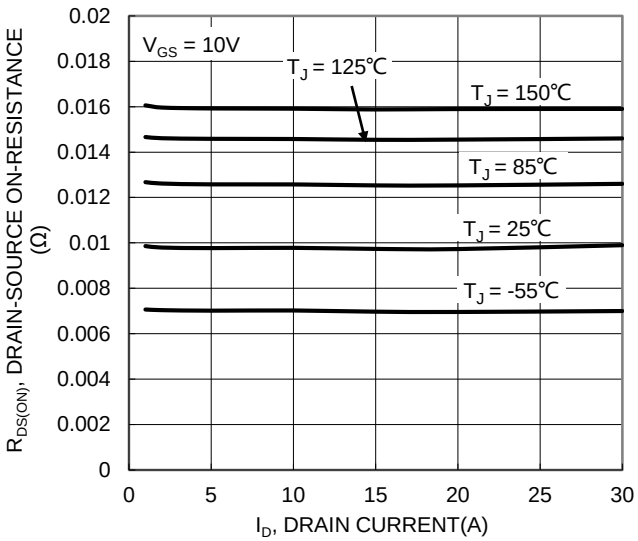

Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

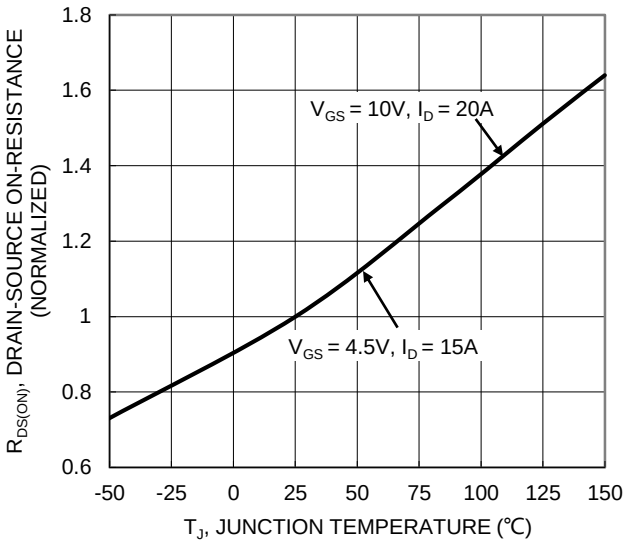

Figure 6. On-Resistance Variation with Junction Temperature

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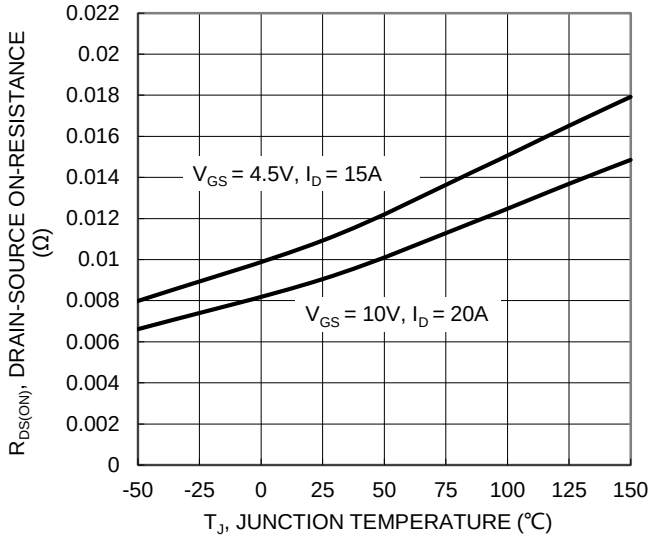

Figure 7. On-Resistance Variation with Junction Temperature

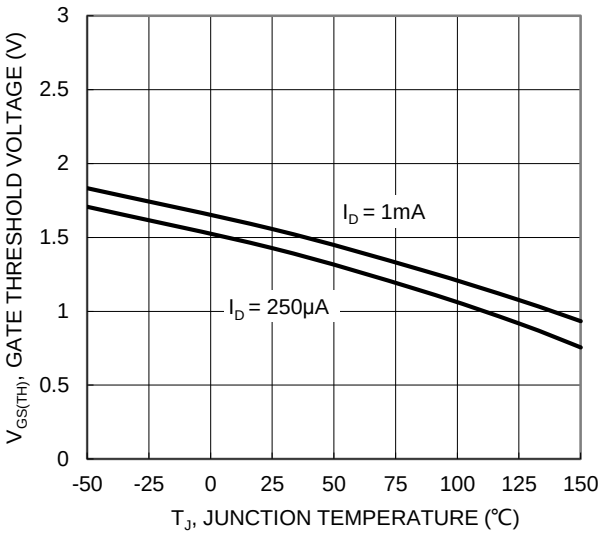

Figure 8. Gate Threshold Variation vs. Junction Temperature

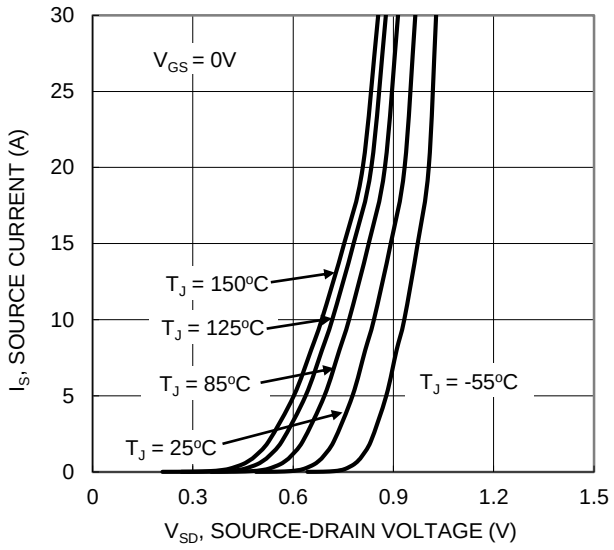

Figure 9. Diode Forward Voltage vs. Current

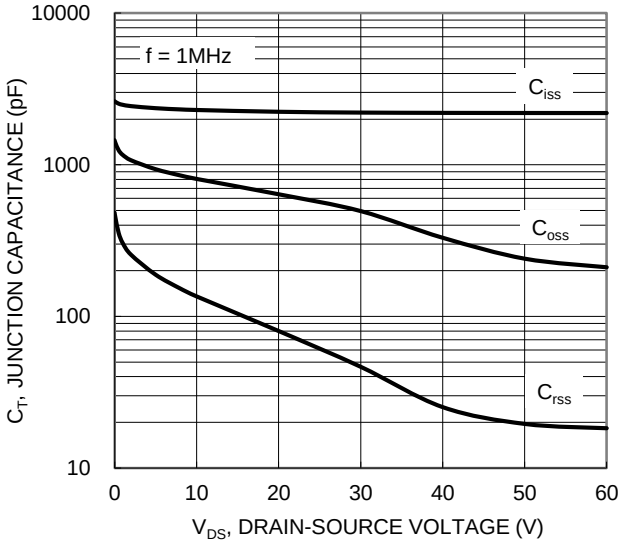

Figure 10. Typical Junction Capacitance

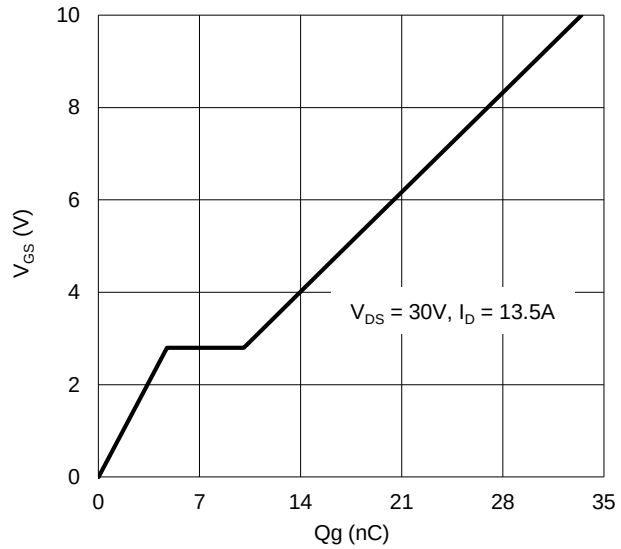

Figure 11. Gate Charge

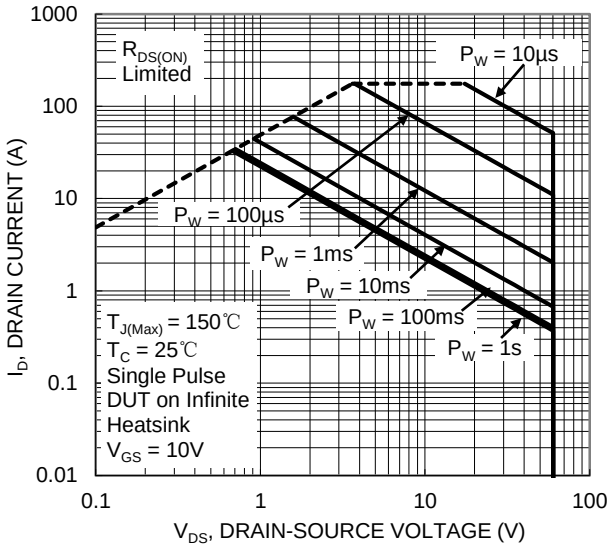

Figure 12. SOA, Safe Operation Area

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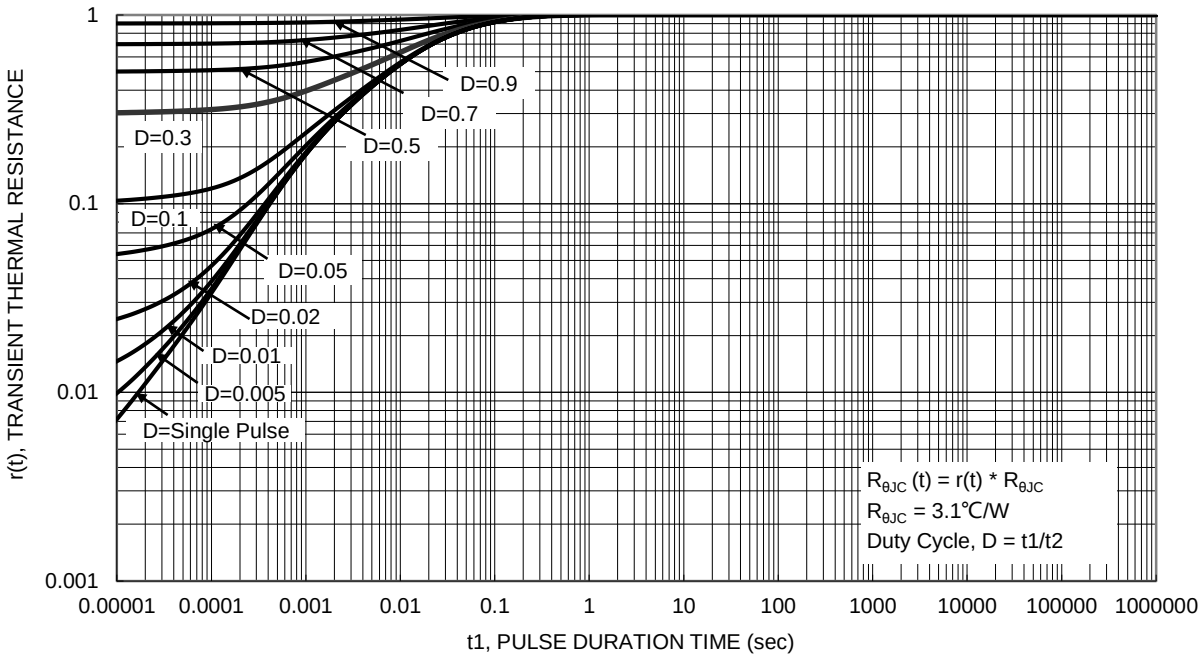

Figure 13. Transient Thermal Resistance

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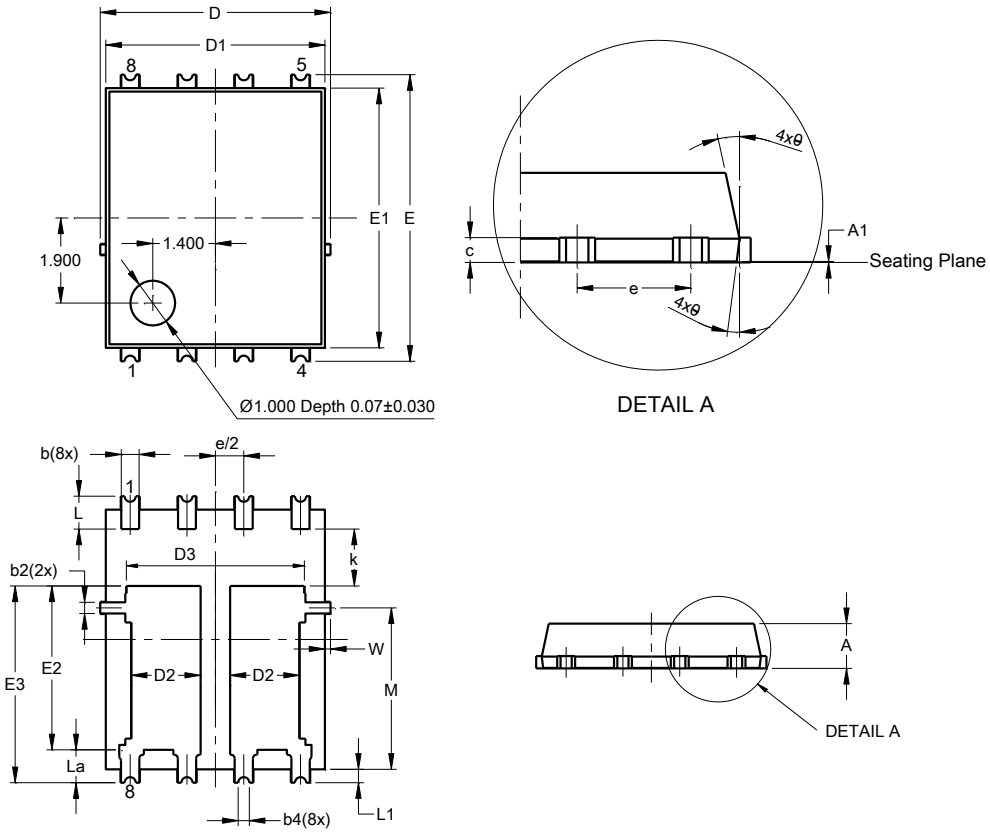
Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UXD)

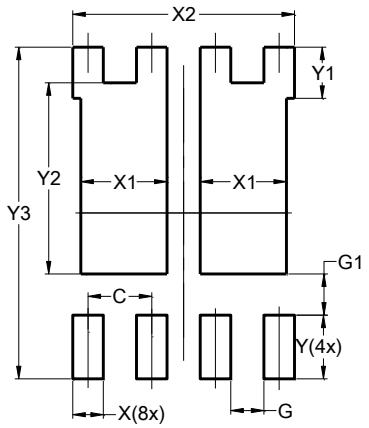


PowerDI5060-8/SWP (Type UXD)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0.00	0.05	--
b	0.30	0.50	0.41
b2	0.20	0.35	0.25
b4	0.25REF		
c	0.230	0.330	0.277
D	5.15 BSC		
D1	4.70	5.10	4.90
D2	1.46	1.66	1.55
D3	3.78	4.18	3.98
E	6.40 BSC		
E1	5.60	6.00	5.80
E2	3.46	3.86	3.66
E2a	4.195	4.595	4.395
e	1.27BSC		
k	1.05	--	--
L	0.635	0.835	0.735
La	0.635	0.835	0.735
L1	0.200	0.400	0.300
M	3.205	4.005	3.605
W	0.025	0.225	0.125
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8/SWP (Type UXD)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	1.720
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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