

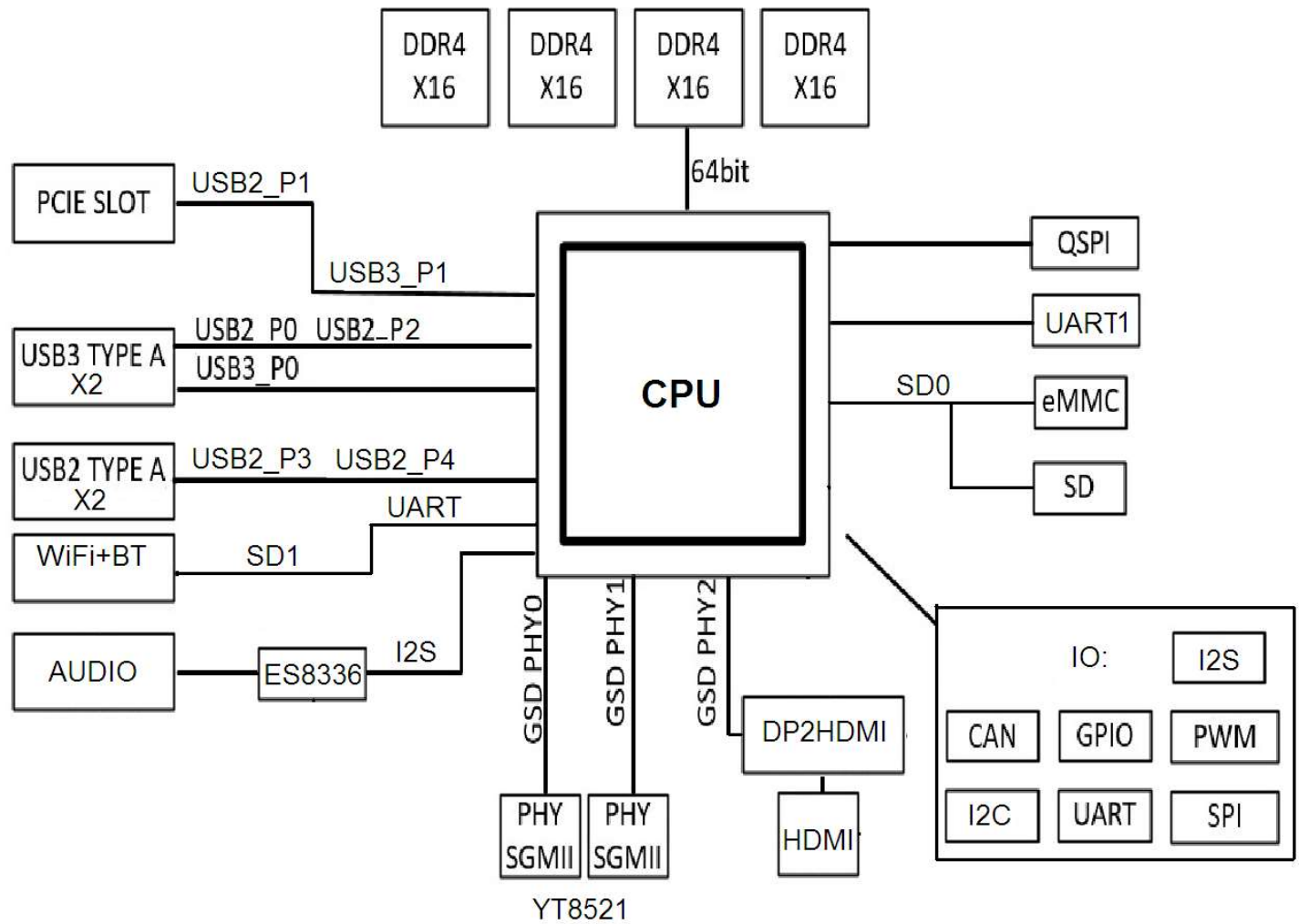
CEK8903-E2KQ_DDR4_ONBOARD

PHYTIUM
CONFIDENTIAL

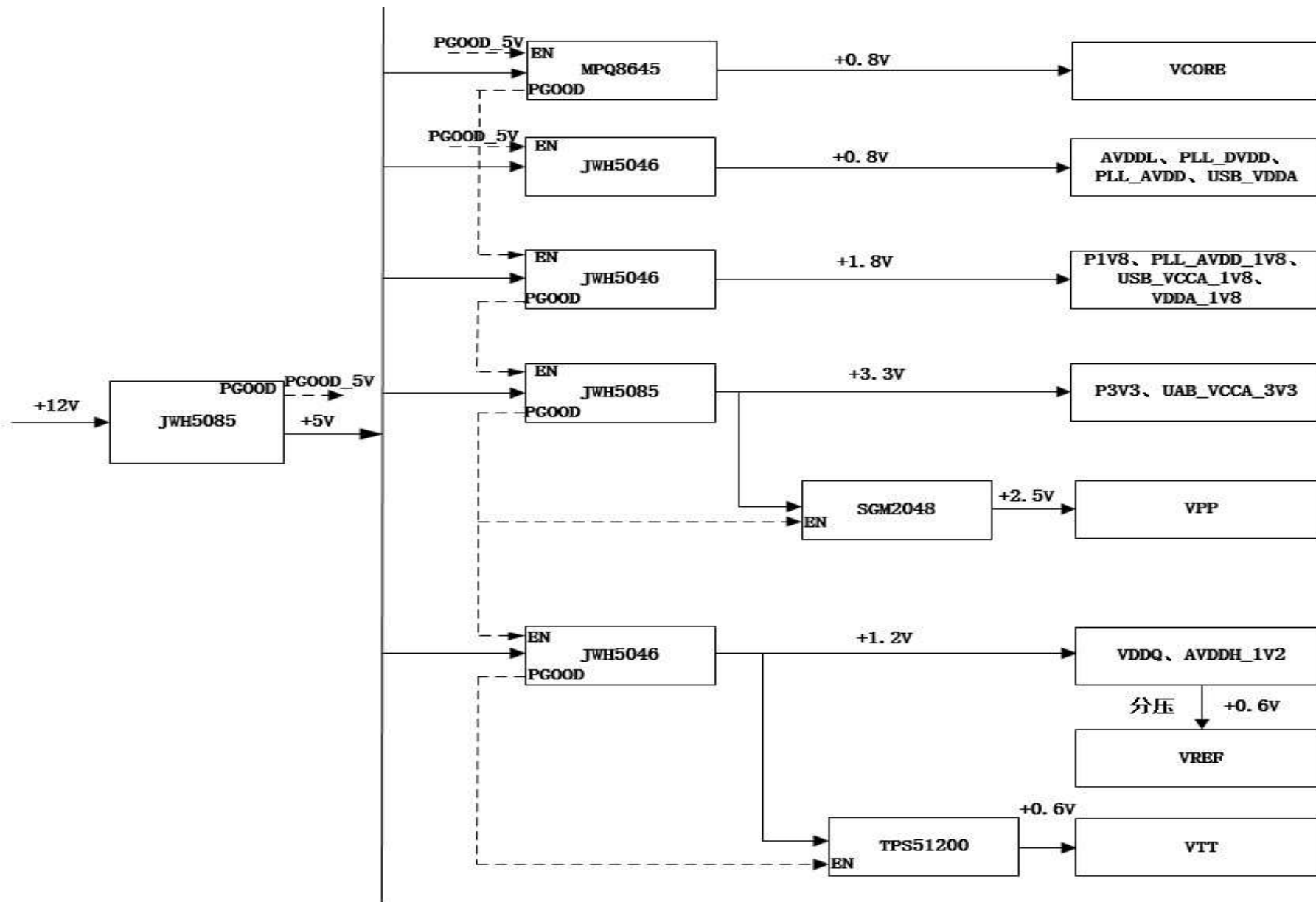
CONTENTS

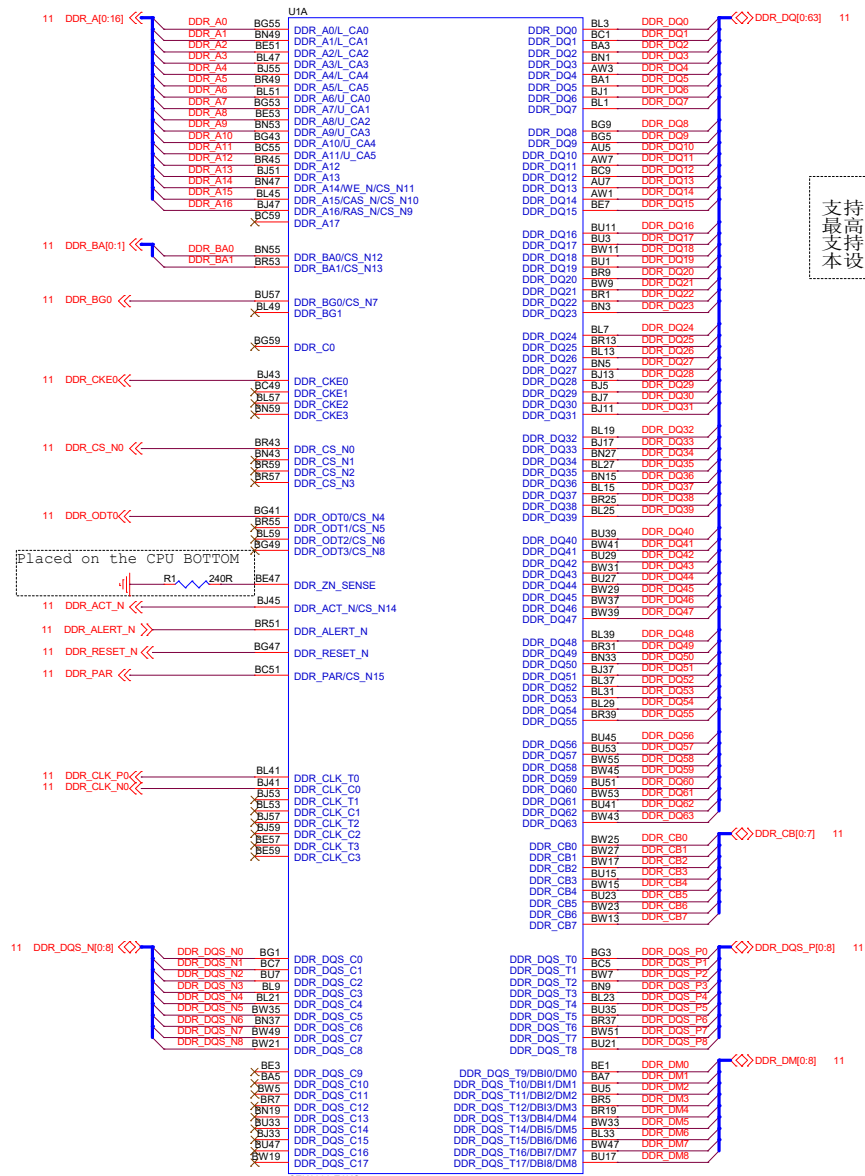
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CECport Firefly Workshop		
CEK8903-E2KQ		
Title: COVER_PAGE		
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YT8521





支持器件: DDR4: x4、x8、x16; LPDDR4: x16、x32,
 最高支持72个数据位。
 支持全位宽模式和半位宽模式(仅支持低32位数据和低4位ECC)
 本设计采用DDR4 x16颗粒

CECport Firefly Workshop

CEK8903-E2KQ

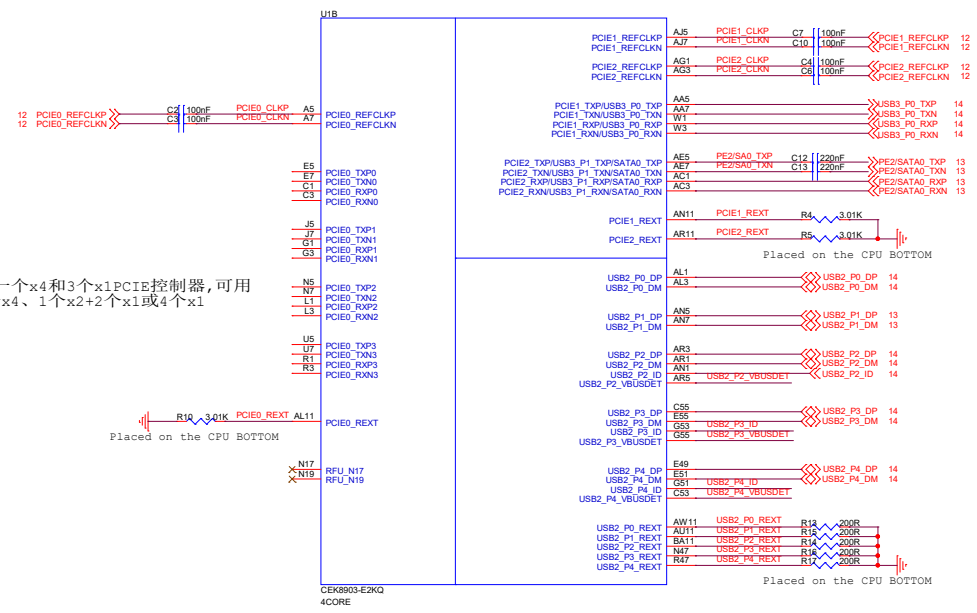
Title: CPU_MCU

Size: Custom Document Number: SCH20221128

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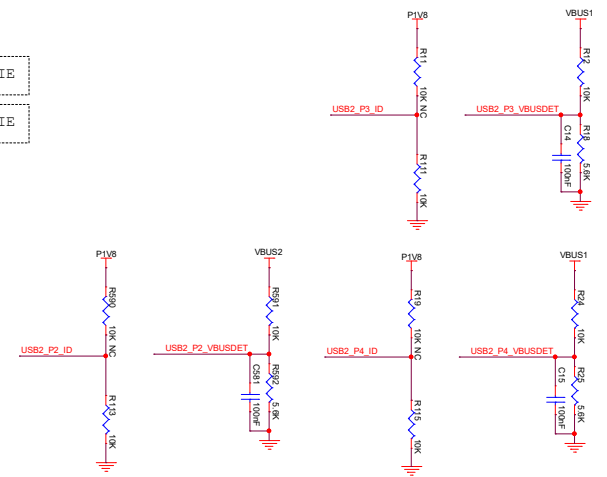
Rev: V1

包含一个x4和3个x1PCIE控制器,可用
作1个x4、1个x2+2个x1或4个x1



可用作x1PCIE

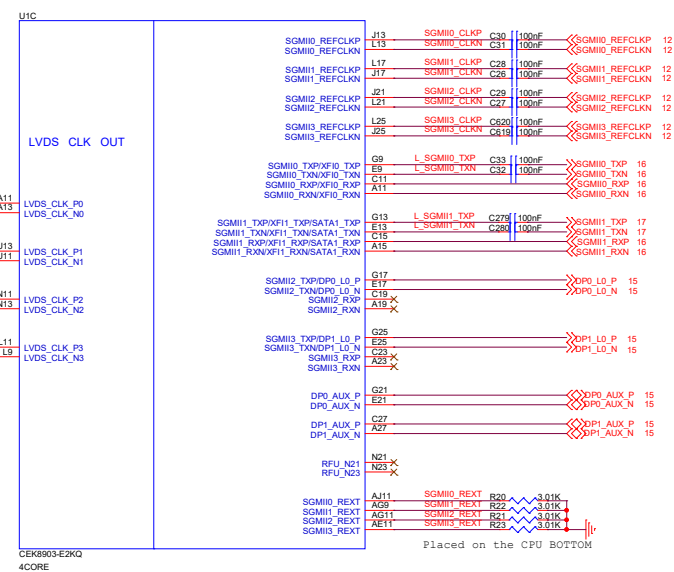
可用作x1PCIE



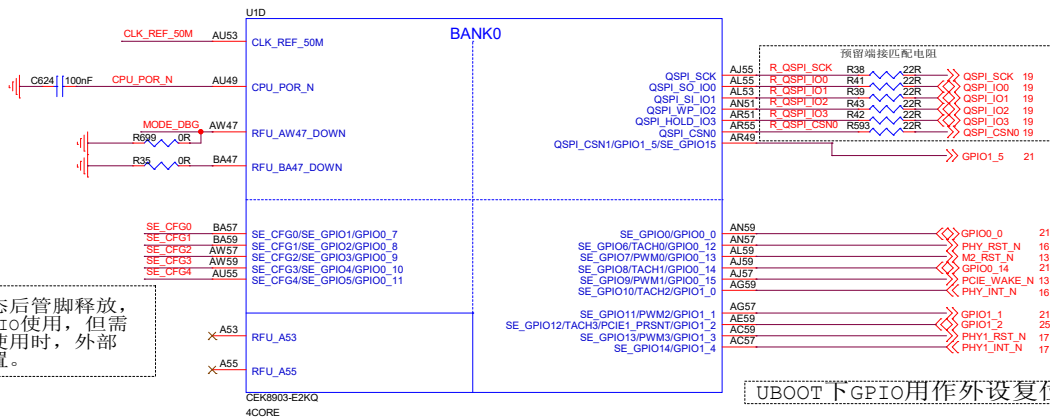
CEK8903-E2KQ包含了4个MAC控制器MAC0/1支持XFI和SGMII; MAC2/3支持SGMII和RGMII,且共用MDIO。

MDIO管理接口与MAC端口对应关系

MDIO管理接口	MAC端口类型
MDIO0/MDC0	SGMII0
MDIO1/MDC1	SGMII1
MDIO2/MDC2	SGMII2/RGMII0
MDIO3/MDC3	SGMII3/RGMII1



25 CPU_POR_N >> CLK_REF_50M TP2 TP



SE_CFG识别到启动设置状态后管脚释放，
可以作为通用GPIO与SE_GPIO使用，但需
注意这些管脚作为普通IO使用时，外部
电气环境不能干扰启动配置。

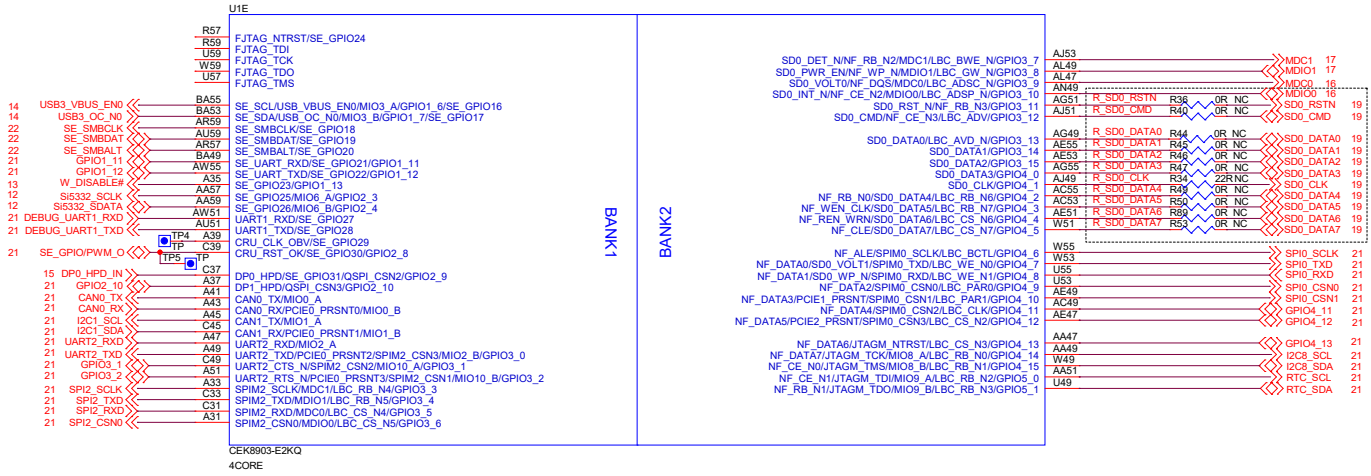
UBOOT下GPIO用作外设复位

具体应用场景下，建议使用4.7K电阻
上下拉确定启动配置信号

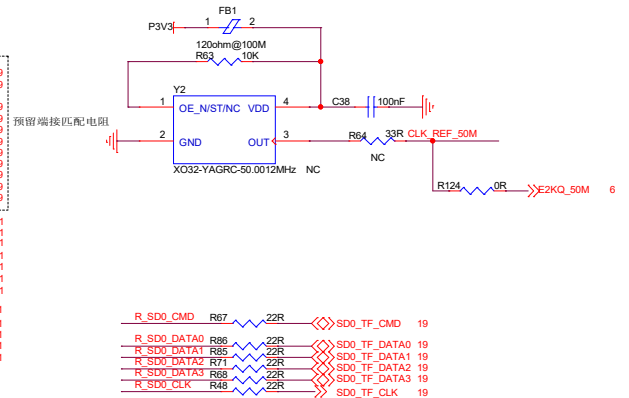


启动配置

SE_CFG[2:0]启动介质：
000:RESERVED
001:QSPI Default
010:LBC
011:NandFlash
100:SD0---SD CARD
101:SD1---SD CARD
110:SD0---eMMC
111:RESERVED
SE_CFG[4:3]启动段位：
00:Default (RECOVER0)
01:RECOVER1
10:RECOVER2
11:RECOVER3



本设计的BANK 电压如下：
bank (0、1、2) ----> 3.3V
bank (3、4、5) ----> 1.8V



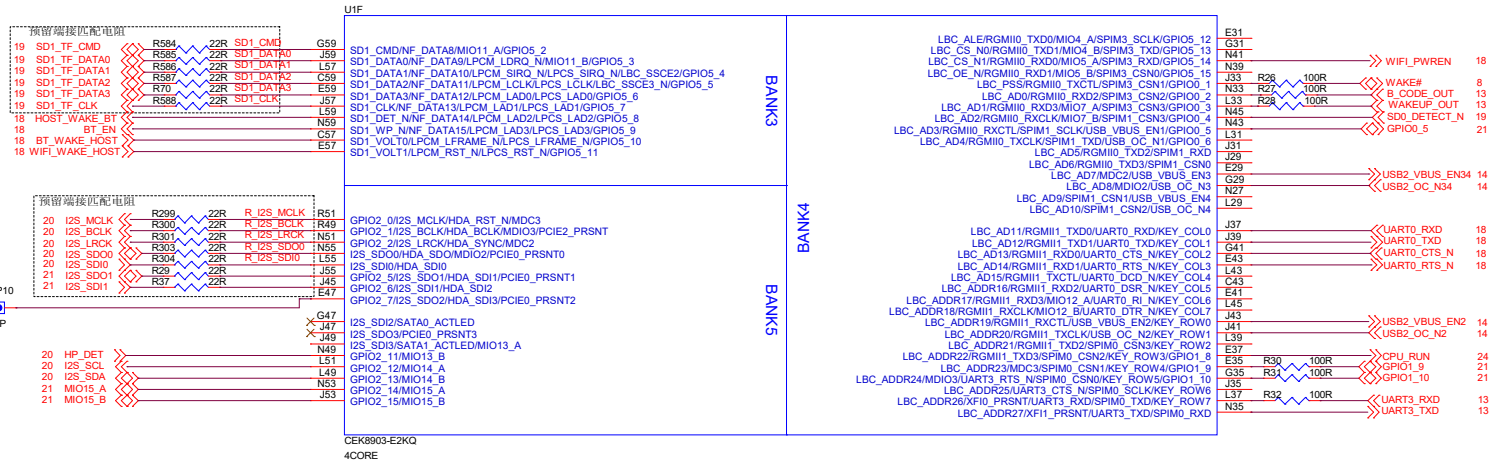
CECport Firefly Workshop

CEK8903-E2KQ

Title: CPU_GPIO_1

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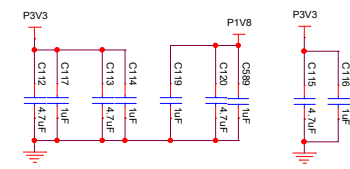
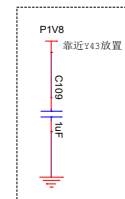
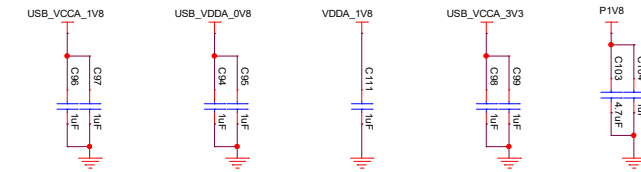
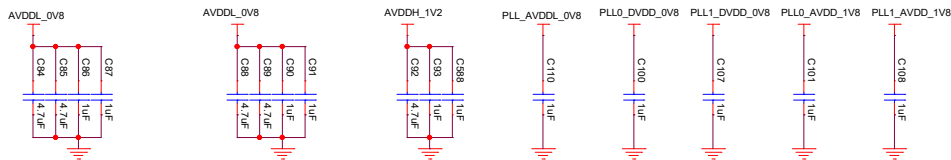
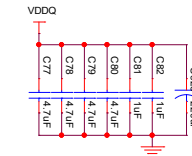
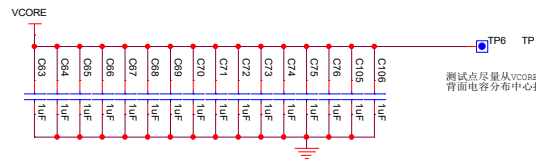
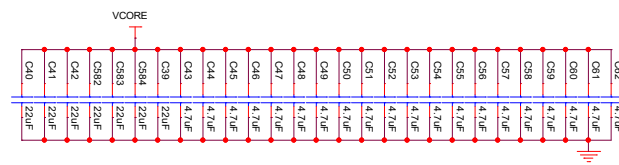
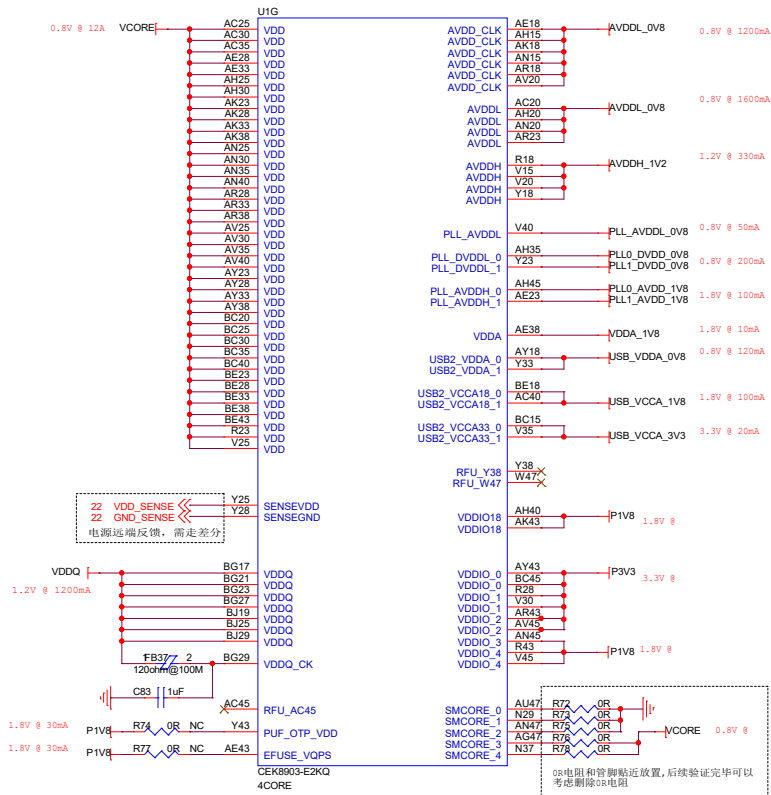
CECport Firefly Workshop

CEK8903-E2KQ

Title: CPU_GPIO_2

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BANK0~BANK4 供电电源为VDDIO x(0-4),均支持1.8V或3.3V电平;
SMCORE_x(0-4)为各bank电平控制信号,其与VDDIO_x(0-4)对应关系如下表:

SMCORE_x	VDDIO_x
0	3.3V
1	1.8V

1表示SMCORE_x(0-4)接CEK8903-E2KQ核心电压VDD
0表示SMCORE_x(0-4)接地

VDDIO18电源为各BANK IO保持电源及BANK5 IO
供电电源,需要保持常供电状态,且固定1.8V。

VDDIO_x接3.3V电源前,SMCORE_x必须接地,上下电过程中须保证
VDDIO_x(3.3V)和VDDIO18的电压压差在1.98V以内,否则有可靠性问题。

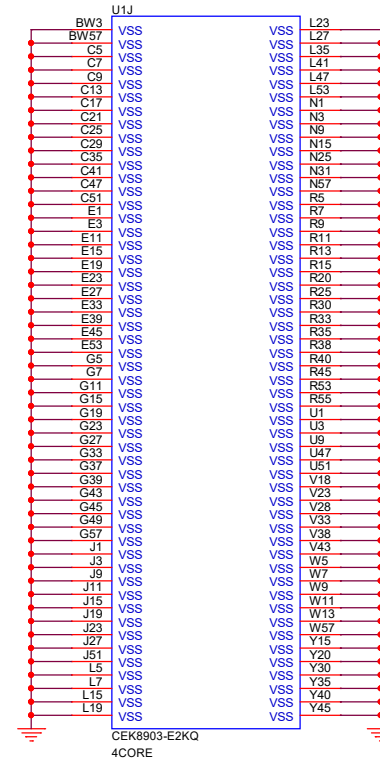
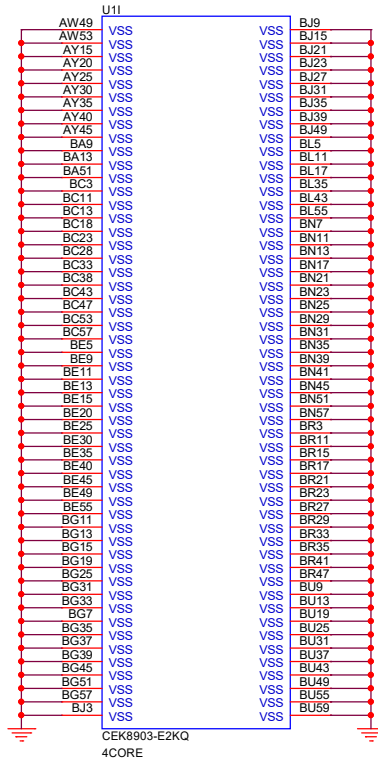
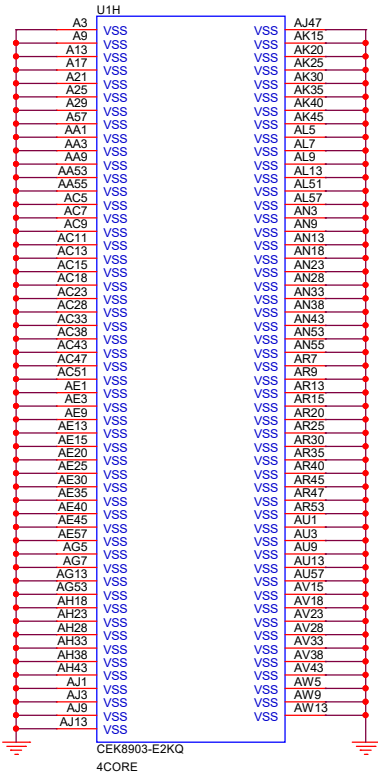
CECport Firefly Workshop

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File: CPU_POWER

Size: Custom Document Number: SCH20221128 Rev: V1

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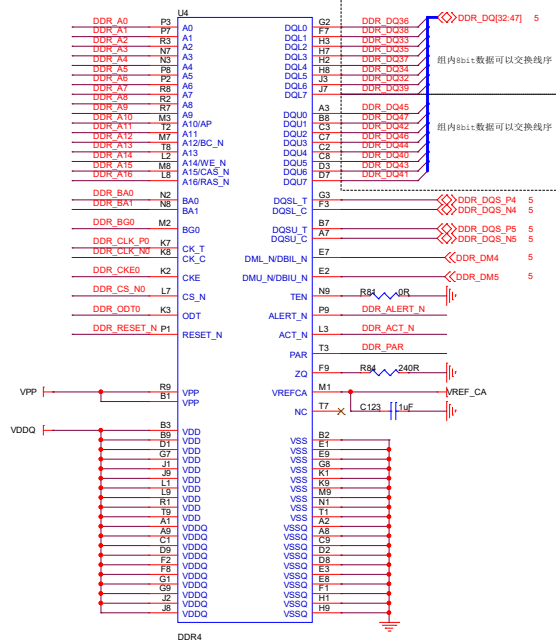
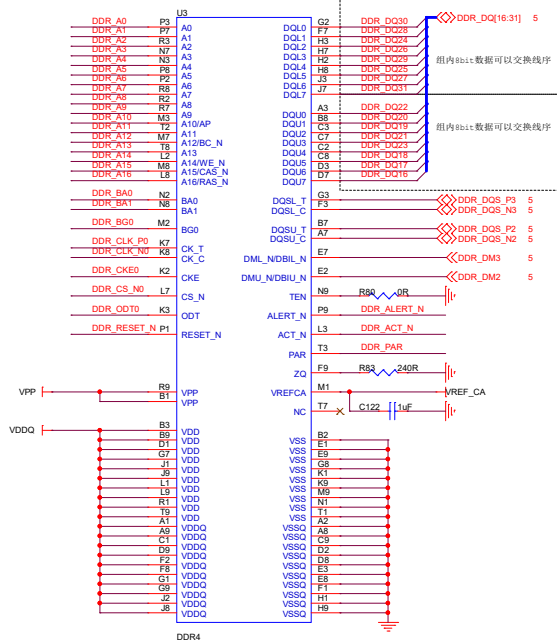
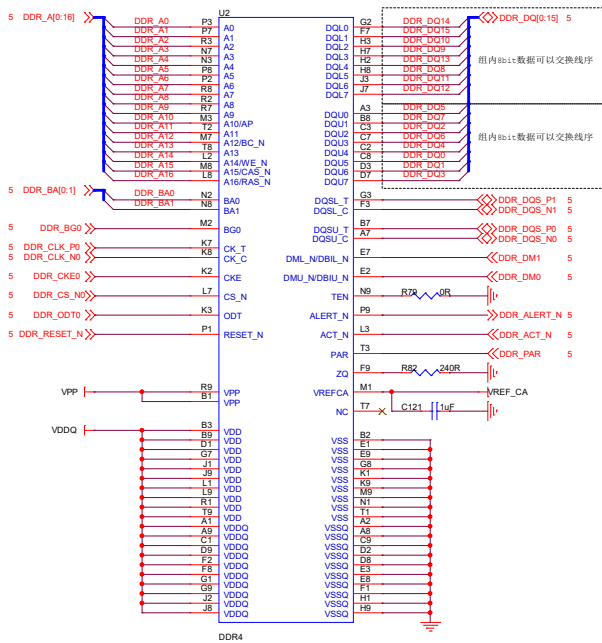
CECport Firefly Workshop

CEK8903-E2KQ

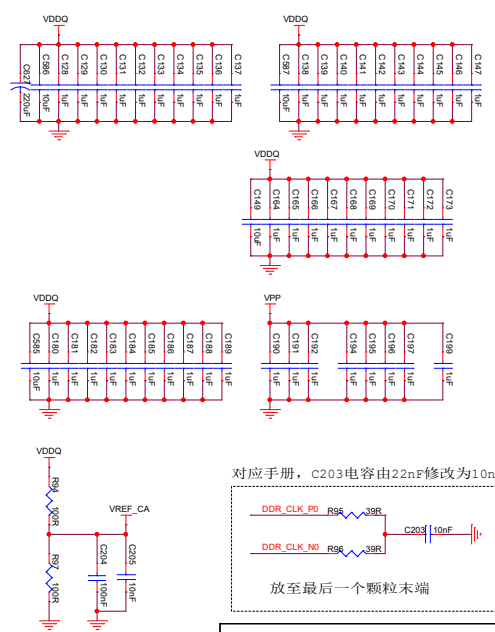
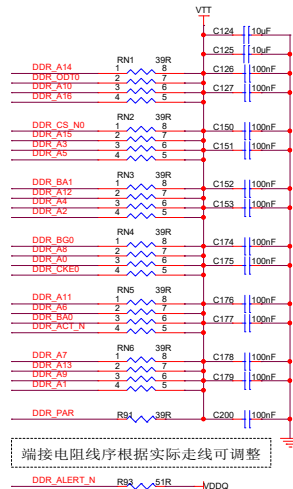
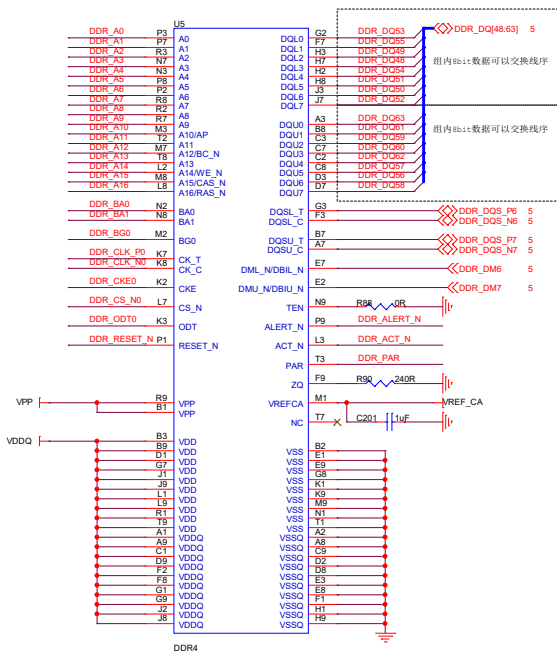
Title: CPU_VSS

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除ECC外，每个slice之间可以交换



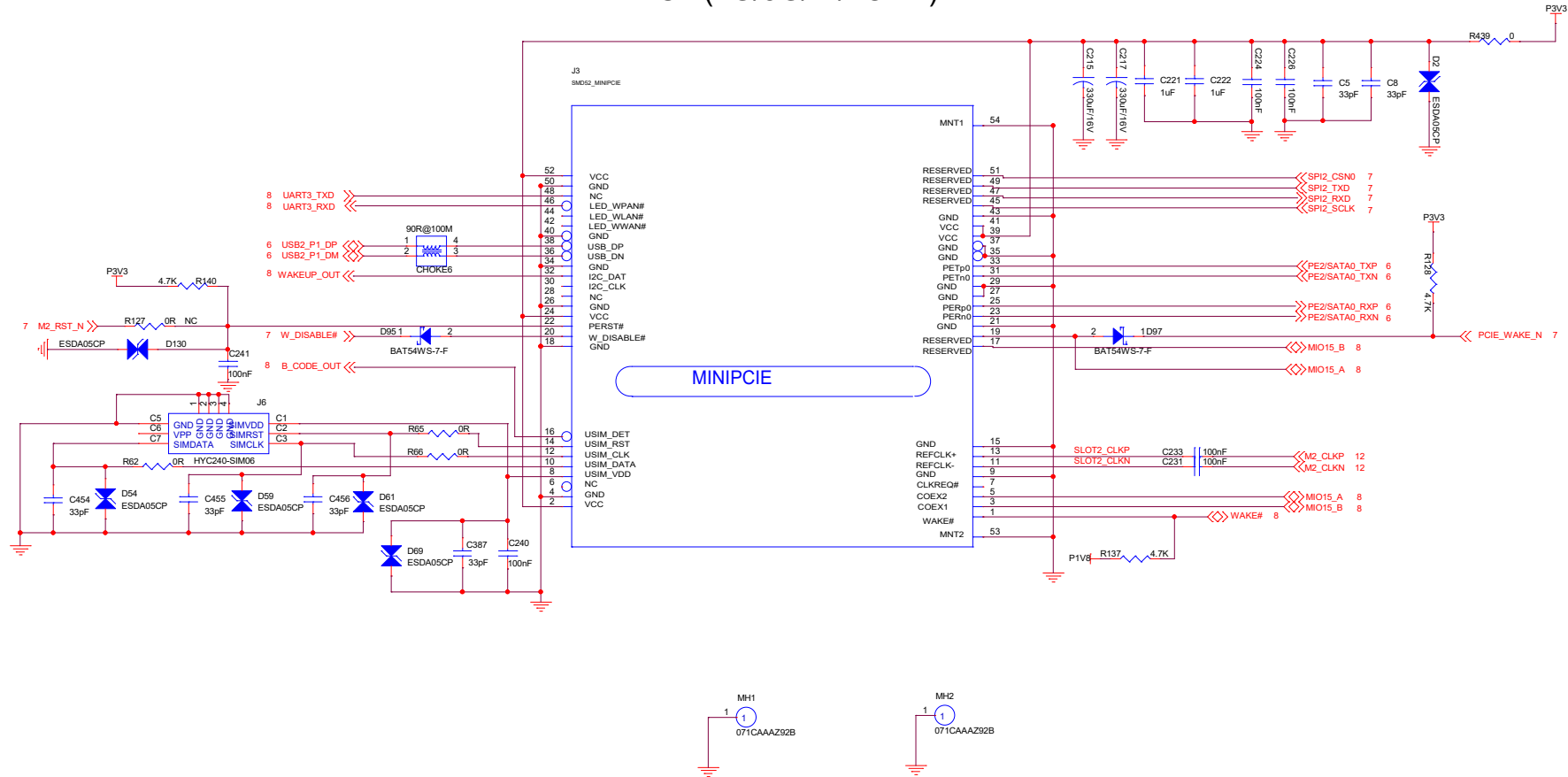
端接电阻线序根据实际走线可调整

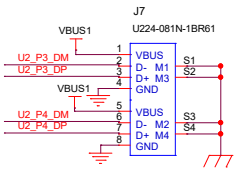
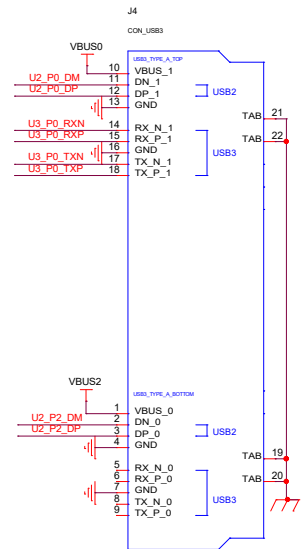
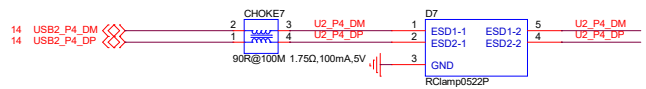
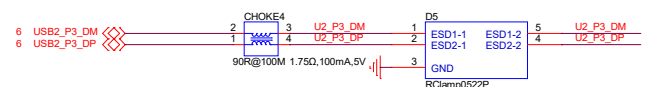
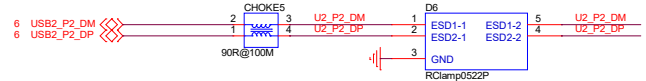
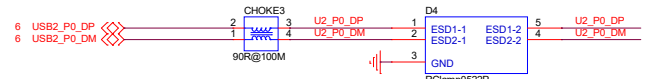
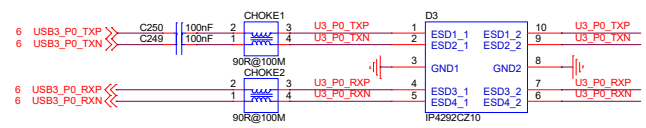
对应手册，C203电容由22nF修改为10nF



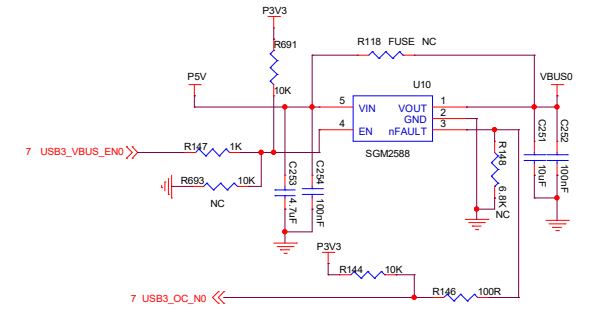
放至最后一个颗粒末端

MiniPCle(4G/5G/AI/LORA)

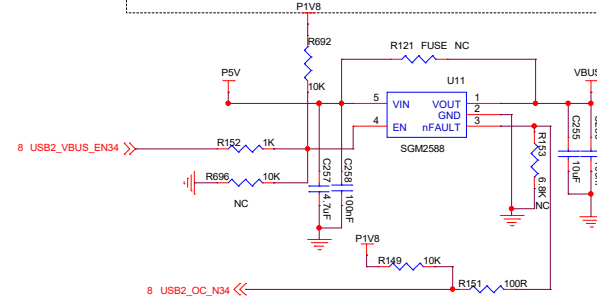




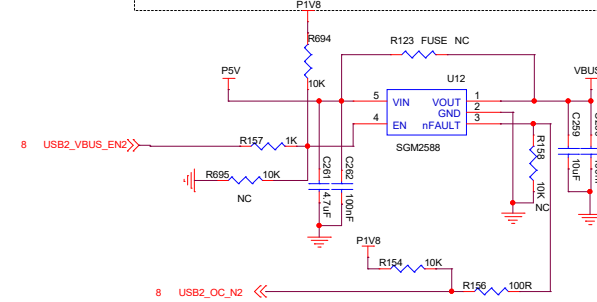
USB3.0和USB2.0做HOST时，VBUS_EN和OC_N可用GPIO代替
 用户如需上电直接使能USB，则上拉使能即可（本设计预留）



用户如需上电直接使能USB，则上拉使能即可（本设计预留）



用户如需上电直接使能USB，则上拉使能即可（本设计预留）



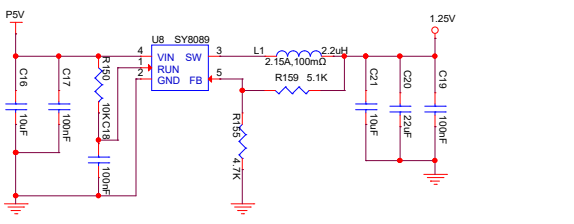
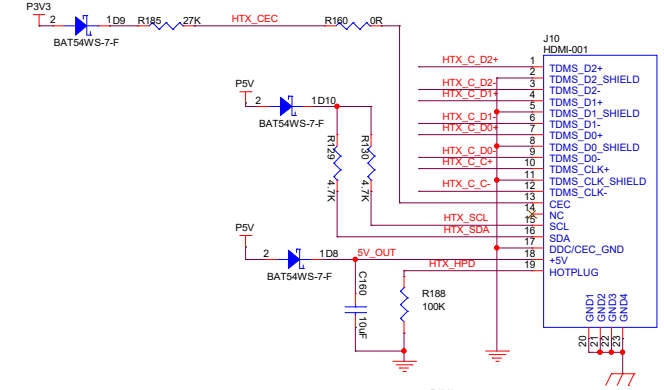
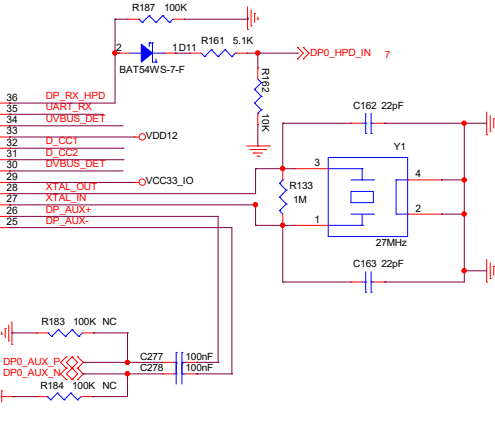
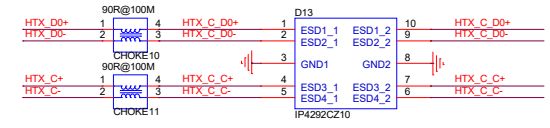
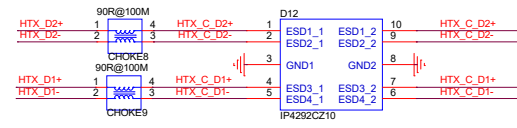
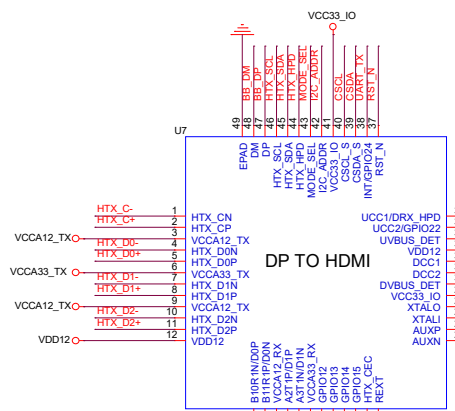
CECport Firefly Workshop

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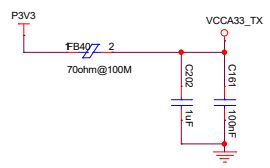
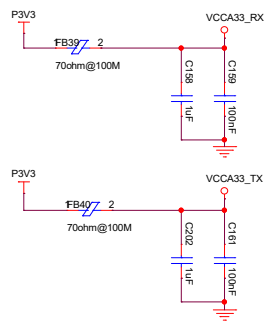
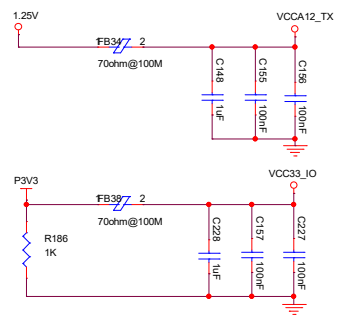
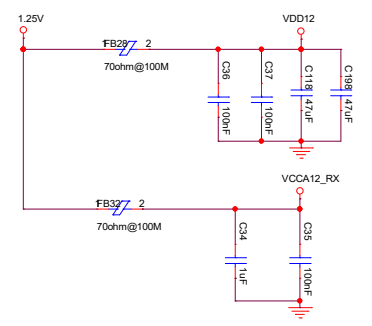
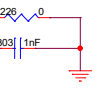
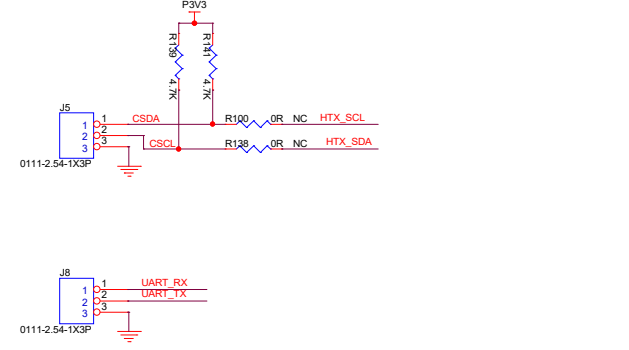
Title: CONN_USB_A

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Default : 0X52;
6.04K+ 5.1K: 0X5E;
11K + 27K : 0X76;
10K Pull up: 0X7E.



- MARK MARK1
- MARK MARK2
- MARK MARK3
- MARK MARK4

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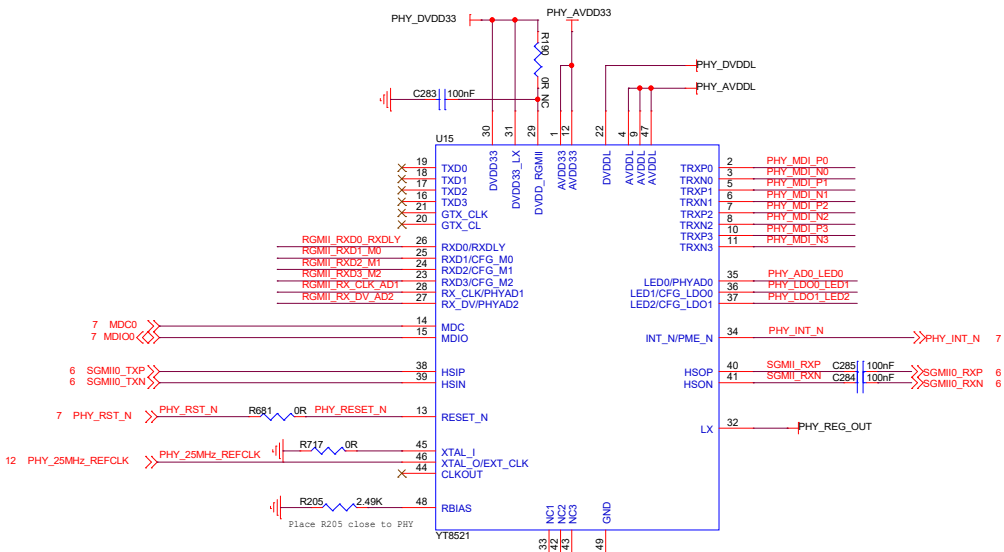
CEK8903-E2KQ

Title: DP to HDMI

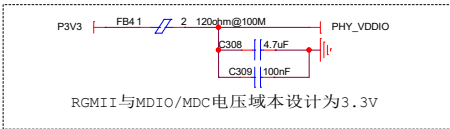
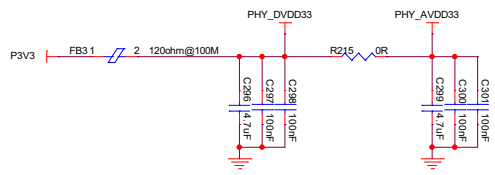
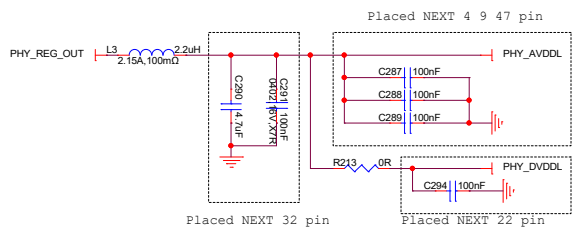
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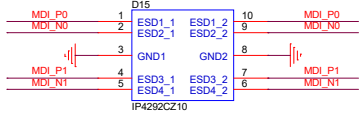
Rev: V1



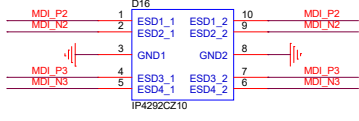
用户可根据实际需求MAC端选择RGMII或者SGMII
本设计使用SGMII



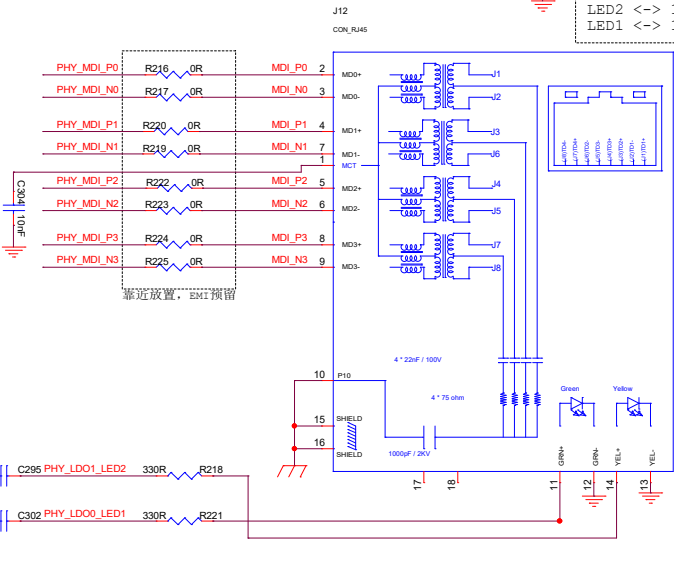
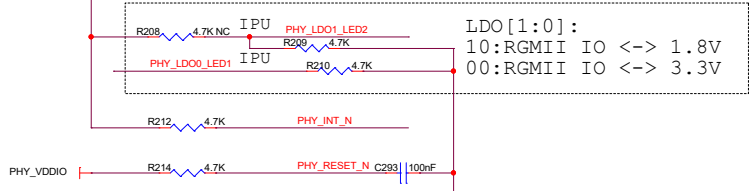
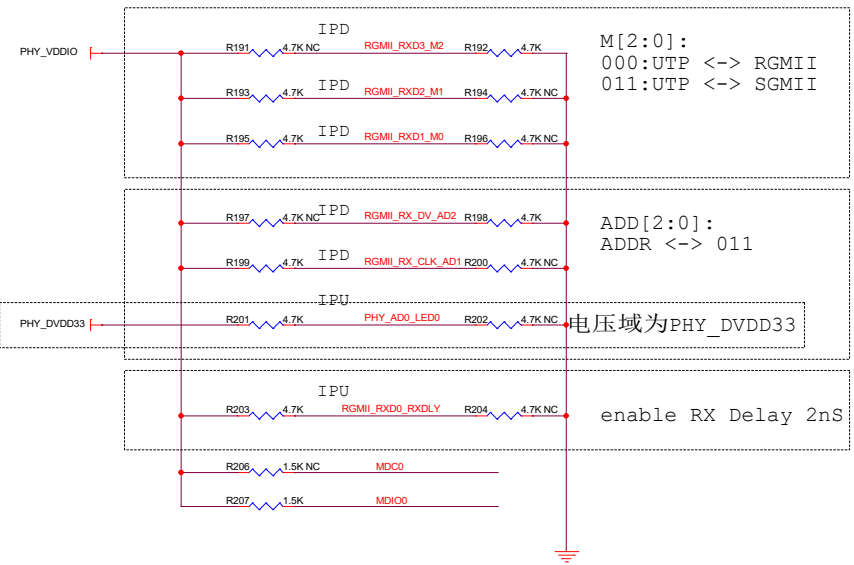
RGMII与MDIO/MDC电压域本设计为3.3V



ESD靠近RJ45放置



ESD靠近RJ45放置



CECport Firefly Workshop

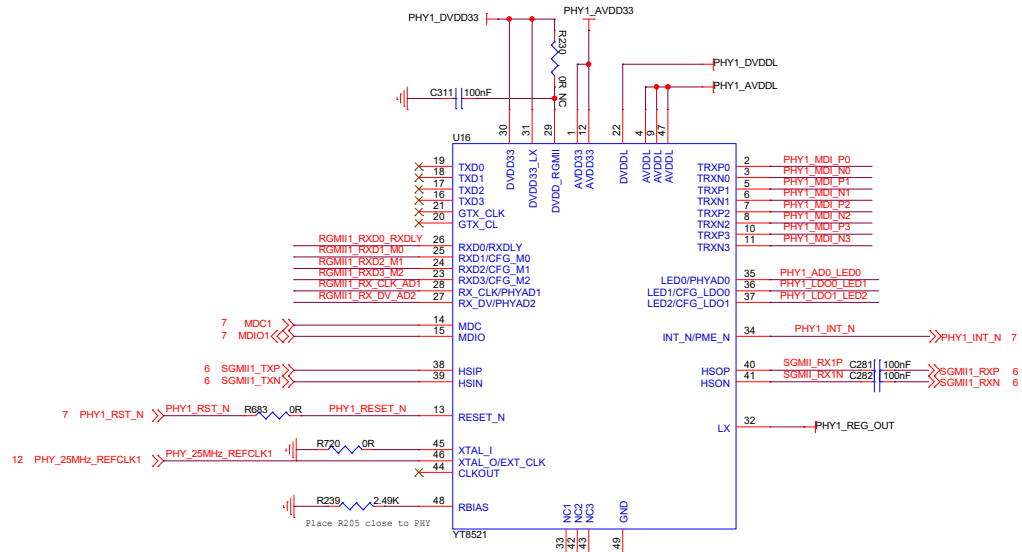
CEK8903-E2KQ

File: SGMII_ETHERNET

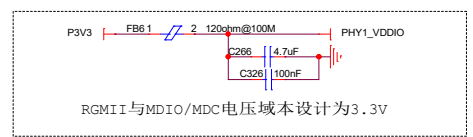
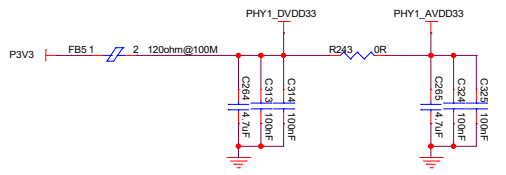
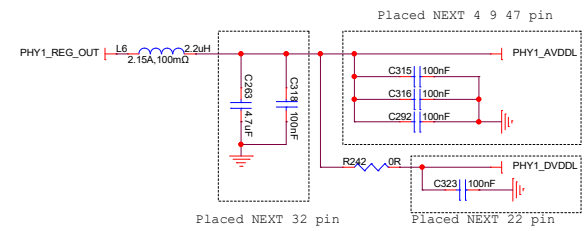
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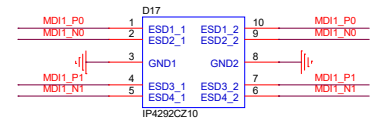
Rev V1



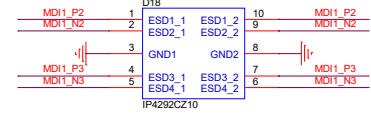
用户可根据实际需求选择RGMII或者SGMII
本设计使用SGMII



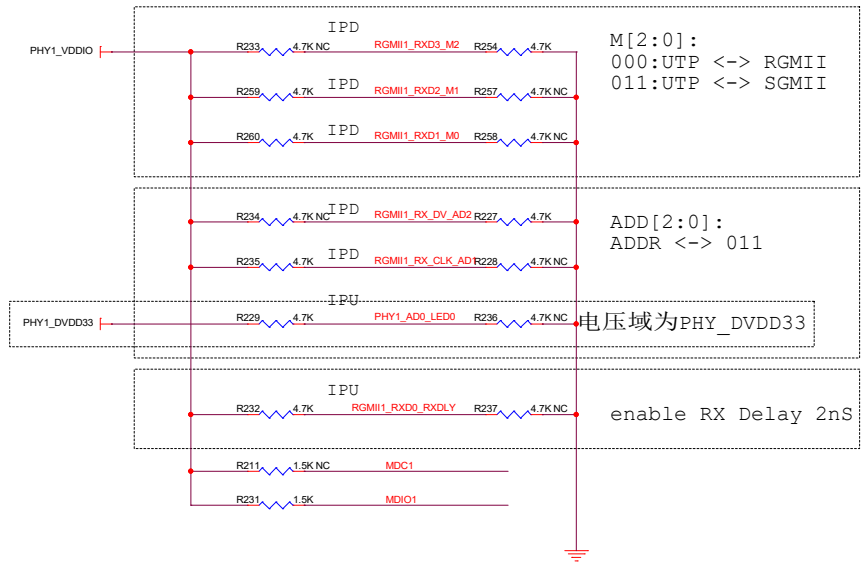
RGMII与MDIO/MDC电压域本设计为3.3V



ESD靠近RJ45放置



ESD靠近RJ45放置

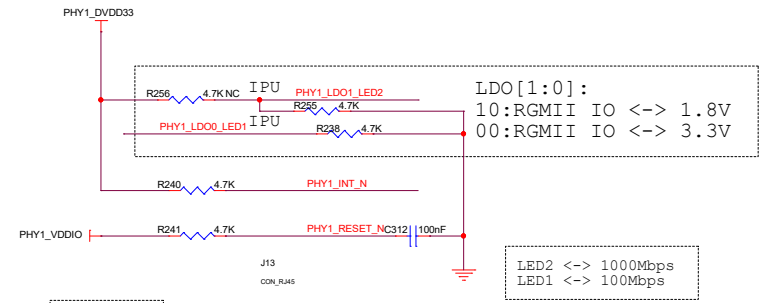


M[2:0]:
000:UTP <-> RGMII
011:UTP <-> SGMII

ADD[2:0]:
ADDR <-> 011

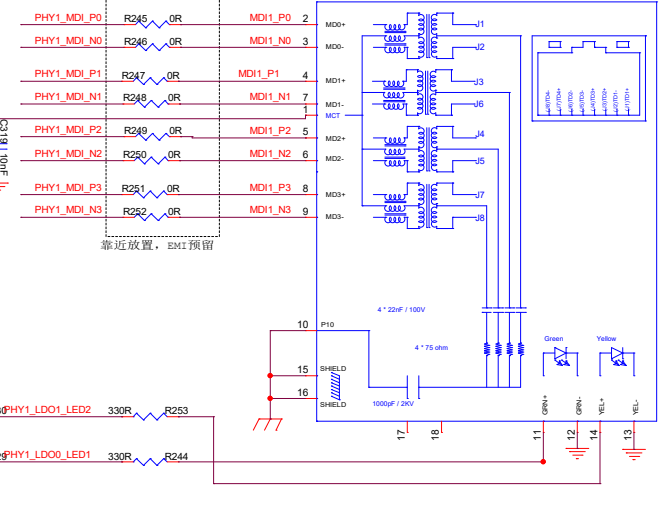
电压域为PHY_DVDD33

enable RX Delay 2nS



LDO[1:0]:
10:RGMII IO <-> 1.8V
00:RGMII IO <-> 3.3V

LED2 <-> 1000Mbps
LED1 <-> 100Mbps



靠近放置，ESD预留

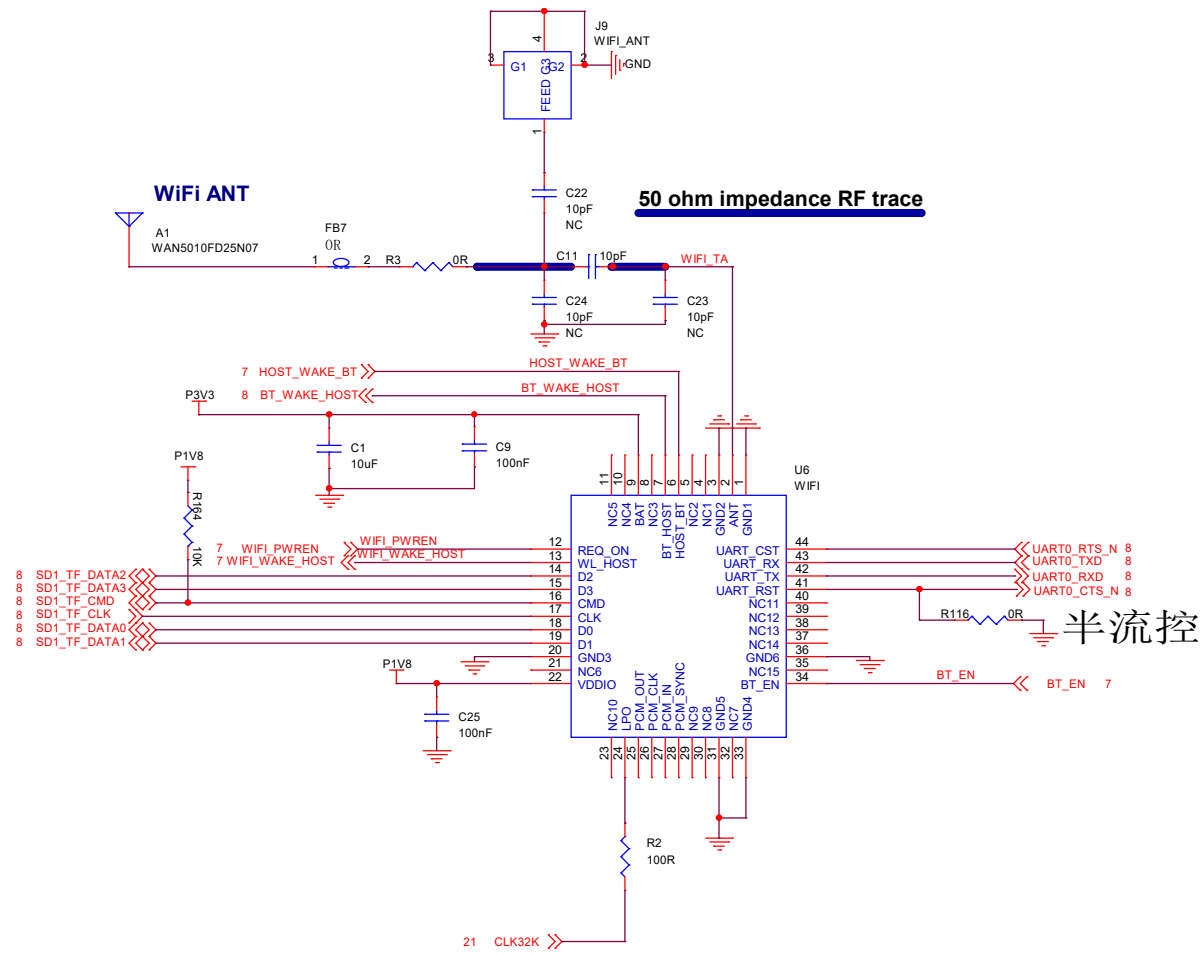
CECport Firefly Workshop

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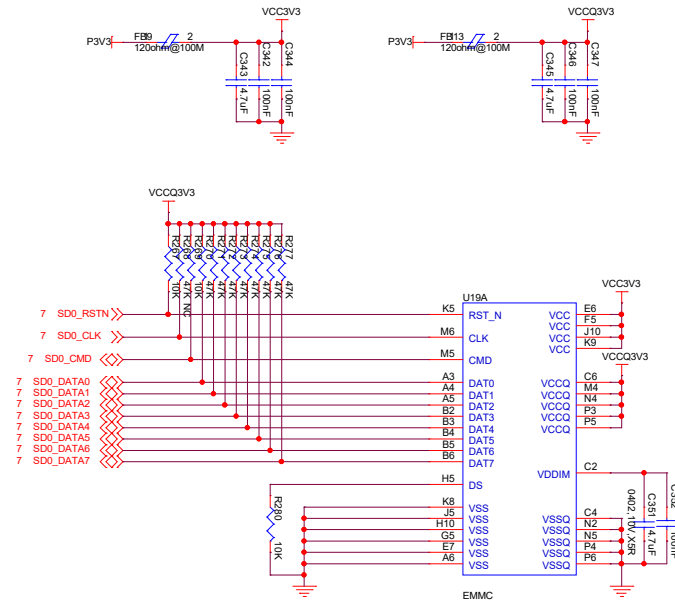
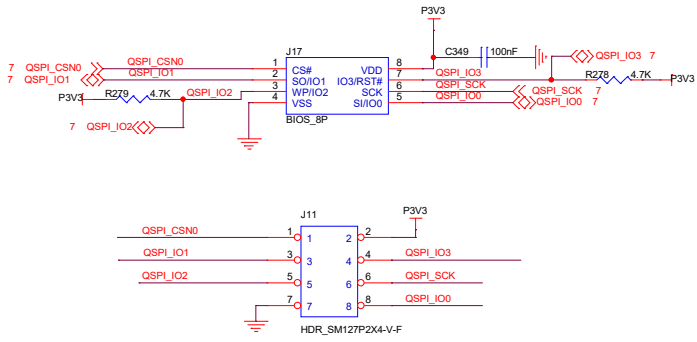
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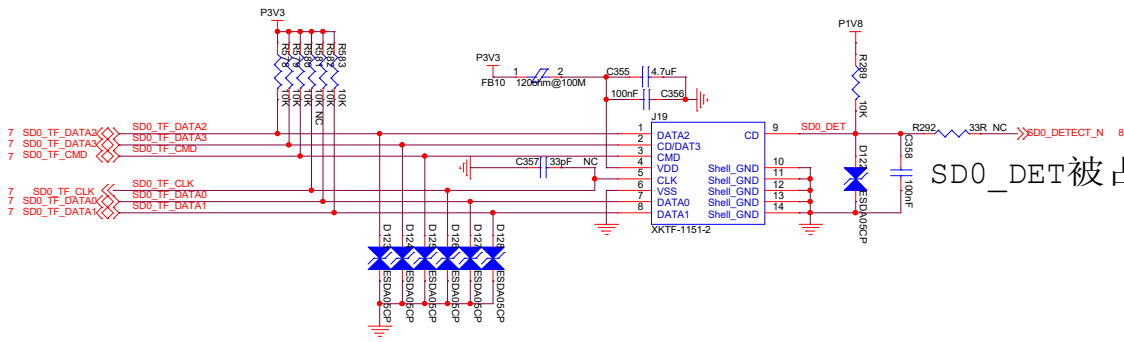


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QSPI BIOS



U19B		
A1	NC49	G1
A2	NC50	G2
A8	NC51	G3
A9	NC52	G12
A10	NC53	G13
A11	NC54	G14
A12	NC55	H1
A13	NC56	H2
A14	NC57	H3
B1	NC58	H12
B7	NC59	H13
B8	NC60	H14
B9	NC61	J1
B10	NC62	J2
B11	NC63	J3
B12	NC64	J12
B13	NC65	J13
B14	NC66	J14
C1	NC67	K1
C5	NC68	K2
C6	NC69	K3
C7	NC70	K12
C8	NC71	K13
C9	NC72	K14
C10	NC73	L1
C11	NC74	L2
C12	NC75	L3
C13	NC76	L12
C14	NC77	L13
D1	NC78	L14
D2	NC79	M1
D3	NC80	M2
D4	NC81	M3
D12	NC82	M7
D13	NC83	M8
D14	NC84	M9
E1	NC85	M10
E2	NC86	M11
E3	NC87	M12
E12	NC88	M13
E13	NC89	M14
E14	NC90	N1
F1	NC91	N3
F2	NC92	N5
F3	NC93	N7
F12	NC94	N8
F13	NC95	N9
F14	NC96	N10
G7	NC97	N11
K7	RFU1	NC98
K8	RFU2	NC99
E5	RFU3	NC100
A7	RFU4	NC101
		P2
		P7
E8	VSF1	NC103
E9	VSF2	NC104
E10	VSF3	NC105
G10	VSF4	NC106
F10	VSF5	NC107
	VSF6	NC108
	VSF7	NC109



SD0_DET被占用，使用GPIO0_4模拟

ESD靠近TF卡槽放置

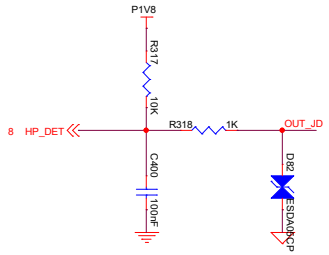
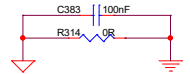
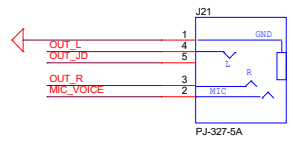
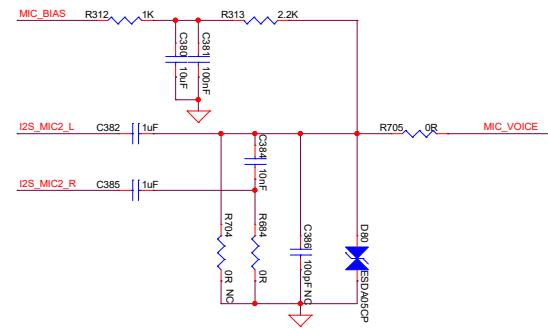
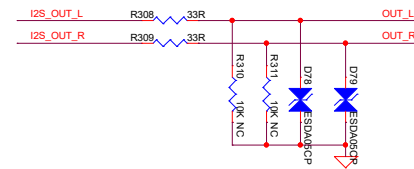
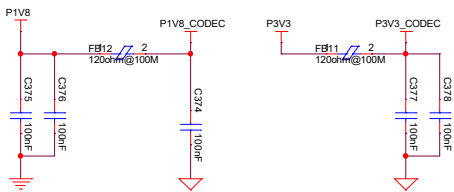
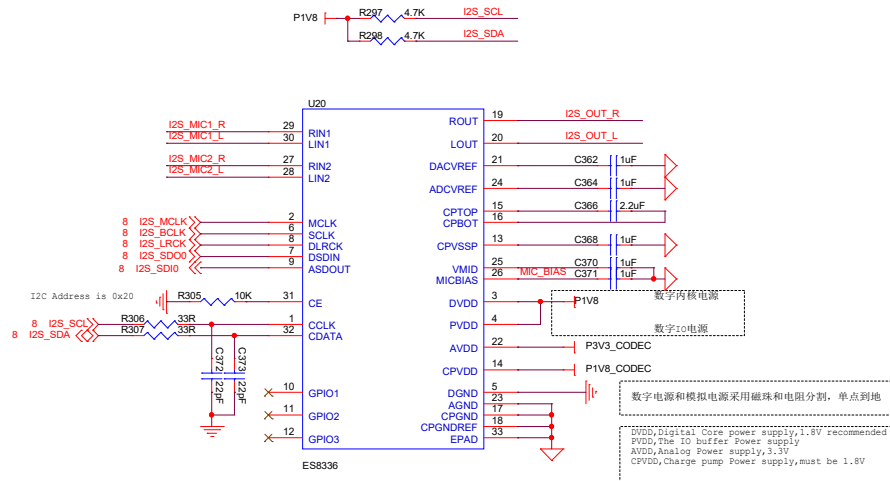
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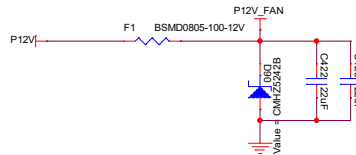
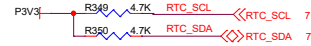
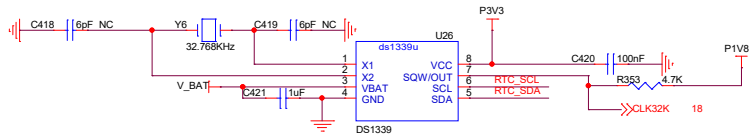
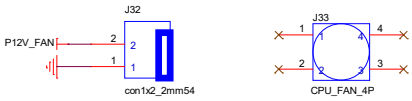
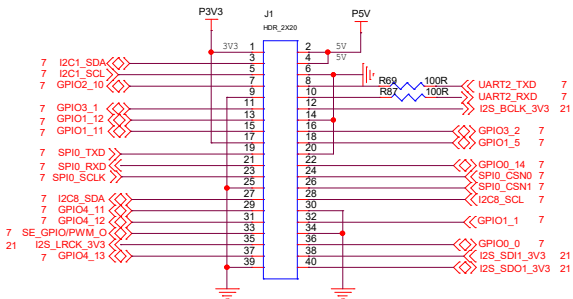
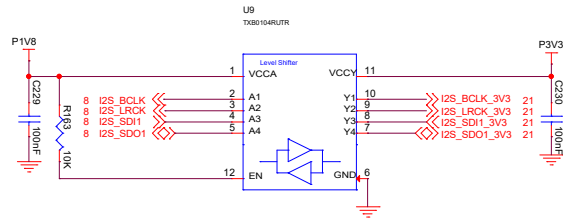
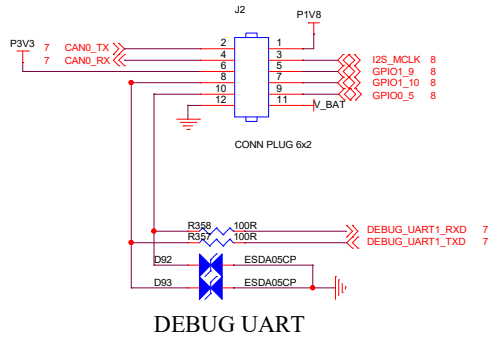
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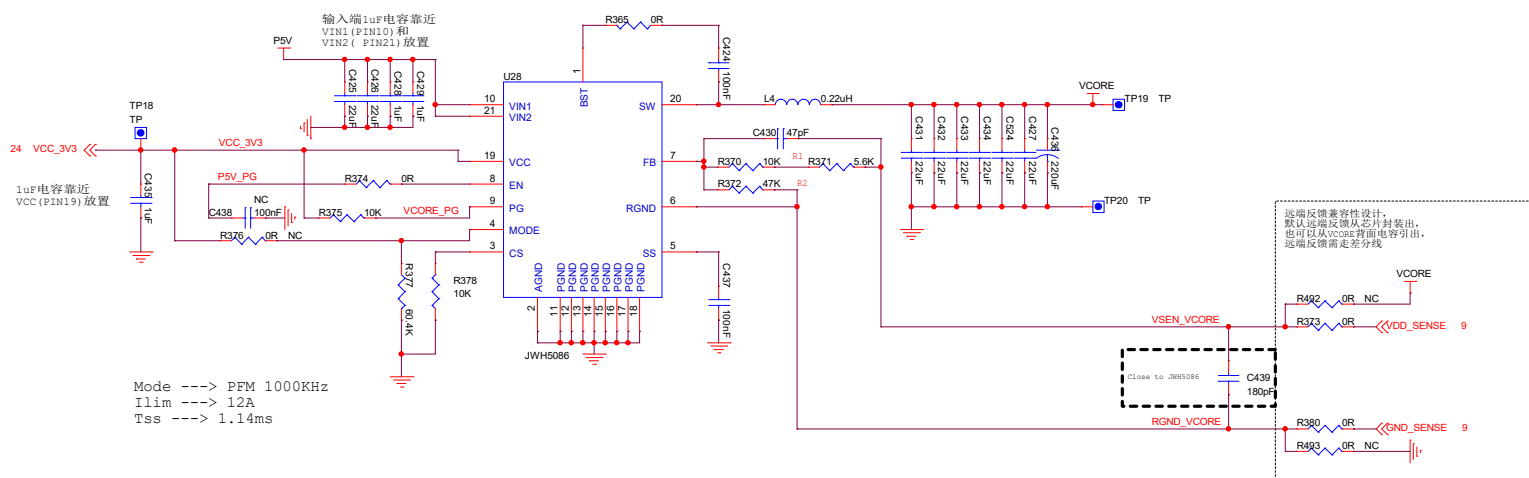


1.8V IO:I2S_MCLK,GPIO0_5 ,GPIO1_9, GPIO1_10



24.25 P5V_PG TP
 24 VCORE_PG TP

Keep VFB = 0.6V
 $V_{out} = 0.6 * (R1+R2) / R2$
 $= 0.6 * (10+5.6+47) / 47 \text{ ---} 0.799V$



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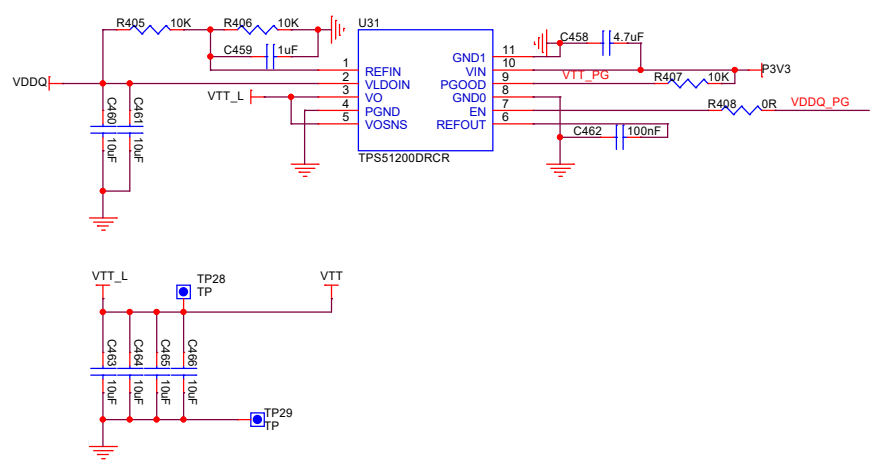
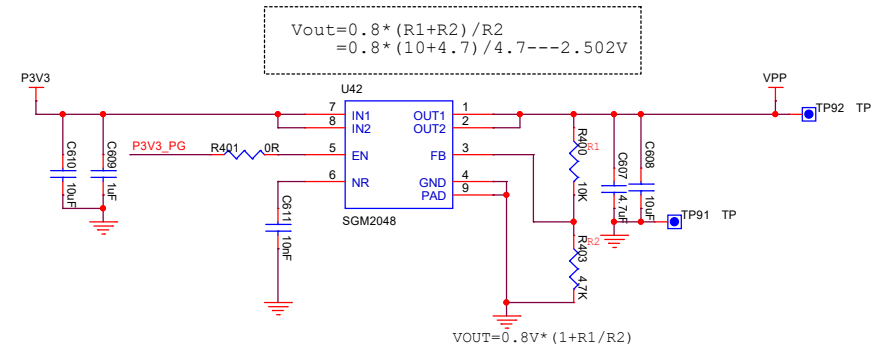
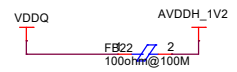
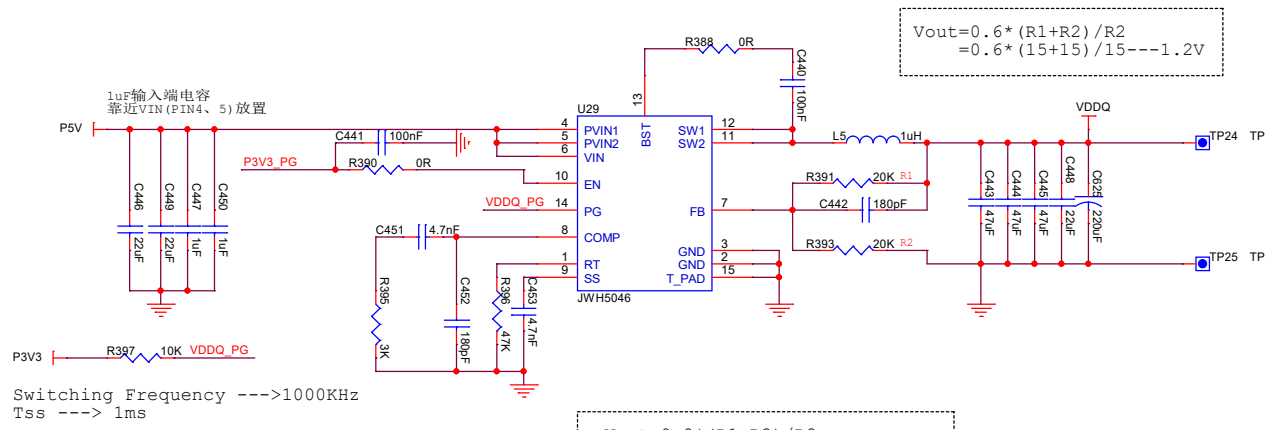
CEK8903-E2KQ

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24 P3V3_PG >> TP21 TP

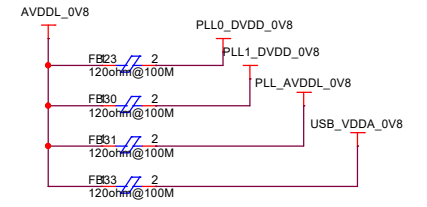
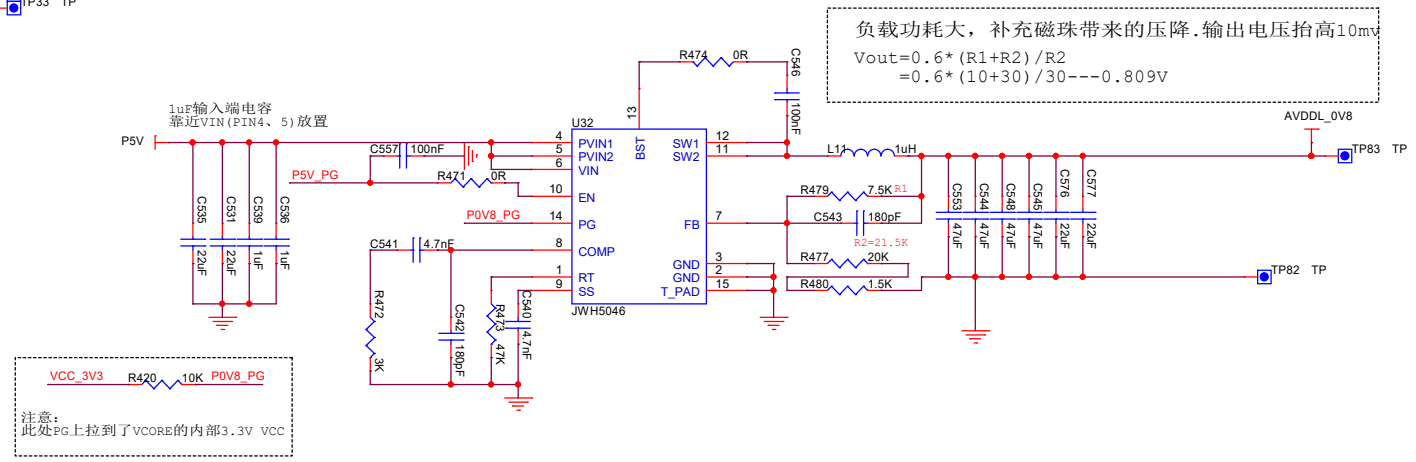


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TP31 TP
TP32 TP
TP33 TP

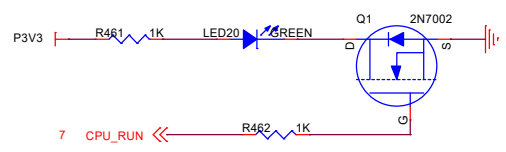
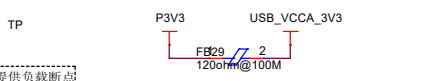
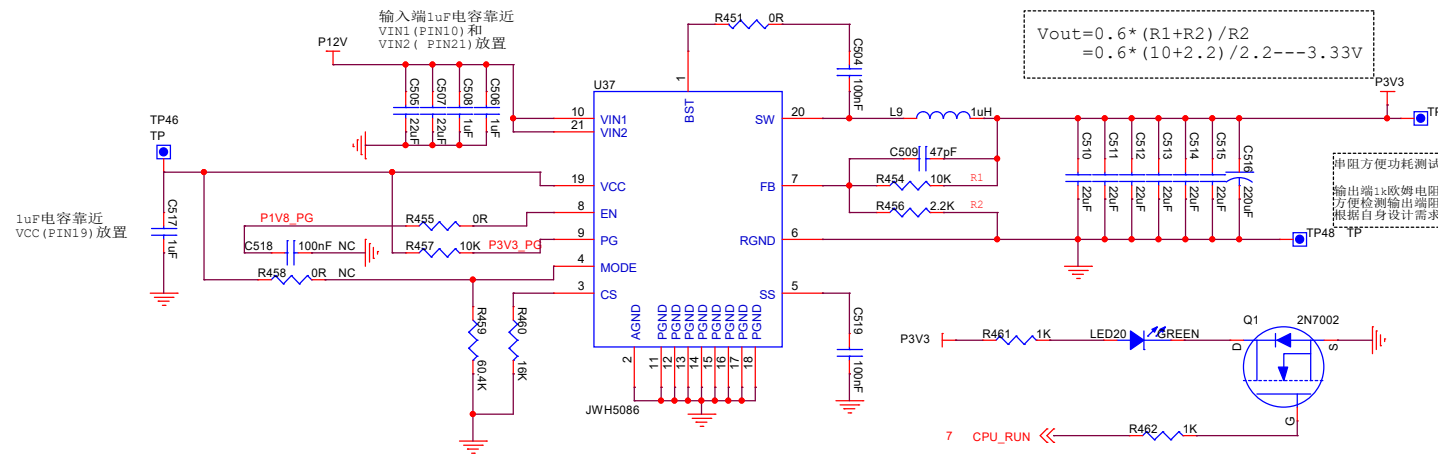
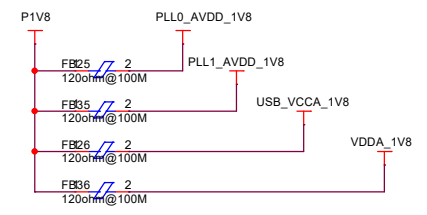
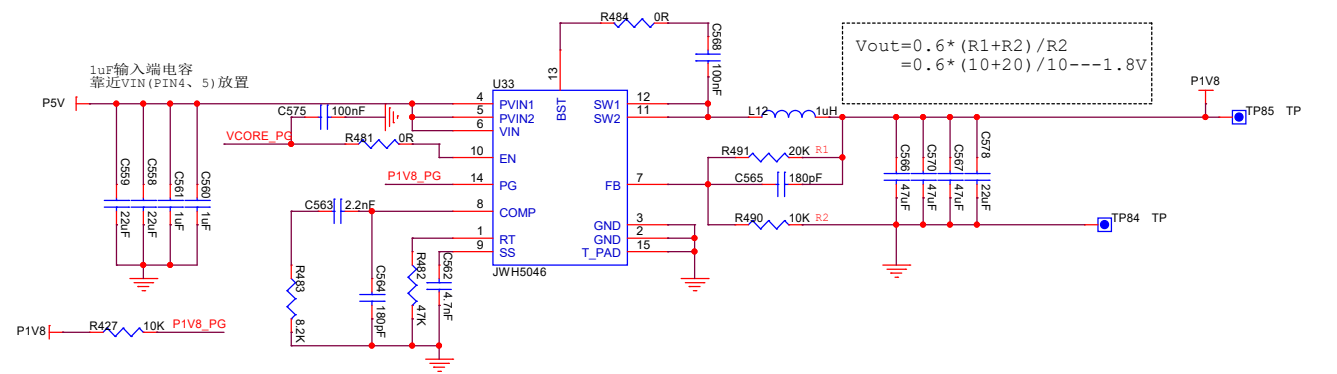
22 VCORE_PG
22.25 P5V_PG

23 P3V3_PG
22 VCC_3V3



VCC_3V3 R420 10K P0V8_PG

注意:
此处PG上拉到了VCORE的内部3.3V VCC



Mode ---> PFM 1000KHz
 Ilim ---> 9.5A
 Tss ---> 1.14ms

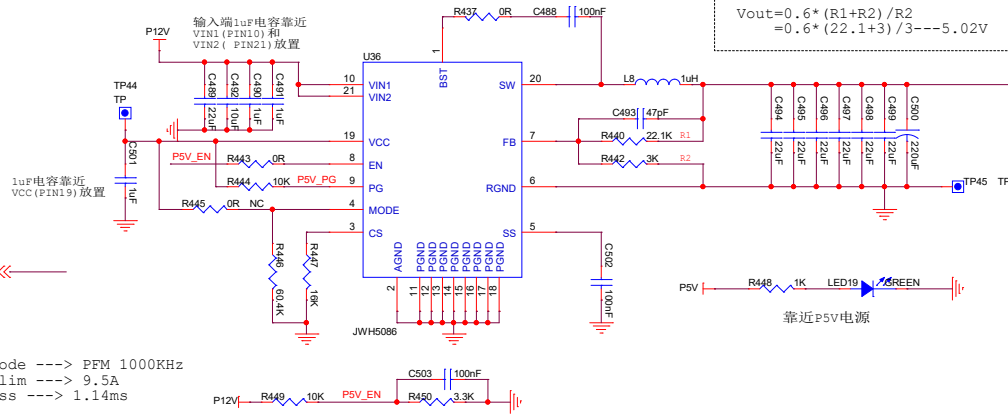
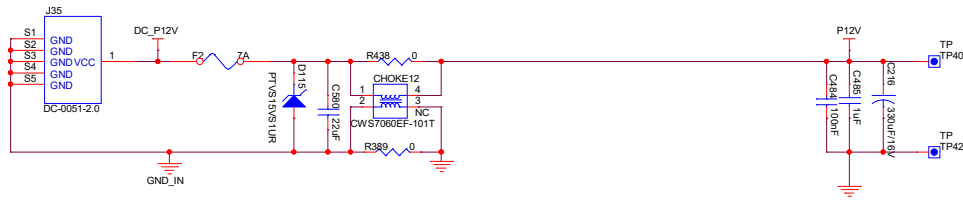
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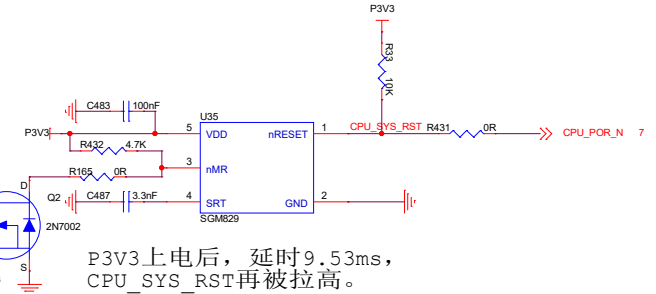
Title: PWR_P0V8&P1V8&P3V3

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$$V_{out} = 0.6 * (R1 + R2) / R2 = 0.6 * (22.1k + 3k) / 3k = 5.02V$$



P3V3上电后，延时9.53ms，CPU_SYS_RST再被拉高。

$$T_D(us) = (2.8 \times 10^6) \times C_{STR}(uF) + 290us$$

本参考设计有复位按钮、上电复位、FPGA复位三种方式接入了CPU的POR_RST：

1. 客户如需使用FPGA做LBC锁存或其它用途，建议使用FPGA控制上电复位，本设计有预留；
2. 无FPGA场景，用户可以选择电源PG信号控制上电时序，使用复位芯片上电复位；
3. 本设计与参考板对应，为满足电源PG信号控制上电时序示例的同时，验证LBC启动功能，使用FPGA复位CPU（FPGA锁存需要优先CPU复位）。

