Features

Document No.: AX88796C/V1.17/12/09/14

- **High-performance non-PCI local bus**
  - Supports 8/16-bit SRAM-like host interface (US Patent Approval), easily interfaced to most common embedded MCUs; or 8/16-bit local CPU interface including MCS-51 series, Renesas series CPUs
  - Supports Slave-DMA to minimize CPU overhead and burst mode read & write access for frame reception & transmission on SRAM-like interface for high performance applications
  - Supports variable voltage I/O (1.8/2.5/3.3V) and programmable driving strength (8/16mA)
  - Interrupt pin with programmable timer
- **High-performance SPI slave interface**
  - Supports SPI slave interface for CPU with SPI master. The SPI slave interface supports SPI timing mode 0 and 3, up to 40MHz of SPI CLK, variable voltage I/O and programmable driving strength
  - Supports optional Ready signal as flow control for SPI packet RX/TX
- **Single-chip Fast Ethernet MAC/PHY controller**
  - Embeds 14KB SRAM for packet buffers
  - Supports IPv4/IPv6 packet Checksum Offload Engine to reduce CPU loading, including IPv4 IP/TCP/UDP/ICMP/IGMP & IPv6 TCP/UDP/ICMPv6 checksum generation & check
  - Supports VLAN match filter
  - Integrates IEEE 802.3/802.3u standards compatible 10BASE-T/100BASE-TX (twisted pair copper mode) Fast Ethernet MAC/PHY transceiver in one single-chip
  - Supports twisted pair crossover detection and correction (HP Auto-MDIX)
  - Supports full duplex operation with IEEE 802.3x flow control and half duplex operation with back-pressure flow control
  - Supports auto-polling function
  - Supports 10/100Mbps N-way Auto-negotiation operation
- **Advanced Power Management features**
  - Supports dynamic power management to reduce power dissipation during idle or light traffic period
  - Supports very low power Wake-On-LAN (WOL) mode when the system enters sleep mode and waits for network event to awake it up. The wakeup events supported are network link state change, receipt of a Magic Packet or a pre-programmed Microsoft Wakeup Frame or through GPIO pin
  - Supports Protocol Offload (ARP & NS) for Windows 7 Networking Power Management
  - Supports complete I/O pins isolation during WOL mode or Remote Wakeup Ready mode to reduce leakage current on non-PCI and SPI slave host interface
- Supports optional EEPROM interface to store MAC address
- Supports up to four GPIOs and two of them support Wake-On-LAN
- Supports programmable LED pins for various network activity indications with variable voltage I/O and programmable driving strength
- Integrates voltage regulator, 25MHz crystal oscillator and power on reset circuit on chip
- Supports optional clock output (25, 50 or 100MHz) for system use, if 25MHz crystal is present
- Supports optional clock input (25MHz) from system clock to save the 25MHz crystal cost
- 64-pin LQFP RoHS compliant package
- Operates over 0 to +70°C or -40 to +85°C temperature range

ASIX ELECTRONICS CORPORATION
4F, NO.8, Hsin Ann Rd., Hsinchu Science Park, Hsin-Chu City, Taiwan, R.O.C. 300
TEL: 886-3-579-9500 **FAX: 886-3-579-9558** **http://www.asix.com.tw**

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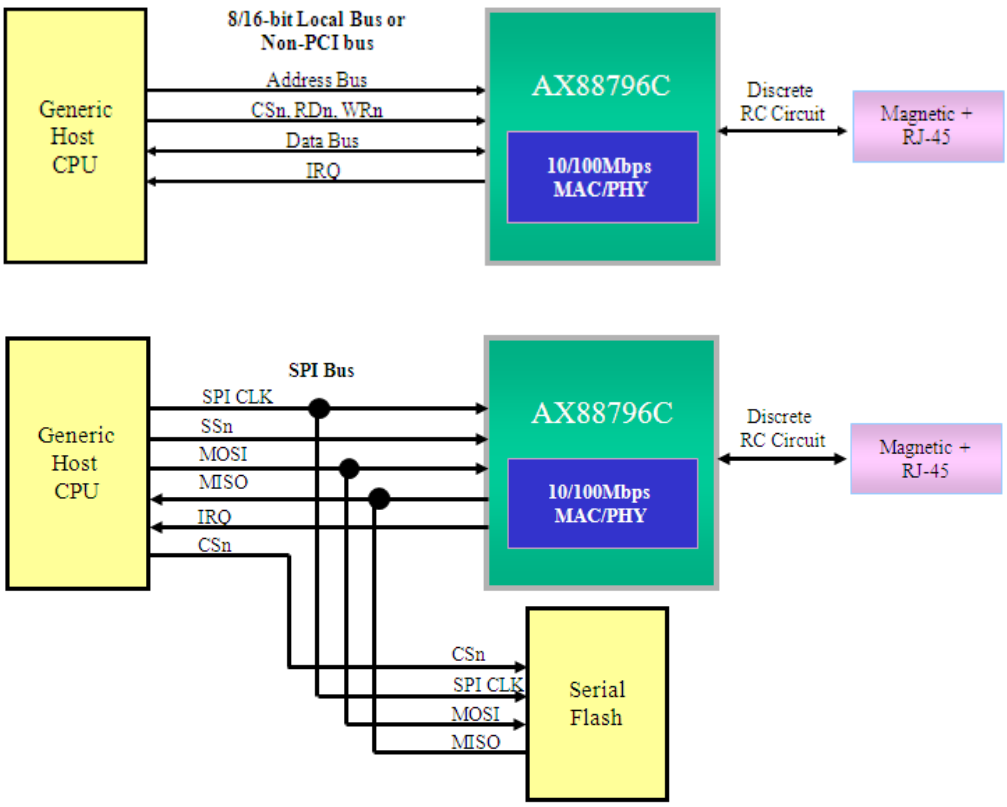
Target Applications

- Netbook
- Industrial Computer
- Cable, Satellite and IP STB
- IPTV, Digital Media Adapter
- Network DVD, DVR-R, HDD
- IP/Video Phone, VoIP ATA
- Internet Radio
- POS Terminal, Kiosk
- Multi Functional Printer
- RFID Reader
- Time Attendance
- RS232/422/485 to Ethernet
- Building / Home Automation
  - HVAC Control
  - Networked Home Appliance
- Security System
  - Biometric Access Control
  - Fingerprint Reader
  - Network Camera
  - Remote Surveillance
  - Professional DVR
  - Fire and Safety
- Industrial Control
  - Remote Data Collection Equipment
  - Remote Monitor
  - Remote Control and Management
  - Environment Monitoring or Network Sensor
  - Automatic Meter Reading
  - Networked UPS
  - Lighting Control

System Block Diagram



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1.0 Introduction

1.1 General Description

The AX88796C is a SPI or non-PCI Ethernet controller with low power, low-pin-count and variable voltage I/O for the Embedded and Industrial Ethernet applications. The AX88796C supports 8/16-bit SRAM-like or Address-Data Multiplex host interface with variable voltage I/O, providing a glue-less connection to common or high-end MCUs. The AX88796C also provides an alternative SPI slave interface for MCUs with SPI master for simplifying host interface connection. The AX88796C integrates on-chip Fast Ethernet MAC and PHY, which is IEEE 802.3/802.3u 10BASE-T/100BASE-TX compatible, and 14KB embedded SRAM for packet buffering to accommodate high bandwidth applications. The AX88796C offers a wide array of features including support for advanced power management, high performance data transfer on host interface, IPv4/IPv6 checksum offload engine, HP Auto-MDIX, and IEEE 802.3x and back-pressure flow control. The AX88796C supports two operating temperature ranges, namely, commercial grade from 0 to 70 °C and industrial grade from –40 to 85 °C. The small form factor of 64-pin LQFP package helps reduce the overall PCB space. The programming of AX88796C is simple, so the users can easily port the software drivers to many embedded systems very quickly.

1.2 Block Diagram

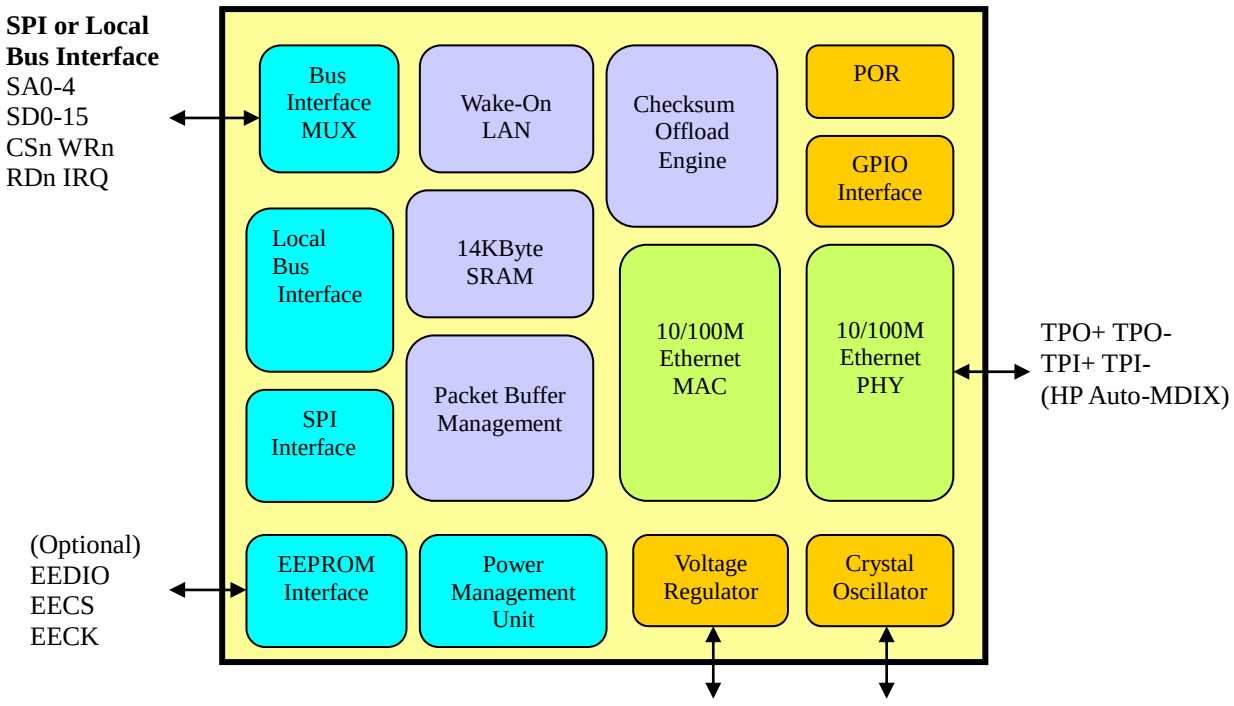


Fig 1 AX88796C BLOCK DIAGRAM

1.3 Pin Connection Diagram

The AX88796C is housed in the 64-pin plastic light quad flat pack.
Note: N/C means No Connect.

1.3.1 8/16-Bit SRAM-like or Renesas SHx Series CPU Bus Mode

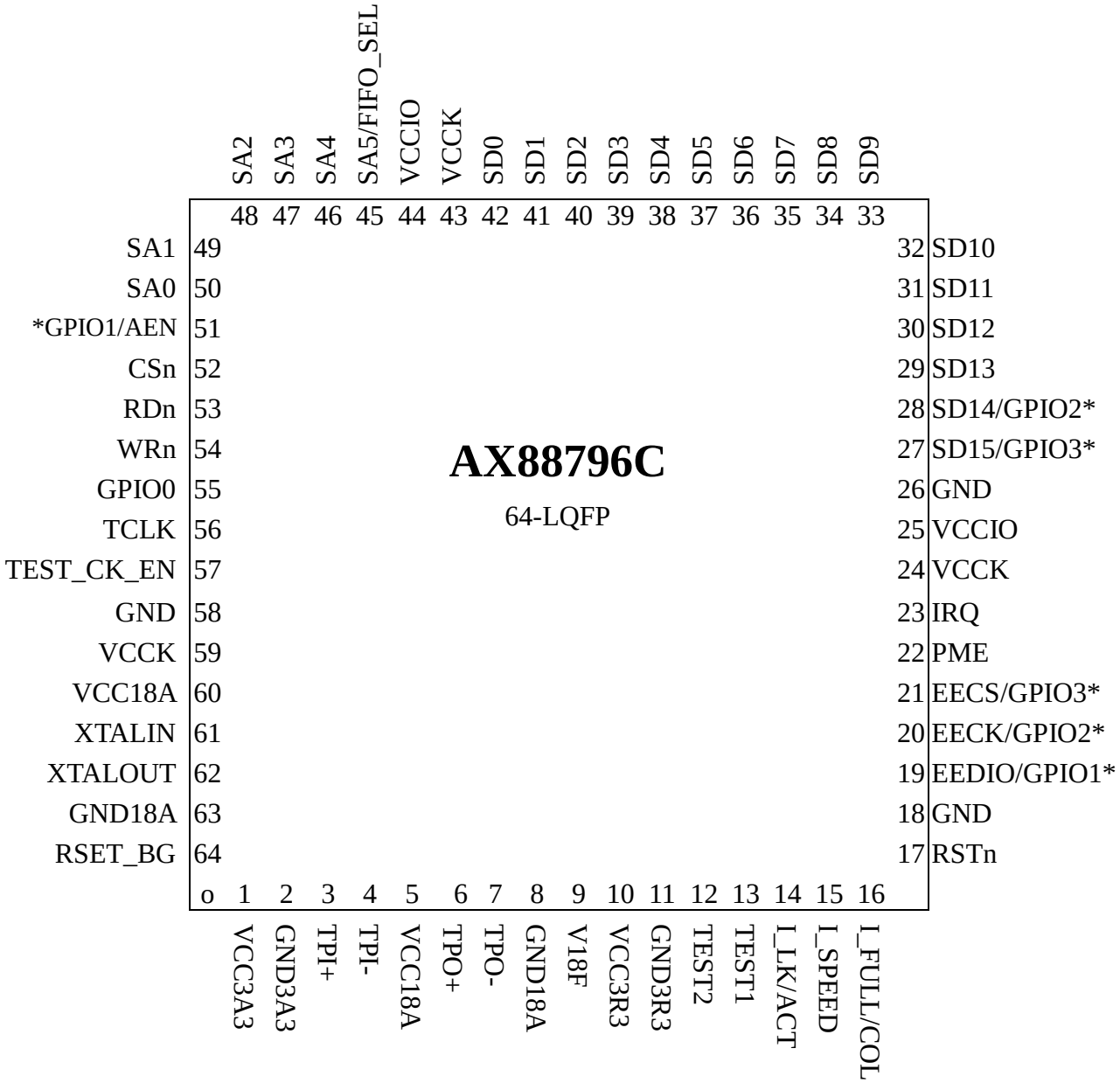


Fig 2 8/16-BIT SRAM-LIKE/RENESAS MODE PIN OUT DIAGRAM

* NOTE: The GPIO1, GPIO2 and GPIO3 can only be enabled when EEPROM is not exist or data bus is not in used or regular pin function is disconnected. Please reference GPIOWCR[10:8] register information to carefully turn on and mux out the GPIO pin when normal pin is not connected.

1.3.2 8/16-Bit Address-Data Multiplex or MCS-51 Bus Mode

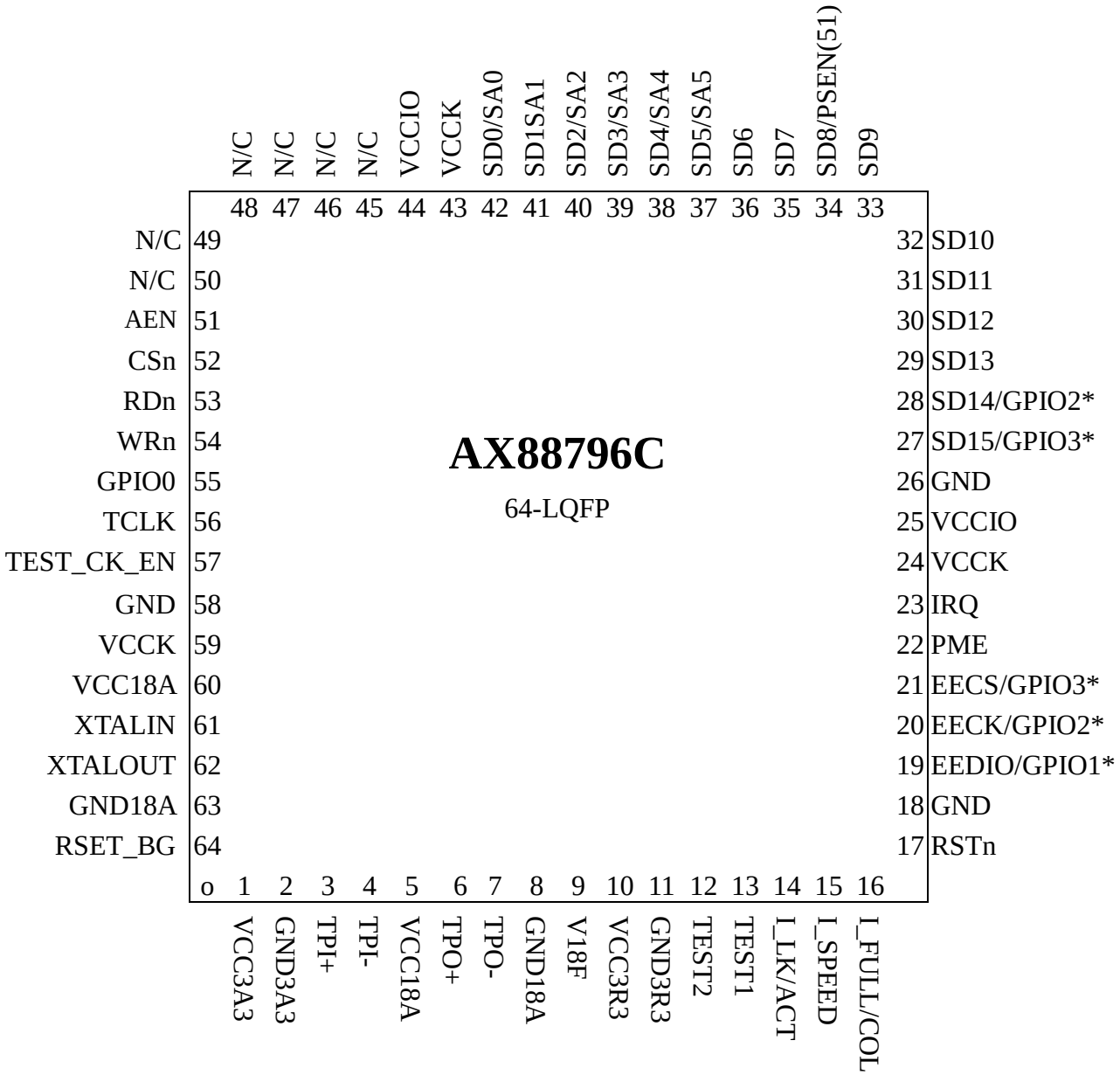


Fig 3 8/16-BIT ADDRESS-DATA MULTIPLEX/MCS-51 MODE PIN OUT DIAGRAM

* NOTE: The GPIO1, GPIO2 and GPIO3 can only be enabled when EEPROM is not exist or data bus is not in used or regular pin function is disconnected. Please reference GPIOWCR[10:8] register information to carefully turn on and mux out the GPIO pin when normal pin is not connected.

1.3.3 SPI Bus Mode

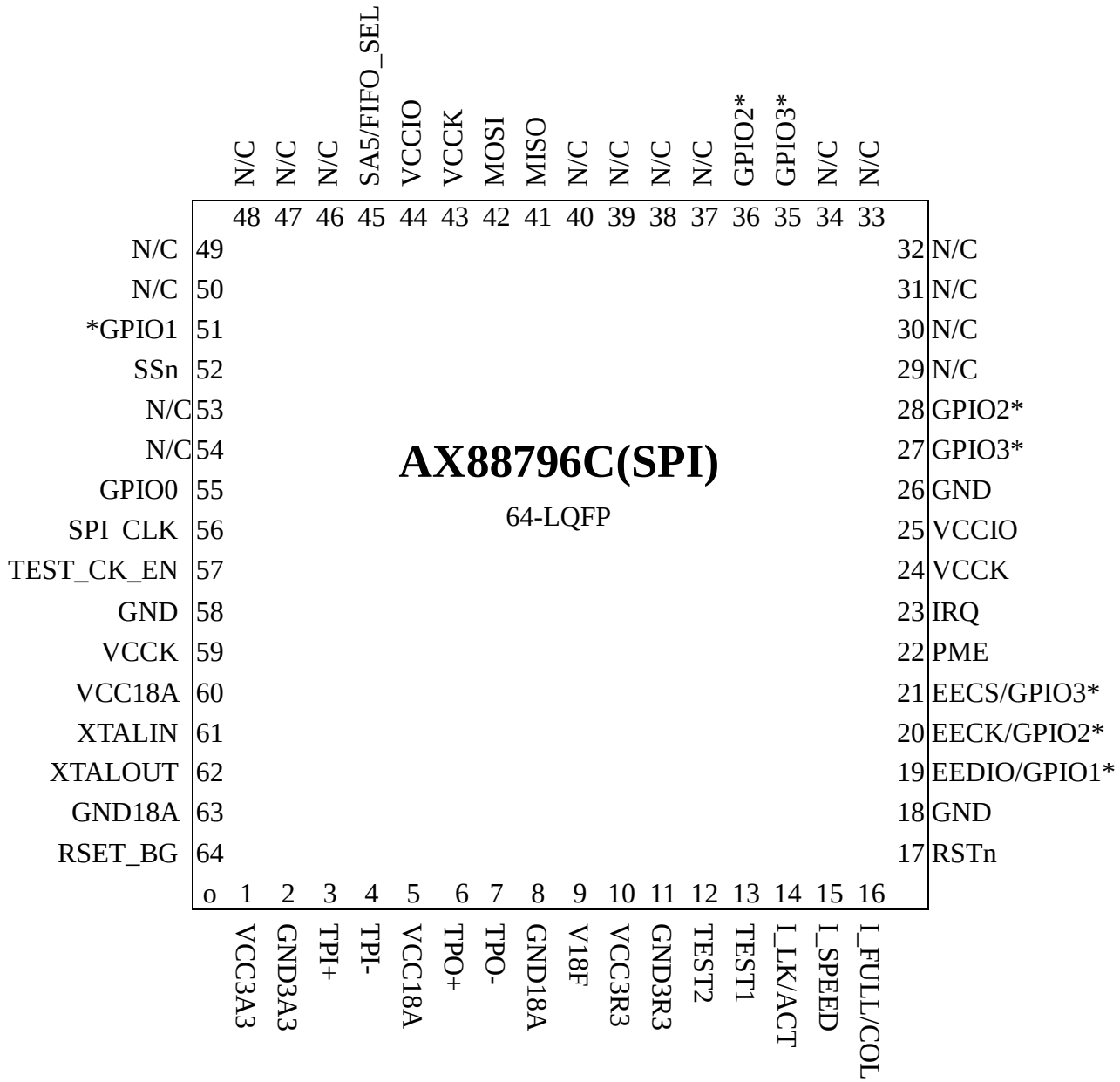


Fig 4 SPI MODE PIN OUT DIAGRAM

* NOTE: The GPIO1, GPIO2 and GPIO3 can only be enabled when EEPROM is not exist or data bus is not in used or regular pin function is disconnected. Please reference GPIOWCR[10:8] register information to carefully turn on and mux out the GPIO pin when normal pin is not connected.

1.4 Bus Interface Configuration Table and Application

The AX88796C supports total seven different types of bus interfaces include 8/16 Bit SRAM-like bus interface, 8/16-Bit Address-Data Multiplex interface, Renesas CPU series bus interface, MCS-51 and SPI bus interface. The AX88796C can be configured to the specific bus type automatically by pull-up and pull-down the EECS/EECK/I_FULL pins. Assume the external crystal is used. Please pull-down the TEST2, TEST1, and TEST_CK_EN three pins to ground.

I_FULL	EECS	EECK	Bus Type
PD	PD	PD	8-bit SRAM-like bus
PD	PD	PU	8-bit Address/Data multiplexed bus
PD	PU	PD	Reserved
PD	PU	PU	MCS-51 (805x)
PU	PD	PD	16-bit SRAM-like bus
PU	PD	PU	16-bit Address/Data multiplexed bus
PU	PU	PD	SPI Mode
PU	PU	PU	16-bit local bus with byte write enable (Renesas SHx CPU bus style)

TAB - 1 THE AX88796C BUS INTERFACE CONFIGURATION TABLE

1.4.1 8-Bit SRAM-like Bus Interface

An example, the AX88796C's bus setting to 8-bit SRAM-like bus mode. Three external pull-down resistors are connected to pin I_FULL, pin EECS and pin EECK. Please reference TAB-1 for the AX88796C bus type setting and pull down the unused SD[15:8] pins via 47K resistors. The pin SA5 suggest connect to the address higher than 2K address space and make sure SA0 is toggling when burst mode access data in and out of buffer memory. Note: A12 is just a reference minimal address pin to tie to SA5.

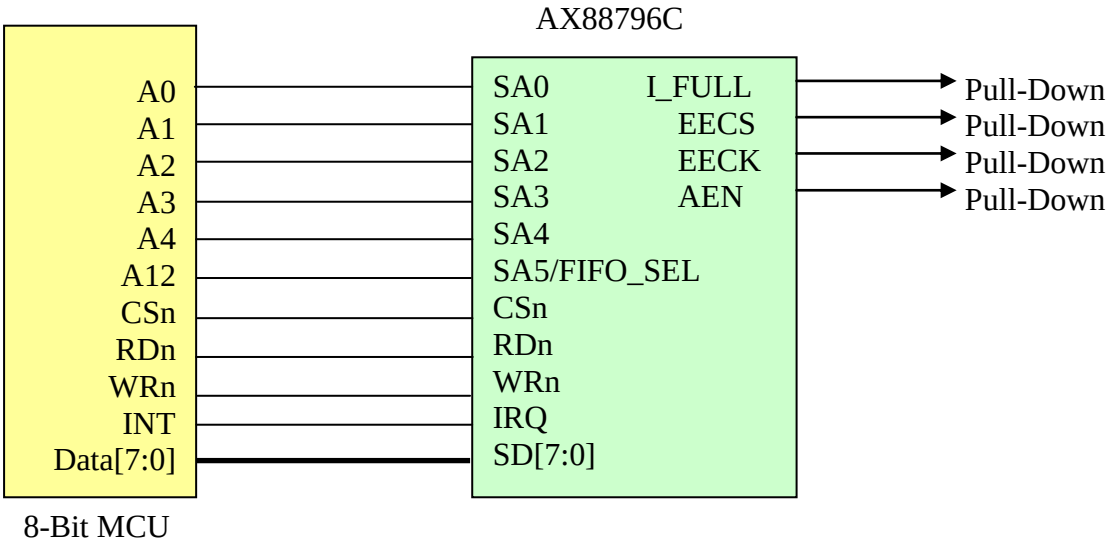


Fig 5 8-BIT SRAM-LIKE BUS APPLICATION DIAGRAM

1.4.2 16-Bit SRAM-like Bus Interface

An example, the AX88796C's bus setting to 16-bit SRAM-like bus mode. Please reference TAB-1 for the AX88796C bus type setting. The pin SA5 suggest connect to the address higher than 2K address space and make sure SA0 is toggling when burst mode access data in and out of buffer memory. Note: A12 is just a reference minimal address pin to tie to SA5.

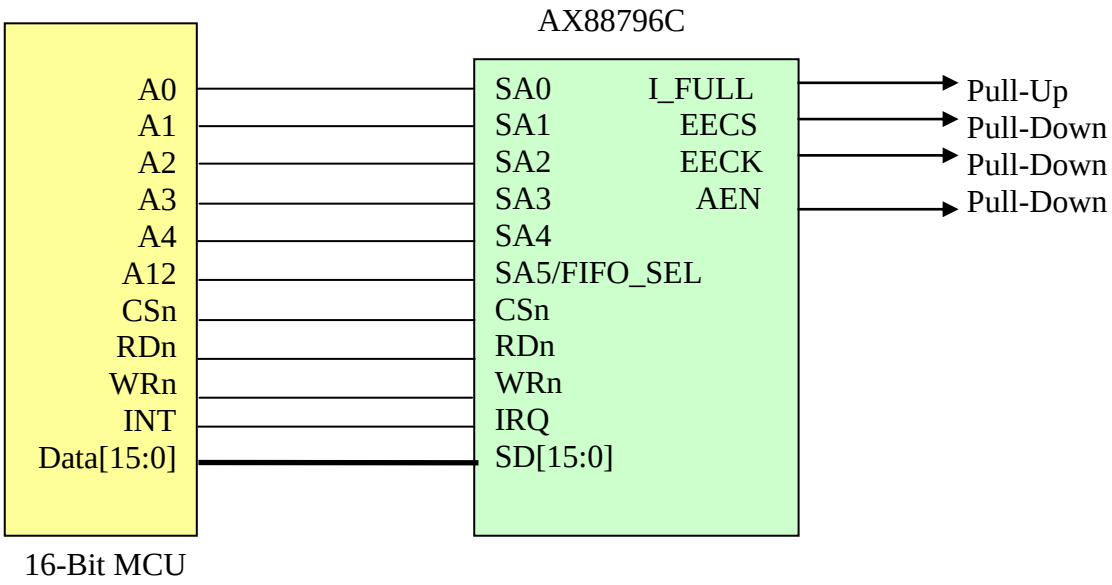


Fig 6 16-BIT SRAM-LIKE BUS APPLICATION DIAGRAM

1.4.3 MCS-51 Bus Interface

An example, the AX88796C's bus setting as MCS-51 mode. Two external pull-up resistors are connected to pin EECS and pin EECK. One pull down resistor is connected to the I_FULL pin. Please reference TAB-1 for the AX88796C bus type setting.

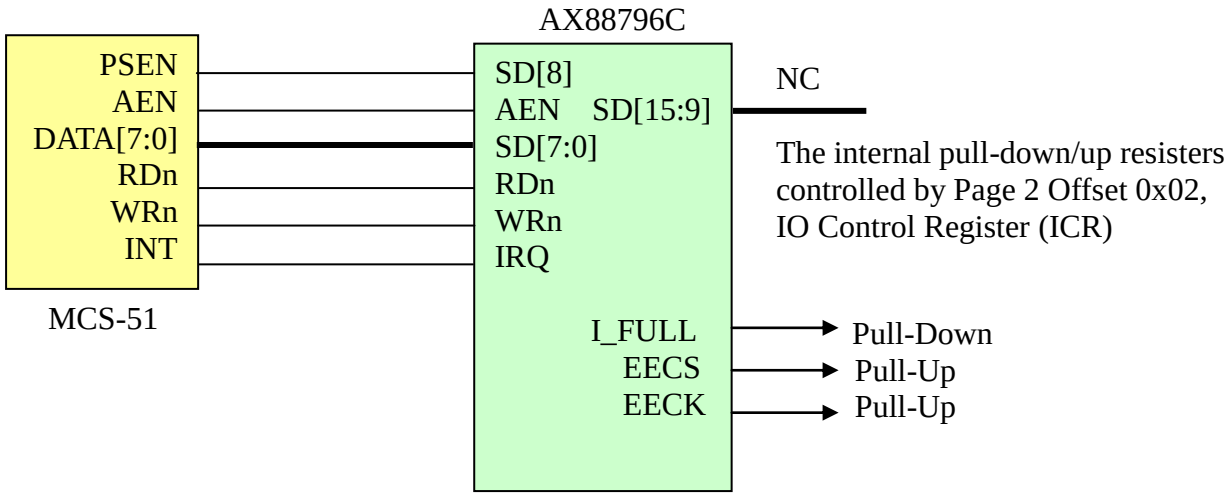


Fig 7 MCS-51 BUS APPLICATION DIAGRAM

1.4.4 8-Bit Address-Data Multiplex Bus Interface

The AX88796C's bus interface can set to 8-bit Address-Data multiplex bus mode. Please reference TAB-1 for the AX88796C bus type setting and pull down the unused SD[15:8] pins via 47K resistors.

The AX88796C 8-bit Address-Data multiplex bus mode only supports single read and single write data access mode.

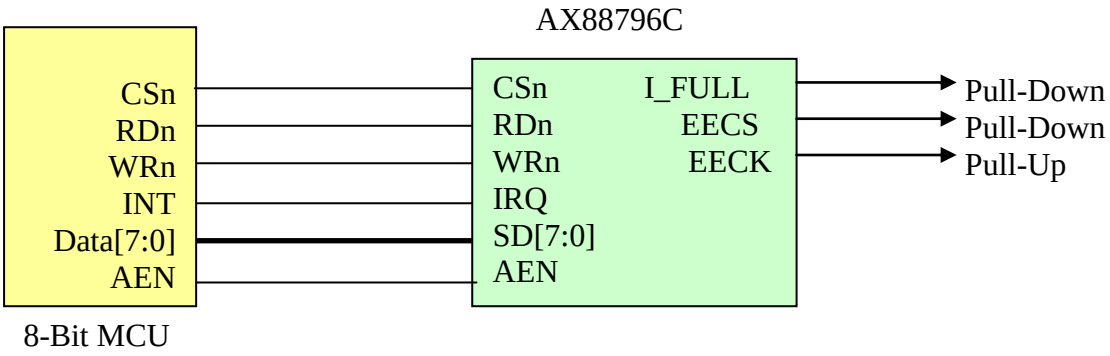


Fig 8 8-BIT ADDRESS-DATA MULTIPLEX BUS APPLICATION DIAGRAM

1.4.5 16-Bit Address-Data Multiplex Bus Interface

The AX88796C's bus interface can set to 16-bit Address-Data multiplex bus mode. Please reference TAB-1 for the AX88796C bus type setting.

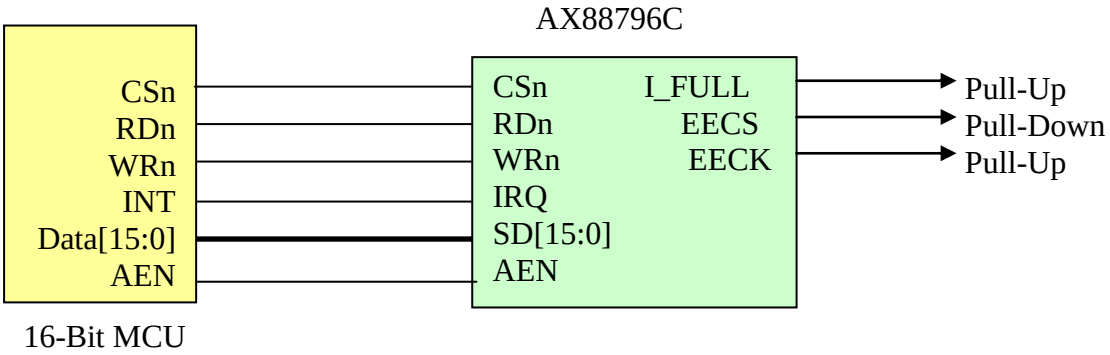


Fig 9 16-BIT ADDRESS-DATA MULTIPLEX BUS APPLICATION DIAGRAM

1.4.6 Renesas SHx series CPU Bus Interface

The AX88796C supports Renesas SHx series CPU bus interface. Please reference TAB-1 for bus type setting.

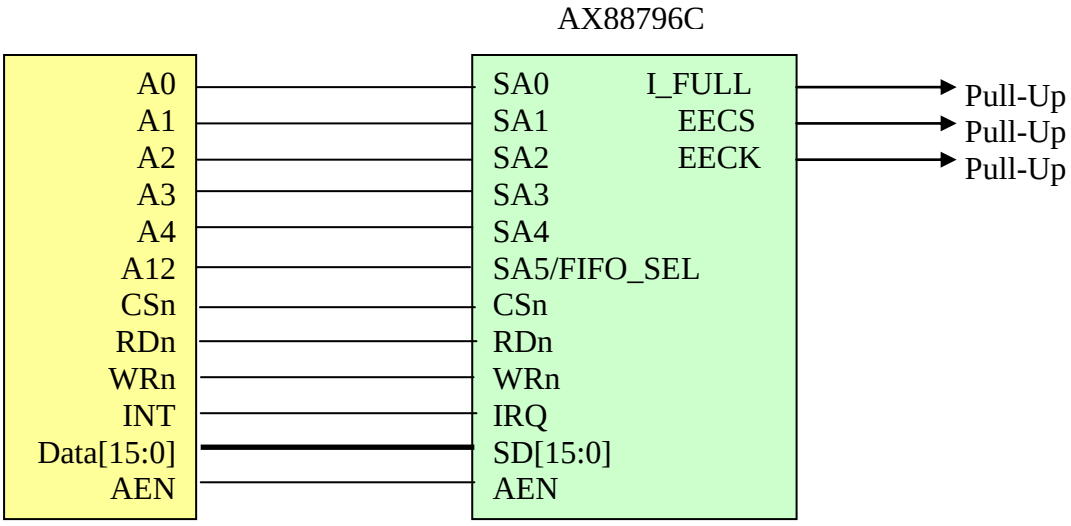


Fig 10 RENESAS SHX SERIES CPU BUS APPLICATION DIAGRAM

1.4.7 SPI Mode Bus Interface

The AX88796C supports single SPI mode and please reference 5.4.1 for instruction set table that supports this setting.

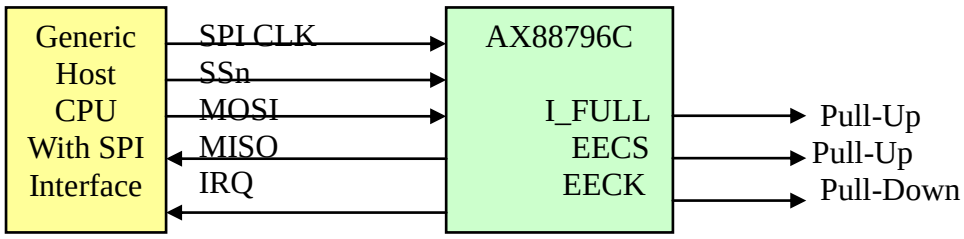


Fig 11 SINGLE SPI BUS APPLICATION DIAGRAM

2.0 Signal Description

The following abbreviations are used in AX88796C pinout:
All pin names with the "n" suffix are low-active signals. The following abbreviations are used in following Tables.

MI	**Multivoltage Input (3.3/2.5/1.8V)**	**PU**	**Pull Up (75Kohm)**
MO	**Multivoltage Output (3.3/2.5/1.8V)**	**PD**	**Pull Down (75Kohm)**
MB	**Bi-directional multivoltage I/O**	**AB**	**Analog IO differential pair**
T	**Tri-state**	**P**	**Power Pin**
4mA	**4mA driving strength**	**A**	**Analog**
8mA	**8mA driving strength**	**S**	**Schmitt trigger**
I	**1.8V input**	**AO**	**Analog Output**
O	**1.8V output**		

2.1 Local CPU Bus Interface Signals Group

<table>
<tr><th>Signal</th><th>Type</th><th>Pin No.</th><th>Description</th></tr>
<tr><td>SA[4:0]</td><td>MI</td><td>46, 47, 48, 49, 50</td><td>System Address: Signals SA[4:0] are address bus input lines. The internal PSR register bit [3] Address Shifter Control bit select the internal address decoding sequence.
<table>
<tr><td>PIN 46 ~ 50</td><td>CHIP Internal Address Bus Decode</td><td></td></tr>
<tr><td>AddressShifter Control Bit
Page0
Offset 0x00 [3]</td><td>0 (Default, Disable)</td><td>1 (Enable)</td></tr>
<tr><td>SA0</td><td>SA0</td><td>SA1</td></tr>
<tr><td>SA1</td><td>SA1</td><td>SA2</td></tr>
<tr><td>SA2</td><td>SA2</td><td>SA3</td></tr>
<tr><td>SA3</td><td>SA3</td><td>SA4</td></tr>
<tr><td>SA4</td><td>SA4</td><td>N/A</td></tr>
</table></td></tr>
<tr><td>SD[15:0]</td><td>MB/8mA</td><td>27, 28, 29, 30, 31, 32, 33, 34, 35, 36, 37, 38, 39, 40, 41, 42</td><td>System Data Bus: Signals SD[15:0] constitute the bi-directional data bus.
NOTE:
1.When the Bus Type is set to MCS-51 mode then SD8 pin will become PSEN.
2.SD14 and SD6 can be configured to GPIO2 through GPIOWCR [10:9] register setting when not used.
3.SD15 and SD7 can be configured to GPIO3 through GPIOWCR [10:9] register setting when not used..</td></tr>
<tr><td>IRQ</td><td>MO/T/8mA</td><td>23</td><td>Programmable Interrupt request. Programmable polarity, source and buffer types. The IRQ polarity can be configured by EEPROM auto-loader or FER register</td></tr>
</table>

SA[5] or FIFO_SEL	MI/PD	45	System Address or FIFO Select: When driven high, all accesses to the AX88796C are to the RX or TX data buffer FIFO (Data Port). The AX88796C supports two kinds of Data Port for receiving/transmitting packets from/to the AX88796C. One is the PIO (Program I/O) Data Port; the other one is the SRAM-like Data Port. The SRAM-like Data Port address range depends on which address line of host processor is being connected to the address line SA5/FIFO_SEL of the AX88796C. Please reserve minimal 2K address space for burst access. Software on host CPU can issue a Single Data Read/Write command to both PIO Data Port and SRAM-like Data Port. However, to use Burst Data Read/Write commands, one has to use SRAM-like Data Port, which requires SA5/FIFO_SEL (pin 45) of the AX88796C connecting to an upper address line of the host CPU. Our reference schematic has SA5/FIFO_SEL pin connected to upper address line for supporting Burst Data Read/Write commands.
CSn	MI/PU	52	Chip Select: Active low. If the AX88796C bus type (TAB-1) is set to SPI Mode then this pin is Slave Select input for SPI bus.
RDn	MI/PU	53	Read: Active low strobe to indicate a read cycle.
WRn	MI/PU	54	Write: Active low strobe to indicate a write cycle. This signal also used to wakeup the AX88796C when it is in reduced power state.
GPIO0	MB/8mA	55	General purpose IO pin #0
AEN/GPIO1	MI	51	Address enable for 8/16-Bit Address-Data Multiplex, MCS-51 bus modes and low byte write select for Renesas bus mode. Please pull-down this pin when configured to 8/16-Bit SRAM-like bus modes. If the AX88796C bus type (TAB-1) is set to SPI Mode then this pin can be configured to GPIO1 provide extra GPIO selection. NOTE: AEN can be configured to GPIO1 through GPIOWCR [8] register setting when not used.
PME	MO/T/8mA	22	Wakeup Indicator: When programmed to do so, is asserted when the AX88696C detects a wakeup event and is requesting the system to wake up from the sleep state. The polarity and buffer type of this signal is programmable through the WFCR register setting.

TAB - 2 LOCAL CPU BUS INTERFACE SIGNALS GROUP

2.2 10/100Mbps Twisted-Pair Interface Signals Group

Signal	Type	Pin No.	Description
TPI+	AB	3	Twisted Pair Receive Input, Positive
TPI-	AB	4	Twisted Pair Receive Input, Negative
TPO+	AB	6	Twisted Pair Transmit Output, Positive
TPO-	AB	7	Twisted Pair Transmit Output, Negative
RSET_BG	AO	64	Off-chip resister. Must be connected 12.1K ohm ± 1% to ground.

TAB - 3 10/100MBPS TWISTED-PAIR INTERFACES SIGNALS GROUP

2.3 Build-in PHY LED Indicator Signals Group

Signal	Type	Pin No.	Description
I_FULL/COL	MB/PU/ 8mA	16	Full-Duplex/Collision Status. If this signal is low, it indicates full-duplex link established, and if it is high, then the link is in half-duplex mode. When in half-duplex and collision occurrence, the output will be driven low for 80ms and driven high at minimum 80ms. The users can also programmed register LCR0 [7:0] and change this LED output function. The LCR1 [15] configure this LED polarity to active high or active low (default). The pull-up or pull-down on pin I_FULL is also used to configure the AX88796C bus type. Please also reference AX88796C bus type table (TAB-1) for detail information.
I_SPEED	MO/8mA	15	Speed Status: If this signal is low, it indicates 100Mbps, and if it is high, then the speed is 10Mbps. The LCR0 [15:8] register provides a register setting to configure this LED output function. The users can change the default setting by program this register.
I_LK/ACT	MO/8mA	14	Link Status/Active: If this signal is low, it indicates link, and if it is high, then the link is fail. When in link status and line activity occurrence, this signal is pulsed high (LED off) for 80ms whenever transmit or receive activity is detected. This signal is then driven low again for a minimum of 80ms, after which time it will repeat the process if TX or RX activity is detected. The register LCR1 [7:0] provides a programmable setting to configure this LED output function. The users can change the default setting by program this register.

TAB - 4 BUILT-IN PHY LED INDICATOR SIGNALS GROUP

2.4 EEPROM Signals Group

<table>
<tr><th>Signal</th><th>Type</th><th>Pin No.</th><th colspan="4">Description</th></tr>
<tr><td>EECS</td><td>MB/4mA/PD</td><td>21</td><td colspan="4">EEPROM Chip Select: EEPROM chip select signal.
NOTE: EECS can be configured to GPIO3 through GPIOWCR [10:9] register setting when not used.</td></tr>
<tr><td rowspan="11">EECK</td><td rowspan="11">MB/4mA/PD</td><td rowspan="11">20</td><td colspan="4">EEPROM Clock: Signal connected to EEPROM clock pin. EECS, EECK can load BUS type setting during power on reset cycle.(PD: Pull Down PU: Pull Up)
NOTE: EECK can be configured to GPIO2 through GPIOWCR [10:9] register setting when not used.</td></tr>
<tr><td>I_FULL</td><td>EECS</td><td>EECK</td><td>Bus Type</td></tr>
<tr><td>PD</td><td>PD</td><td>PD</td><td>8-bit SRAM-like bus (AEN unused and must be pull-low.)</td></tr>
<tr><td>PD</td><td>PD</td><td>PU</td><td>8-bit Address/Data multiplexed bus (AEN=1 address cycle, AEN=0 data cycle).
Pin SD7 ~ SD0 is used. SD5 ~ SD0 represent address bus when AEN =1. Pin SD7 ~SD0 represent data bus when AEN=0. Pin CSN should be low when the AX88796C is selected.</td></tr>
<tr><td>PD</td><td>PU</td><td>PD</td><td>Reserved</td></tr>
<tr><td>PD</td><td>PU</td><td>PU</td><td>MCS-51 (805x)(PSEN/AEN active high)</td></tr>
<tr><td>PU</td><td>PD</td><td>PD</td><td>16-bit SRAM-like bus (AEN unused and must be pull-low.)</td></tr>
<tr><td>PU</td><td>PD</td><td>PU</td><td>16-bit Address/Data multiplexed bus (AEN=1: address cycle, AEN=0 : data cycle)
Pin SD15 ~ SD0 is used. SD5 ~ SD0 represent address bus when AEN =1. SD15 ~SD0 represent data bus when AEN=0. CSN should be low when the AX88796C is selected.</td></tr>
<tr><td>PU</td><td>PU</td><td>PD</td><td>SPI Mode (AEN unused and can be pull-low if GPIO mode is unused.)</td></tr>
<tr><td>PU</td><td>PU</td><td>PU</td><td>16-bit local bus with byte write enable (Renesas SHx style, AEN = low byte SD7 ~ SD0 enable, WRn = high byte SD15 ~ SD8 enable)</td></tr>
<tr><td>EEDIO</td><td>MB/4mA/PU</td><td>19</td><td colspan="4">EEPROM Data In/Out: Signal connected to EEPROM data input and data output pin.
NOTE: EEDIO can be configured to GPIO1 through GPIOWCR [8] setting when not used.</td></tr>
</table>

TAB - 5 EEPROM BUS INTERFACE SIGNALS GROUP

2.5 SPI Interface Signals Group

Signal	Type	Pin No.	Description
MOSI	MI/8mA	42	SPI data input
MISO	MO/T/8mA	41	SPI data output
SSn	MI/PU	52	SPI slave select signal (active low)
SPI_CLK	MI	56	SPI clock input

TAB - 6 SINGLE SPI INTERFACE SIGNALS GROUP

2.6 Miscellaneous Signals Group

Signal	Type	Pin No.	Description
XTALIN	I	61	Crystal/Oscillator Input: A 25MHz crystal, +/- 50 PPM can be connected across XTALIN and XTALOUT. CMOS Local Clock: A 25MHz clock, +/- 50 PPM, 40%-60% duty cycle. Note that the pin does not support 3.3V or 5V voltage supply.
XTALOUT	O	62	Crystal/Oscillator Output: A 25MHz crystal, +/- 50 PPM can be connected across XTALIN and XTALOUT. If a single-ended external clock (LCLK) is connected to XTALIN, the crystal output pin should be left floating.
RSTn	MI/S/PU	17	Chip Reset. Reset is active low. Place the AX88796C under the reset mode. During the rising edge, the AX88796C loads the power on setting data.
TCLK	MB/PD	56	TCLK is bi-direction I/O type pin and support 25MHz system clock input when XTALIN (Pin 61) and XTALOUT (Pin 62) are unused or 25/50/100MHz extra clock output when configure to clock output port. NOTE: 1. TCLK and SPI CLK share the same pin. When AX88796C is configured to SPI mode the TCLK will be used as SPI CLK. 2. TCLK output clock is not free-running clock. If the AX88796C is in Power Saving Mode 2 (PS2)/Sleep Mode and TCLK clock output is enabled then NO clock will be send out due to power saving function gated the internal clock source. 3. Please make sure FER[4:3] setting to the right clock output frequency. 4. TCLK clock output source is from internal PHY. When power saving in Power Saving Mode 2 (PS2) mode, this clock output source will be gated.

<table>
<tr><td></td><td></td><td></td><td>
<table>
<tr><th>TEST2</th><th>TEST1</th><th>TEST_CK_EN</th><th>TCLK</th><th>Comment</th></tr>
<tr><td>PD</td><td>PD</td><td>PD</td><td>Clock output</td><td>Register setting to decide 25, 50 or 100MHz clock output. The register FER[4:3] is the clock output select register.
<table>
<tr><th>[4]</th><th>[3]</th><th>TCLK Output</th></tr>
<tr><td>0</td><td>0</td><td>Disable. (Default input direction and internal pull-down, compatible with AX88796B)</td></tr>
<tr><td>0</td><td>1</td><td>25MHz clock output</td></tr>
<tr><td>1</td><td>0</td><td>50MHz clock output</td></tr>
<tr><td>1</td><td>1</td><td>100MHz clock output</td></tr>
</table></td></tr>
<tr><td>PD</td><td>PD</td><td>PU</td><td>25MHz clock input</td><td>XTALOUT/XTALIN not used</td></tr>
<tr><td>PD</td><td>PU</td><td>X</td><td>N/A</td><td>N/A</td></tr>
<tr><td>PU</td><td>X</td><td>X</td><td>N/A</td><td>IC test mode</td></tr>
</table>
</td></tr>
<tr><td>TEST_CK_EN</td><td>MI/PD/S</td><td>57</td><td>TCLK mode select. Please reference TCLK table setting</td></tr>
<tr><td>TEST2</td><td>MI/PD/S</td><td>12</td><td>TCLK mode select. Please reference TCLK table setting</td></tr>
<tr><td>TEST1</td><td>MI/PD/S</td><td>13</td><td>TCLK mode select. Please reference TCLK table setting</td></tr>
<tr><td>VCC3A3</td><td>P</td><td>1</td><td>Power Supply for Analog Circuit: +3.3V DC.</td></tr>
<tr><td>GND3A3</td><td>P</td><td>2</td><td>Power Supply for Analog Circuit: +0V DC or Ground Power.</td></tr>
<tr><td>VCC18A</td><td>P</td><td>5, 60</td><td>Analog power for oscillator, PLL, and Ethernet PHY differential I/O pins, 1.8V</td></tr>
<tr><td>GND18A</td><td>P</td><td>8, 63</td><td>Analog ground for oscillator, PLL, and Ethernet PHY differential I/O pins.</td></tr>
<tr><td>V18F</td><td>P</td><td>9</td><td>On-chip 3.3V to 1.8V Regulator output +1.8V DC with 150mA driving current.</td></tr>
<tr><td>VCC3R3</td><td>P</td><td>10</td><td>On-chip 3.3V to 1.8V Regulator power supply: +3.3V DC.</td></tr>
<tr><td>GND3R3</td><td>P</td><td>11</td><td>On-chip 3.3V to 1.8V Regulator ground.</td></tr>
<tr><td>GND</td><td>P</td><td>18, 26, 58</td><td>Ground.</td></tr>
<tr><td>VCCIO</td><td>P</td><td>25, 44</td><td>Multi-voltage Power Supply for IO Pad: +3.3V/2.5V/1.8V DC.</td></tr>
<tr><td>VCCK</td><td>P</td><td>24, 43, 59</td><td>Power Supply for core logic: +1.8V DC.</td></tr>
</table>

TAB - 7 MISCELLANEOUS SIGNALS GROUP

3.0 Memory Mapping Table

3.1 EEPROM Memory Format Table

The AX88796C supports 16-bit mode 93C56/93C66 EEPROM. The EEPROM content will be auto-loaded to respective AX88796C registers setting described in below EEPROM mapping format during AX88796C hardware reset.

During hardware reset, the EEPROM loader will check the high-byte of the EEPROM first word data and the Check Sum field value at low-byte of EEPROM address 0x27. Please make sure the high-byte of first word is equal to 0x5A before programming the EEPROM data. If the hardware calculated the checksum value of EECSR register plus the Check Sum filed of EEPROM address 0x27 is not equal to 0xFF then the EEPROM loader will proclaim that wrong EEPROM data and stop auto-loading EEPROM.

Please check PSCR [15] EEPROM_OK and EECSR register checksum value for EEPROM auto-loading status. If PSCR [15] EEPROM_OK is one and EECSR register is 0xFF then external EEPROM device is not connected. If PSCR [15] EEPROM_OK is zero, then the device report checksum value did not match with expected checksum value and no EEPROM data can load into the AX88796C internal registers.

The EEPROM data can be indirectly accessed through the EECR and EEDR registers. The EECSR register saves the pre-calculated checksum complement value for EEPROM auto-loading finish check. The EECSR provides hardware calculated total checksum value from 0x00 up to the valid address location. If 0xFF minus EECSR checksum value is equal to the EEPROM address 0x27's checksum value then the checksum test is passed. The users can change the EEPROM length value (address 00h, low-byte) to 0Fh if the wakeup frame function is not supported that can reduce the EEPROM auto-loading time.

The following is a sample EEPROM data with the desired MAC address 00-12-34-56-78-9A.

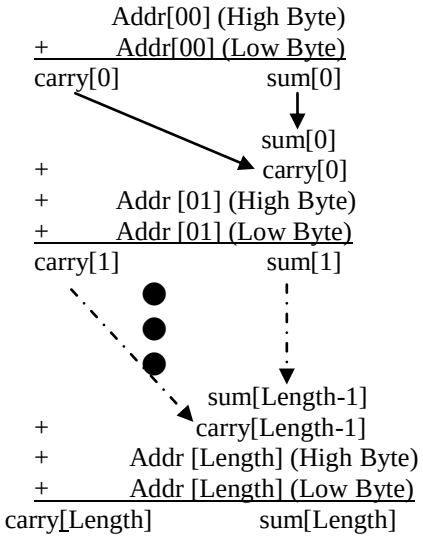
- Please reference register description section and set the correspondent value for your specific application.

Addr	D[15:0]*	Page #, Offset#	Register Description
0x00	0x5A, Length	Length (low-byte)	Length: Indicates the total of word counts for auto loading
0x01	0x789A	Page 3 Offset0x02	MAC Address Setup Register0 (MACASR0) MAC address [39:32], [47:40]
0x02	0x3456	Page 3 Offset 0x04	MAC Address Setup Register1 (MACASR1) MAC address [23:16], [31:24]
0x03	0x0012	Page 3 Offset 0x06	MAC Address Setup Register2 (MACASR2) MAC Address [7:0], [15:8]
0x04	0x0003	Page 0 Offset 0x04	Function Enable Register (FER)
0x05	0xFFFF	Page 0 Offset 0x08	Interrupt Mask Register (IMR)
0x06	0x0820	Page 0 Offset 0x0C	Power Saving Configuration Register (PSCR) NOTE: Bit 11 (PHY_Reset) can't be written from EEPROM load process and should be force to default value!!

0x07	0x0018	Page 0 Offset 0x0E	MAC Configuration Register (MACCR)
0x08	0x0000	Page 2 Offset 0x02	IO Control Register (ICR)
0x09	0x1002	Page 2 Offset 0x04	PHY Control Register (PCR)
0x0A	0x0C00	Page 4 Offset 0x0A	SPI Configuration Register (SPICR)
0x0B	0xFF00	Page 4 Offset 0x0C	SPI Interrupt Status and Mask Register (SPIISMR)
0x0C	0x0000	Page 4 Offset 0x02	GPIO Enable Register (GPIOER)
0x0D	0xF000	Page 4 Offset 0x04	GPIO IRQ Control Register (GPIOCR)
0x0E	0x0000	Page 4 Offset 0x06	GPIO Wakeup Control Register (GPIOWCR)
0x0F	0x0000	Page 5 Offset 0x02	Wakeup Frame Timer Register (WFTR)
0x10	0x0000	Page 5 Offset 0x04	Wakeup Frame Cascade Command Register (WFCCR)
0x11	0x0000	Page 5 Offset 0x06	Wakeup Frame Command 0~3 Register (WFCR03)
0x12	0x0000	Page 5 Offset 0x08	Wakeup Frame Command 4~7 Register (WFCR47)
0x13	0x0000	Page 5 Offset 0x0A	Wakeup Frame 0 Byte Mask [15:0] Register (WF0BMR0)
0x14	0x0000	Page 5 Offset 0x0C	Wakeup Frame 0 Byte Mask [31:16] Register (WF0BMR1)
0x15	0x0000	Page 5 Offset 0x0E	Wakeup Frame 0 CRC Register (WF0CR)
0x16	0x0000	Page 5 Offset 0x10	Wakeup Frame 0 Offset Byte Register (WF0OBR)
0x17	0x0000	Page 5 Offset 0x12	Wakeup Frame 1 Byte Mask [15:0] Register (WF1BMR0)
0x18	0x0000	Page 5 Offset 0x14	Wakeup Frame 1 Byte Mask [31:16] Register(WF1BMR1)
0x19	0x0000	Page 5 Offset 0x16	Wakeup Frame 1 CRC Register (WF1CR)
0x1A	0x0000	Page 5 Offset 0x18	Wakeup Frame 1 Offset Byte Register (WF1OBR)
0x1B	0x0000	Page 5 Offset 0x1A	Wakeup Frame 2 Byte Mask [15:0] Register (WF2BMR0)
0x1C	0x0000	Page 5 Offset 0x1C	Wakeup Frame 2 Byte Mask [31:16] Register (WF2BMR1)
0x1D	0x0000	Page 6 Offset 0x02	Wakeup Frame 2 CRC Register (WF2CR)
0x1E	0x0000	Page 6 Offset 0x04	Wakeup Frame 2 Offset Byte 0 Register (WF2OBR)
0x1F	0x0000	Page 6 Offset 0x06	Wakeup Frame 3 Byte Mask [15:0] Register (WF3BMR0)
0x20	0x0000	Page 6 Offset 0x08	Wakeup Frame 3 Byte Mask [31:16] Register (WF3BMR1)
0x21	0x0000	Page 6 Offset 0x0A	Wakeup Frame 3 CRC Register (WF3CR)
0x22	0x0000	Page 7 Offset 0x12	Wakeup Frame Reply 0 ~ 1 Register (WFR01)
0x23	0x0000	Page 7 Offset 0x14	Wakeup Frame Reply 2 ~ 3 Register (WFR23)
0x24	0x0000	Page 7 Offset 0x1A	Wakeup Frame Partial Checksum 0 Register (WFPC0)
0x25	0x0000	Page 7 Offset 0x1C	Wakeup Frame Partial Checksum 1 Register (WFPC1)
0x26	0x0000	Page 0 Offset 0x0A	Wakeup Frame Configuration Register (WFCR) NOTE: Please make sure checksum value is correct before write this value. To protect sleep mode being write incorrectly causing chip in sleep state.
0x27	0x00, <CheckSum>	Check Sum (low-byte)	The Check Sum value of EEPROM address 00h ~ <Length-1>h fields. This field will always be auto-loaded into the EECSR register no matter the <Length> field value.

TAB - 8 EEPROM DATA FORMAT

The AX88796C EEPROM 8 bits Checksum Algorithm:



Addr [27h](Low)= 0xFF – (sum[Length] + carry[Length]) EECSR value

3.2 Internal Memory Mapping Table

The AX88796C internal register address [7:0] is mapping to {SA5=0, PS2, PS1, PS0, SA4, SA3, SA2, SA1, SA0}. The SA5 set to zero to enable internal register access. If SA5 set to one then the internal TX/RX buffer memory access will be enabled. There are total 8 pages within the register space and each page has total 32 byte data. The SA4, SA3 SA2, SA1 and SA0 will be the offset inside each page. The three page select bits PS2, PS1 and PS0 configured from the PSR [2:0] decide which page to select.

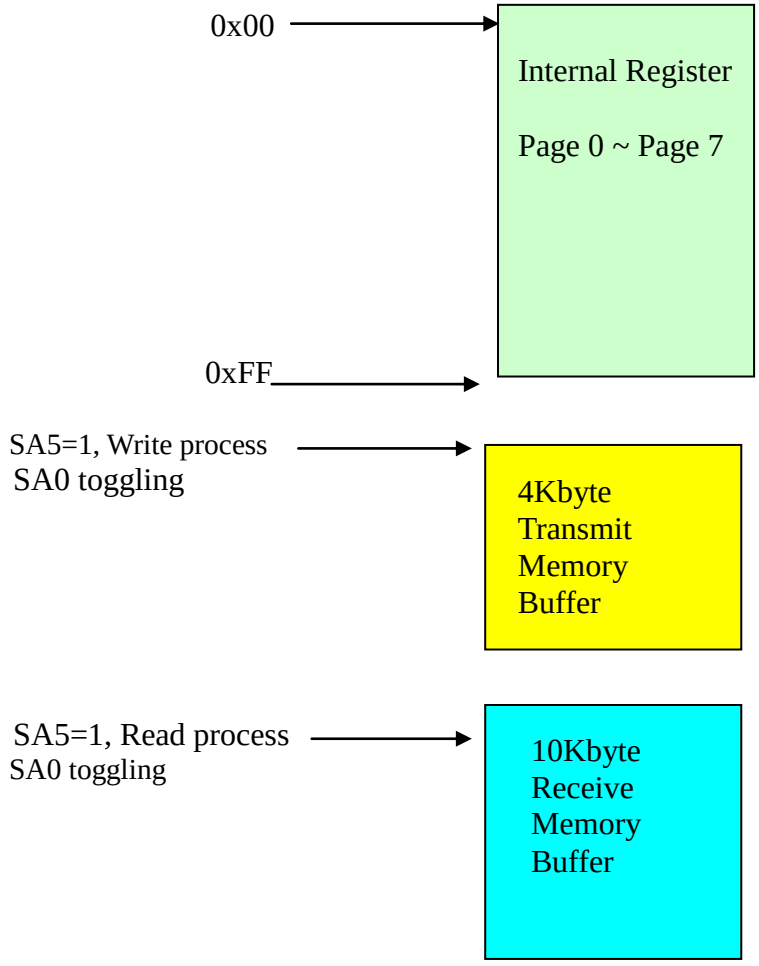


Fig 12 INTERNAL SRAM MAP

3.2.1 Register Read/Write Access

The AX88796C provides direct access to internal register through read/write operation when SA5 is set to zero. The PSR [2:0] define the page select information (Page 0 ~ Page 7). Pin SA4 ~ SA0 provide the offset information. The AX88796C supports register burst read or burst write access when the chip select signal is continuous stay low.

3.2.2 RX/TX Packet Buffer Access

The AX88796C provides 4Kbyte TX Buffer RAM and 10Kbyte RX Buffer RAM for packet reception and transmission. When SA5=1, the burst operation to access TX/RX buffer will be enabled as long as chip select stay low. The AX88796C also supports PIO access to TX/RX buffer RAM through page 0 offset 14h register setting. Please always reserve at least 2KB memory buffer when access through SA5 burst access.

4.0 Basic Operation

4.1 Receiver Filtering

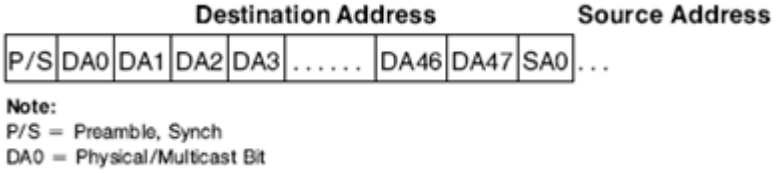
The address filtering logic compares the Destination Address Field (first 6 bytes of the received packet) to the Physical address registers stored in the Address Register Array. If any one of the six bytes does not match the pre-programmed physical address, the Protocol Control Logic rejects the packet. This is for unicast address filtering. All multicast destination addresses are filtered using a hashing algorithm. (See following description.) If the multicast address indexes a bit that has been set in the filter bit array of the Multicast Address Register Array the packet is accepted, otherwise the Protocol Control Logic rejects it. Each destination address is also checked for all 1's, which is the reserved for broadcast address.

4.1.1 Unicast Address Match Filter

The physical address registers are used to compare the destination address of incoming packets for rejecting or accepting packets. Comparisons are performed on a byte wide basis. The bit assignment shown below relates the sequence in MACASR2/MACASR1/MACASR0 to the bit sequence of the received packet.

	D7	D6	D5	D4	D3	D2	D1	D0
MACASR2[15:8]	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
MACASR2[7:0]	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
MACASR1[15:8]	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
MACASR1[7:0]	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
MACASR0[15:8]	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
MACASR0[7:0]	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Note: The bit sequence of the received MAC address is DA0, DA1, … DA46, DA47 ….



4.1.2 Multicast Address Match Filter

The Multicast Address Registers provide filtering of multicast addresses hashed by the CRC logic. All destination addresses are fed through the 32 bits CRC generation logic and as the last bit of the destination address enters the CRC, the 6 most significant bits of the CRC generator are latched. These 6 bits are then decoded by a 1 of 64 decode to index a unique filter bit (FB0-63) in the Multicast Address Registers. If the filter bit selected is set, the multicast packet is accepted. The system designer would use a program to determine which filter bits to set in the multicast registers. All multicast filter bits that correspond to Multicast Address Registers accepted by the node are then set to one. To accept all multicast packets all of the registers are set to all ones.

	D7	D6	D5	D4	D3	D2	D1	D0
MFAR0	FB7	FB6	FB5	FB4	FB3	FB2	FB1	FB0
MFAR1	FB15	FB14	FB13	FB12	FB11	FB10	FB9	FB8
MFAR2	FB23	FB22	FB21	FB20	FB19	FB18	FB17	FB16
MFAR3	FB31	FB30	FB29	FB28	FB27	FB26	FB25	FB24
MFAR4	FB39	FB38	FB37	FB36	FB35	FB34	FB33	FB32
MFAR5	FB47	FB46	FB45	FB44	FB43	FB42	FB41	FB40
MFAR6	FB55	FB54	FB53	FB52	FB51	FB50	FB49	FB48
MFAR7	FB63	FB62	FB61	FB60	FB59	FB58	FB57	FB56

{MFAR67 [15:0], MFAR54 [15:0], MFAR23 [15:0], MFAR01 [15:0]} = the multicast address bit map for multicast frame filtering block. For example, see below Fig-13.

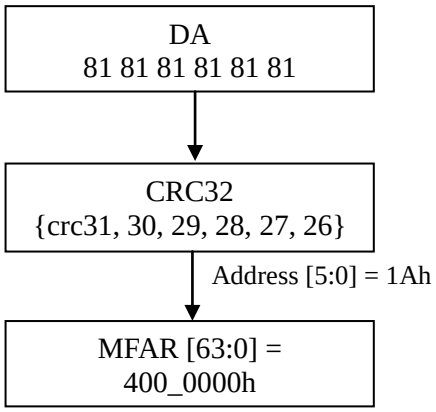


Fig 13 MULTICAST FILTER EXAMPLE

As shown in below figure, the Multicast Filter Array Register (MFAR) provides filtering of multicast addresses hashed through the CRC logic. All Destination Address field are fed through the 32 bits CRC generation logic. As the last bit of the Destination Address field enters the CRC, the 6 most significant bits of the CRC generator are latched. These 6 bits are then decoded by a 1-to-64 decoder and index a unique filter bit (FB0-63) in the Multicast Filter Array. If the filter bit selected is set, the multicast packet is accepted. The system designer should use a program to determine which filter bits to set in the multicast registers. All multicast filter bits that correspond to Multicast Filter Array Registers accepted by the node are then set to one. To accept all multicast packets all of the registers are set to all ones.

Note that the Ethernet MAC regardless of MFAR setting always filters all the receiving Pause Frames.

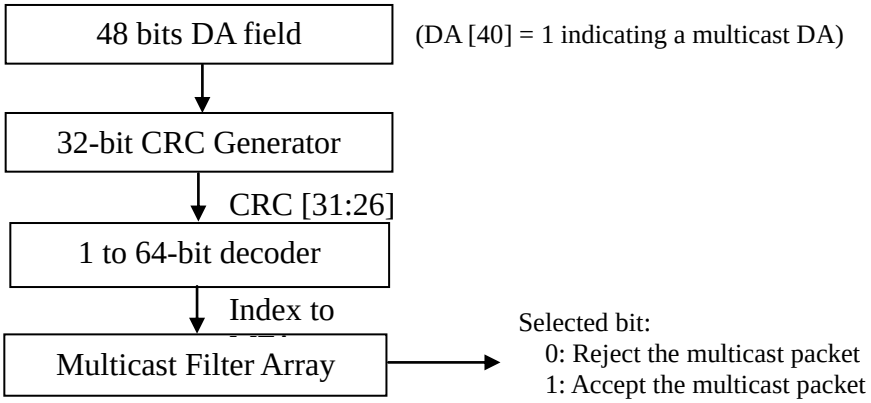


Fig 14 MULTICAST FILTER ARRAY HASHING ALGORITHM

EXAMPLE: If the accepted multicast packet's destination address Y is found to hash to the value 32 (0x20), then FB32 in MFAR34 should be initialized to "1". This will allow the Ethernet MAC to accept any multicast packet with the destination address Y. Although the hashing algorithm does not guarantee perfect filtering of multicast address, it will perfectly filter up to 64 logical address filters if these addresses are chosen to map into unique locations in the multicast filter. Note: The LSB bit of received packet's first byte being "1" signifies a Multicast Address.

Following is the truth table about multicast packet filtering condition. (Please also refer to RXCR register description)

PRO bit	AMALL bit	AM bit	Pass Hashing Algorithm?	Multicast Packet Filtered by Ethernet MAC?
0	0	0	0	Yes
0	0	0	1	Yes
0	0	1	0	Yes
0	0	1	1	No
0	1	0/1	0/1	No
1	0/1	0/1	0/1	No

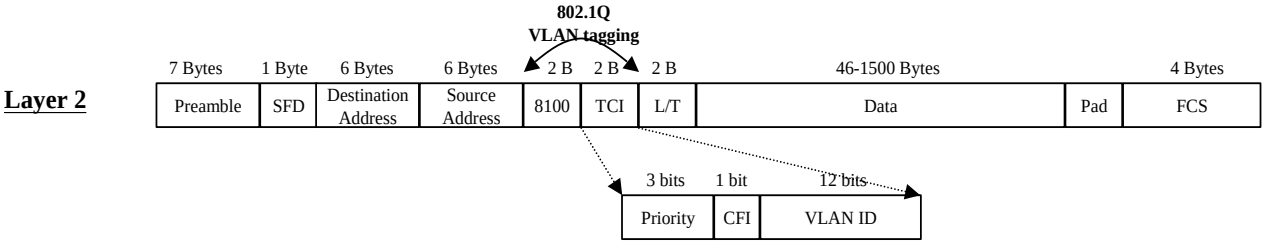
Note: Passing Hashing Algorithm means that the selected bit in MFAR of CRC-32 result is set to "1".

4.1.3 Broadcast Address Match Filter

The Broadcast check logic compares the Destination Address Field (first 6 bytes of the received packet) to all 1's, which is the values are "FF FF FF FF FF FF" in Hex format. If any bit of the six bytes does not equal to 1's, the Protocol Control Logic rejects the packet.

4.1.4 VLAN Match Filter

The AX88796C compares the thirteenth and fourteenth bytes of receive frames. If not match with VLAN_ID1 (VID1FR), VLAN_ID_0 (VID0FR) then reject current frame. The VLAN filter will always accept VLAN_ID is zero of receive frames due to it is IEEE-802.1Q (for priority purpose) frames. The maximum length of the good packet is thus change from 1518 bytes to 1522 bytes.



The VLAN ID field (12 bits) within the received IEEE-802.1Q tagged packet will be used to compare with VID1 and VID2 setting. If it matches either VID1 or VID2, or its value is equal to all zeros, the received IEEE-802.1Q tagged packets will be forwarded to the Host interface. Meanwhile, the VSO bit (VID0FR [15]) determines whether the VLAN Tag bytes (4 bytes) are stripped off or not during forwarding to the Host interface. Also, if the incoming packets contain no VLAN Tag bytes, they will be forwarded to the Host interface by default. If there is no match between the received IEEE-802.1Q tagged packets and VID1 and VID2, the packets will be discarded. Please reference TAB-9 below.

Received packet / VID1, VID2	Untagged	Tagged	
		VID=Zero	VID= Not zero
Zero	Forwarded	Forwarded	Discarded
Not zero	Forwarded	Forwarded	Match: Forwarded No Match: Discarded

TAB - 9 VID1/VID2 SETTING TO FILTER RECEIVED PACKET

4.2 Buffer Management Operation

There are four buffer memory access types used in the AX88796C buffer access flow.

1. Packet Reception: write data to RX memory buffer from MAC
2. Packet Transmission: read data from TX memory buffer to MAC
3. Filling Packets to Transmit Buffer: Host interface write data to TX memory
4. Removing Packets from the Receive Buffer Ring: Host interface read data from RX memory

The type 1 and 2 operations act as Local DMA. Type 1 does Local DMA write operation and type 2 does Local DMA read operation. The type 3 and 4 operations act as Remote DMA. Type 3 does Remote DMA write operation and type 4 does Remote DMA read operation.

4.3 Packet Reception

The Local DMA receives channel use a Buffer Ring Structure comprised of a series of contiguous fixed length 128 byte buffers for storage of received packets. Ethernet packets consist of minimum packet size (64 bytes) to maximum packet size (1522 bytes), the 128 byte buffer length provides a good compromise between short packets and longer packets to most efficiently use memory. In addition these buffers provide memory resources for storage of back-to-back packets in loaded networks. Buffer Management Logic in the AX88796C controls the assignment of buffers for storing packets. The Buffer Management Logic provides three basic functions: linking receives buffers for long packets, recovery of buffers when a packet is rejected, and recalculation of buffer pages that have been read by the host.

Beginning Of Reception

When the first packet begins arrive the AX88796C and begins storing the packet at the location pointed to by the RMPR. An offset of 8 bytes is reserved in this first buffer to allow room for storing receives status corresponding to this packet.

Linking Receive Buffer Pages

If the length of the packet exhausts the first 128 bytes buffer, the DMA performs a forward link to the next buffer to store the remainder of the packet. For a maximal length packet the buffer logic will link 12 buffers to store the entire packet. Buffers cannot be skipped when linking; a packet will always be stored in contiguous buffers.

Successful Reception

If the packet is successfully received as shown, the DMA is restored to the first buffer used to store the packet. The DMA then stores the Receive Status, a Pointer to where the next packet will be stored and the number of received bytes. Note that the remaining bytes in the last buffer are discarded and reception of the next packet begins on the next empty 128 byte buffer boundary. The AX88796C is then initialized to the next available buffer in the Buffer Ring. (The location of the next buffer had been previously calculated and temporarily stored in an internal scratchpad register.)

Buffer Recovery For Rejected Packets

If the packet is a runt packet or contains CRC or Frame Alignment errors, it is rejected. The buffer management logic resets the DMA back to the first buffer page used to store the packet (pointed to by CPR), recovering all buffers that had been used to store the rejected packet. This operation will not be performed if the AX88796C is programmed to accept either runt packets or packets with CRC or Frame Alignment errors. The received CRC is always stored in buffer memory after the last byte of received data for the packet.

4.4 Packet Transmission

The Local DMA Read is also used during transmission of a packet. When the AX88796C receives a command to transmit the packet, the buffer memory data will be moved into the FIFO as required during transmission. The AX88796C Controller will generate and append the preamble, synch and CRC fields. The AX88796C supports options of transmit queue function to enhance transmit performance.

Transmit Packet Assembly

The AX88796C requires a contiguous assembled packet with the format shown below. The transmit byte count includes the Destination Address, Source Address, Length Field and Data. It does not include preamble and CRC. When transmitting data smaller than 64 bytes, The AX88796C can auto padding to a minimum length of 64 bytes Ethernet frame. The packets are placed in the buffer RAM by the system. System programs the AX88796C Core's Remote DMA to move the data from the system buffer RAM to internal transmit buffer RAM.

The data transfer must be 16-bits (1 word) when in 16-bit mode, and 8-bits when the AX88796C Controller is set in 8-bit mode. The data width is selected by setting the WTS bit in the Data Configuration Register.

Destination Address	6 Bytes
Source Address	6 Bytes
Length / Type	2 Bytes
Data (Pad if < 46 Bytes)	46 Bytes Minimal

Fig 15 GENERAL TRANSMIT PACKET FORMAT

Conditions Required To Begin Transmission

In order to transmit a packet, the following three conditions must be met:
1. The Inter-packet Gap Timer has timed out
2. At least one byte has entered the FIFO.
3. If a collision had been detected then before transmission the packet back-off time must have timed out.

Collision Recovery

During transmission, the Buffer Management logic monitors the transmit circuitry to determine if a collision has occurred. If a collision is detected, the Buffer Management logic will reset the FIFO and restore the Transmit DMA pointers for retransmission of the packet. The COL bit will be set and the NCR (Number of Collisions Register) will be incremented. If 15 retransmissions each result in a collision the transmission will be aborted.

Transmit Packet Assembly Format

The following diagrams describe the format for how packets must be assembled prior to transmission for different byte ordering schemes. The various formats are selected in the Data Configuration Register.

D15 D8	D7 D0
Destination Address 1	Destination Address 0
Destination Address 3	Destination Address 2
Destination Address 5	Destination Address 4
Source Address 1	Source Address 0
Source Address 3	Source Address 2
Source Address 5	Source Address 4
Type / Length 1	Type / Length 0
Data 1	Data 0
…	…

This format is used with 16-bit bus interface

D7 D0
Destination Address 0 (DA0)
Destination Address 1 (DA1)
Destination Address 2 (DA2)
Destination Address 3 (DA3)
Destination Address 4 (DA4)
Destination Address 5 (DA5)
Source Address 0 (SA0)
Source Address 1 (SA1)
Source Address 2 (SA2)
Source Address 3 (SA3)
Source Address 4 (SA4)
Source Address 5 (SA5)
Type / Length 0
Type / Length 1
Data 0
Data 1
…

This format is used with 8-bit bus interface

Note: All examples above will result in a transmission of a packet in order of DA0 (Destination Address 0), DA1, DA2, DA3 and so on in byte. Bits within each byte will be transmitted least significant bit first.

4.5 Filling Packet to Transmit Buffer: Host write data to TX memory

The Remote DMA channel is used to both assemble packets for transmission, and move the received packets from the Receive Buffer Ring. It may also be used as a general-purpose slave DMA channel for moving blocks of data or commands between host memory and local buffer memory. There are two modes of operation, Remote Write and Remote Read Packet.

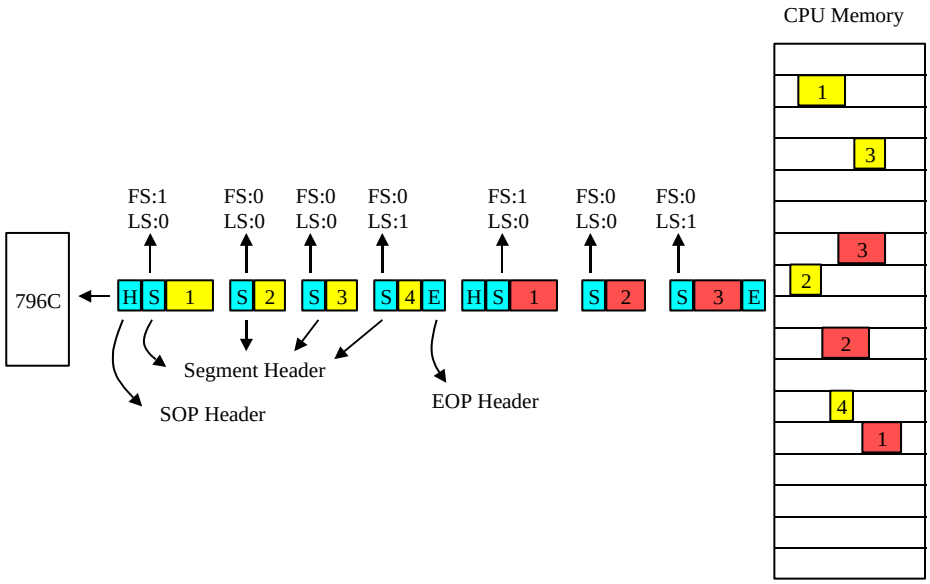
Remote Write

A Remote Write transfer is used to move a block of data from the host into local buffer memory. The Remote DMA will read data from the I/O port and sequentially write it to local buffer memory beginning at the Remote Start Address. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches a count of zero.

For detail programming procedure please reference the **AX88796C Software Programming Guide** documentation for further detail information.

Scatter memory approach (Packet data distributed in difference memory locations)

The scatter memory approach assumes the packet information is located in different memory pages. The AX88796C driver will copy these slices of the data into the TX memory in segment header format without re-grouping the packet. For example, the first yellow packet has the Layer 2 payload located in memory location 1, Layer 3 data in yellow location 2, Layer 4 data stored in yellow location 3 and the rest data in yellow location 4. The AX88796C is able to support direct moving each segment data with different segment ID to the AX88796C TX memory buffer and reassemble in to one packet before pass to TX MAC.



Sequence number should continuous between each dma burst

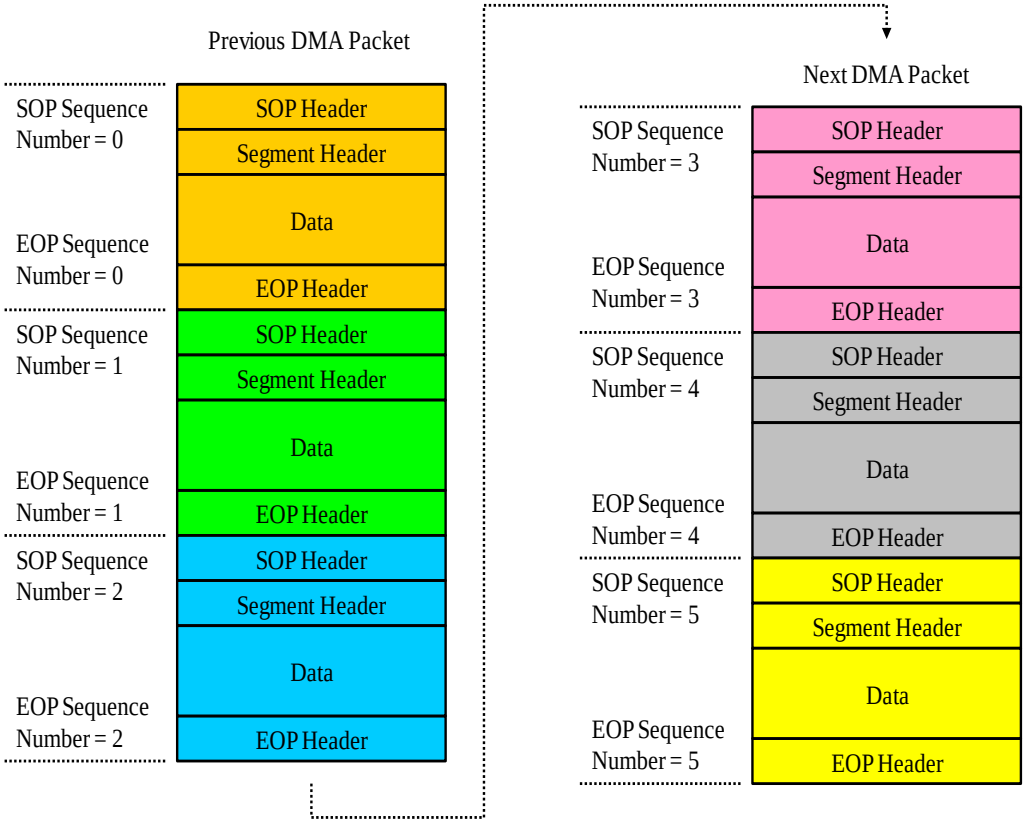


Fig 16 HOST FILL PACKET TO TX MEMORY THROUGH SCATTER MEMORY APPROACH

TX Header Format:

The AX88796C TX header format is list in Fig 17 for reference.

1. The SOP Header contains the packet length information, sequence ID, checksum, de-queue control information.
2. The Segment Header include segment length, segment number ID, alignment information, first/last index information.
3. The EOP header has packet length and segment number for hardware end of the packet check.

TX SOP Header

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DICF	CPHI	INT	Manual dequeue		Packet Length [10:0]										
Sequence Number [4:0]					Packet Length Bar [10:0]										

TX Segment Header

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FS	LS	Segment Number[2:0]			Segment Length [10:0]										
End Offset [1:0]		Start Offset [2:0]			Segment Length Bar [10:0]										

TX EOP Header

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Sequence Number [4:0]					Packet Length [10:0]										
Sequence Number Bar [4:0]					Packet Length Bar [10:0]										

Fig 17 TX HEADER FORMAT

TX SOP Header Format:

Bit	Name	Function Description
31:27	Sequence Number[4:0]	Packet pre-assigned ID for tracking
26:16	Packet Length Bar [10:0]	TX packet length invert. For header check.
15	DICF	Disable TX checksum insertion function. 1: Disable checksum insertion. 0: Enable checksum insertion function.
14	CPHI	Pseudo header checksum value included. 1: Pseudo header checksum value included in Layer four checksum field. 0: No meaning in L4 checksum field.
13	INT	Generate interrupt when transmit complete
12	Manual dequeue	1: Current packet will be paused until packet stay timer over TX timer limit if TX timer is enabled.

		0: Current packet will be transmitted immediately.
11	N/A	N/A
10:0	Packet Length[10:0]	Total packet size information

TX Segment Header Format:

Bit	Name	Function Description
31:30	End Offset[1:0]	The data transfer unit by DMA. The software must use set field to tell AX88796C the data transfer unit of DMA operation. The AX88796C doesn't check this field in PIO mode. 0: The DMA controller transfer data in unit of 32-bit. 1: The DMA controller transfer data in unit of 64-bit. 2: The DMA controller transfer data in unit of 128-bit. 3: The DMA controller transfer data in unit of 256-bit.
29:27	Start Offset[2:0]	Data starting index location. The starting byte of the packet.
26:16	SegmentLength Bar[10:0]	Invert of segment length for internal checking purpose
15	FS	First Segment of the packet if set to one
14	LS	Last Segment of the packet if set to one
13:11	Segment Number[2:0]	Segment ID for grouping purpose and internal checking.
10:0	Segment Length [10:0]	Packet segment length information.

TX EOP Header Format:

Bit	Name	Function Description
31:27	SequenceNumberBar[4:0]	The inverse of the sequence number for header check
26:16	Packet Length Bar [10:0]	Inverse of Packet length for header check
15:11	Sequence Number [4:0]	The packet segment number
10:0	Packet Length [10:0]	Packet total length information

4.6 Removing Packets from the Ring: Host read data from RX memory

Remote Read

A Remote Read transfer is used to move a block of data from local buffer memory to the host. The Remote DMA will sequentially read data from the local buffer memory, beginning at the Remote Start Address, and write data to the I/O port. The DMA Address will be incremented and the Byte Counter will be decremented after each transfer. The DMA is terminated when the Remote Byte Count Register reaches zero.

Please reference the **AX88796C Software Programming Guide** for further detail guideline for read process.

RX Packet Format for Received Packets

The following diagrams (Fig 18) describe the format for how received packets are placed into memory by the local DMA channel. The AX88796C RX packet format includes three of RX packet header information plus regular Ethernet packet format include DA MAC, SA MAC, packet type, and payload.

D15 D8	D7 D0
RX Header1 [15:0]	
RX Header1 [31:16]	
RX Header2 [15:0]	
RX Header3 [15:0](optional, if FER[2] is set to one)	
RX Header3 [31:16](optional, if FER[2] is set to one)	
Destination Address 1	Destination Address 0
Destination Address 3	Destination Address 2
Destination Address 5	Destination Address 4
Source Address 1	Source Address 0
Source Address 3	Source Address 2
Source Address 5	Source Address 4
Type / Length 1	Type / Length 0
Data 1	Data 0
…	…

Fig 18 THE AX88796C RX PACKET FORMAT

RX Header Format:

The AX88796C RX packet headers provide the receiving packet length, VLAN/L2/3/4 packet type, checksum information, and packet error-type information. The RX header information will smooth and easy for host to speed up their read process and enhance the overall RX performance. Fig 19 shows the AX88796C RX header format.

RX Header 1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MC/ BC	Runt Pkt	MII Error	CRC Error		Packet Length [10:0]										
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Sequence Number [4:0]					Packet Length Bar [10:0]										

RX Header 2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CE	L3_Pkt_Type		L4_PKT_Type			L3_ Err	L4_ Err	Reserved	Priority[2:0]			Strip	VLAN IND[2:0]		

RX Header 3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Csum [15:0]															
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Offset [7:0]								Protocol [7:0]							

Fig 19 RX HEADER FORMAT

RX Header 1 Format:

Bit	Name	Function Description
31:27	Sequence Number[4:0]	Packet Sequence number ID for tracking
26:16	Packet Length Bar[10:0]	Inverse of Packet Length[10:0] for header check
15	MC/BC	1: Multicast or Broadcast Packet 0: Unicast Packet
14	Runt Packet	Receive runt packet. Packet size is less than 64 bytes
13	MII Error	1: RX Error found on receive packet 0: No MII Error found
12	CRC Error	1: Receive packet CRC checksum error 0: Good CRC checksum
11	N/A	N/A
10:0	Packet Length[10:0]	Receive Packet Size information

RX Header 2 Format:

Bit	Name	Function Description
15	CE	This bit combines 4 kinds of status, IPv4 version check error, IPv6 version check error, fragment packet and IPv6 parameter error. 1: One of listed status occurred in this packet. 0: No listed status in this packet.
14:13	L3_PKT_Type[1:0]	Layer 3 Packet type information 11: IPv6 in IPv4 tunnel 01: IPv6 10: IPv4 00: NON_IP packet
12:10	L4_PKT_Type[2:0]	Layer 4 Packet type information 001 : UDP 100 : TCP 010 : ICMP 011 : IGMP 101 : ICMPv6 100 : IP only 000 : IP only or COE do not parse Layer 4 header.
9	L3_Err	Layer 3 checksum error. If this bit asserted, means this packet is a L3 error packet judged by COE. This packet did not pass the L3 checksum check
8	L4_Err	Layer 4 checksum error. If this bit asserted, means this packet is a L4 error packet judged by COE. This packet did not pass the L4 checksum check..
7	N/A	N/A
6:4	Priority[2:0]	3-bit field which refers to the IEEE 802.1p priority. It indicates the frame priority level from 0 (lowest) to 7 (highest), which can be used to prioritize different classes of traffic (voice, video, data, etc). (When VLAN_IND is equal to 3'b000, than this field is no effect.)
3	Strip	VLAN Tag Strip 0: Received non-TAG frame or received TAG frame but hardware does not enable TAG strip function. 1: Received TAG-frame and TAG stripped by hardware
2:0	VLAN ID[2:0]	VLAN Indication 000: This packet contains no VLAN tag. 100: This packet contains the VLAN id of 0 that is used for priority. 101: This packet contains the VLAN id of VID1 in the VLAN Control Register. 110: This packet contains the VLAN id of VID2 in the VLAN Control Register. 111: This packet contains the VLAN id which no match all zero, VID1 and VID2.

RX Header 3 Format: (Optional, enabled if register FER RH3M bit is set to one)

Bit	Name	Function Description
31:24	Offset[7:0]	The offset of where Csum start calculate
23:16	Protocol[7:0]	The protocol field of this packet
15:0	Csum[15:0]	Partial checksum of layer 4 payload

4.7 Wake-up Detection

4.7.1 Wake-up frame

The AX88796C supports up to eight programmable filters that can go through many different kind of receive packet patterns, if the remote wakeup function is enabled. The remote wakeup function receives all the incoming frames and checks each frame against the enabled filter rule and recognizes the frame as a remote wake-up frame if it passes the MAC address filtering and CRC value match. In order to determine which bytes of the frames should be checked by the CRC-32 module. The AX88796C use a programmable byte mask and a programmable pattern offset for each of the eight supported filters. The AX88796C also provides the last byte match check and options cascade up to eight programmable filters. So these eight pattern detectors can operate simultaneously or sequentially.

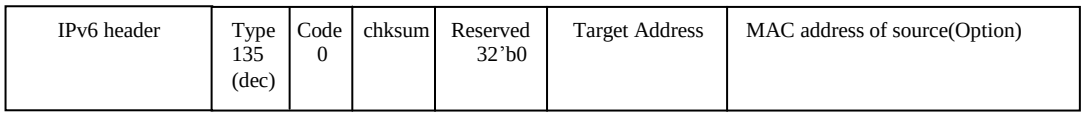
The byte mask is a 32-bit field that specifies whether or not each of the next 32 contiguous bytes within the frame, beginning in the pattern offset, should be checked. If bit j in the byte mask is set, the diction logic checks byte offset +j in the frame.

The pattern offset define on Offset 7 ~ 0 for each wake-up filter 7 ~ 0 and the real offset value equal to Offset register multiplied by 2. (For example, the real offset value equal to 12 if set 6 on Offset register field)

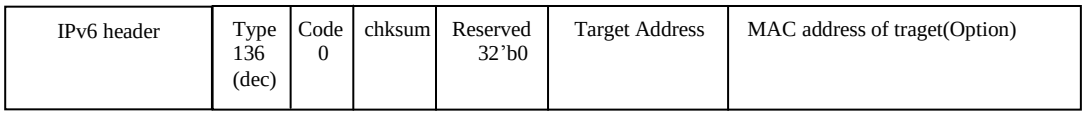
Last bytes 7 ~ 0 for each wake-up filter 7 ~ 0 also. The contents of Last Byte register must equal to the last of Byte Mask bit indicates of byte value. For example, if set Byte Mask [31:0] as 00C30003h then Byte Mask [23] is the last byte. Thus, the contents of Last byte register must equal to byte value of offset + 23.

Microsoft Windows 7 ARP and NS Offload Support

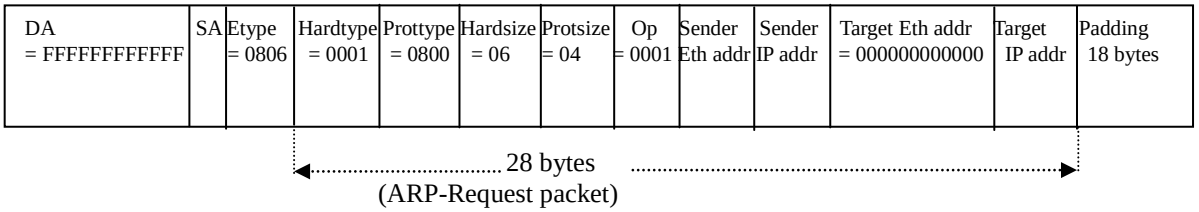
The AX88796C also supports the Microsoft Windows 7 ARP and NS offload function. The AX88796C will reply ARP and Neighbor Solicitation packets automatically before PME signal send out when the system is still in the Wake-Up mode setting with the ARP and NS protocol offload function is enabled and the good Wakeup frame is received. The AX88796C will latch the received wakeup frame's SA and SIP and filled in the reply frame's DA and DIP field plus re-calculate the good checksum value before sending out the reply packet. And the PME signal will be triggered after the ARP packet sending out from the PHY interface. The reference ARP frame format is list below. The following diagrams are the reference ARP packet format.



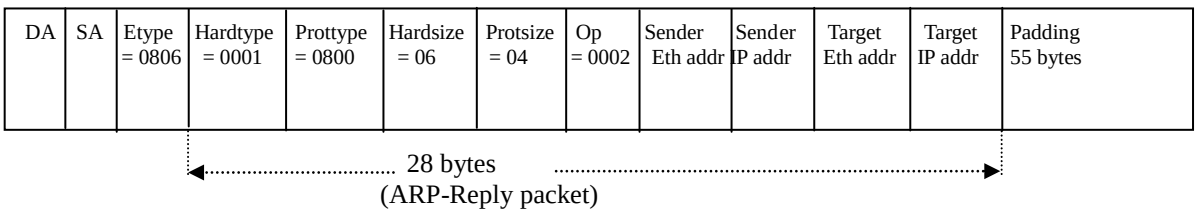
(IPv6 ICMPv6 Neighbor Solicitation packet)



(IPv6 ICMPv6 Neighbor Advertisement packet)



(ARP-Request packet)



(ARP-Reply packet)

4.7.2 Magic Packet frame

The Magic Packet technology is used to remotely wake up a sleeping or powered off PC on a network. The user can first turn on Magic Packet enable bit from the WFCR register bit [9] and set the MAC address before turn on the WFCR [5] enter the wakeup mode chip setting.
Once the AX88796C has been put into the Magic Packet Wakeup mode, it scans all incoming Ethernet frames addressed to the node for a specific data sequence, which indicates to the controller that this is a Magic Packet frame.

A Magic Packet frame must also meet the basic requirements for the Ethernet frame, such as SOURCE MAC ADDRESS, DESTINATION MAC ADDRESS (which may be the receiving station's IEEE address or a MULTICAST address which includes the BROADCAST address), and good CRC. The specific sequence consists of 16 duplications of the IEEE address of this node, with no breaks or interruptions. This sequence can be located anywhere within the packet, but must be preceded by a synchronization stream. The synchronization stream allows the scanning state machine to be much simpler.

The synchronization stream is defined as 6 bytes of 0xFF. The device will also accept a BROADCAST frame, as long as the 16 duplications of the IEEE address matches the address of the machine to be awakened. If the IEEE address for a particular node on the network is 0x112233445566, then the AX88796C scans for the data sequence
(Assuming an Ethernet Frame):

DA + SA + Misc. + FF FF FF FF FF FF 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 11 22 33 44 55 66 + Misc. + CRC.

There are no other restrictions on a Magic Packet frame. For instance, the sequence could be in a TCP/IP packet, an IPX packet, etc. The frame may be bridged or routed across the network, without affecting its ability to wake up a node at the destination of the frame.

If the AX88796C scans a frame and does not find the specific sequence shown above, it discards the frame and takes no further action. If the controller detects the data sequence, however, then it alerts the PC's power management circuitry to wake up the system.

A Wake-up frame is a special data packet containing the Ethernet address of the remote network card. Somewhere in this frame should exist a byte stream (magic sequence) composed by, at the least, 16 times the repetition of the Ethernet address and preceded by a synchronization stream of 6 bytes of 0xFF.

4.7.3 Link Change Wakeup

The AX88796C supports the PHY link change wake up event by detecting the PHY link status signal. Any time when the internal PHY's link status changes (one-to-zero or zero-to-one) and the Link-Status Change Wake-up option in the WFCR register bit [8] and bit [5] is enabled, then the AX88786C will detect a link-status change wakeup event and generate a valid PME signal to inform the host processor. When power saving function is turn on, please make sure WFTR register has at least 4 to 8 seconds delay setting to wait for the internal PHY enter the power saving mode when unplug the cable.

4.7.4 GPIO Wakeup

The AX88796C supports up to two GPIO pin Wakeup function. Only the pin GPIO0 and pin GPIO1 pin is supported this function. Please make sure the pin GPIO0 and pin GPIO1 is enabled, and the GPIO wakeup register (GPIOWCR) is configured to expected wakeup even state (edge or level triggered).

The wakeup function can be enabled if the wakeup enable bit and GPIO enable bit both set to one. And the wakeup status bit will show if the wakeup event is detected or not. The wakeup event can be configured from the GPIO Wakeup Select Register. If the Wakeup Select bit is set to 00 then the wakeup event will be triggered if detect a falling edge. If the Wakeup Select is configured to 01 then any rising edge will trigger wakeup event.

GPIO	Wakeup Enable	Wakeup Status	Wakeup Select
GPIO0	GPIOWR[0]	GPIOWR[12]	GPIOWR[5:4]
GPIO1	GPIOWR[1]	GPIOWR[13]	GPIOWR[7:6]

TAB - 10 GPIO WAKEUP CONFIGURATION TABLE

4.8 Flow Control

The AX88796C supports Full-duplex flow control using the pause control frame. It also supports half-duplex flow control using collision base of back-pressure method.

4.8.1 Full-Duplex Flow Control

The format of a PAUSE frame is illustrated below. It conforms to the standard Ethernet frame format but includes a unique type field and other parameters as follows:
The destination address of the frame may be set to either the unique DA of the station to be paused, or to the globally assigned multicast address 01-80-C2-00-00-01 (hex). The IEEE 802.3 standard for use in MAC control PAUSE frames has reserved this multicast address. The "Type" field of the PAUSE frame is set to 88-08 (hex) to indicate the frame is a MAC Control frame.

The MAC Control op-code field is set to 00-01 (hex) to indicate the type of MAC Control frame being used is a PAUSE frame. The PAUSE frame is the only type of MAC Control frame currently defined.
The MAC Control Parameters field contains a 16-bit value that specifies the duration of the PAUSE event in units of 512-bit times. Valid values are 00-00 to FF-FF (hex). If an additional PAUSE frame arrives before the current PAUSE time has expired, its parameter replaces the current PAUSE time, so a PAUSE frame with parameter zero allows traffic to resume immediately.

A 42-byte reserved field (transmitted as all zeros) is required to pad the length of the PAUSE frame to the minimum Ethernet frame size.

Preamble (7-bytes)	Start Frame Delimiter (1-byte)	Dest. MAC Address (6-bytes) **= (01-80-C2-00-00-01)**	Source MAC Address (6-bytes)	Length/Type (2-bytes) **= 802.3 MAC Control (88-08)**	**MAC Control Opcode (2-bytes) = PAUSE (00-01)**	**MAC Control Parameters (2-bytes) = (00-00 to FF-FF)**	**Reserved (42-bytes) = all zeros**	Frame Check Sequence (4-bytes)

Fig 21 PAUSE PACKET FORMAT

The AX88796C will inhibit transmit frames for a specified period of time if a PAUSE frame received and CRC is correct. If a PAUSE request is received while a transmit frame is in progress, then the pause will take effect after the transmitting is completed.

A programmable of high water free-page-count in “Flow Control Register” used to measure the water level of receive buffer. The AX88796C use XOFF / XON flow-control method to avoid missing packet if receive buffer almost full. A XON transmitting when the total of free page count equal to or less then “high water free-page-count”. A XOFF transmitting when the total of free page count equal to or greater then (“high water free-page-count” + 6 pages).

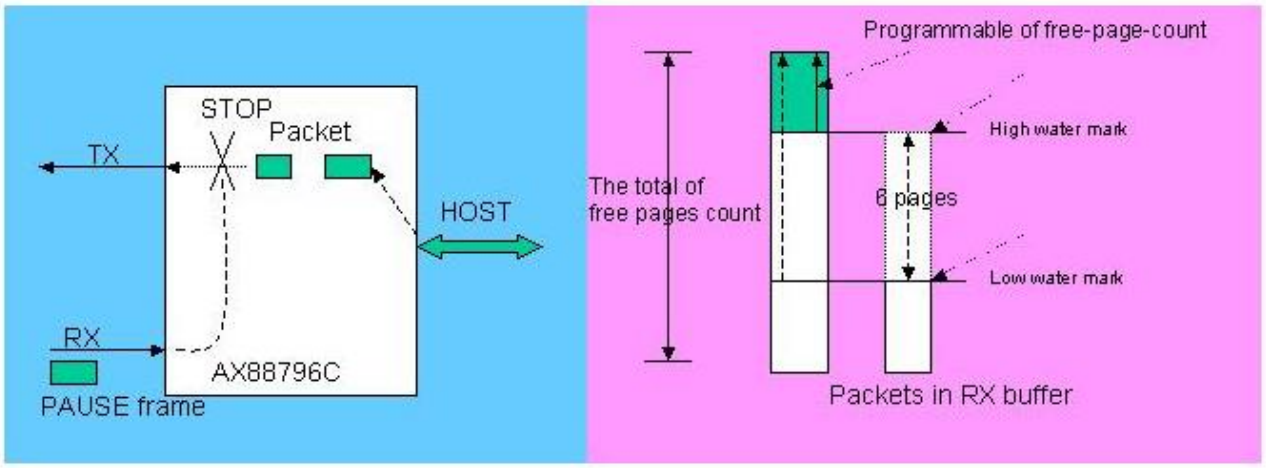


Fig 22 TX / RX FLOW CONTROL

4.8.2 Half-Duplex Flow Control

Whenever the receive buffer becomes full crosses a certain threshold level, The MAC starts sending a Jam signal, which will result in a collision. After sensing the collision, the remote station will back off its transmission. The AX88796C only generates this collision-based of back-pressure when it receives a new frame, in order to avoid any late collisions.

A programmable of "Back-pressure Jam Limit count" (Offset 17h) is used for avoid HUB port partition due to many continues of collisions. The AX88796C will reset the "Back-pressure Jam Limit count" when either a transmitted or received frame without collision. A back-pressure leakage allow when senses continue of collisions count up to "Back-pressure Jam Limit count", it will be no jamming one of receive frame even receive buffer is full.

4.9 Auto-Polling Function

The AX88786C supports PHY management function through the internal serial MDIO/MDC interface. That is, the AX88786C can access related PHY registers via MDIO/MDC interface after power on reset. The AX88786C will periodically and continuously poll and update the link status and link partner's ability which include speed, duplex mode, and 802.3x flow control capable status of the connected PHY devices through MDIO/MDC serial interface. All the polling status will be automatically update in the register MACCR RE [0], FD[1], Speed[2] and RFC/TFC[4:3] location if the auto-polling function is enable in the PCR register bit [0].

The AX88796C also supports indirect read or write internal PHY register through the local bus interface. The MDIOCR and MDIODR registers provide the read or write setting to access the internal PHY register. Please reference these related register information for further detail.

4.10 Mixed Endian Byte Ordering

The AX88796C supports “Big-“or “Little-endian” processor with 16-bit bus interfaces. The AX88796C provides mixed Endian byte ordering function for user configuration. The following table is to summarize of mixed Endian byte ordering configuration.

Additionally, please refer to Byte Order Register (BOR), for additional information on status indication on big- or little-endian modes. The AX88796C provides two bytes of fixed patterns for user confirming the byte lane order configuration. The following table shows the fixed pattern on Byte1 and Byte0. These fixed patterns can be used to determine the byte lane ordering of current configuration. The users can write one to BOR to change the byte ordering.

Fixed pattern on Byte Order register (read offset 02h Page 0)	Fixed Value
Data [15:0]	0x1234

Fig 23 FOUR FIXED PATTERNS FOR BYTE LANE TEST

The AX88796C also supports TX/RX packet data swapping function. The FER register bit [8] is the packet data word swap function enable control bit. When enabled this word swap function then the upper word will swap with the lower word packet data.

The FER register bit [9] is the packet data byte swap enable function. When enabled this byte swap function by setting one to this bit, then the AX88796C will enable byte swap function on both RX and TX packet data buffer and packet data bit [7:0] will swap to bit [15:8]. The packet data swapping function intends to convert the packet data when the host CPU is processing the packet in different Endian type purpose.

4.11 EEPROM Interface

The AX88796C can optionally load its MAC address from an external serial EEPROM. If a properly configured EEPROM is detected by the AX88796C at power-up, hard reset or host set a reload EEPROM request, the constants of EEPROM data will be auto loading to internal memory automatically. A detailed explanation of the EEPROM data format in section 3.0 "EEPROM Memory Mapping". After auto load EEPROM completed, the MAC address will be auto-loaded into the MACASR0~MACASR2 registers (Page3 Offset 02h ~ 06h) and then AX88796C will know its MAC address. In addition to have EEPROM auto load the MAC address, the Host driver can also manually configure the AX88796C MAC address by writing the MACASR0~MACASR2 registers.

The AX88796C EEPROM use 3 PINs to connect to a most "93C56/66" type EEPROM configured for x16-bit operation. A connect diagram as below

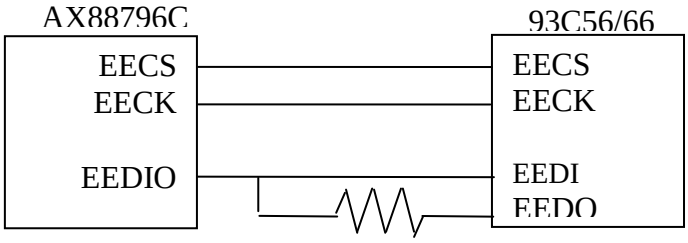


Fig 24 EEPROM CONNECTIONS

After EEPROM loader has finished reading the MAC after power-on, hard reset or host set a reload EEPROM request (CR page3 offset 0Ch), the Host is free to perform EECS, EECK and EEDIO as General Purpose I/O pin.

4.12 Power Management Function

The AX88796C supports power saving modes to allow applications to minimize power consumption. There is one normal operation power state and there are two power saving states: Power Saving Mode 1 (PS1) and Power Saving Mode 2 (PS2). The "Power Management Register" (Page0 Offset 0Ch) controls those of power management modes. In WOL state, the AX88796C supports Wake on LAN function. In Sleep state, the AX88796C will turn off almost all function block power supply and gated clocks to minimize power consumption. In cable-off power saving 1 and 2 mode the AX88796C will turn off the different functional blocks within the internal PHY to reduce cable off power consumption. After wakeup event, the "Power Management Register" will be cleared and stay at normal operation power state. When the AX88796C is in Sleep mode, the host CPU can write "Host Wake Up Register" (Offset 1Eh) for non-SPI interface or set AX88796C SPI "ABh Exit Power Down (S3)" instruction for SPI interface to return the AX88796C to the normal operation state. The AX88976C Power consumption can be reduced to different level by disabling the different clocks under different power saving mode as outlined in table as below.

The AX88796C BLOCK	Normal Operation	PS1	PS2	WOL	Sleep Mode
Internal 100MHz clock	On	On	Off	On	Off
MAC Rx/Tx clock	On	Off	Off	Off	Off
TX Driver	On	Periodic on	Off	Off	Off
Power Management Block	On	On	On	On	Off
PHY Osc. 25MHz clock	On	On	Off	On	Off

TAB - 11 POWER MANAGEMENT STATUS

The AX88796C support the following power saving states:
1. PS1: Internal Ethernet PHY enter Power Saving state 1
2. PS2: Internal Ethernet PHY enter Power Saving State 2
3. WOL: Internal Ethernet PHY enters Wake-On-LAN power saving State, link to 10MHz to reduce power consumption if the remote PHY support 10M speed.
4. Sleep Mode: Host force the AX88796C enters the sleep state and wait for host wake-up command. The internal Ethernet PHY is in power down state.

NOTE; When TCLK is configured to provide reference clock output, Please make sure power saving mode is either disabled or only set on Power Saving Mode 1 (PS1) mode cause the power saving function will gated the output reference clock when turn on.

4.12.1 Hardware-detect Cable-Off Power Saving Mode (PSCR [4]=0, default)

The AX88796C power management module supports the hardware cable-off power saving function when PSCR [4] software power-saving function is disabled. When the AX88796C hardware detects the cable-off event on Ethernet PHY interface, then power management module will check PSCR [2:0] register setting and automatically change the internal PHY to the correspondent power saving state to reduce the power consumption. If the PSCR [2:0] is set to 001 and the cable-off is detected then the AX88796C will enter Power Saving Mode 1 (PS1) state. If PSCR [2:0] is set to 010 and cable-off is detected then the AX88796C will enter Power Saving Mode 2 (PS2) state. When the Ethernet cable is plug in then power management will change back to the normal ready state.

The AX88796C will go back to Normal Operation state when internal PHY detect cable plug-in event from PS1 and PS2 state.

4.12.2 Software Control Cable-Off Power Saving Mode (PSCR [4]=1)

The AX88796C supports software control power saving function for Power Saving Mode 2 (PS2). When PSCR [4] is set to one, the host software got the fully control of the internal power saving state transition; the host also needs to set MACCR [6] to enable Software Cable-Off Power Saving Interrupt.

The AX88796C will report the cable-off interrupt to the external host through IRQ pin. The host can then program PSCR [2:0] register value to 010 to force the AX88796C enters PS2 state.

When the cable plug-in event detected, the host interface can issue a resume command by writing “Host Wake Up Register” (Offset 1Eh) for non-SPI interface or setting AX88796C SPI “ABh Exit Power Down (S3)” instruction for SPI interface to return the AX88796C to the normal operation state.

4.12.3 Sleep Mode

The host can write one to WFCR [4] sleep mode bit and the AX88796C will enter the sleep mode deep power saving state with Ethernet PHY power down and internal clock shut down. The host interface can issue a resume command by writing "Host Wake Up Register" (Offset 1Eh) for non-SPI interface or setting AX88796C SPI "ABh Exit Power Down (S3)" instruction for SPI interface to return the AX88796C to the normal operation state. Please check the device ready on PSR [7] for non-SPI interface and check the Device Ready bit of AX88796C SPI "05h Read Status" instruction for SPI interface to make sure the chip is in ready state because it will take a few ms for PHY and clock to recover back. It will take about 160ms for the AX88796C internal PHY back to device ready state after the host interface issue the resume command to exit the sleep mode. The software driver can either polling the AX88796C device ready status (PSR) for non-SPI interface, or polling the Device Ready bit of SPI "05h Read Status" register for SPI interface or wait about 160ms before the normal operation.

4.12.4 Wake-On-LAN Power Saving Mode

The AX88796C supports the power saving function even the chip is in Wake-On-LAN mode state with WFCR [5] is set to one. The AX88796C can enter Wake-On-LAN power saving mode through the following two ways:

1. Hardware-enabled power saving control:
   When the AX88796C is in WOL state and the Ethernet cable is unplugged and PSCR [5] is pre-configured to one.
2. Software-enabled power saving control:
   When software detect link done on WOL mode then software can write one to PSCR [5] to turn on power saving mode

When the AX88796C enter the WOL power-saving mode, the internal Ethernet PHY will check remote PHY's speed ability and try link to 10MHz speed in order to reduce the power consumption when waiting the wake up event to be triggered.

4.13 Checksum Offload Function

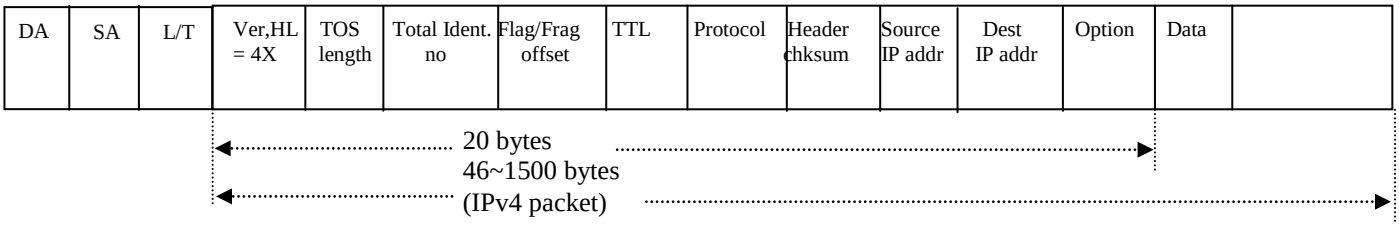
The AX88796C Checksum Offload function supports Layer 3 IPv4, Ipv6 protocol and Layer 4 TCP, UDP, ICMP, ICMPv6 and IGMP protocol include receive packet checksum value check and transmit packet checksum calculation and replacement offload CPU loading.

The detail of the AX88796C Checksum Offload Function list below:

- IP header parsing, including Ipv4 and Ipv6
- Ipv4 header checksum check and generation (There is no checksum field in Ipv6 header)
- Version error detecting on RX direction for IP packets with version not equal to 4 or 6
- Detect RX IP packet header checksum error
- TCP and UDP checksum check and generation
- ICMP, ICMPv6 and IGMP message checksum check and generation

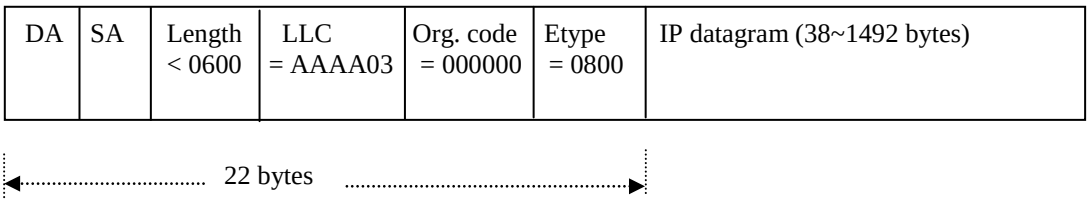
The AX88796C supports the following Layer 2 Protocols checksum offload processing.

1. Ethernet II Encapsulation (RFC894)



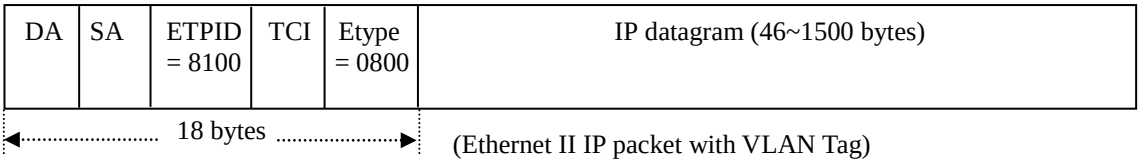
2. IEEE 802.2/802.3 SNAP Encapsulation (RFC 1042)

This Ipv4 packet format is the same as above except that the Ipv4 packet length has changed to 38~1492 bytes instead.



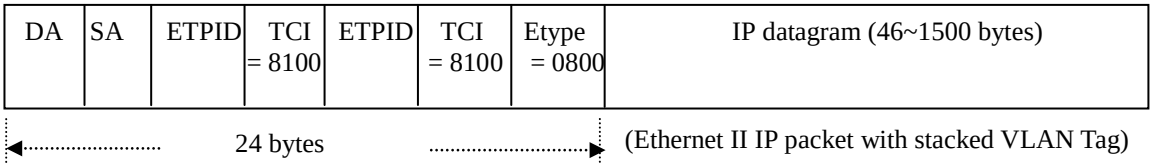
3. **Ethernet II Encapsulation (RFC894) with VLAN-tagge**d

This Ipv4 packet format is the same as above without VLAN-tagged case. In other words, in addition to DA, SA, and Etype bytes in the MAC frame, there are the VLAN Tag byes: ETPID and TCI.



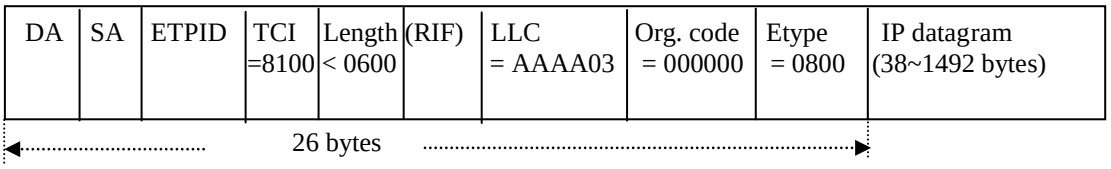
4. Ethernet II Encapsulation (RFC894) with stacked VLAN-tag (QinQ)

This Ipv4 packet format is the same as above without VLAN-tagged case. There are two VALN tags, including ETPID and TCI field (stacked VLAN).



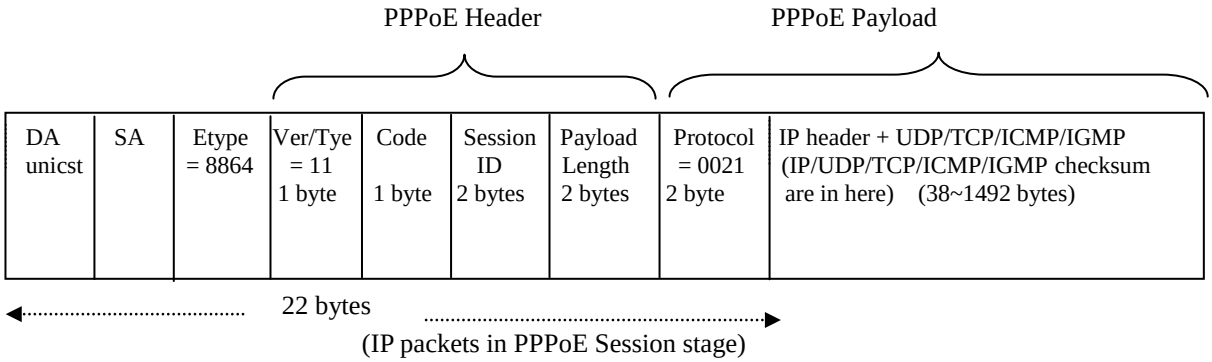
5. IEEE 802.2/802.3 SNAP Encapsulation (RFC 1042) with VLAN-tagged

This Ipv4 packet format is the same as above without VLAN-tagged case and the packet length is 38~1492 bytes long. So in addition to DA, SA, Length, LLC, Org. code, and Etype bytes in MAC frame, the L2_Engine shall also remove the VLAN Tag byes: ETPID, TCI, and RIF bytes, before sending the packet towards L3_Engine.



6. PPPoE Encapsulation with VLAN-tagged

PPPoE frames with (Etype = 8864 and Protocol = 0021) will have their IP/UDP/TCP/ICMP/IGMP checksums checked by L3/4 Engine. All other PPPoE frames with (Etype = 8863) or (Etype = 8864 and Protocol != 0021) will be treated as non-IP packets and passed to the software.



Layer 3 Processing

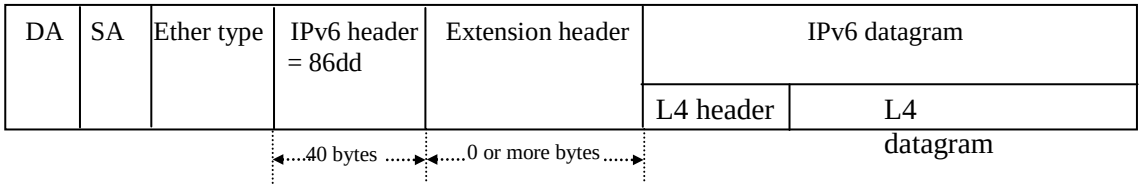
The Layer 3 engine includes checksum check and generation, header parsing, functions in Ipv4 and header parsing function in Ipv6. The checksum engine will calculate the checksum of Ipv4 header and compare it with received checksum value. The checksum engine is used for pseudo header checksum calculation in Ipv6. The block also calculates the checksum for the transmitted IP header. The header parser will parse the Ipv4 header and capture some fields into registers for further processing by other blocks. In order to speed up the L4 checksum calculation and reduce the latency, L3 engine will control the L4 engine to pre-calculate the L4 pseudo header (protocol, SIP and DIP).

The following received IP packets will be discarded by the L3 Engine.

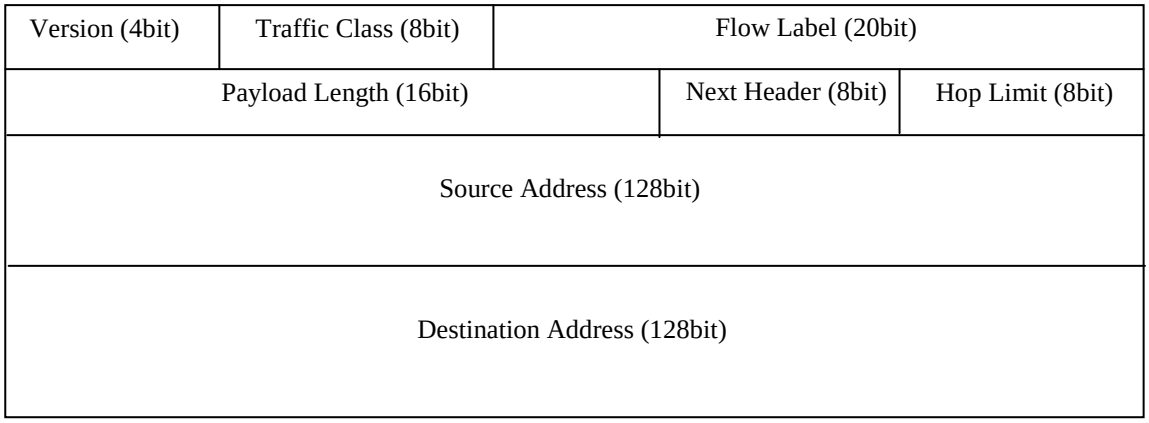
- Ethernet type is 0800 but IP version not equal to 4
- Ethernet type is 86dd but IP version no equal to 6
- Ipv4 header checksum error

Ipv6 frame

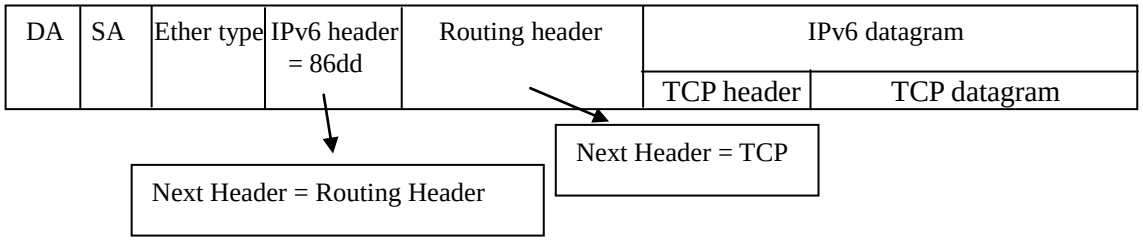
The L3 engine supports Ipv6 frame, the Ipv6 parser can indicate the correct start point of L4 frame and pre-calculate the pseudo header check sum for L4 packet.



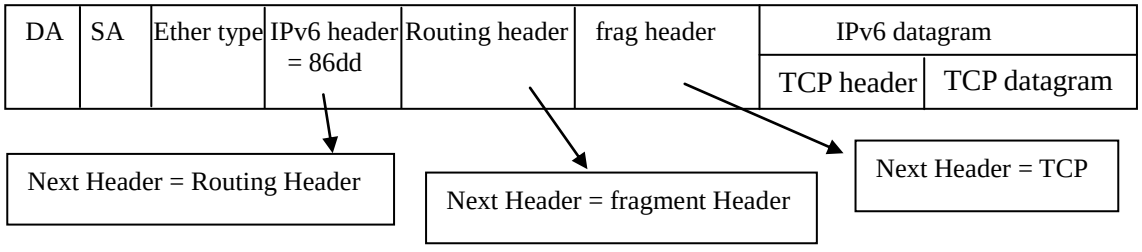
IPv6 packet format



IPv6 header format



IPv6 TCP packet with Routing Header



IPv6 TCP packet with Routing Header and Fragment Header

Fig 25 IPv6 PACKET FORMAT

4.14 GPIO Function

The AX88796C has an optional feature to support up to four GPIO functions through multi-functional pin out when some of the functional pin is not enabled. Each GPIO pin is able to trigger interrupt event and only GPIO0 and GPIO1 support wakeup function and pass PME event to external host.

GPIO	GPIO Enable	Input	Output	Output Enable	Interrupt Enable	Interrupt Mask	Interrupt Status	Interrupt Select
GPIO0	GPIOER[0]	GPIOER[4]	GPIOER[8]	GPIOER[12]	GPIOCR[0]	GPIOCR[12]	GPIOCR[8]	GPIOCR[4]
GPIO1	GPIOER[1]	GPIOER[5]	GPIOER[9]	GPIOER[13]	GPIOCR[1]	GPIOCR[13]	GPIOCR[9]	GPIOCR[5]
GPIO2	GPIOER[2]	GPIOER[6]	GPIOER[10]	GPIOER[14]	GPIOCR[2]	GPIOCR[14]	GPIOCR[10]	GPIOCR[6]
GPIO3	GPIOER[3]	GPIOER[7]	GPIOER[11]	GPIOER[15]	GPIOCR[3]	GPIOCR[15]	GPIOCR[11]	GPIOCR[7]

TAB - 12 GPIO CONFIGURATION TABLE

When GPIO Enable is set to one, GPIO pin will be configured to output pin and pass output data from register to pin if the correspondent Output Enable is set to one. Otherwise, if output enable is set to zero then GPIO pin will consider as input pin and pass the pin data save to input register.

The GPIO pins support the interrupt function if the interrupt enable bit and GPIO enable bit both set to one. The Interrupt Select register will define interrupt polarity active high if set to one or active low if set to zero. The interrupt mask register is able to mask the interrupt if the mask bit is set to one. The interrupt status value can read out from the Interrupt Status register and write one to clear the interrupt status bit.

5.0 SPI Interface

5.1 Introduction

The AX88796C SPI slave module provides the interface between the host's SPI master and the AX88796C's local bus interface. It is compatible with the SPI serial bus interface. The host SPI can access the whole AX88796C's internal registers space, TX FIFO and RX FIFO through SPI master commands.

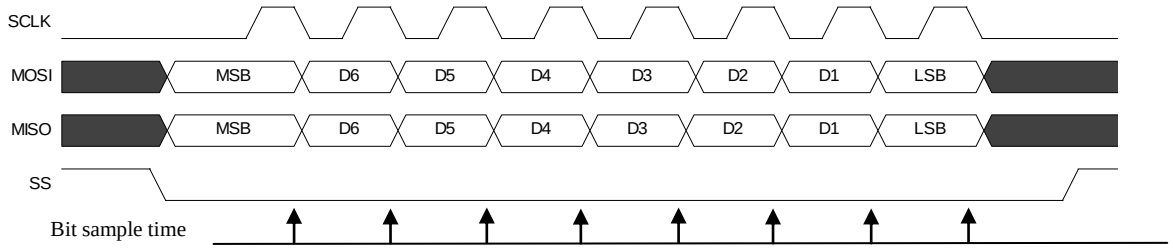
5.2 Features

- SPI compatible serial bus interface
- Supports mode 0 and mode 3 timing modes
- Supports maximum operation frequency up to 40MHz for all SPI access modes
- Supports special command to clear the SPI mode status bits.
- Supports the "Exit power down" command to wake up the AX88796C from the power saving or WOL suspend mode.
- Supports the SPI interrupt
- Supports register/status odd byte(s) access.

5.2.1 Mode Access

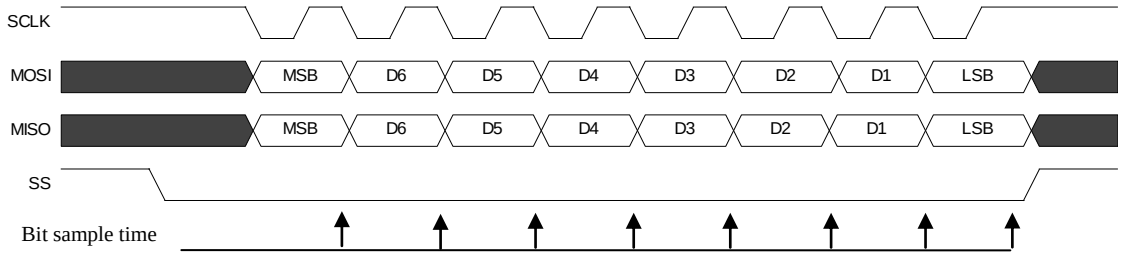
The AX88796C supports mode 0 and mode 3 SPI timing modes.

Mode 0: Timing diagram (the access length is based on command)



Note: SPI CLK (SCLK) pin needs external pull-down resistor and SSn pins need external pull-up resistor in Mode 0, SPI master mode.

Mode 3: Timing diagram. (the access length is based on command)



Note: SPI CLK (SCLK) pin needs external pull-up resistor and SSn pins need external pull-up resistor in Mode 3, SPI master mode.

Fig 26 SPI TIMING DIAGRAM

5.3 SPI Module Operation

To access the TX FIFO and RXFIFO, the AX88796C SPI data transfer only supports the word access (16 bits). If there is a non-word data transfer for the TX FIFO and RX FIFO access, then the SPI slave module will issue an interrupt and raise a non-Word access flag to the SPI interrupt status register to indicate this error. For the internal register read or write access, the AX88796C can read or write all internal register's odd bytes.

There is a SPI status read command "05H" to read out the internal SPI status and the AX88796C interrupt status. The status output order are: the AX88796C status first (interrupt status) Low byte-> and the AX88796C status (interrupt status) High byte-> and the SPI status byte last.

If the SPI slave module receives a un-define SPI command, the AX88796C SPI slave module will issue an interrupt and raise the un-define command access flag in the SPI interrupt status register to indicate this error.

5.4 Instruction Set Summary

5.4.1 SPI Mode Instruction Table

Instruction	Description	Op code	Address Cycles	Dummy Cycles	Data Cycles	Note
03h Read Data	Read from register Compression = 0	03h	8	16	8	
	Read from register Compression = 1	03h	8	8	8	
D8h Write Register	Writ Register compression=0	D8h	8	X	8	
0Bh Fast Read Data	RXQ Read Compression = 0	0Bh	X	32	16-∞	
	RXQ Read Compression = 1	0Bh	X	8	16-∞	
02h Page Program write	TXQ Compression =0	02h	X	24	16-∞	
	TXQ Compression =1	02h	X	X	16-∞	
38h Enable QCS Mode	Enter QCS mode	38h	X	X	X	
FFh Reset Mode bit	Reset mode bit to abort register random read	FFh	X	X	X	
05h Read Status	Read Status	05h	X	X	24	
ABh Exit Power Down(S3)	Exit Power Down	ABh	X	X	X	
B2h Bi-direction Fast read and program	RXQ Read and TXQ program Compression =0	B2h	X	32	16~∞	
	RXQ Read and TXQ program Compression =1	B2h	X	8	16~∞	

X: This parameter is not required.

TAB - 13 SPI MODE INSTRUCTION TABLE

NOTE: The RXQ means the RX FIFO or the RX memory access within the AX88796C core and the TXQ means the TX FIFO or the TX memory access.

5.5 Commands Waveform

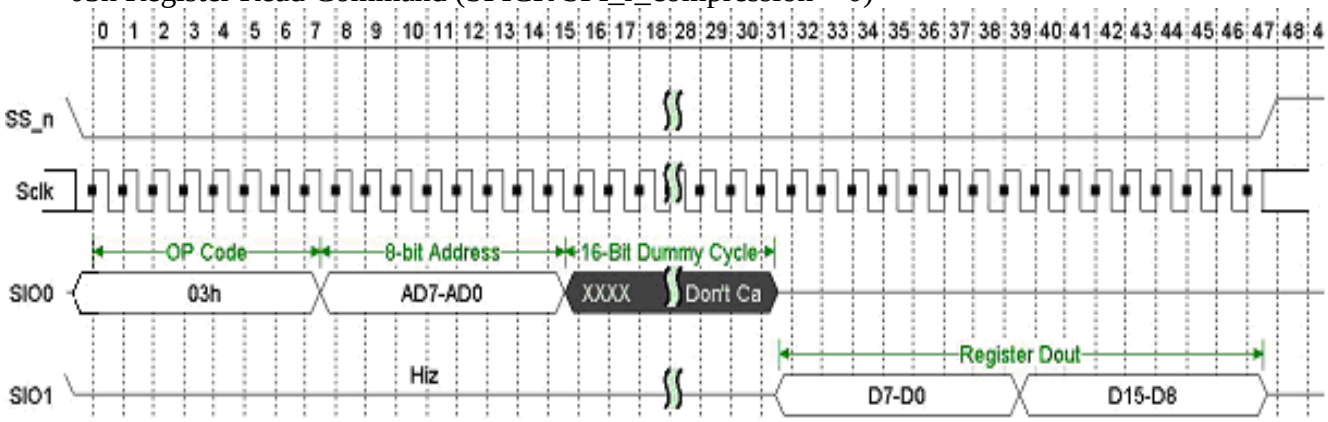
5.5.1 SPI Mode

NOTE :

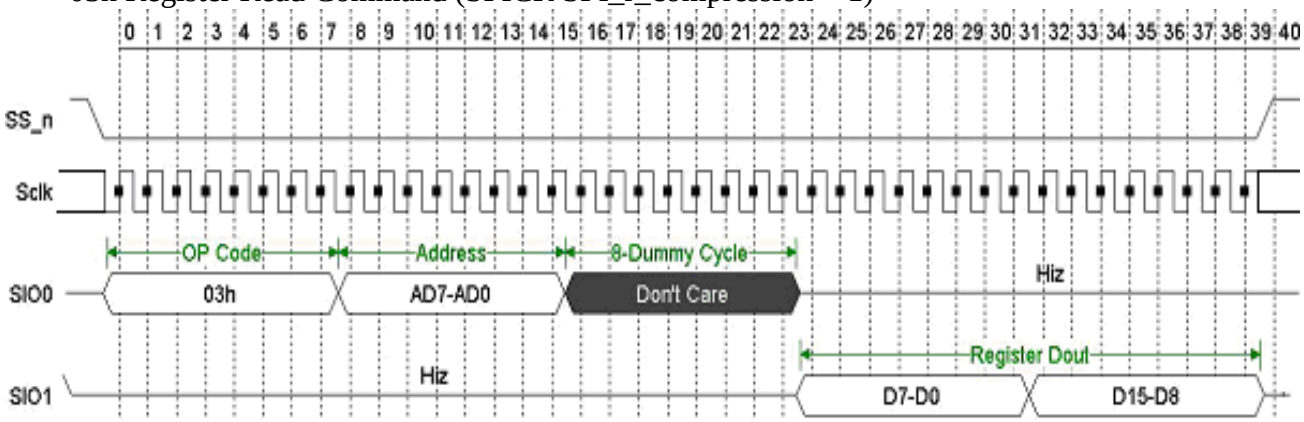
Signal	Pin Name
SIO0	MOSI
SIO1	MISO
SS_n	SSn
Sclk	SPI_CLK

5.5.1.1 Read command

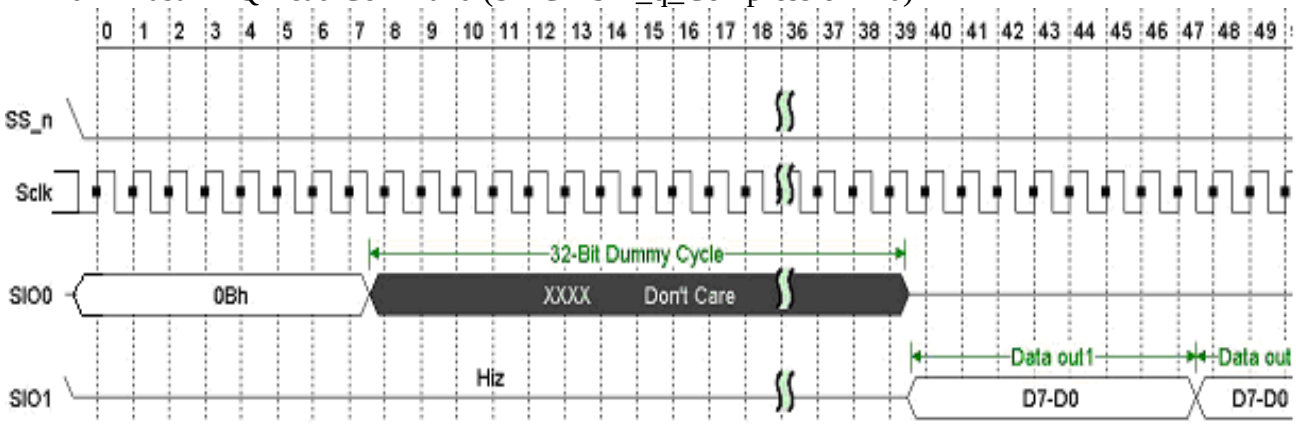
03h Register Read Command (SPICR SPI_r_compression = 0)



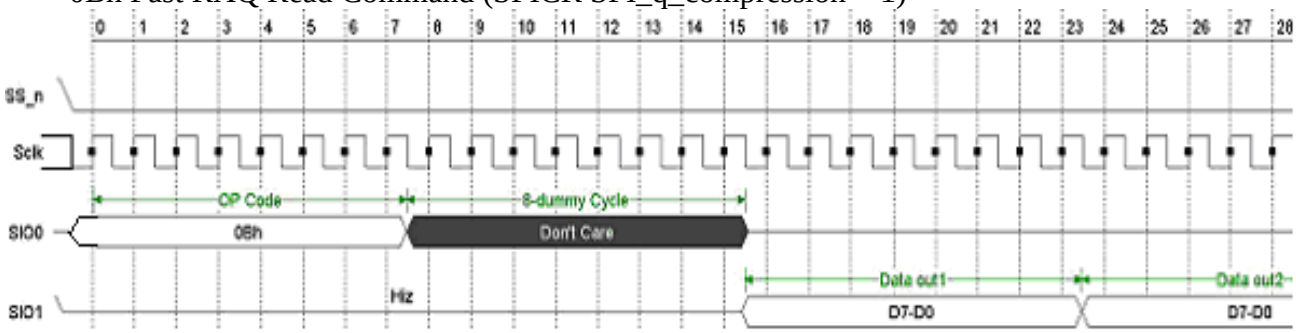
03h Register Read Command (SPICR SPI_r_compression = 1)



0Bh Fast RXQ Read Command (SPICR SPI_q_Compression = 0)



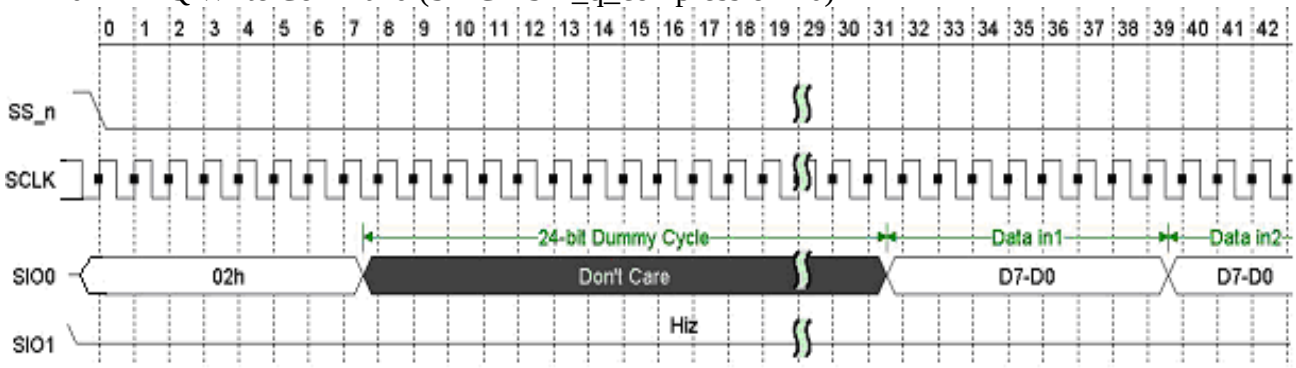
0Bh Fast RXQ Read Command (SPICR SPI_q_compression = 1)



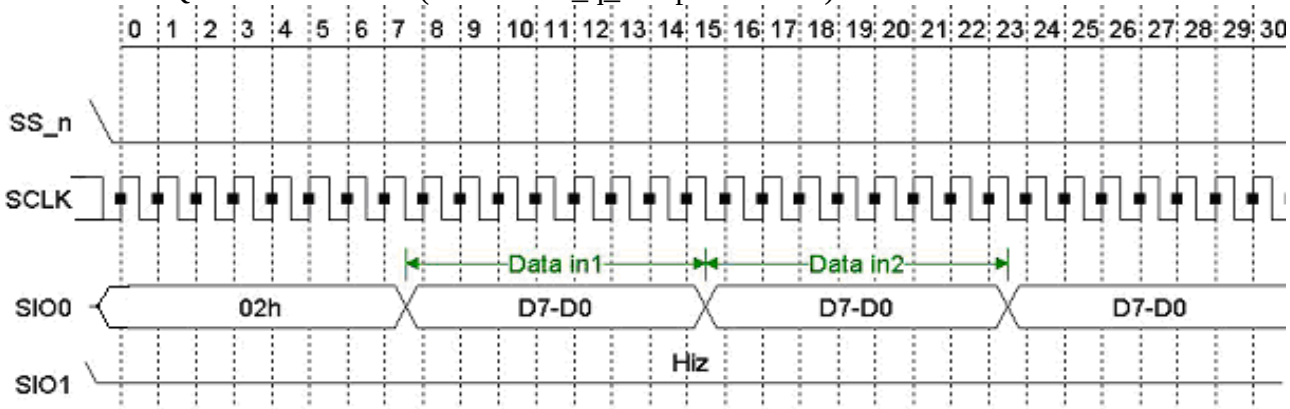
5.5.1.2 Write command

D8h Register Write Command

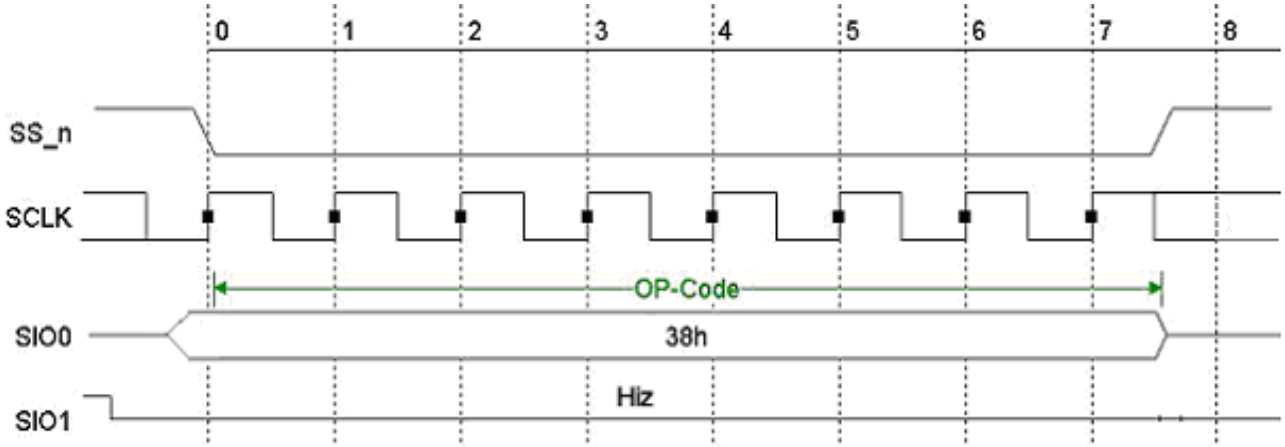
02h TXQ Write Command (SPICR SPI_q_compression =0)



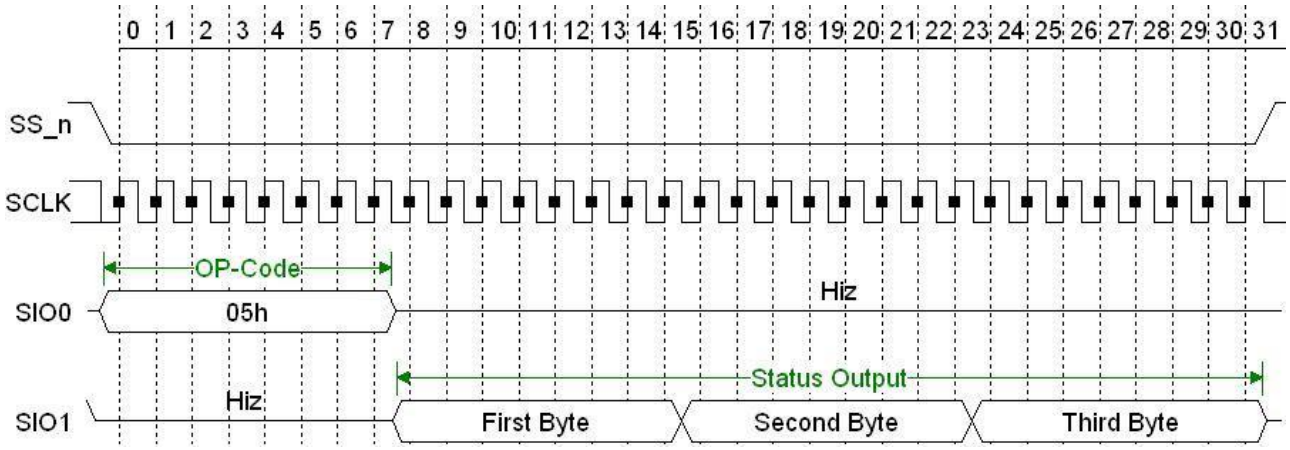
02h TXQ Write Command (SPICR SPI_q_compression =1)



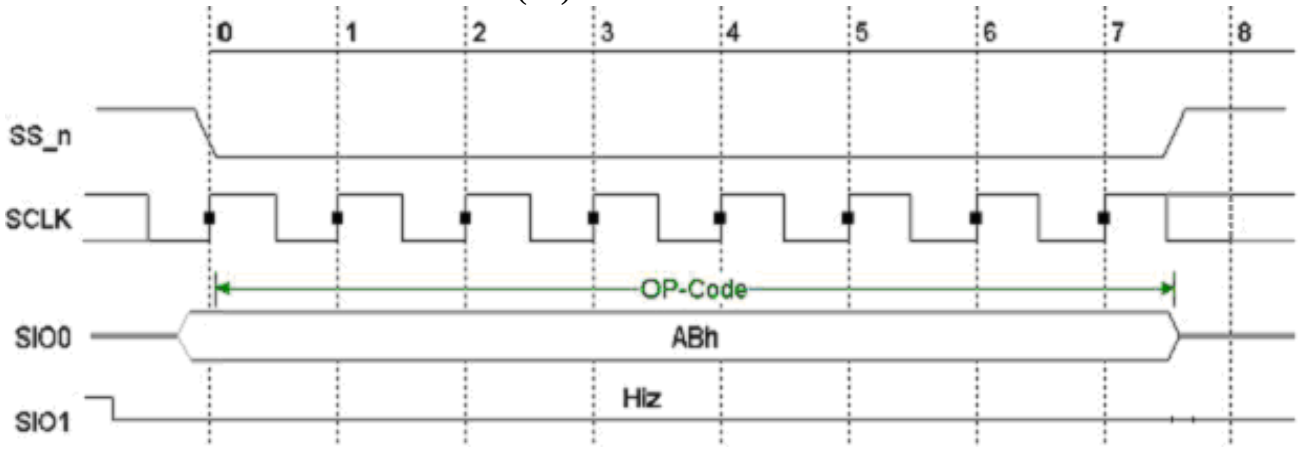
38h Enable QCS Mode



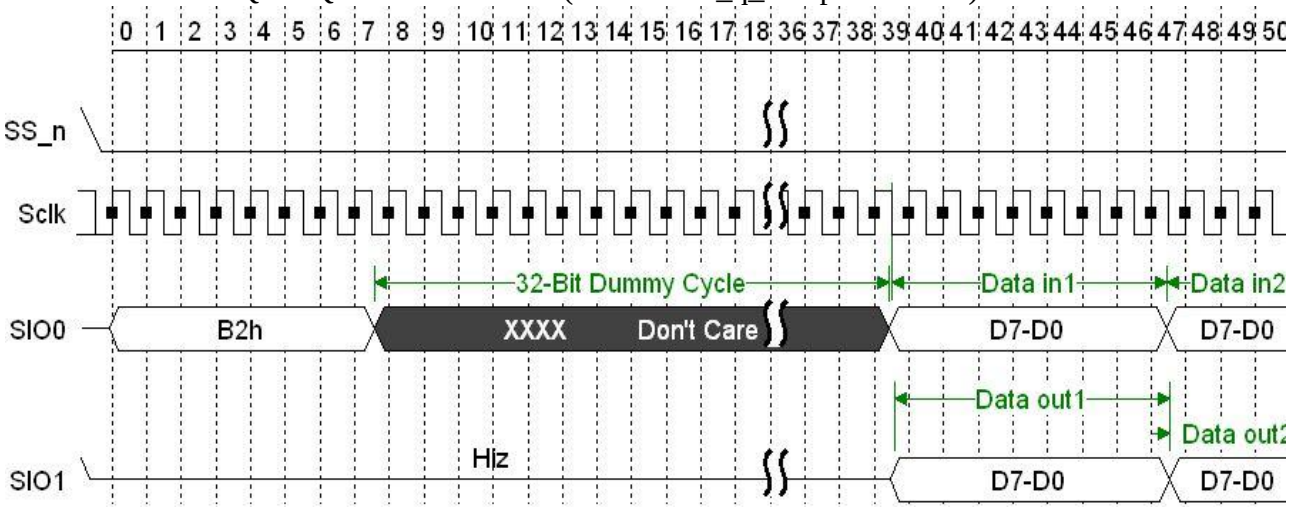
05h Read SPI Status Command



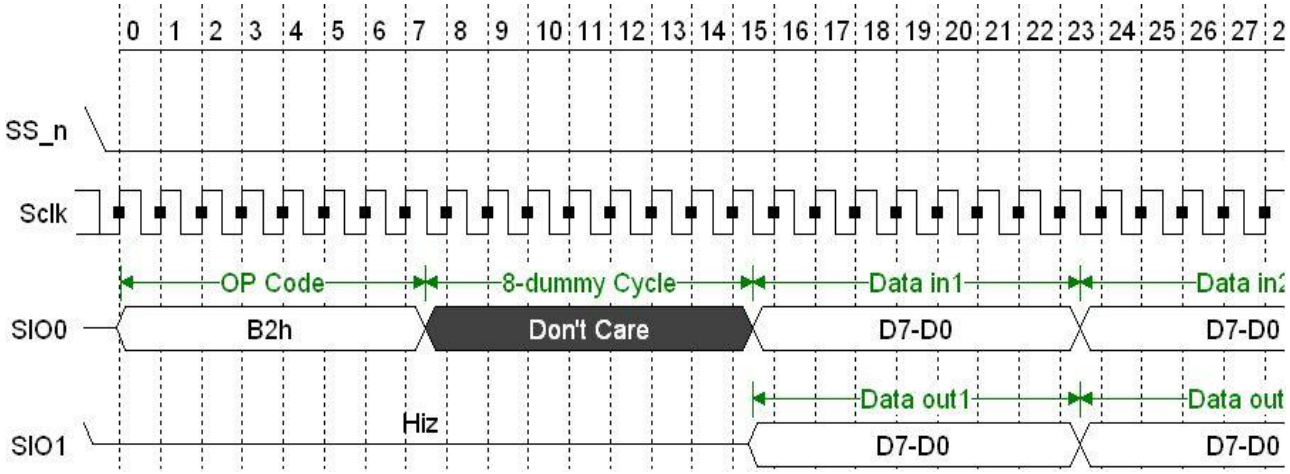
ABh Exit Power Down Command (S3)



B2h Fast RXQ/TXQ Write Command (SPICR SPI_q_compression =0)



B2h Fast RXQ/TXQ Write Command (SPICR SPI_q_compression =1)



5.6 SPI Status Access

When the host SPI Master use the status read command “05h” to access the AX88796C interrupt status and SPI status. The status output order are: the AX88796C status come out first (interrupt status, Low byte)-> and the AX88796C status (interrupt status, High byte)-> and the SPI status byte last. For the interrupt status, please reference the register page 0 offset 0x06 for detail description. For the SPI status content, please check the following table.

Bit	Name	Default Value	R/W	Description
[0]	TXQ_IC/ RXQ_IC	0	R	TXQ initial complete/RXQ initial complete: Complete SPI TXQ or RXQ data path clear. If SPI slave get the TXQ/RXQ initial signal from TXQ/RXQ, SPI will clear TX/RX data paths. 1: SPI get TXQ/RXQ initial and clear TX/RX data path content already. 0: SPI didn’t get TXQ/RXQ initial signal or it is still doing TX data path clear.
[1]	Reserved	0	R	Reserved
[6:2]	PMM_ST[4:0]	00000	R	Power Management Module Status 00001: Chip Reset State 00010: Wait State 00011: Device Ready State (Normal Operation) 00100: PS1 State (Cable-off) 00101: PS2 State (Cable-off) 00111:Wake-On-LAN State 01000 PS1 and Wake-On-LAN State (Cable-off) 01001: PS2 and Wake-On-LAN State (Cable-off) 01010: Sleep Mode 01011: PHY in Reset State 10000: Software force in PS1 State 10001: Software force in PS2 State
[7]	Device Ready	0	R	Device Ready Status. 1: Device ready(register access available) 0: Device not ready yet(register access unavailable)

TAB - 14 SPI STATUS TABLE

6.0 Registers Description

6.1 Internal Register Mapping Table

All the AX88796C internal registers are 16-bit wide. The Offset 0x02 to 0x1D mapped into page0 ~ page7, which are selected by PS (Page Select) in the Page Select Register (PSR, Offset 0x00). The Offset 0x1E and 0x1F through page 1 to page 7 are shared registers for chip level control purpose.

Offset	Page0	Page1	Page2	Page3
0x00	PSR 0x8040 (Register Default Value)			
0x02	BOR 0x1234	RPPER 0x0000	ICR 0x0000	MACASR0 0x0000
0x04	FER 0x0043		PCR 0x1002	MACASR1 0x0000
0x06	ISR 0x0000		PHYSR 0x05FF	MACASR2 0x0000
0x08	IMR 0xFFFF	MRCR 0x2000	MDIODR 0x0000	MFAR01 0x0000
0x0A	WFCR 0x0000	MDR 0x0000	MDIOCR 0x0000	MFAR23 0x0000
0x0C	PSCR 0x1820	RMPR 0x0101	LCR0 0x0204	MFAR45 0x0000
0x0E	MACCR 0x0318	TMPR 0x0101	LCR1 0x1508	MFAR67 0x0000
0x10	TFBFCR 0x001F	RXBSPCR 0xC000	IPGCR 0x120C	VID0FR 0x0000
0x12	TSNR 0x0040	RXMCR 0x0900	CRIR 0x0000	VID1FR 0x0000
0x14	RTDPR 0x0000		FLHWCR 0x4224	EECSR 0x0000
0x16	RXBCR1 0x0000		RXCR 0x0001	EEDR 0xFFFF
0x18	RXBCR2 0x4000		JLCR 0x043F	EECR 0x2000
0x1A	RTWCR 0x0000			TPCR 0x1500
0x1C	RCPHR 0x0000		MPLR 0x0600	TPLR 0x0048
0x1E	Remote Wakeup Register (RWR) 0x0000			

Offset	Page4	Page5	Page6	Page7
0x00	PSR 0x8040			
0x02	GPIOER 0x0000	WFTR 0x0000	WF2CR 0x0000	WF6BMR0 0x0000
0x04	GPIOCR 0xF000	WFCCR 0x0000	WF2OBR 0x0000	WF6BMR1 0x0000
0x06	GPIOWCR 0x0000	WFCR03 0x0000	WF3BMR0 0x0000	WF6CR 0x0000
0x08		WFCR47 0x0000	WF3BMR1 0x0000	WF6OBR 0x0000
0x0A	SPICR 0x0C00	WF0BMR0 0x0000	WF3CR 0x0000	WF7BMR0 0x0000
0x0C	SPIISMR 0xFF00	WF0BMR1 0x0000	WF3OBR 0x0000	WF7BMR1 0x0000
0x0E		WF0CR 0x0000	WF4BMR0 0x0000	WF7CR 0x0000
0x10		WF0OBR 0x0000	WF4BMR1 0x0000	WF7OBR 0x0000
0x12	COERCR0 0x0000	WF1BMR0 0x0000	WF4CR 0x0000	WFR01 0x0000
0x14	COERCR1 0x0000	WF1BMR1 0x0000	WF4OBR 0x0000	WFR23 0x0000
0x16	COETCR0 0x0000	WF1CR 0x0000	WF5BMR0 0x0000	WFR45 0x0000
0x18	COETCR1 0x0000	WF1OBR 0x0000	WF5BMR1 0x0000	WFR67 0x0000
0x1A		WF2BMR0 0x0000	WF5CR 0x0000	WFPC0 0x0000
0x1C		WF2BMR1 0x0000	WF5OBR 0x0000	WFPC1 0x0000
0x1E	Remote Wakeup Register (RWR) 0x0000			

6.1.1 Page 0 Offset 0x00: Page Select Register (PSR)

<table>
<tr><th>Bit</th><th>Name</th><th>Default Value</th><th>R/W</th><th>Function</th></tr>
<tr><td>[2:0]</td><td>PS[2:0]</td><td>000</td><td>RW</td><td>Page Select
The three bits select which register’s page is to be accessed.
<table>
<tr><th>PS[2]</th><th>PS[1]</th><th>PS[0]</th><th>Page Number</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Page 0 (Default Page)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Page 1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Page 2</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Page 3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Page 4</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Page 5</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Page 6</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Page 7</td></tr>
</table></td></tr>
<tr><td>[3]</td><td>AddressShifter</td><td>0</td><td>RW</td><td>Shift SA3~SA0 to SA4~SA1 for address decode process.</td></tr>
<tr><td>[6:4]</td><td>Bus Setting</td><td>100</td><td>R</td><td>
<table>
<tr><th>Bus Setting</th><th>Bus Function</th></tr>
<tr><td>000</td><td>8-bit SRAM-like bus (AEN should be pull-low.)</td></tr>
<tr><td>001</td><td>8-bit Address/Data multiplexed bus (AEN=1 address cycle, AEN=0 data cycle).
Pin SD7 ~ SD0 is used. SD5 ~ SD0 represent address bus when AEN =1. SD7 ~SD0 represent data bus when AEN=0. CSN should be low when the AX88796C is selected.</td></tr>
<tr><td>010</td><td>Reserved</td></tr>
<tr><td>011</td><td>MCS-51 (805x) (PSEN/AEN active high)</td></tr>
<tr><td>100</td><td>16-bit SRAM-like bus (AEN should be pull- low.)</td></tr>
<tr><td>101</td><td>16-bit Address/Data multiplexed bus (AEN=1 address cycle, AEN=0 data cycle)
Pin SD15 ~ SD0 is used. SD5 ~ SD0 represent address bus when AEN =1. SD0 ~SD15 represent data bus when AEN=0. CSN should be low when the AX88796C is selected.</td></tr>
<tr><td>110</td><td>SPI Mode (AEN unused and can be pull-low if GPIO mode is unused.)</td></tr>
<tr><td>111</td><td>16-bit local bus with byte write enable (Renesas SHx style, AEN = low byte SD7~SD0 enable, WRn = low byte SD15 ~ SD8 enable)</td></tr>
</table></td></tr>
<tr><td>[7]</td><td>Device_Ready</td><td>0</td><td>R</td><td>Device ready status
1: Device ready
0: Device not ready yet</td></tr>
<tr><td>[14:8]</td><td>Reserved</td><td>0x00</td><td>R</td><td>Reserved</td></tr>
<tr><td>[15]</td><td>Soft reset</td><td>1</td><td>RW</td><td>Whole chip software reset (Active Low)
1: Normal (Default)
0: Reset the whole chip</td></tr>
</table>

6.1.2 Page 0 Offset 0x02 : Byte Order Register (BOR)

Bit	Name	Default Value	R/W	Function
[15:0]	ByteSwap_EN	0x0000	W	Byte Swap function for all register If ByteSwap_EN=0x0000 (by default), SD bus = SD [15:0] If ByteSwap_EN≠0x0000 (by default), SD bus = {SD [7:0], SD [15:8]}
[15:0]	Test Byte	0x1234	R	Test pattern to check Endian swap result

Note: Driver should always read out the register value 0x1234 or 0x3412 to decide whether the bus is little endian or big endian.

6.1.3 Page 0 Offset 0x04: Function Enable Register (FER)

Bit	Name	Default Value	R/W	Function
[0]	IPALM	1	RW	RX IP header aligned 32-bit. 1: Enable RX IP header aligned double word. (Default) 0: Disable RX IP header aligned double word
[1]	DropCRC	1	RW	RX Drop CRC Enable. 1: CRC byte is dropped on received MAC frame forwarding to host 0: CRC byte is not dropped.
[2]	RH3M	0	RW	Checksum 2 byte + dummy 2 byte 1: RX Header 3 Csum append. 0: Disable RX Header 3 Header append (default).
[4:3]	TCLK_SELECT	00	RW	TCLK Output clock select 00: No clock output(Default) 01: 25MHz clock output 10: 50MHz clock output 11: 100MHz clock output
[5]	One_RnW	0	RW	RDn use enable 0:RDn use 1:RDn doesn't use,WRn replease RDn
[6]	ALECLK_HL	1	RW	ALE Clock Select 1: positive edge trigger 0: negative edge trigger
[7]	Reserved	0	R	Reserved
[8]	WordSwap_EN	0	RW	Word Swap function for TX and RX Bridge (Packet data only) 0: Disable (default) 1: Word swap enable
[9]	ByteSwapF_EN	0	RW	Byte Swap function for TX and RX Bridge (Packet data only) 0:Disable (default) SD bus = SD [15:0] 1:Enable byte swap function SD bus = {SD [7:0], SD [15:8]}
[10]	IRQ_Active	0	RW	Interrupt active high/low selection 1: Interrupt active high 0: Interrupt active low (default)
[11]	IRQ_TYPE	0	RW	Interrupt I/O Buffer Type 0: Enable IRQ to function as an open-drain buffer for use in a wired-OR interrupt configuration. The interrupt output is always active low. 1: IRQ output is a Push-Pull driver
[13:12]	RESERVED	00	RW	Reserved
[14]	RX Bridge Enable	0	RW	RX Bridge Enable 1: Enable RX Bridge 0: Disable RX Bridge
[15]	TX Bridge Enable	0	RW	TX Bridge Enable 1: Enable TX Bridge 0: Disable TX Bridge

6.1.4 Page 0 Offset 0x06: Interrupt Status Register (ISR)

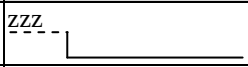
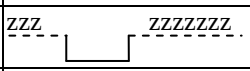
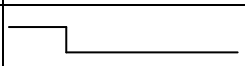
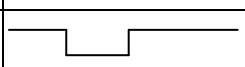
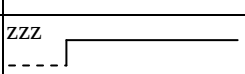
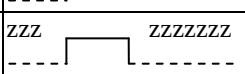
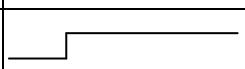
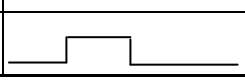
Bit	Name	Default Value	R/W	Function
[0]	RXPCT	0	R/WC	RX packet receive status bit 1: RX interrupt active 0: RX interrupt inactive Write 1 to clear this interrupt event.
[1]	Reserved	0	R/WC	Reserved
[2]	Reserved	0	R/WC	Reserved
[3]	Reserved	0	R/WC	Reserved
[4]	MDQ	0	R/WC	TX manual dequeue interrupt 1: TX manual dequeue interrupt active 0: TX manual dequeue interrupt inactive Write 1 to clear this interrupt event.
[5]	TXT	0	R/WC	TX packet transmit complete interrupt 1: TX packet transmit complete interrupt active 0: TX packet transmit complete interrupt inactive Write 1 to clear this interrupt event.
[6]	TX_Pages	0	R/WC	TX Free Page buffer more than driver require interrupt 1: TX_Pages interrupt active 0: TX_Pages inactive Write 1 to clear this interrupt event.
[7]	Reserved	0	R/WC	Reserved
[8]	TXERR	0	R/WC	TX packet error interrupt status bit 1: TX packet error interrupt active 0: TX packet error interrupt inactive Write 1 to clear this interrupt event.
[9]	LinkChange	0	R/WC	PHY Link Change interrupt status bit 1: PHY Link Change interrupt active 0: PHY Link Change not detect Write 1 to clear this interrupt event.
[10]	GPIO	0	R/WC	GPIO interrupt status bit 1: GPIO interrupt active 0: GPIO interrupt inactive Write 1 to clear this interrupt event.
[11]	SPI	0	R/WC	SPI interrupt status bit 1: SPI interrupt active 0: SPI interrupt inactive Write 1 to clear this interrupt event.
[15:12]	Reserved	0	R/WC	Reserved

6.1.5 Page 0 Offset 0x08: Interrupt Mask Register (IMR)

Bit	Name	Default Value	R/W	Function
[0]	RXPCT_mask	1	RW	RX packet receive interrupt mask bit 1: Mask RX packet interrupt on IRQ pin 0: Unmask RX packet interrupt on IRQ pin
[1]	Reserved	1	RW	Reserved
[2]	Reserved	1	RW	Reserved
[3]	Reserved	1	RW	Reserved
[4]	MDQ_mask	1	RW	TX manual dequeue interrupt complete 1: Mask TX manual dequeue interrupt on IRQ pin 0: Unmask TX manual dequeue interrupt on IRQ pin
[5]	TXT_mask	1	RW	TX packet transmit complete interrupt mask 1: Mask TX packet transmit complete interrupt on IRQ pin 0: Unmask TX packet transmit complete interrupt on IRQ pin
[6]	TX_Pages_mask	1	RW	TX Free Page buffer more than driver require interrupt mask 1: Mask TX Pages interrupt on IRQ pin. 0: Unmask TX Pages on IRQ pin.
[7]	Reserved	1	RW	Reserved
[8]	TXERR_mask	1	RW	TX packet error interrupt mask bit 1: Mask TX packet error interrupt on IRQ pin 0: Unmask TX packet error interrupt on IRQ pin
[9]	LinkChange_mask	1	RW	PHY Link Change interrupt mask bit 1: Mask PHY Link Change interrupt on IRQ pin 0: Unmask PHY Link Change interrupt on IRQ pin
[10]	GPIO_mask	1	RW	GPIO interrupt mask bit 1: Mask GPIO interrupt on IRQ pin 0: Unmask GPIO interrupt on IRQ pin
[11]	SPI_mask	1	RW	SPI interrupt mask bit 1: Mask SPI interrupt on IRQ pin 0: Unmask SPI interrupt on IRQ pin
[15:12]	Reserved	111	RW	Reserved

6.1.6 Page 0 Offset 0x0A: Wakeup Frame Configuration Register (WFCR)

Bit	Name	Default Value	R/W	Function
[0]	PME_IND	0	RW	PME indication 0: A static signal active when detect wake-up event. (Default) 1: A pulse when detect wake-up event.
[1]	PME_TYPE	0	RW	PME I/O Type. When cleared, PME_POL is ignored, and the output is always active low. 0: PME to function as an open-grain buffer for use in a wired-or configuration. (Default) 1: PME output is a Push-Pull driver.
[2]	PME_POL	0	RW	PME Polarity. 0: PME active low (Default) 1: PME active high (ignore when PME_TYPE is low)
[3]	Reset_pme	0	RW	Reset PME pin to default value before re-start WOL detection 1: Reset PME 0: Normal
[4]	Sleep mode	0	WC	1: Sleep/Suspend Mode. The switch will turn off all the internal clocks. And the chip is in the minimum power consumption state. 0: Disable sleep mode The host CPU can write "Host Wake Up Register" (Offset 1Eh) for non-SPI interface or set AX88796C SPI "ABh Exit Power Down (S3)" instruction for SPI interface to return the AX88796C to the normal operation state.
[5]	Wakeup mode	0	RW	1: Enable Wake-On-LAN detection function 0: Disable Wakeup mode
[7:6]	PME_pulse	00	RW	PME_pulse. 00:2ms 01:8ms 10:32ms 11:64ms
[8]	En_linkchange	0	RW	Enable link status change as one of the wake up condition. Wakeup condition: PHY link done status toggle from low to high or high to low. 1: Enable 0: Disable

PME_POL	PME_TYPE	PME_IND	PME
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

[9]	En_MagicPacket	0	RW	Enable Magic Packet detection as one of the wake up condition. Wakeup condition: Detect 0xFFFFFFFFFFFF follow by repeated 16 times DA_MAC pattern anywhere within the payload and good CRC value present. 1: Enable 0: Disable
[10]	En_WakeUpframe	0	RW	Enable Microsoft wakeup frame detector as one of the wakeup condition. Wakeup condition: Calculate CRC value across all the mask bits that match the expected CRC value and the packet has a good CRC value in the end. 1: Enable 0: Disable
[11]	PME_Enable	0	RW	1: Enable PME pin 0: Tri-state PME signal
[12]	Linkchange_status	0	R	Link change status 1: Link change event found 0: Idle
[13]	MagicPacket_status	0	R	Magic frame detection status 1: Magic Frame found 0: Idle
[14]	WakeUpframe_status	0	R	Microsoft wakeup detection status 1: Microsoft wakeup frame found 0: Idle
[15]	PME_status	0	R	PME status 1: PME output is high 0: PME output is low

6.1.7 Page 0 Offset 0x0C: Power Saving Configuration Register (PSCR)

Bit	Name	Default Value	R/W	Function
[2:0]	PowerSaving	000	RW	PHY power saving state configurable register 000: Disable Power saving function 001: Cable Off Power Saving Level 1 010: Cable Off Power Saving Level 2
[3]	Reserved	0	RW	Reserved
[4]	SWPowerSavingEn	0	RW	Software power saving control enable 1: Software Control Power Saving Function 0: Select [12:8] as pre-configure power saving mode
[5]	WOLPowerSaving_en	1	RW	WOL power saving enable 1: Enable power saving when WOL (Link to 10M) 0: Normal NOTE: Please set to 0 when ARP and NS offload function is enabled.
[6]	SW_WOL	0	RW	Software WOL Select enable 1: Software configure [13] WOLPowerSaving_en bit dynamically 0: Always use [13] as pre-defined WOLPowerSaving_en value(Default)
[7]	Reserved	0	RW	Reserved
[8]	Reserved	0	RW	Reserved
[9]	Reserved	0	RW	Reserved
[10]	Reserved	0	RW	Reserved
[11]	PHY_ Reset	1	RW	PHY reset signal. Active low and should be longer than 500ns. 1: Normal 0: Reset internal PHY The host CPU should write one to enable PHY back to normal state if this bit is set to 0.
[12]	PHY_Cabsilent	1	R	PHY Cable-off detect enable. Toggling when receive signal. 1: Cable-off detect 0: No Cable-off detect
[13]	PHY_Cableoff	0	R	PHY Cable off 1: PHY Detect cable off 0: Normal
[14]	PHY_Link	0	R	PHY Link Status 1: PHY in Link state 0: PHY not Link yet
[15]	EEPROM_OK	0	R	EEPROM load complete 1: EEPROM load complete. Please also check EECSR register data. If EECSR data is 0xFF then external EEPROM does not exist 0: EEPROM not finish loading due to checksum failure

6.1.8 Page 0 Offset 0x0E: MAC Configuration Register (MACCR)

Bit	Name	Default Value	R/W	Function
[0]	RE	0	RW	RX path Enable 1: Enable RX path of the ASIC. 0: Disabled (default).
[1]	FD	0	RW	Full-Duplex 1: Full Duplex mode (default). 0: Half Duplex mode.
[2]	Speed	0	RW	Speed mode 1: 100 Mbps (default). 0: 10 Mbps.
[3]	RFC	1	RW	RX Flow Control Enable 1: Enable RX Flow Control 0: Disable (Default)
[4]	TFC	1	RW	TX Flow Control Enable 1: Enable TX Flow Control 0: Disable (Default)
[5]	TXAbortAllow	0	RW	Allow TX Abort 1: Enable 0: Disable
[6]	Reserved	0	RW	Reserved
[7]	PF	0	RW	Check only “length/type” field for Pause Frame. 1: Enable. Pause frames are identified only based on L/T filed. 0: Disabled. Pause frames are identified based on both DA and L/T fields (default).
[12:8]	PMM_st	00011	R	Power Management Module Status 00001: Chip Reset State 00010: Wait State 00011: Device Ready State (Normal Operation) 00100: PS1 State (Cable-off) 00101: PS2 State (Cable-off) 00111:Wake-On-LAN State 01000 PS1 and Wake-On-LAN State (Cable-off) 01001: PS2 and Wake-On-LAN State (Cable-off) 01010: Sleep Mode 01011: PHY in Reset State 10000: Software force in PS1 State 10001: Software force in PS2 State
[15:13]	Reserved	0x00	R	Reserved

6.1.9 Page 0 Offset 0x10: TX Free Buffer Count Register (TFBFCR)

Bit	Name	Default Value	R/W	Function
[6:0]	TX_FreeBuf	0x1F	R	Indicate how many free page buffers in TX packet memory.
[12:7]	TX_Pages[5:0]	0	RW	Driver set this register to let 796C know how many tx page that driver require.
[13]	TX_Pages_Set	0	WC	If driver set this bit and TX_Pages[5:0] , then the AX88796C will compare TX_FreeBuf and TX_Pages[5:0] , if TX_FreeBuf[5:0] value big then TX_Pages[5:0], the AX88796C will send TX_Pages interrupt to CPU. (Interrupt status in page0 offset 6 , bit 6)
[14]	TXDPT_start	0	WC	Set 1 to start or restart TX dispatch timer. Reference page 1, offset 6, bit [15-8].
[15]	TX_Transmit	0	WC	If Interrupt assert and manual-enqueue status set, CPU should set this bit to 1 to continue transmit packet.

6.1.10 Page 0 Offset 0x12: TX Sequence Number Register (TSNR)

Bit	Name	Default Value	R/W	Function
[4:0]	TXB_SN[4:0]	0	R	Sequence number in TX Bridge. Cpu can read this signal to know the last succeed transmit packet's sequence number.
[5]	TXB_ERR	0	R	Indicate TX Bridge in error state. 1: TX Bridge in error state. 0: TX Bridge not in error state.
[6]	TXB_Idle	1	R	Indicate TX Bridge in idle state. 1: TX Bridge in idle state. 0: TX Bridge not in idle state.
[7]	Reserved	0	R	Reserved
[13:8]	TXB_PktCnt[5:0]	0	RW	Indicate how many packets will send from CPU to TX Bridge.
[14]	TXB_reinitial	0	WC	Set this bit to 1 can let TX Bridge module state machine reinitialize.
[15]	TXB_Start	0	WC	Indicate TX Bridge start to receive packet from CPU.

6.1.11 Page 0 Offset 0x14: RX/TX Data Port Register (RTDPR)

Bit	Name	Default Value	R/W	Function
[15:0]	TXB_Data	0	W	The host CPU can use this register to write TXB_Data[15:0] to TX Bridge.
[15:0]	RXB_Data	0	R	The host CPU can read RXB_Date[15:0] from RX Bridge.

6.1.12 Page 0 Offset 0x16: RX Bridge Control Register 1 (RXBCR1)

Bit	Name	Default Value	R/W	Function
[13:0]	RXB_BL	0	RW	The host CPU should set this register to tell RX Bridge module how many DMA burst (in word count) will send.
[14]	RXB_discard	0	WC	The host CPU can set this bit to discard current packet in RX Bridge module.
[15]	RXB_start	0	WC	The host CPU should set this bit to 1 before DMA burst read packet.

6.1.13 Page 0 Offset 0x18: RX Bridge Control Register 2 (RXBCR2)

Bit	Name	Default Value	R/W	Function
[7:0]	RXPC	0	R	The host CPU can read this register to know how many packets in RX memory. Before read this register, the CPU should set RX_Latch register to 1 in page 0 offset 0x1A bit 15.
[12:8]	RXB_SN[4:0]	0	R	Indicate current packet's sequence number in RX Bridge
[13]	RXB_Ready	0	R	Indicate RX Bridge is ready for read. After CPU set RXB_start, the CPU should polling this register to make sure RX Bridge is ready for read or burst read. 0: RX Bridge is not ready for host CPU read or burst read operation 1: RX bridge is ready for host CPU read or burst read operation
[14]	RXB_Idle	1	R	Indicate RX Bridge in idle state. 1: RX Bridge in idle state. 0: RX Bridge not in idle state.
[15]	RXB_Reinitial	0	WC	Set this bit to 1 can let RX Bridge module state machine reinitialize.

6.1.14 Page 0 Offset 0x1A: RX Total Valid Word Count Register (RTWCR)

Bit	Name	Default Value	R/W	Function
[13:0]	RXWC	0	R	The host CPU can read this register to know total packet word count in RX memory, and then the CPU use this register to set the RXB_BL field of RXBCR1 register. Before read this register, the CPU should set RX_Latch register to 1 in page 0 offset 0x1A bit 15.
[14]	Reserved	0	R	Reserved
[15]	RX_Latch	0	WC	Before the CPU read RXWC[13:0] register in page 0 offset 0x1A or RXPC[7:0] register in page 0 offset 0x18 , the CPU should set this register to 1 first.

6.1.15 Page 0 Offset 0x1C: RX Current Packet Header Register (RCPHR)

Bit	Name	Default Value	R/W	Function
[15:0]	RXB_FFL	0	R	The host CPU can read this register to get current packet's header1 in RX Bridge module. Bit 15 : indicate this packet is multicast or broadcast packet. 1: this packet is multicast or broadcast packet. 0: this packet is unicast packet Bit 14 : indicate this packet is runt packet. 1: this packet is runt packet. 0: this packet is normal size packet Bit 13 : indicate this packet got MII interface error. 1: this packet got MII interface error. 0: this packet no MII interface error Bit 12 : indicate this packet got CRC error. 1: this packet got CRC error. 0: this packet no CRC error Bit 11:Reserved Bit 10-0 : indicate this packet's length.

6.1.16 Page 0 ~ 7 Offset 0x1E: Remote Wakeup Register (RWR)

Bit	Name	Default Value	R/W	Function
[15:0]	Sleep_mode_exit	0x0000	WC	Any write command to this address will cause the chip exit the sleep mode and back to normal mode operation. (This register is only valid for non-SPI interface.)

Note: Any write to this register within any page for non-SPI interface will resume the AX88796C back to normal state; please set AX88796C SPI "ABh Exit Power Down (S3)" instruction for SPI interface to resume AX88796C back to normal state.

6.1.17 Page 1 Offset 0x02: RX Packet Process Enable Register (RPPER)

Bit	Name	Default Value	R/W	Function
[0]	RX Packet Enable	0	RW	0 : RX packet process disable 1: RX packet process enable NOTE: Please write 1 to this bit to enable normal RX packet processing.
[6:1]	Reserved	0x00	RW	
[7]	Reserved	0	R	Reserved
[14:8]	Reserved	0x00	RW	Reserved
[15]	Reserved	0	R	Reserved

6.1.18 Page 1 Offset 0x08: Memory Read/Write Control Register (MRCR)

Bit	Name	Default Value	R/W	Function
[11:0]	MM_Addr	0x000	RW	TX/RX memory address.
[12]	MM_RW	0	WC	Set 1 to read/write TX/RX memory. 1: read memory 0: write memory
[13]	MM_ready	1	R	Indicate read or write memory finish.
[14]	MM_RX	0	WC	Set 1 to access RX memory
[15]	MM_TX	0	WC	Set 1 to access TX memory

6.1.19 Page 1 Offset 0x0A: Memory Data Register (MDR)

Bit	Name	Default Value	R/W	Function
[15:0]	MM_Data	0x0000	RW	Data to write TX/RX memory or read from TX/RX memory.

6.1.20 Page 1 Offset 0x0C: RX Memory Pointer Register (RMPR)

Bit	Name	Default Value	R/W	Function
[7:0]	MACRX_writepoint	0x01	R	Indicate current write page pointer in RX LAN module
[15:8]	MACRX_readpoint	0x01	R	Indicate current read page pointer in TX host module.

6.1.21 Page 1 Offset 0x0E: TX Memory Pointer Register (TMPR)

Bit	Name	Default Value	R/W	Function
[7:0]	MACTX_writepoint	0x01	R	Indicate current write page pointer in RX host module
[15:8]	MACTX_readpoint	0x01	R	Indicate current read page pointer in TX LAN module.

6.1.22 Page 1 Offset 0x10: RX Bridge Stuffing Packet Control Register (RXBSPCR)

Bit	Name	Default Value	R/W	Function
[11:0]	Reserved	0x000	R	Reserved
[14:12]	RXB_SPW	100	RW	RX bridge stuffing packet double word count. Minimum value is 1 and maximum value is 7. Default value is 4.
[15]	RXB_SP	1	RW	Enable the RX bridge stuffing packet function. 1: Enable (Default) 0: Disable

6.1.23 Page 1 Offset 0x12: RX MAC Control Register (RXMCR)

Bit	Name	Default Value	R/W	Function
[7:0]	Reserved	0x00	R	Reserved
[8]	SBP	1	RW	Stop Backpressure. 1: When TFC bit = 1, setting this bit enables backpressure on TX direction “continuously” during RX buffer full condition in half duplex mode. 0: When TFC bit = 1, setting this bit enable backpressure on TX direction “intermittently” during RX buffer full condition in half duplex mode (default).
[9]	SM	0	RW	Super Mac support. 1: Enable Super Mac to shorten exponential back-off time during transmission retrying. 0: Disabled (default).
[10]	Reserved	0	RW	Reserved
[11]	crcenLAN	1	RW	TX Append CRC Enable. 1: CRC byte is generated and appended by the hardware for every transmitted MAC frame (default). 0: CRC byte is not appended.
[12]	stp	0	RW	Stop receiving packet process
[13]	Reserved	0	RW	Reserved
[15:14]	Reserved	00	R	Reserved

6.1.24 Page 2 Offset 0x02: IO Control Register (ICR)

<table>
<tr><th>Bit</th><th>Name</th><th>Default Value</th><th>R/W</th><th>Function</th></tr>
<tr><td>[0]</td><td>PDSDLO</td><td>0</td><td>RW</td><td>Pull-Down Data Pad 7-0</td></tr>
<tr><td>[1]</td><td>PUSDLO</td><td>0</td><td>RW</td><td>Pull-Up Data Pad 7-0</td></tr>
<tr><td>[2]</td><td>PDSDHI</td><td>0</td><td>RW</td><td>Pull-Down Data Pad 15-8</td></tr>
<tr><td>[3]</td><td>PUSDHI</td><td>0</td><td>RW</td><td>Pull-Up Data Pad 15-8</td></tr>
<tr><td>[4]</td><td>PDSA</td><td>0</td><td>RW</td><td>Pull-Down SA0-5</td></tr>
<tr><td>[5]</td><td>PUSA</td><td>0</td><td>RW</td><td>Pull-Up SA0-5</td></tr>
<tr><td>[7:6]</td><td>IPME</td><td>0</td><td>RW</td><td>PME Output Current
<table><tr><td></td><td>3.3V</td><td>2.5V</td><td>1.8V</td></tr><tr><td>0</td><td>8mA</td><td>4.4mA</td><td>2.8mA</td></tr><tr><td>1</td><td>16mA</td><td>8.8mA</td><td>5.6mA</td></tr></table></td></tr>
<tr><td>[7]</td><td>IIRQ</td><td>0</td><td>RW</td><td>IRQ Output Current
<table><tr><td></td><td>3.3V</td><td>2.5V</td><td>1.8V</td></tr><tr><td>0</td><td>8mA</td><td>4.4mA</td><td>2.8mA</td></tr><tr><td>1</td><td>16mA</td><td>8.8mA</td><td>5.6mA</td></tr></table></td></tr>
<tr><td>[9:8]</td><td>ISD</td><td>00</td><td>RW</td><td>Data Pad Output Current
<table><tr><td>[1:0]</td><td>3.3V</td><td>2.5V</td><td>1.8V</td></tr><tr><td>00</td><td>2mA</td><td>1.1mA</td><td>0.7mA</td></tr><tr><td>01</td><td>4mA</td><td>2.2mA</td><td>1.4mA</td></tr><tr><td>10</td><td>8mA</td><td>4.4mA</td><td>2.8mA</td></tr><tr><td>11</td><td>16mA</td><td>8.8mA</td><td>5.6mA</td></tr></table></td></tr>
<tr><td>[10]</td><td>SDSR</td><td>0</td><td>RW</td><td>SD0-15 IO pad output slew rate
0: Fast
1: Slow</td></tr>
<tr><td>[12:11]</td><td>ICLK</td><td>00</td><td>RW</td><td>TCLK output current
<table><tr><td>[1:0]</td><td>3.3V</td><td>2.5V</td><td>1.8V</td></tr><tr><td>00</td><td>2mA</td><td>1.1mA</td><td>0.7mA</td></tr><tr><td>01</td><td>4mA</td><td>2.2mA</td><td>1.4mA</td></tr><tr><td>10</td><td>8mA</td><td>4.4mA</td><td>2.8mA</td></tr><tr><td>11</td><td>16mA</td><td>8.8mA</td><td>5.6mA</td></tr></table></td></tr>
<tr><td>[13]</td><td>IGPIO</td><td>00</td><td>RW</td><td>GPIO output current
<table><tr><td></td><td>3.3V</td><td>2.5V</td><td>1.8V</td></tr><tr><td>0</td><td>8mA</td><td>4.4mA</td><td>2.8mA</td></tr><tr><td>1</td><td>16mA</td><td>8.8mA</td><td>5.6mA</td></tr></table></td></tr>
<tr><td>[14]</td><td>IEEPROM</td><td>0</td><td>RW</td><td>EEPROM output current
<table><tr><td></td><td>3.3V</td><td>2.5V</td><td>1.8V</td></tr><tr><td>0</td><td>8mA</td><td>4.4mA</td><td>2.8mA</td></tr><tr><td>1</td><td>16mA</td><td>8.8mA</td><td>5.6mA</td></tr></table></td></tr>
<tr><td>[15]</td><td>ILED</td><td>0</td><td>RW</td><td>LED output current
<table><tr><td></td><td>3.3V</td><td>2.5V</td><td>1.8V</td></tr><tr><td>0</td><td>8mA</td><td>4.4mA</td><td>2.8mA</td></tr><tr><td>1</td><td>16mA</td><td>8.8mA</td><td>5.6mA</td></tr></table></td></tr>
</table>

6.1.25 Page 2 Offset 0x04: PHY Control Register (PCR)

Bit	Name	Default Value	R/W	Function
[0]	Auto_Poll_En	0	RW	PHY Auto-Polling Function. Enable If set to one then hardware will auto-polling internal PHY register setting and update Mac Control Register enable, speed, and duplex information. 1: Enable Auto-polling function 0: Disable (Default)

[1]	Poll_fc	1	RW	Enable Auto-polling Flow control function.
				Auto-polling PHY's register and update flow control information.
				If PHY is in full duplex mode then
				1: MAC Flow control depend on PHY and PHY's link partner PHY pause capability
				0: MAC disable Flow control
				If PHY is in half duplex mode then
				1: MAC enable Flow control
				0: MAC disable Flow control

[2]	Poll_sel	0	RW	Polling function select 1: Auto-polling logic will Check MR0 register (PHY addr. 0x0) status to make decision on MAC's speed and duplex 0: Auto-polling logic will check MR4 register (PHY address 0x4) status to make decision on MAC's speed and duplex. (Default)
[3]	Reserved	0	R	Reserved
[7:4]	Opmode	0000	RW	PHY Operation mode 0000: Auto-negotiation mode 0001: Auto-negotiation with 100 BASE-TX FDX/HDX ability 0010: Auto-negotiation with 10 BASE-T FDX/HDX ability 0011: Reserved 0100: Manual selection of 100 BASE-TX FDX 0101: Manual selection of 100 BASE-TX HDX 0110: Manual selection of 10 BASE-T FDX 0111: Manual selection of 10 BASE-T HDX
[12:8]	Phyid[4:0]	10000	RW	Programmable PHY ID Registers. This address is used when multiple PHY are accessed through management interface. If the value is changed, new setting will effective after hardware/software is reset. The default value is 10000.
[15:13]	Reserved	000	RW	Reserved

6.1.26 Page 2 Offset 0x06: PHY Status Register (PHYSR)

Bit	Name	Default Value	R/W	Function
[0]	Speed Led	1	R	PHY Link Speed Status 0: 100MBps 1: 10MBps
[1]	Duplex Led	1	R	PHY Full Duplex Mode Status 0: Full Duplex Mode 1: Half Duplex Mode
[2]	Link Led	1	R	PHY Link Status 0: Link up 1: Link Down
[3]	TX Led	1	R	PHY TX activity 0: TX traffic passing 1: No Traffic
[4]	RX Led	1	R	PHY RX activity 0: RX traffic passing 1: No Traffic
[5]	COL Led	1	R	PHY Collision Status 0: Collision Detect 1: No Collision
[6]	Reserved	1	R	Reserved
[7]	Reserved	1	R	Reserved
[8]	Reserved	1	R	Reserved
[9]	Reserved	0	R	Reserved
[10]	XtalClkSelect	1	R	PHY XTLP/XTLN clock select 1: Use Crystal clock input XTLP/XTLN as PHY clock source 0: Disable
[11]	ASICClkSelect	0	R	PHY ASIC clock select 1: Select TCLK as PHY clock source 0: Disable
[15:12]	Reserved	0x0	R	Reserved

6.1.27 Page 2 Offset 0x08: MDIO Read/Write Data Register (MDIODR)

Bit	Name	Default Value	R/W	Function
[15:0]	Mdio_Data	0x0000	RW	MDIO data [15:0] When CPU set MDIO read command register to 1, The MDC/MDIO controller will show the read data from PHY register here. When CPU set MDIO write command register to 1, The MDC/MDIO controller will write this register data to the PHY register.

6.1.28 Page 2 Offset 0x0A: MDIO Read/Write Control Register (MDIOCR)

Bit	Name	Default Value	R/W	Function
[4:0]	Reg_addr	00000	RW	PHY Register address. CPU should set this register to let the MDC/MDIO controller knows which PHY register to be accessed.
[7:5]	Reserved	000	R	Reserved
[12:8]	Phy_addr	00000	RW	PHY Physical ID. The CPU should set this register to let the MDC/MDIO controller know what PHY ID to be accessed.
[13]	MDIORD_ok	0	R	MDIO data valid After the CPU set the MDIO read command register to one, CPU should continue polling this bit to confirm that the MII management interface read cycle is done and Data [15:0] is also valid. After CPU set the MDIO write command register to one, CPU should continue polling this bit to confirm that the MII management interface write cycle is done. 1: MII management interface read/write cycle is done. 0: MII management interface read/write cycle is not done.
[14]	MDIORead	0	WC	MDIO Read command to PHY 1: Read command 0: Idle The CPU should set this bit to one to let the MDC/MDIO controller perform MII management interface read cycle. CPU also needs to program the reg_addr and phy_addr value in MDIOCR first.
[15]	MDIOWrite	0	WC	MDIO Write command to PHY 1: Write command 0: Idle The CPU should set this bit to one to let the MDC/MDIO controller perform MII management interface write cycle. CPU also needs to set the reg_addr, phy_addr and Data register in MDIOCR first.

6.1.29 Page 2 Offset 0x0C: I_Full/I_Speed LED Control Register 0 (LCR0)

Bit	Name	Default Value	R/W	Function
[7:0]	Sel_led0[7:0]	0x04	RW	Select LED pin I_FULL output function [7] Full Duplex/Collision [6] 10Base-T [5] Collision [4] TX/RX activity [3] Link/Act. [2] Full duplex [1] 100Base-TX [0] Enable LED pin (Please reference page 2 offset 0xE [15] setting to select I_FULL LED polarity) 1: enable LED 0: disable LED NOTE: The user can turn on multiple functions at the same time. For example, Sel_led0=0001_0001 then any RX or TX activity will turn on the LED light on LED0 pin. NOTE: I_FULL LED polarity can also set to active high or active low. So when Page 2 0xC [0] enable is off then output value will decide by I_FULL LED polarity setting in Page 2 offset 0x0E bit [15], I_FULL LED output 1 when I_FULL_select is active low and 0 when active high.
[15:8]	Sel_led1[7:0]	0x02	RW	Select LED pin I_Speed output function [7] Full Duplex/Collision [6] 10Base-T [5] Collision [4] TX/RX activity [3] Link/Act. [2] Full duplex [1] 100Base-TX [0] Enable LED pin (active low) NOTE: The user can turn on multiple functions at the same time.

6.1.30 Page 2 Offset 0x0E: I_LK/Act LED Control Register 1 (LCR1)

Bit	Name	Default Value	R/W	Function
[7:0]	Sel_led2[7:0]	0x08	RW	Select LED pin I_LK/Act output function [7] Full Duplex/Collision [6] 10Base-T [5] Collision [4] TX/RX activity [3] Link /Act. [2] Full duplex [1] 100Base-TX [0] Enable LED pin (active low) NOTE: The user can turn on multiple functions at the same time.
[14:8]	IPG	0x15	RW	Inter Packet Gap for back-to-back transfer on TX direction in MII mode (default = 15h).
[15]	I_FULL_active	0	RW	I_FULL LED active select 0: active low if the I_FULL of bus type setting is pulled up 1: active high if the I_FULL of bus type setting is pulled down Please refer to TAB-1 for bus type setting.

6.1.31 Page 2 Offset 0x10: IPG Control Register (IPGCR)

Bit	Name	Default Value	R/W	Function
[6:0]	IPG1	0x0C	RW	IPG part1 value (default = 0Ch).
[7]	Reserved	0	R	Reserved
[14:8]	IPG2	0x12	RW	IPG part1 value + part2 value (default = 12h).
[15]	Reserved	0	R	Reserved

6.1.32 Page 2 Offset 0x12: Chip Revision ID Register (CRIR)

Bit	Name	Default Value	R/W	Function
[3:0]	Chip_rev_ID	0000	RW	Chip Revision ID
[15:4]	Reserved	0x000	RW	Reserved

6.1.33 Page 2 Offset 0x14: Flow Control High/Low Watermark Control Register (FLHWCR)

Bit	Name	Default Value	R/W	Function
[6:0]	FCHW	0x24	RW	Flow Control High-water mark [7:0]: RX free page count high water level, once internal RX free page counter lower than this threshold and Flow control is enabled, then TX MAC will send Pause ON Frame out to informal remote PHY stop transmit packets.
[7]	Reserved	0	R	Reserved
[14:8]	FCLW	0x42	RW	Flow Control Low-water mark [7:0]: When Flow control is enabled and pause is ON, RX free page counter if higher than this low water mark value then TX MAC will send pause OFF frame to inform remote PHY back to normal state and re-start transmit packets.
[15]	Reserved	0	R	Reserved

6.1.34 Page 2 Offset 0x16: RX Control Register (RXCR)

Bit	Name	Default Value	R/W	Function
[0]	PRO	1	RW	PACKET_TYPE_PROMISCUOUS. 1: All frames received by the ASIC are forwarded up toward the host. 0: Disabled
[1]	AMALL	0	RW	PACKET_TYPE_ALL_MULTICAST. 1: All multicast frames received by the ASIC are forwarded up toward the host, not just the frames whose scrambling result of DA matching with multicast address list provided in Multicast Filter Array Register. 0: Disabled. This only allows multicast frames whose scrambling result of DA field matching with multicast address list provided in Multicast Filter Array Register to be forwarded up toward the host (Default).
[2]	SEP	0	RW	Accept Error Packet. 1: Accept save Error Packet. 0: Disabled, Reject Error Packet. (Default)
[3]	AB	0	RW	PACKET_TYPE_BROADCAST. 1: All broadcast frames received by the MAC are forwarded to the host interface. 0: Disabled. (Default)
[4]	AM	0	RW	PACKET_TYPE_MULTICAST. 1: All multicast frames who's scrambling result of DA matching with multicast address list are forwarded to the host interface. (Please reference to section 4.1.2) 0: Disabled. (Default)
[5]	AP	0	RW	Accept Physical Address from Multicast Filter Array. 1: Allow unicast packets to be forwarded up toward host if the lookup of scrambling result of DA is found within multicast address list. 0: Disabled, that is, unicast packets filtering are done without regarding multicast address list (Default).
[6]	ARP	0	RW	Accept Runt Packet. 1: Accept Runt Packet. 0: Disabled, Reject the runt packet (byte count less then 64 bytes) (Default).
[7]	Reserved	0	RW	Reserved
[15:8]	Reserved	0x00	R	Reserved

6.1.35 Page 2 Offset 0x18: Jam Limit Count Register (JLCR)

Bit	Name	Default Value	R/W	Function
[5:0]	Jam[5:0]	0x3F	RW	Jam_Limit[5:0]: This is used for flow-control in half-duplex mode, which is based on force collision mechanisms to backpressure transmitting network node. During the force collision backpressure process, the Ethernet MAC will continue counting total collision count. When it has reached the Jam_Limit setting, the Ethernet MAC will stop backpressure to avoid Ethernet HUB from being partitioned (default = 3Fh) due to excessive collision on network link.
[6]	Reserved	0	RW	Reserved
[7]	cpteff	0	RW	Capture Effective Mode. 1: Enable capture effective mode. 0: Disabled.
[8]	LDRND	0	RW	LDRND: To load Random number into MAC's exponential back-off timer, the user writes a "1" to enable the ASIC to load a small random number into MAC's back-off timer to shorten the back-off duration in each retry after collision. This register is used for test purpose. Default value = 0.
[15:9]	Reserved	0x02	R	Reserved

6.1.36 Page 2 Offset 0x1C: Max Packet Length Register (MPLR)

Bit	Name	Default Value	R/W	Function
[11:0]	MPL	0x600	RW	Maximum packet Length [11:0] Programmable maximum packet size allowed to be received range from 64 to 2047.Default value is 1522.
[15:12]	Reserved	0x0	R	Reserved

6.1.37 Page 3 Offset 0x02: MAC Address Setup Register 0 (MACASR0)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC [47:40]	0x00	RW	Default MAC address for host port. MAC address [47:40]
[15:8]	MAC [39:32]	0x00	RW	MAC address [39:32]

6.1.38 Page 3 Offset 0x04: MAC Address Setup Register 1 (MACASR1)

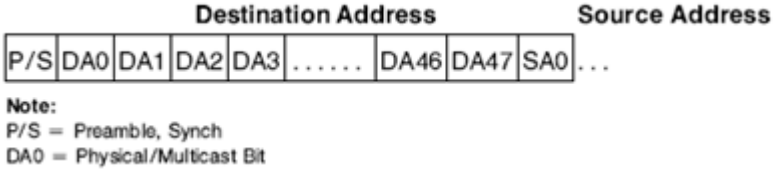
Bit	Name	Default Value	R/W	Function
[7:0]	MAC [31:24]	0x00	RW	Default MAC address for host port. MAC address [31:24]
[15:8]	MAC [23:16]	0x00	RW	MAC address [23:16]

6.1.39 Page 3 Offset 0x06: MAC Address Setup Register 2 (MACASR2)

Bit	Name	Default Value	R/W	Function
[7:0]	MAC [15:8]	0x00	RW	Default MAC address for host port MAC address [15:8]
[15:8]	MAC [7:0]	0x00	RW	MAC address [7:0]

	D7	D6	D5	D4	D3	D2	D1	D0
MACASR2[15:8]	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
MACASR2[7:0]	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
MACASR1[15:8]	DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16
MACASR1[7:0]	DA31	DA30	DA29	DA28	DA27	DA26	DA25	DA24
MACASR0[15:8]	DA39	DA38	DA37	DA36	DA35	DA34	DA33	DA32
MACASR0[7:0]	DA47	DA46	DA45	DA44	DA43	DA42	DA41	DA40

Note: The bit sequence of the received MAC address is DA0, DA1, … DA46, DA47 ….



6.1.40 Page 3 Offset 0x08: Multicast Filter Array Register (MFAR01)

Bit	Name	Default Value	R/W	Function
[7:0]	MA0 [7:0]	0x00	RW	Multicast Filter Array0 [7:0]
[15:8]	MA1 [7:0]	0x00	RW	Multicast Filter Array1 [7:0]

6.1.41 Page 3 Offset 0x0A: Multicast Filter Array Register (MFAR23)

Bit	Name	Default Value	R/W	Function
[7:0]	MA2 [7:0]	0x00	RW	Multicast Filter Array2 [7:0]
[15:8]	MA3 [7:0]	0x00	RW	Multicast Filter Array3 [7:0]

6.1.42 Page 3 Offset 0x0C: Multicast Filter Array Register (MFAR45)

Bit	Name	Default Value	R/W	Function
[7:0]	MA4 [7:0]	0x00	RW	Multicast Filter Array4 [7:0]
[15:8]	MA5 [7:0]	0x00	RW	Multicast Filter Array5 [7:0]

6.1.43 Page 3 Offset 0x0E: Multicast Filter Array Register (MFAR67)

Bit	Name	Default Value	R/W	Function
[7:0]	MA6 [7:0]	0x00	RW	Multicast Filter Array6 [7:0]
[15:8]	MA7 [7:0]	0x00	RW	Multicast Filter Array7 [7:0]

6.1.44 Page 3 Offset 0x10: VLAN ID0 Filter Register (VID0FR)

Bit	Name	Default Value	R/W	Function
[11:0]	VID0 [11:0]	0x000	RW	VLAN ID0 Filter Register
[13:12]	Reserved	00	R	Reserved
[14]	VFE	0	RW	VLAN filter enable 1: Enable VLAN filter. The VLAN ID field (12 bits) received 802.1q tagged packets, which will be used to compare with VID1 and VID2 setting. If it matches either VID1 or VID2, or its value is equal to all zeros, the received 802.1q tagged packets will be forwarded to the Host. 0: Disable VLAN filter. The received packets with or without 802.1q Tag bytes will always be forwarded to the Host (default).
[15]	VSO	0	RW	VLAN Strip off. The VSO bit determines whether the VLAN Tag bytes (4 bytes) are stripped off or not during forwarding to the Host. 1: Strip off VLAN Tag (4 bytes) from the incoming packet. 0: Preserve VLAN Tag in the incoming packet (default).

6.1.45 Page 3 Offset 0x12: VLAN ID1 Filter Register (VID1FR)

Bit	Name	Default Value	R/W	Function
[11:0]	VID1 [11:0]	00	RW	VLAN ID1 Filter Register
[15:12]	Reserved	0x0	R	Reserved

6.1.46 Page 3 Offset 0x14: EEPROM Checksum Register (EECSR)

Bit	Name	Default Value	R/W	Function
[7:0]	EEChecksum [7:0]	0x00	R	EEPROM hardware calculated Checksum value over the valid address space. If this value plus the EEPROM 0x27 checksum data equal to 0xFF then the checksum value check is passed.
[15:8]	Reserved	0x00	R	Reserved

6.1.47 Page 3 Offset 0x16: EEPROM Data Register (EEDR)

Bit	Name	Default Value	R/W	Function
[15:0]	EEPromdata [10:0]	0xffff	RW	EEPROM Data Register

6.1.48 Page 3 Offset 0x18: EEPROM Control Register (EECR)

Bit	Name	Default Value	R/W	Function
[7:0]	EepromAddr [7:0]	0x00	RW	EEPROM Address Register
[11:8]	EE_command	0x00	RW	0x0 EEPROM Idle 0x1 Read EEPROM 0x2 Write EEPROM 0x4 Disable EEPROM Write 0x8 Enable EEPROM Write
[12]	Reserve	0	R	Reserved
[13]	EE_READY	1	RW	EEPROM Ready 1: EEPROM Ready, Indicate EEPROM ready to execute command 0: EEPROM not ready
[14]	EE_reload	0	RW	EEPROM Auto Reload 1: EEPROM re-load function 0: Normal (Default)
[15]	EE_Reset	0	RW	EEPROM module reset 1:Reset EEPROM Control 0:Idel (Default)

6.1.49 Page 3 Offset 0x1A: Test Packet Configuration Register (TPCR)

Bit	Name	Default Value	R/W	Function
[7:0]	TPPattern[7:0]	0x00	RW	Data pattern or random seed
[13:8]	TPInterval[5:0]	0x15	RW	Test Packet inter-frame gape
[14]	TPRandom	0	RW	Test Packet with Random pattern
[15]	TPFix	0	RW	Test Packet with fix pattern

The transmit test packets without padding CRC 4 bytes.

6.1.50 Page 3 Offset 0x1C: Test Packet Length Register (TPLR)

Bit	Name	Default Value	R/W	Function
[11:0]	TPLength	0x48	RW	Set Test Packet Length [11:0]
[15:12]	Reserved	0x0	R	Reserved

6.1.51 Page 4 Offset 0x02: GPIO Enable Register (GPIOER)

Bit	Name	Default Value	R/W	Function
[3:0]	GPIO_En	0x0	RW	GPIO3~GPIO0 Enable Register Enable GPIO function when set to one. 1: Enable 0: Disable
[7:4]	GPIO_In	0x0	RW	GPIO3~GPIO0 Input Data Register. Store the input data when GPIO output enable is not turned on.
[11:8]	GPIO_Out	0x0	RW	GPIO3~GPIO0 Output Data Register. The output data register will load to the GPIO pin when output enable is set to one.
[15:12]	GPIO_OE	0x0	RW	GPIO3~GPIO0 Output Enable Register. If set to one then GPIO pin is used as output pin. Otherwise, the GPIO is an input pin. 1: Output Enable 0: Disable

6.1.52 Page 4 Offset 0x04: GPIO IRQ Control Register (GPIOCR)

Bit	Name	Default Value	R/W	Function
[3:0]	GPIO_IntEn	0x0	RW	GPIO3~GPIO0 Interrupt Enable Register. Enable GPIO interrupt function when set to one. 1: GPIO Interrupt Enable 0: Disable
[7:4]	GPIO_Int_HL	0x0	RW	GPIO3~GPIO0 Interrupt Polarity Select Register Active high if set to one and Active low if set to zero. 1: Active high interrupt 0: Active low interrupt (Default)
[11:8]	GPIO_Int_Status	0x0	WC	GPIO3~GPIO0 Interrupt Status Register Write one to clear interrupt status bit.
[15:12]	GPIO_Int_Mask	0xf	RW	GPIO3~GPIO0 Interrupt Mask Register Mask Interrupt output when set to one. 1: Interrupt Mask Enable 0: Mask disable

6.1.53 Page 4 Offset 0x06: GPIO Wakeup Control Register (GPIOWCR)

Bit	Name	Default Value	R/W	Function
[1:0]	GPIO_Wakeup_En[1:0]	0x00	RW	GPIO1~GPIO0 Wakeup Enable Register When set to one will enable GPIO Wakeup Function 1: Enable GPIO Wakeup function 0: Disable
[3:2]	Reserved	00	R	Reserved
[7:4]	GPIO_Wakeup_Sel[3:0]	0000	RW	GPIO1~GPIO0 Wakeup Select Register GPIO_Wakeup_Sel[1:0]:GPIO0 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high GPIO_Wakeup_Sel[3:2]:GPIO1 Wakeup Select 00: Falling edge 01: Rising edge 10: Level low 11: Level high
[8]	GPIO1	0	RW	GPIO1 pin selection 1: GPIO1 on AEN pin if GPIOER [1] is set to 1 (GPIO1 enable) 0: GPIO1 on EEDIO pin if GPIOER [1] is set to 1 (GPIO1 enable)
[10:9]	GPIO23	00	RW	GPIO2 and GPIO3 output pin selection Please select correct GPIO2/GPIO3 pins location based on hardware design circuit and also make sure GPIOER [2] or GPIOER [3] is enabled.
[11]	Reserved	0	R	Reserved
[13:12]	GPIO_Wakeup_Status[1:0]	00	R	GPIO1 ~GPIO0 Wakeup Status Register 1: Wakeup State 0: Normal State
[15:14]	Reserved	00	R	Reserved

	GPIO2	GPIO3
00	EECK	EECS
01	SD14	SD15
10	SD6	SD7
11	N/A	N/A

6.1.54 Page 4 Offset 0x0A: SPI Configuration Register (SPICR)

Bit	Name	Default Value	R/W	Function
[0]	SPI_r_compression	0	RW	SPI Register compression 1: Enable 0: Disable
[1]	SPI_q_compression	0	RW	SPI RX/TX Queue Compression 1: Enable 0: Disable
[2]	Reserved	0	RW	Reserved
[3]	RBRE	0	RW	Register Burst Read Enable. 1: It indicates SPI register access at Burst read mode. 0. It indicates SPI register access at Single read mode.
[4]	PMM	0	R	Power management mode. 1: It indicates chip at PMM status (no core clock). 0: It indicates chip at normal operation mode.
[5]	Reserved	0	RW	Reserved
[6:7]	Reserved	00		Reserved
[8]	Loopback	0	RW	SPI loopback mode enable 1: Enable 0: Disable
[9]	Reserved	0	R	Reserved
[10]	SPICoreCLK Reset	1	WC	Reset SPI core clock domain related logic
[11]	SPI SPICLK Reset	1	WC	Reset SPI SPI Clock domain related logic
[15:12]	Reserved	0x000	R	Reserved

6.1.55 Page 4 Offset 0x0C: SPI Interrupt Status and Mask Register (SPIISMR)

Bit	Name	Default Value	R/W	Function
[0]	NWA_P_Int	0	R/WC	Non-Word Access Interrupt for primary SPI: If the data transfer for RXQ/TXQ is Non-word (for example odd bytes), this bit will be asserted. 1: Data access RXQ/TXQ end at odd byte. 0: Data access RXQ/TXQ end at words.
[1]	UDC_P_Int	0	R/WC	Un-Define Command Interrupt for primary SPI: After Slave received un-define command, SPI slave will arise this bit. 1: SPI slave receive un-define command. 0: SPI receive correct command. If SPI slave receive un-define command, it will ignore all TX data in this access.
[2]	NBA_P_Int	0	R/WC	Non-Byte Access Interrput for primary SPI:If the data transfer is Non-byte (for example 1~7 bits), this bit will be asserted. 1: Data access with non-byte edge. 0: Data access with byte edge.
[3]	Reserved	0	R/WC	Reserved.
[4]	Reserved	0	R/WC	Reserved
[5]	Reserved	0	R/WC	Reserved
[6]	Reserved	0	R/WC	Reserved
[7]	Reserved	0	R/WC	Reserved
[8]	Mask NWA_P Int	1	R/W	Primary “Non-Word Access” interrupt Mask bit for primary SPI. 1: Mask Primary Non-word access interrupt. 0: Allow Primary Non-word access interrupt.
[9]	Mask UDC_P Int	1	R/W	Primary “Un-Define Command” interrupt Mask bit for primary SPI. 1:Mask Primary un-define commands interrupt. 0: Allow Primary un-define commands interrupt.
[10]	Mask NBA_P Int	1	R/W	Primary “Non-Byte Access” interrupt Mask bit for primary SPI. 1: Mask Primary Non-byte access interrupt. 0: Allow Primary Non-byte access interrupt.
[11]	Reserved	1	R/W	Reserved
[12]	Reserved	1	R/W	Reserved
[13]	Reserved	1	R/W	Reserved
[14]	Reserved	1	R/W	Reserved
[15]	Reserved	1	R/W	Reserved

6.1.56 Page 4 Offset 0x12: COE RX Control Register 0(COERCR0)

Bit	Name	Default Value	R/W	Function
[0]	RXIPCE	0	RW	Enable Ipv4 checksum check. 1: Enables IP packet checksum check. 0: Disable IP packet checksum check
[1]	RXIPVE	0	RW	Enable IP version check. 1: Enables IP packet version field check. 0: Disables IP packet version field check.
[2]	RXV6PE	0	RW	Enable Ipv6 header parsing function. 1: Enables Ipv6 supporting. 0: Disable Ipv6 supporting.
[3]	RXTCPE	0	RW	Enable TCP packet checksum check in RX path. 1: Enables the TCP packet checksum check function. 0: Disables the TCP packet checksum check function.
[4]	RXUDPE	0	RW	Enable UDP packet checksum check in RX path. 1: Enables the UDP packet checksum check function. 0: Disables the UDP packet checksum check function.
[5]	RXICMP	0	RW	Enable ICMP packet checksum check in RX path. 1: Enables the ICMP packet checksum check function. 0: Disables the ICMP packet checksum check function.
[6]	RXIGMP	0	RW	Enable IGMP packet checksum check in RX path. 1: Enables the IGMP packet checksum check function. 0: Disables the IGMP packet checksum check function.
[7]	RXICV6	0	RW	Enable ICMPv6 packet checksum check in RX path. 1: Enables the ICMPv6 packet checksum check function. 0: Disables the ICMPv6 packet checksum check function.
[8]	RXTCPV6	0	RW	Enable TCP packet checksum check in RX path for Ipv6 packet. 1: Enables the TCP packet checksum check function for Ipv6 packet. 0: Disables the TCP packet checksum check function for Ipv6 packet.
[9]	RXUDPV6	0	RW	Enable UDP packet checksum check in RX path for Ipv6 packet. 1: Enables the UDP packet checksum check function for Ipv6 packet. 0: Disables the UDP packet checksum check function for Ipv6 packet.
[10]	RXICMV6	0	RW	Enable ICMP packet checksum check in RX path for Ipv6 packet. 1: Enables the ICMP packet checksum check function for Ipv6 packet. 0: Disables the ICMP packet checksum check function for Ipv6 packet.
[11]	RXIGMV6	0	RW	Enable IGMP packet checksum check in RX path for Ipv6 packet. 1: Enables the IGMP packet checksum check function for Ipv6 packet. 0: Disables the IGMP packet checksum check function for Ipv6 packet.
[12]	RXICV6V6	0	RW	Enable ICMPv6 packet checksum check in RX path for Ipv6 packet. 1: Enables the ICMPv6 packet checksum check function for Ipv6 packet. 0: Disables the ICMPv6 packet checksum check function for Ipv6 packet.
[14:13]	Reserved	00	RW	Reserved
[15]	FOPC	0	RW	Enable Fixed Offset Partial Checksum mode. 1: Enable Fixed Offset Partial Checksum mode. If enabled this bit, COE RX part will calculate partial checksum from fixed offset 14 (bytes) to the end of packet (CRC is NOT included). Other bits should be disabled when FOPC turned ON. 0: Disable FOPC mode

6.1.57 Page 4 Offset 0x14: COE RX Control Register 1(COERCR1)

Bit	Name	Default Value	R/W	Function
[0]	IPCEDP	0	RW	Drop received packet with IP checksum error. 1: Drop received IP packets with IP checksum error. 0: Do not drop received IP packets with IP checksum error, but indicate checksum error in RX header.
[1]	IPVEDP	0	RW	Drop received packet with IP version error. 1: Drop received IP packets with IP version error. 0: Do not drop received IP packets with IP version error, but indicate version error in RX header.
[2]	V6VEDP	0	RW	Drop received packet with Ipv6 version error. 1: Drop received Ipv6 packets with Ipv6 version error. 0: Do not drop received Ipv6 packets with Ipv6 version error, but indicate version error in RX header.
[3]	TCPEDP	0	RW	Drop received packet with TCP checksum error. 1: Drop received TCP packets with TCP checksum error. 0: Do not drop received TCP packets with TCP checksum error, but indicate checksum error in RX header.
[4]	UDPEDP	0	RW	Drop received packet with UDP checksum error. 1: Drop received UDP packets with UDP checksum error. 0: Do not drop received UDP packets with UDP checksum error, but indicate checksum error in RX header.
[5]	ICMPDP	0	RW	Drop received packet with ICMP checksum error. 1: Drop received ICMP packets with ICMP checksum error. 0: Do not drop received ICMP packets with ICMP checksum error, but indicate checksum error in RX header.
[6]	IGMPDP	0	RW	Drop received packet with IGMP checksum error. 1: Drop received IGMP packets with IGMP checksum error. 0: Do not drop received IGMP packets with IGMP checksum error, but indicate checksum error in RX header.
[7]	ICV6DP	0	RW	Drop received packet with ICMPv6 checksum error. 1: Drop received ICMPv6 packets with ICMPv6 checksum error. 0: Do not drop received ICMPv6 packets with ICMPv6 checksum error, but indicate checksum error in RX header.
[8]	RX64TE	0	RW	Support Ipv6 in Ipv4 tunnel mode. 0: COE will not check L4 checksum in a Ipv6 in Ipv4 tunnel packet. 1: COE will check L4 checksum in a Ipv6 in Ipv4 tunnel packet.
[9]	RXPPPE	0	RW	L2 parser support PPPoE encapsulated packet in RX path. 1: COE support PPPoE encapsulated packet in RX path. 0: COE do not support PPPoE encapsulated packet in RX path.
[10]	TCP6DP	0	RW	Drop received packet with TCP checksum error for Ipv6 packet. 1: Drop received TCP packets with TCP checksum error for Ipv6 packet. 0: Do not drop received TCP packets with TCP checksum error, but indicate checksum error in RX header for Ipv6 packet.
[11]	UDP6DP	0	RW	Drop received packet with UDP checksum error for Ipv6 packet. 1: Drop received UDP packets with UDCP checksum error for Ipv6 packet. 0: Do not drop received UDP packets with UDP checksum error, but indicate checksum error in RX header for Ipv6 packet.
[12]	IC6DP	0	RW	Drop received packet with ICMP checksum error for Ipv6 packet. 1: Drop received ICMP packets with ICMP checksum error for Ipv6 packet. 0: Do not drop received ICMP packets with ICMP checksum error, but indicate checksum error in RX header for Ipv6 packet.
[13]	IG6DP	0	RW	Drop received packet with IGMP checksum error for Ipv6 packet. 1: Drop received IGMP packets with IGMP checksum error for Ipv6 packet. 0: Do not drop received IGMP packets with IGMP checksum error, but indicate checksum error in RX header for Ipv6 packet.
[14]	ICV66DP	0	RW	Drop received packet with ICMPv6 checksum error for Ipv6 packet. 1: Drop received ICMPv6P packets with ICMPv6 checksum error for Ipv6 packet. 0: Do not drop received ICMPv6 packets with ICMPv6

				checksum error, but indicate checksum error in RX header for Ipv6 packet.
[15]	Reserved	0	RW	Reserved

6.1.58 Page 4 Offset 0x16: COE TX Control Register 0(COETCR0)

Bit	Name	Default Value	R/W	Function
[0]	TXIP	0	RW	Enable Ipv4 checksum insertion function. 1: Enables Ipv4 packet checksum insertion function. 0: Disables Ipv4 packet checksum insertion function.
[1]	TXTCP	0	RW	Enable TCP checksum insertion function. 1: Enables TCP packet checksum insertion function. 0: Disables TCP packet checksum insertion function.
[2]	TXUDP	0	RW	Enable UDP checksum insertion function. 1: Enables UDP packet checksum insertion function. 0: Disables UDP packet checksum insertion function.
[3]	TXICMP	0	RW	Enable ICMP checksum insertion function. 1: Enables ICMP packet checksum insertion function. 0: Disables ICMP packet checksum insertion function.
[4]	TXIGMP	0	RW	Enable IGMP checksum insertion function. 1: Enables IGMP packet checksum insertion function. 0: Disables IGMP packet checksum insertion function.
[5]	TXICV6	0	RW	Enable ICMPv6 checksum insertion function. 1: Enables ICMPv6 packet checksum insertion function. 0: Disables ICMPv6 packet checksum insertion function.
[7:6]	Reserved	0	RW	Reserved
[8]	TXTCPV6	0	RW	Enable TCP checksum insertion function for Ipv6 packet. 1: Enables TCP packet checksum insertion function for Ipv6 packet. 0: Disables TCP packet checksum insertion function for Ipv6 packet.
[9]	TXUDPv6	0	RW	Enable UDP checksum insertion function for Ipv6 packet. 1: Enables UDP packet checksum insertion function for Ipv6 packet. 0: Disables UDP packet checksum insertion function for Ipv6 packet.
[10]	TXICMV6	0	RW	Enable ICMP checksum insertion function for Ipv6 packet. 1: Enables ICMP packet checksum insertion function for Ipv6 packet. 0: Disables ICMP packet checksum insertion function for Ipv6 packet.
[11]	TXIGMV6	0	RW	Enable IGMP checksum insertion function for Ipv6 packet. 1: Enables IGMP packet checksum insertion function for Ipv6 packet. 0: Disables IGMP packet checksum insertion function for Ipv6 packet.
[12]	TXICV6V6	0	RW	Enable ICMPv6 checksum insertion function for Ipv6 packet. 1: Enables ICMPv6 packet checksum insertion function for Ipv6 packet. 0: Disables ICMPv6 packet checksum insertion function for Ipv6 packet.
[15:13]	Reserved	000	RW	Reserved

6.1.59 Page 4 Offset 0x18: COE TX Control Register 1(COETCR1)

Bit	Name	Default Value	R/W	Function
[0]	TX64TE	0	RW	Support Ipv6 in Ipv4 tunnel mode. 0: COE will not insert L4 checksum in a Ipv6 in Ipv4 tunnel packet. 1: COE will insert L4 checksum in a Ipv6 in Ipv4 tunnel packet.
[1]	TXPPPE	0	RW	L2 parser support PPPoE encapsulated packet in TX path. 0: COE support PPPoE encapsulated packet in TX path. 0: COE do not support PPPoE encapsulated packet in TX path.
[15:2]	Reserved	0	RW	Reserved

6.1.60 Page 5 Offset 0x02: Wakeup Frame Timer Register (WFTR)

Bit	Name	Default Value	R/W	Function
[3:0]	WKTimer[3:0]	00	RW	Mask Wakeup Timer: Mask wakeup event trigger to host timer.(Due to some system took a long time to enter suspend state) NOTE: Make sure change the setting to 0xC or oxD when the AX88796C is in the wakeup mode and power saving function is turn on this will help when the chip change the speed to reduce the power consumption when unplug the cable.
[15:4]	Reserved	0x000	RW	Reserved

[3:0]	Delay	TimeUnit
0000	0	ms
0001	2	ms
0010	4	ms
0011	8	ms
0100	16	ms
0101	32	ms
0110	64	ms
0111	128	ms
1000	256	ms
1001	512	ms
1010	1024	ms
1011	2048	ms
1100	4096	ms
1101	8192	ms
1110	16384	ms
1111	32768	ms

6.1.61 Page 5 Offset 0x04: Wakeup Frame Cascade Command Register (WFCCR)

Bit	Name	Default Value	R/W	Function
[6:0]	WFCSCD	00	RW	Byte Mask Cascade Command for wake-up frame filter Bit-0: cascade wake-up filter 1 and 0 Bit-1: cascade wake-up filter 2 and 1 Bit-2: cascade wake-up filter 3 and 2 Bit-3: cascade wake-up filter 4 and 3 Bit-4: cascade wake-up filter 5 and 4 Bit-5: cascade wake-up filter 6 and 5 Bit-6: cascade wake-up filter 7 and 6 Note: (1) If both Bit 0 and Bit 1 set '1', Byte Mask 2 and Byte Mask 1 and Byte Mask 0 are cascaded to become one wake-up frame filter that allows defining up to 96 masked bytes. (2) If both Bit 1 and Bit 2 set '1', Byte Mask 3 and Byte Mask 2 and Byte Mask 1 are cascaded to become one wake-up frame filter that allows defining up to 96 masked bytes. (3) If Bit 3 ~ Bit 0 set '1', Byte Mask 3 ~Byte Mask 0 are cascaded to become one wake-up frame filter that allows defining up to 128 masked bytes. (4) If Bit 6 ~ Bit 0 set '1', Byte Mask 7 ~Byte Mask 0 are cascaded to become one wake-up frame filter that allows defining up to 256 masked bytes maximum.
[7]	Reserved	0	RW	Reserved
[8]	DA Match	0	RW	1: DA match only enable. When receiving frame has DA matching Node ID register, then the packet is considered as valid wakeup frame. 0: DA match only disable.
[9]	MC Match	0	RW	1: Multicast address match only enable. When receiving frame is a multicast frame and meets Multicast Filter Array, the packet is considered as valid wakeup frame. 0: Multicast address match only disable.
[15:10]	Reserved	00	RW	Reserved

6.1.62 Page 5 Offset 0x06: Wakeup Frame Command 0 ~ 3 Register (WFCR03)

Bit	Name	Default Value	R/W	Function
[3:0]	WFCMD0	0x0	RW	Byte Mask Command for wake-up frame filter 0. Host continue write 4 times to completed 32-bits of Byte Mask Command of 3, 2, 1, 0 filter and Mask cascade commend. Bit0: wake-up frame filter enable 1: Enable. 0: Disable. Bit1: destination match enable 1: The DA field of received packet will be compared with the MAC address of AX88796C. When receiving frame with DA matching Node ID register and the wakeup frame filter is also matched, then the packet is considered as valid wakeup frame. 0: When receiving frame with any DA value and the wakeup frame filter is matched, then the packet is considered as valid wakeup frame. Bit2: Multicast match enable 1: The DA field of received packet will be examined if it is a multicast frame and compared with the Multicast Filter Array. When receiving frame is a multicast frame, meets Multicast Filter Array, and also matches the wakeup frame filter, the packet is considered as valid wakeup frame. 0: When receiving frame with any DA value matches the wakeup frame filter, the packet is considered as valid wakeup frame. Bit3: Microsoft Windows 7 ARP and NS offload function enable 1:Enable Microsoft Windows 7 ARP and NS offload function function 0:disable Microsoft Windows 7 ARP and NS offload function function
[7:4]	WFCMD1	0x0	RW	Byte Mask Command for wake-up frame filter 1.
[11:8]	WFCMD2	0x0	RW	Byte Mask Command for wake-up frame filter 2.
[15:12]	WFCMD3	0x0	RW	Byte Mask Command for wake-up frame filter 3.

6.1.63 Page 5 Offset 0x08: Wakeup Frame Command 4 ~ 7 Register (WFCR47)

Bit	Name	Default Value	R/W	Function
[3:0]	WFCMD4	0x0	RW	Byte Mask Command for wake-up frame filter 0. Host continue write 4 times to completed 32-bits of Byte Mask Command of 7, 6, 5, 4 filter and Mask cascade commend. Bit0: wake-up frame filter enable Bit1: destination match enable Bit2: Multicast match enable Bit3: Microsoft Windows 7 ARP and NS offload function enable 1:Enable Microsoft Windows 7 ARP and NS offload function function 0:disable Microsoft Windows 7 ARP and NS offload function function
[7:4]	WFCMD5	0x0	RW	Byte Mask Command for wake-up frame filter 5.
[11:8]	WFCMD6	0x0	RW	Byte Mask Command for wake-up frame filter 6.
[15:12]	WFCMD7	0x0	RW	Byte Mask Command for wake-up frame filter 7.

6.1.64 Page 5 Offset 0x0A: Wakeup Frame 0 Byte Mask [15:0] Register (WF0BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM0 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 0 [15:0]

6.1.65 Page 5 Offset 0x0C: Wakeup Frame 0 Byte Mask [31:16] Register (WF0BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM0 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 0 [31:16]

6.1.66 Page 5 Offset 0x0E: Wakeup Frame 0 CRC Register (WF0CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC0	0x0000	RW	Byte mask CRC for wake-up frame filter 0. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.67 Page 5 Offset 0x10: Wakeup Frame 0 Offset Byte Register (WF0OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB0	0x00	RW	Byte mask Offset for wake-up frame filter 0. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB0	0x00	RW	Mask Last Byte for wake-up frame filter 0. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.68 Page 5 Offset 0x12: Wakeup Frame 1 Byte Mask [15:0] Register (WF1BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM1 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 1 [15:0]

6.1.69 Page 5 Offset 0x14: Wakeup Frame 1 Byte Mask [31:16] Register (WF1BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM1 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 1 [31:16]

6.1.70 Page 5 Offset 0x16: Wakeup Frame 1 CRC Register (WF1CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC1	0x0000	RW	Byte mask CRC for wake-up frame filter 1. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.71 Page 5 Offset 0x18: Wakeup Frame 1 Offset Byte Register (WF1OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB1	0x00	RW	Byte mask Offset for wake-up frame filter 1. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB1	0x00	RW	Mask Last Byte for wake-up frame filter 1. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.72 Page 5 Offset 0x1A: Wakeup Frame 2 Byte Mask [15:0] Register (WF2BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM2 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 2 [15:0]

6.1.73 Page 5 Offset 0x1C: Wakeup Frame 2 Byte Mask [31:16] Register (WF2BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM2 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 2 [31:16]

6.1.74 Page 6 Offset 0x02: Wakeup Frame 2 CRC Register (WF2CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC2	0x0000	RW	Byte mask CRC for wake-up frame filter 2. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.75 Page 6 Offset 0x04: Wakeup Frame 2 Offset Byte Register (WF2OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB2	0x00	RW	Byte mask Offset for wake-up frame filter 2. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB2	0x00	RW	Mask Last Byte for wake-up frame filter 2. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.76 Page 6 Offset 0x06: Wakeup Frame 3 Byte Mask [15:0] Register (WF3BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM3 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 3 [15:0]

6.1.77 Page 6 Offset 0x08: Wakeup Frame 3 Byte Mask [31:16] Register (WF3BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM3 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 3 [31:16]

6.1.78 Page 6 Offset 0x0A: Wakeup Frame 3 CRC Register (WF3CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC3	0x0000	RW	Byte mask CRC for wake-up frame filter 3. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.79 Page 6 Offset 0x0C: Wakeup Frame 3 Offset Byte Register (WF3OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB3	0x00	RW	Byte mask Offset for wake-up frame filter 3. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB3	0x00	RW	Mask Last Byte for wake-up frame filter 3. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.80 Page 6 Offset 0x0E: Wakeup Frame 4 Byte Mask [15:0] Register (WF4BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM4 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 4 [15:0]

6.1.81 Page 6 Offset 0x10: Wakeup Frame 4 Byte Mask [31:16] Register (WF4BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM4 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 4 [31:16]

6.1.82 Page 6 Offset 0x12: Wakeup Frame 4 CRC Register (WF4CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC4	0x0000	RW	Byte mask CRC for wake-up frame filter 4. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.83 Page 6 Offset 0x14: Wakeup Frame 4 Offset Byte Register (WF4OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB4	0x00	RW	Byte mask Offset for wake-up frame filter 4. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB4	0x00	RW	Mask Last Byte for wake-up frame filter 4. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.84 Page 6 Offset 0x16: Wakeup Frame 5 Byte Mask [15:0] Register (WF5BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM5 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 5 [15:0]

6.1.85 Page 6 Offset 0x18: Wakeup Frame 5 Byte Mask [31:16] Register (WF5BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM5 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 5 [31:16]

6.1.86 Page 6 Offset 0x1A: Wakeup Frame 5 CRC Register (WF5CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC5	0x0000	RW	Byte mask CRC for wake-up frame filter 5. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.87 Page 6 Offset 0x1C: Wakeup Frame 5 Offset Byte Register (WF5OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB5	0x00	RW	Byte mask Offset for wake-up frame filter 5. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB5	0x00	RW	Mask Last Byte for wake-up frame filter 5. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.88 Page 7 Offset 0x02: Wakeup Frame 6 Byte Mask [15:0] Register (WF6BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM6 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 6 [15:0]

6.1.89 Page 7 Offset 0x04: Wakeup Frame 6 Byte Mask [31:16] Register (WF6BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM6 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 6 [31:16]

6.1.90 Page 7 Offset 0x06: Wakeup Frame 6 CRC Register (WF6CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC6	0x0000	RW	Byte mask CRC for wake-up frame filter 6. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.91 Page 7 Offset 0x08: Wakeup Frame 6 Offset Byte Register (WF6OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB6	0x00	RW	Byte mask Offset for wake-up frame filter 6. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB6	0x00	RW	Mask Last Byte for wake-up frame filter 6. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.92 Page 7 Offset 0x0A: Wakeup Frame 7 Byte Mask [15:0] Register (WF7BMR0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM7 [15:0]	0x0000	RW	Byte mask for wake-up frame filter 7 [15:0]

6.1.93 Page 7 Offset 0x0C: Wakeup Frame 7 Byte Mask [31:16] Register (WF7BMR1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFBM7 [31:16]	0x0000	RW	Byte mask for wake-up frame filter 7 [31:16]

6.1.94 Page 7 Offset 0x0E: Wakeup Frame 7 CRC Register (WF7CR)

Bit	Name	Default Value	R/W	Function
[15:0]	WFCRC7	0x0000	RW	Byte mask CRC for wake-up frame filter 7. Based on desired wakeup frame patterns, software should calculate CRC-16 and set it here. The value is used to compare with the CRC-16 calculated on the incoming frame on the bytes defined by Byte Mask 0~7. When matched and the Last Byte 0~7 is also matched, then the frame is considered as a valid wakeup frame. CRC-16 Polynomials = X^16 + X^15 + X^2 + 1. If wakeup frame filters are cascaded, the Wakeup Frame CRC must be cumulatively calculated. The last CRC value is used for verification.

6.1.95 Page 7 Offset 0x10: Wakeup Frame 7 Offset Byte Register (WF7OBR)

Bit	Name	Default Value	R/W	Function
[7:0]	WFOB7	0x00	RW	Byte mask Offset for wake-up frame filter 7. This defines the offset of the first byte in the incoming frame from which the CRC-16 is calculated for the wakeup frame recognition. Each offset value represents two bytes in the frame. For example: The offset value of 0 is the first byte of the incoming frame's destination address. The offset value of 1 is the 3rd byte of the incoming frame, etc.
[15:8]	WFLB7	0x00	RW	Mask Last Byte for wake-up frame filter 7. This 1-byte pattern is used to compare the last masked byte in the incoming frame. The last masked byte is the byte of the last bit mask being 1 in Byte Mask 0~7. A valid wakeup frame shall have match condition on both Wakeup Frame 0~7 CRC and Last Byte 0~7. If wake-up frame filters are cascaded, the Last Byte for the last cascaded wake-up frame filter is used to verify correctness.

6.1.96 Page 7 Offset 0x12: Wakeup Frame Reply 0 ~ 1 Register (WFR01)

Bit	Name	Default Value	R/W	Function
[7:0]	WFR0 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.
[15:8]	WFR1 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.

6.1.97 Page 7 Offset 0x14: Wakeup Frame Reply 2 ~ 3 Register (WFR23)

Bit	Name	Default Value	R/W	Function
[7:0]	WFR2 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.
[15:8]	WFR3 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.

6.1.98 Page 7 Offset 0x16: Wakeup Frame Reply 4 ~ 5 Register (WFR45)

Bit	Name	Default Value	R/W	Function
[7:0]	WFR4 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.
[15:8]	WFR5 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.

6.1.99 Page 7 Offset 0x18: Wakeup Frame Reply 6 ~ 7 Register (WFR67)

Bit	Name	Default Value	R/W	Function
[7:0]	WFR6 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.
[15:8]	WFR7 [7:0]	0x00	RW	Reply TX Page point: Bit 4~0: The power management offload auto reply packet was stored in different page of TX buffer SRAM. Bit 6~5: Reply type. 00: Original packet in TX buffer. 01: Neighbor advertisement (partial checksum 0). 10: Neighbor advertisement (partial checksum 1). 11: ARP.

6.1.100 Page 7 Offset 0x1A: Wakeup Frame Partial Checksum 0 Register (WFPC0)

Bit	Name	Default Value	R/W	Function
[15:0]	WFPC0 [7:0]	0x00	RW	Calculated partial checksum of neighbor advertisement packet.

6.1.101 Page 7 Offset 0x1C: Wakeup Frame Partial Checksum 1 Register (WFPC1)

Bit	Name	Default Value	R/W	Function
[15:0]	WFPC1 [7:0]	0x00	RW	Calculated partial checksum of neighbor advertisement packet.

6.2 PHY Register Detailed Description

The MII management 16-bit register set implemented is as follows. And the following sub-section will describes each field of the registers.

Address	Name	Description	Default value
0	MR0	Control	0x3100
1	MR1	Status	0x7809
2	MR2	PHY Identifier 1	0x003B
3	MR3	PHY Identifier 2	0x1891
4	MR4	Auto-negotiation Advertisement	0x01E1
5	MR5	Auto-negotiation Link Partner Ability	0x0000
6	MR6	Auto-negotiation Expansion	0x0000

TAB - 15 THE EMBEDDED PHY REGISTERS

Key to default:

Reset value
- 1: Bit set to logic one
- 0: Bit set to logic zero
- X: No set value

Access type
- RO: Read only
- RW: Read or write

Attribute
- SC: Self-clearing
- PS: Value is permanently set
- LL: Latch low
- LH: Latch high

6.2.1 MR0: Basic Mode Control Register

Address 00h

Bit	Bit Name	Default	Description
15	Reset	0, RW	Reset: 1: Software reset 0: Normal operation
14	Loopback	0, RW	Loopback: 1: Loopback enabled 0: Normal operation
13	Speed selection	1, RW	Speed selection: 1: 100 Mb/s 0: 10 Mb/s This bit must set to 1 while bit 12 (Auto-negotiation enable) is set to 1.
12	Auto-negotiation enable	1, RW	Auto-negotiation enable: 1: Auto-negotiation enabled. Bit 8 of this register is ignored and Bit 13 of this register must set to 1. 0: Auto-negotiation disabled. Bits 8 and 13 of this register determine the link speed and mode.
11	Power down	0, RW	Power down: 1: Power down 0: Normal operation
10	Isolate	(PHYAD = 00000), RW	Isolate: 1: Isolate 0: Normal operation
9	Restart auto-negotiation	0, RW / SC	Restart auto-negotiation: 1: Restart auto-negotiation 0: Normal operation
8	Duplex mode	1, RW	Duplex mode: 1: Full duplex operation 0: Normal operation
7	Collision test	0, RW	Collision test: 1: Collision test enabled 0: Normal operation
6:0	Reserved	X, RO	Reserved: Write as 0, read as “don’t care”.

6.2.2 MR1: Basic Mode Status Register

Address 01h

Bit	Bit Name	Default	Description
15	100BASE-T4	0, RO / PS	100BASE-T4 capable: 0: This PHY is not able to perform in 100BASE-T4 mode.
14	100BASE-TX full duplex	1, RO / PS	100BASE-TX full-duplex capable: 1: This PHY is able to perform in 100BASE-TX full-duplex mode.
13	100BASE-TX half duplex	1, RO / PS	100BASE-TX half-duplex capable: 1: This PHY is able to perform in 100BASE-TX half-duplex mode.
12	10BASE-T full duplex	1, RO / PS	10BASE-T full-duplex capable: 1: This PHY is able to perform in 10BASE-T full-duplex mode.
11	10BASE-T half duplex	1, RO / PS	10BASE-T half-duplex capable: 1: This PHY is able to perform in 10BASE-T half-duplex mode.
10:7	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
6	MF preamble suppression	0, RO / PS	Management frame preamble suppression: 0: This PHY will not accept management frames with preamble suppressed.
5	Auto-negotiation complete	0, RO	Auto-negotiation completion: 1: Auto-negotiation process completed 0: Auto-negotiation process not completed
4	Remote fault (Not supported)	0, RO / LH	Remote fault: 1: Remote fault condition detected (cleared on read or by a chip reset) 0: No remote fault condition detected
3	Auto-negotiation ability	1, RO / PS	Auto configuration ability: 1: This PHY is able to perform auto-negotiation.
2	Link status	0, RO / LL	Link status: 1: Valid link established (100Mb/s or 10Mb/s operation) 0: Link not established
1	Jabber detect	0, RO / LH	Jabber detection: 1: Jabber condition detected 0: No Jabber condition detected
0	Extended capability	1, RO / PS	Extended capability: 1: Extended register capable 0: Basic register capable only

6.2.3 MR2: PHY Identifier Register 1

Address 02h

Bit	Bit Name	Default	Description
15:0	OUI_MSB	0x003B, RO / PS	OUI most significant bits: Bits 3 to 18 of the OUI are mapped to bits 15 to 0 of this register respectively. The most significant two bits of the OUI are ignored.

6.2.4 MR3: PHY Identifier Register 2

Address 03h

Bit	Bit Name	Default	Description
15:10	OUI_LSB	00_0110, RO / PS	OUI least significant bits: Bits 19 to 24 of the OUI are mapped to bits 15 to 10 of this register respectively.
9:4	VNDR_MDL	00_1001, RO / PS	Vendor model number.
3:0	MDL_REV	0001, RO / PS	Model revision number.

6.2.5 MR4: Auto Negotiation Advertisement Register

Address 04h

Bit	Bit Name	Default	Description
15	NP	0, RO / PS	Next page indication: 0: No next page available. The PHY does not support the next page function.
14	ACK	0, RO	Acknowledgement: 1: Link partner ability data reception acknowledged 0: Not acknowledged
13	RF	0, RW	Remote fault: 1: Fault condition detected and advertised 0: No fault detected
12:11	Reserved	X, RW	Reserved. Write as 0, read as “don’t care”.
10	Pause	1, RW	Pause: 1: Pause operation enabled for full-duplex links 0: Pause operation not enabled
9	T4	0, RO/PS	100BASE-T4 support: 0: 100BASE-T4 not supported
8	TX_FD	1, RW	100BASE-TX full-duplex support: 1: 100BASE-TX full-duplex supported by this device 0: 100BASE-TX full-duplex not supported by this device
7	TX_HD	1, RW	100BASE-TX half-duplex support: 1: 100BASE-TX half-duplex supported by this device 0: 100BASE-TX half-duplex not supported by this device
6	10_FD	1, RW	10BASE-T full-duplex support: 1: 10BASE-T full-duplex supported by this PHY 0: 10BASE-T full-duplex not supported by this PHY
5	10_HD	1, RW	10BASE-T half-duplex support: 1: 10BASE-T half-duplex supported by this PHY 0: 10BASE-T half-duplex not supported by this PHY
4:0	Selector	0_0001, RW	Protocol selection bits: These bits contain the binary encoded protocol selector supported by this PHY. [0 0001] indicates that this PHY supports IEEE 802.3u CSMA/CD.

6.2.6 MR5: Auto Negotiation Link Partner Ability Register

Address 05h

Bit	Bit Name	Default	Description
15	NP	0, RO	Next page indication: 1: Link partner next page enabled 0: Link partner not next page enabled
14	ACK	0, RO	Acknowledgement: 1: Link partner ability for reception of data word acknowledged 0: Not acknowledged
13	RF	0, RO	Remote fault: 1: Remote fault indicated by link partner 0: No remote fault indicated by link partner
12:11	Reserved	X, RO	Reserved. Write as 0, read as “don’t care”.
10	Pause	0, RO	Pause: 1: Pause operation supported by link partner 0: Pause operation not supported by link partner
9	T4	0, RO	100BASE-T4 support: 1: 100BASE-T4 supported by link partner 0: 100BASE-T4 not supported by link partner
8	TX_FD	0, RO	100BASE-TX full-duplex support: 1: 100BASE-TX full-duplex supported by link partner 0: 100BASE-TX full-duplex not supported by link partner
7	TX_HD	0, RO	100BASE-TX half-duplex support: 1: 100BASE-TX half-duplex supported by link partner 0: 100BASE-TX half-duplex not supported by link partner
6	10_FD	0, RO	10BASE-T full-duplex support: 1: 10BASE-T full-duplex supported by link partner 0: 10BASE-T full-duplex not supported by link partner
5	10_HD	0, RO	10BASE-T half-duplex support: 1: 10BASE-T half-duplex supported by link partner 0: 10BASE-T half-duplex not supported by link partner
4:0	Selector	0_0000, RO	Protocol selection bits: Link partner’s binary encoded protocol selector.

6.2.7 MR6: Auto Negotiation Expansion Register

Address 06h

Bit	Bit Name	Default	Description
15:5	Reserved	0, RO	Reserved. Write as 0, read as “don’t care”.
4	PDF	0, RO / LH	Parallel detection fault: 1: Fault detected via the parallel detection function 0: No fault detected
3	LP_NP_AB	0, RO	Link partner next page enable: 1: Link partner next page enabled 0: Link partner not next page enabled
2	NP_AB	0, RO / PS	PHY next page enable: 0: PHY not next page enabled
1	Page_RX	0, RO / LH	New page reception: 1: New page received 0: New page not received
0	LP_AN_AB	0, RO	Link partner auto-negotiation enable: 1: Auto-negotiation supported by link partner

7.0 Electrical Specifications

7.1 DC Characteristics

7.1.1 Absolute Maximum Ratings

Description	Rating	Units
VCCK (Core power supply)	-0.3 to 2.16	V
VCCIO (power supply for 3.3/2.5/1.8V I/O)	-0.3 to 4.0	V
VCCIO (Input voltage of 3.3/2.5/1.8V I/O)	-0.3 to 4.0	V
Storage Temperature	-65 to 150	°C
I_{IN} (DC input current)	20	mA
I_{OUT} (Output short circuit current)	20	mA

7.1.2 General Operating Condition

Description	Symbol	Min	Typ	Max	Units
Operating Temperature	Ta	0		70	°C
		-40		85	
Junction Temperature	Tj	-40	+25	+125	°C
Supply Voltage for core (VCCK, VCC18A)	VCC18	+1.62	+1.8	+1.98	V
Supply Voltage (VCC3A3, VCC3R3)	VCC33	+2.97	+3.30	+3.63	V

7.1.3 DC Characteristics of 3.3V I/O (VCCIO = 3.3V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCCIO	Power supply of 3.3V I/O	3.3V I/O	2.97	3.3	3.63	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	LVTTL spec.			0.8	V
Vih	Input high voltage		2.0			V
Vt-	Schmitt-trigger negative threshold voltage	LVTTL spec.	0.8			V
Vt+	Schmitt-trigger negative threshold voltage				2.0	
Vol	Output low voltage	Iol = 2 ~ 12 mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -2 ~ -12 mA	2.4	-	-	V
Rpu	Input pull-up resistance	Vin = 0V	40	75	190	KΩ
Rpd	Input pull-down resistance	Vin = VCCIO	40	75	190	KΩ
Iin	Input leakage current	Vin = VCCIO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-15	-45	-90	μA
	Input leakage current with pull-down resistance	Vin = VCCIO	15	45	90	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

7.1.4 DC Characteristics of 2.5V I/O (VCCIO = 2.5V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCCIO	Power supply of 2.5V I/O	2.5V I/O	2.25	2.5	2.75	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	CMOS spec.			0.25* VCCIO	V
Vih	Input high voltage		0.625* VCCIO			V
Vt-	Schmitt-trigger negative threshold voltage	CMOS spec.	0.25* VCCIO			V
Vt+	Schmitt-trigger negative threshold voltage				0.625* VCCIO	
Vol	Output low voltage	Iol =1.1 ~ 6.68mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -1.1 ~ -6.6mA	1.85	-	-	V
Rpu	Input pull-up resistance	Vin = 0V	40	110	290	KΩ
Rpd	Input pull-down resistance	Vin = VCCIO	40	110	290	KΩ
Iin	Input leakage current	Vin = VCCIO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-7	-23	-62	μA
	Input leakage current with pull-down resistance	Vin = VCCIO	7	23	62	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

7.1.5 DC Characteristics of 1.8 V I/O (VCCIO = 1.8V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VCCIO	Power supply of 1.8V I/O	1.8V I/O	1.62	1.8	1.98	V
VCCK	Power supply of internal core cells and I/O-to-core interface	1.8V	1.62	1.8	1.98	V
Tj	Junction temperature		-40	25	125	℃
Vil	Input low voltage	CMOS spec.			0.3* VCCIO	V
Vih	Input high voltage		0.7* VCCIO			V
Vt-	Schmitt-trigger negative threshold voltage	CMOS spec.	0.3* VCCIO			V
Vt+	Schmitt-trigger negative threshold voltage				0.7* VCCIO	
Vol	Output low voltage	Iol = 0.7 ~ 4.2mA	-	-	0.4	V
Voh	Output high voltage	Ioh = -0.7 ~ -4.2mA	0.7* VCCIO	-	-	V
Rpu	Input pull-up resistance	Vin = 0V	80	200	510	KΩ
Rpd	Input pull-down resistance	Vin = VCCIO	80	200	510	KΩ
Iin	Input leakage current	Vin = VCCIO or 0V	-5	±1	5	μA
	Input leakage current with pull-up resistance	Vin = 0V	-3	-9	-25	μA
	Input leakage current with pull-down resistance	Vin = VCCIO	3	9	25	μA
I_{OZ}	Tri-state output leakage current		-10	±1	10	μA

7.1.6 DC Characteristics of Voltage Regulator

Symbol	Description	Conditions	Min	Typ	Max	Unit
VCC3R3	Power supply of on-chip voltage regulator.		3.0	3.3	3.9	V
Tj	Operating junction temperature.		-4 0	25	125	℃
Iload	Driving current.	Normal operation	-	-	150	mA
V18F	Output voltage of on-chip voltage regulator.	VCC3R3 = 3.3V	1.71	1.8	1.89	V
Vdrop	Dropout voltage.	∆ V18F = -1%, Iload = 10mA	-	-	0.2	V
△V18F / (△VCC3R3 x V18F)	Line regulation.	VCC3R3 = 3.3V, Iload = 10mA	-	0.2	0.4	%/V
△V18F / (△Iload x V18F)	Load regulation.	VCC3R3 = 3.3V, 1mA ≦ Iload ≦ 150mA	-	0.02	0.05	%/mA
△V18F / △Tj	Temperature coefficient.	VCC3R3 = 3.3V, -40℃ ≦ Tj ≦ 125℃	-	0.4	-	mV/℃
Iq_25℃	Quiescent current at 25 ℃.	VCC3R3 = 3.3V	-	66	96	µA
Iq_125℃	Quiescent current at 125 ℃.	VCC3R3 = 3.3V	-	82	120	µA
Cout	Output external capacitor.		-	3.3	-	MF
ESR	Allowable effective series resistance of external capacitor.		-	0.5	1	Ω

7.2 Thermal Characteristics

Description	Symbol	Rating	Units
Thermal resistance of junction to case	ΘJC	18.7	℃/W
Thermal resistance of junction to ambient	ΘJA	49.2	℃/W

Note: θ_{JA} , θ_{JC} defined as below

$$\theta_{JA} = \frac{T_J - T_A}{P}, \quad \theta_{JC} = \frac{T_J - T_C}{P}$$

T_J: maximum junction temperature
T_A: ambient or environment temperature
T_C: the top center of compound surface temperature
P: input power (watts)

7.3 Power Consumption

- **Device only**

Power measurements base on 3.3V/25 ℃ condition.

Item	Symbol	10BASE-T		100BASE-TX		Cable-Off Power Saving Mode		Wake-On-LAN		Sleep Mode	Units
		Idle	Full Op.	Idle	Full Op.	PS1	PS2	10M	100M		
1	VCCIO	6	6	5	5	2	1	1	5	0.04	mA
2	VCC3A3	14	14	13	13	10	4	10	13	0.06µ	mA
3	VCC3R3*	24	25	78	79	20	2	17	75	0.09	mA
4	VCCK	18	18	40	40	15	1	12	37	<0	mA
5	VCC18A	6	7	38	39	5	1	5	38	<0	mA
6	Total	44	45	96	97	32	7	28	93	0.14	mA
		145	149	317	320	106	23	92	307	0.45	mW

*NOTE: The VCC3R3 current includes the VCCK and VCC18A current.

TAB - 16 DEVICE POWER CONSUMPTION TABLE

- **Device and system components**

  This is the total of Ethernet connectivity solution, which includes external components supporting the AX88796C Ethernet controller as shown in the schematic as below. Power measurements base on 3.3V/25 ℃ condition.

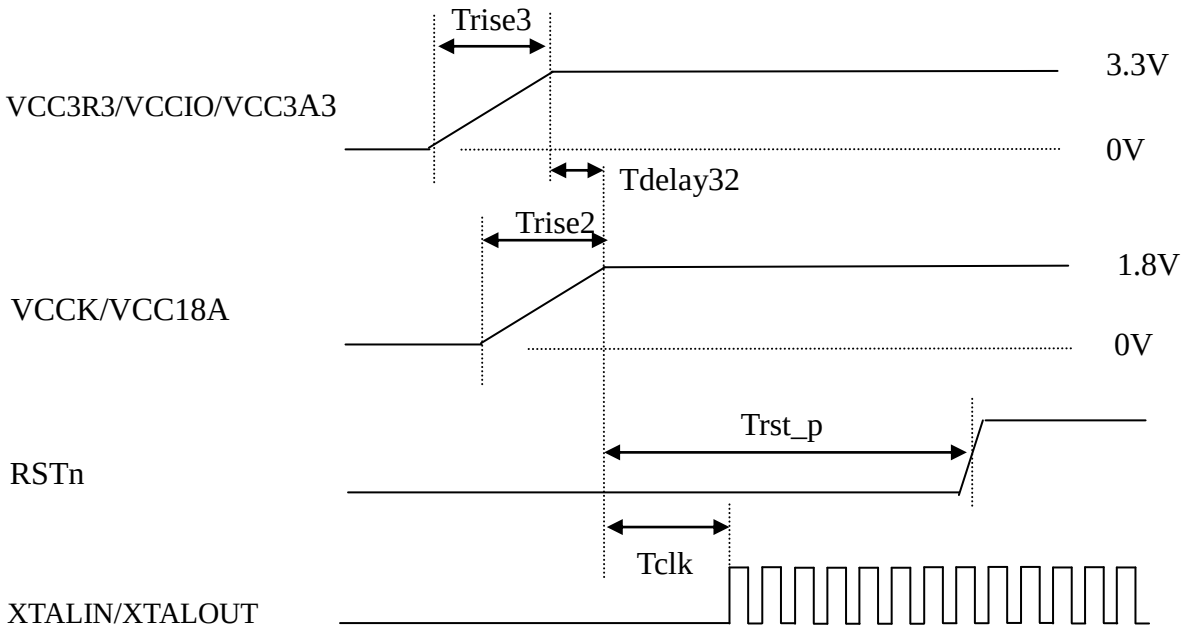
Item	Test Conditions	Total Power (Typical)	Units
1	10BASE-T operation (Full Operation)	479 *	mW
2	100BASE-TX operation (Full Operation)	452 *	mW
3	Cable Unplug Power Saving mode 1 (PS1)	106	mW
4	Cable Unplug Power Saving mode 2 (PS2)	23	mW
5	WOL Power Saving Mode (10M)	92	mW
6	WOL Power Saving Mode (100M)	438 *	mW
7	Sleep mode	0.45	mW

*NOTE: Single port's transformer consumes an additional 40mA @ 3.3V for 100BASE-TX and 100mA @ 3.3V for 10BASE-T.

TAB - 17 SYSTEM POWER CONSUMPTION TABLE

7.4 Power-up Sequence

At power-up, the AX88796C requires the VCC3R3/VCCIO/VCC3A3 power supply to rise to nominal operating voltage within Trise3 and the V18F/VCCK power supply to rise to nominal operating voltage within Trise2.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
Trise3	3.3V power supply rise time	From 0V to 3.3V	1		10	ms
Trise2	1.8V power supply rise time	From 0V to 1.8V	-		10	ms
$T_{delay32}$	3.3V rise to 1.8V rise time delay		-5	-	5	ms
T_{clk}	25MHz crystal oscillator start-up time	From VCC18A = 1.8V to first clock transition of XTALIN or XTALOUT	-	1	-	ms
T_{rst_pu}	RSTn low level interval time from power-up	From VCCK/VCC18A = 1.8V and VCC3IO = 3.3V to RSTn going high	T_{clk} + Trst *1	-	-	ms

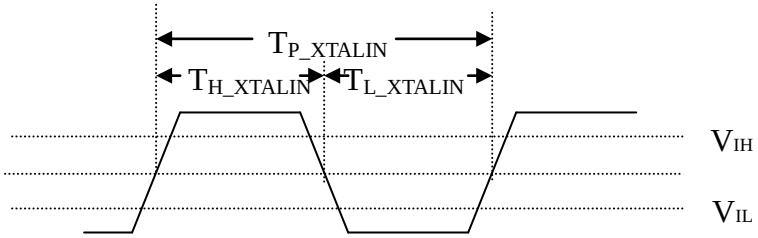
*1 : Please refer to 7.5.2 Reset Timing for the details about the Trst.

7.5 AC Timing Characteristics

Notice that the following AC timing specifications for output pins are based on
C_L (Output load)=25pF if VCCIO = 3.3V with 10% margin
C_L (Output load)=10pF if VCCIO = 1.8V or 2.5V with 10% margin

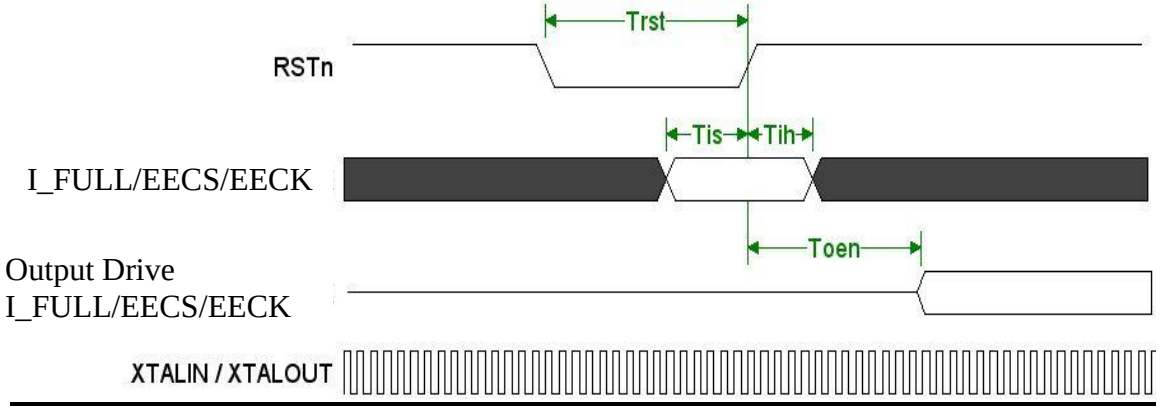
7.5.1 Clock Timing

XTALIN



Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_XTALIN}	XTALIN clock cycle time		-	40.0	-	ns
T_{H_XTALIN}	XTALIN clock high time		-	20.0	-	ns
T_{L_XTALIN}	XTALIN clock low time		-	20.0	-	ns

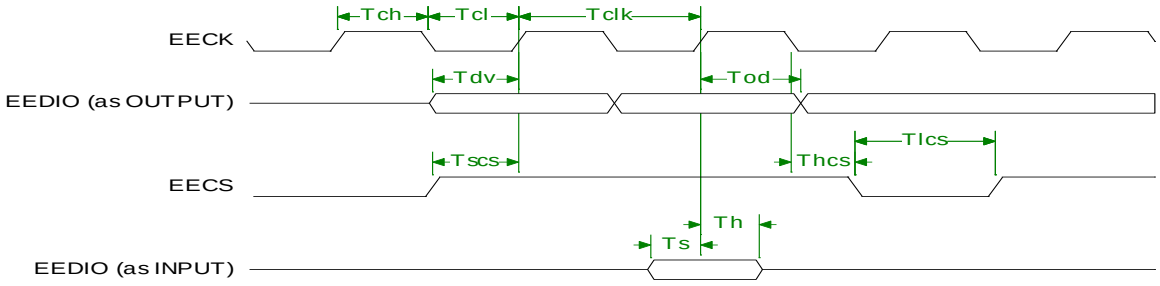
7.5.2 Reset Timing



Symbol	Description	Min	Typ.	Max	Units
Trst	RSTn Reset pulse width	200 *1	-	-	us
Tis	Configuration input setup to RSTn rising	80			ns
Tih	Configuration input hold after RSTn rising	10			ns
Toen	Output drive after RSTn rising			80	ns

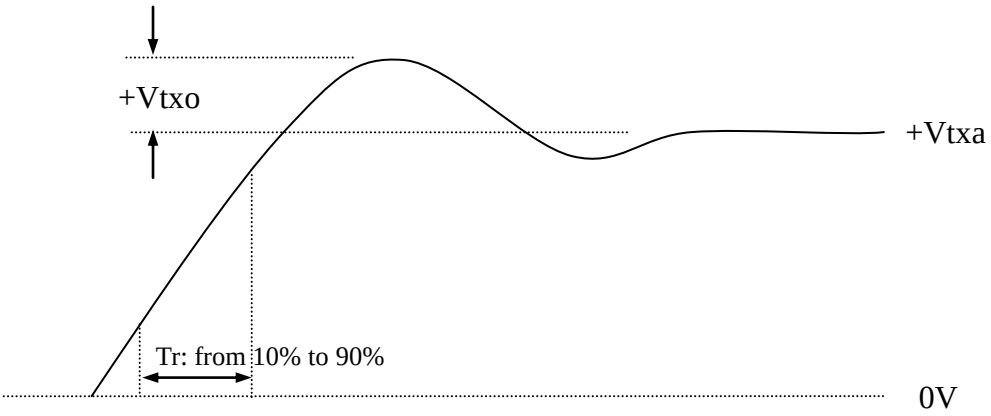
*1 : Please refer to 7.4 Power-up Sequence for the RSTn low level interval time from power-up (T_{rst_pu})

7.5.3 Serial EEPROM Timing



Symbol	Description	Min	Typ	Max	Unit
Tclk	EECK clock cycle time	-	5120	-	ns
Tch	EECK clock high time	-	2560	-	ns
Tcl	EECK clock low time	-	2560	-	ns
Tdv	EEDIO output valid to EECK rising edge time	2560	-	-	ns
Tod	EECK rising edge to EEDIO output delay time	2562	-	-	ns
Tscs	EECS output valid to EECK rising edge time	2560	-	-	ns
Thcs	EECK falling edge to EECS invalid time	7680	-	-	ns
Tlcs	Minimum EECS low time	23039	-	-	ns
Ts	EEDIO input setup time	20	-	-	ns
Th	EEDIO input hold time	0	-	-	ns

7.5.4 10/100M Ethernet PHY Interface Timing



10/100M Ethernet PHY Transmitter Waveform and Spec:

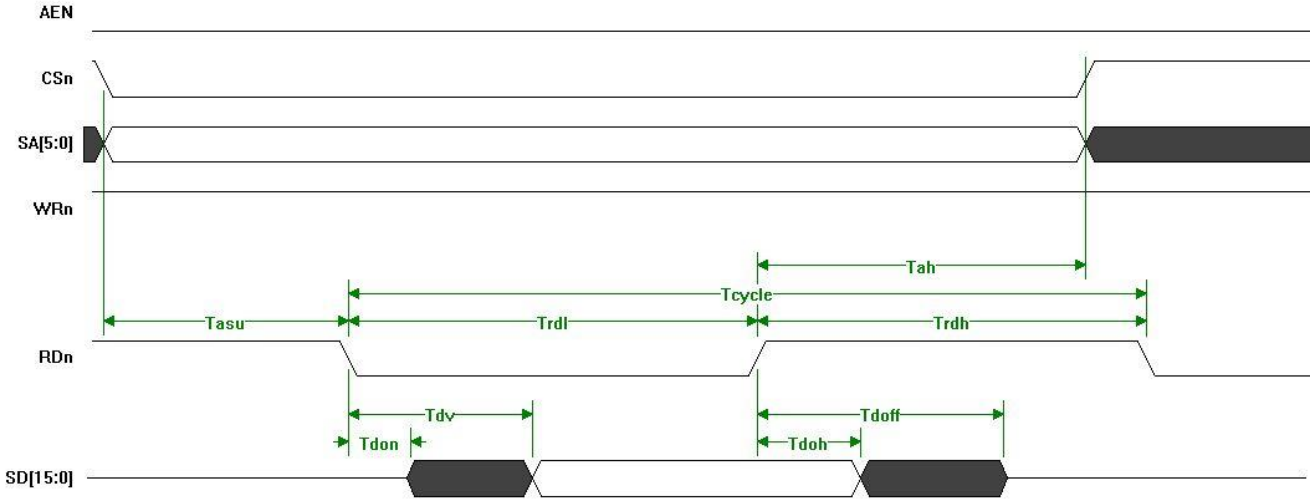
Symbol	Description	Condition	Min	Typ	Max	Units
	Peak-to-peak differential output voltage	10BASE-T mode	4.4	5	5.6	V
Vtxa *2	Peak-to-peak differential output voltage	100BASE-TX mode	1.9	2	2.1	V
Tr / Tf	Signal rise / fall time	100BASE-TX mode	3	4	5	ns
	Output jitter	100BASE-TX mode, scrambled idle signal	-	-	1.4	ns
Vtxov	Overshoot	100BASE-TX mode	-	-	5	%

10/100M Ethernet PHY Receiver Spec:

Symbol	Description	Condition	Min	Typ	Max	Units
	Receiver input impedance		10	-	-	KΩ
	Differential squelch voltage	10BASE-T mode	300	400	500	mV
	Common mode input voltage		2.97	3.3	3.63	V
	Maximum error-free cable length		100	-	-	meter

7.5.5 8/16-Bit SRAM-like Bus Timing

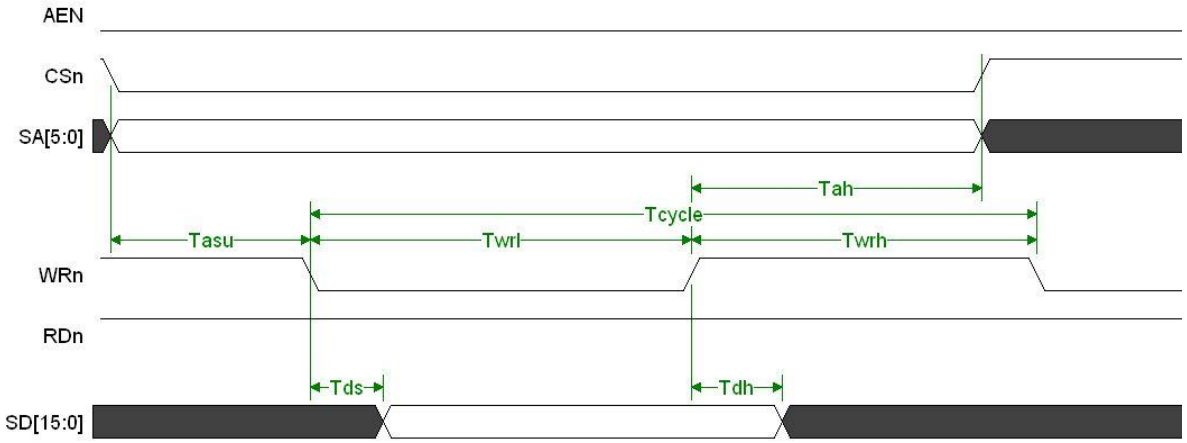
7.5.5.1 Single Read Bus Timing



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35/35/40*	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*: When VCCIO=(3.3V) / (2.5V) / (1.8V)

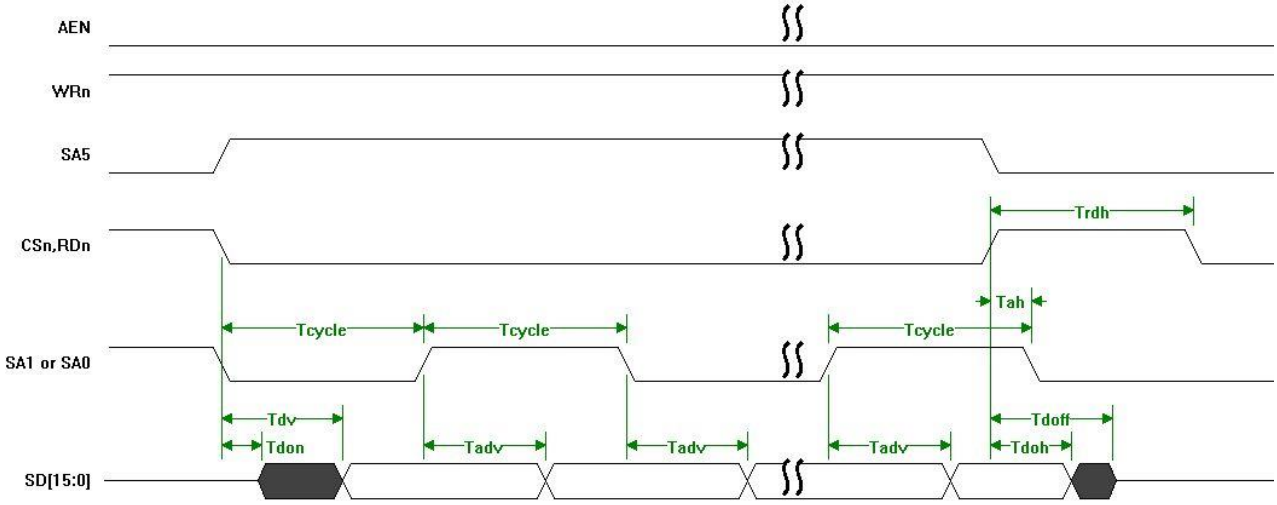
7.5.5.2 Single Write Bus Timing



Symbol	Description	Min	Typ.	Max	Units
Tcycle	WRITE CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdh	DATA HOLD TIME	0	-	-	ns

7.5.5.3 Burst Read Bus Timing

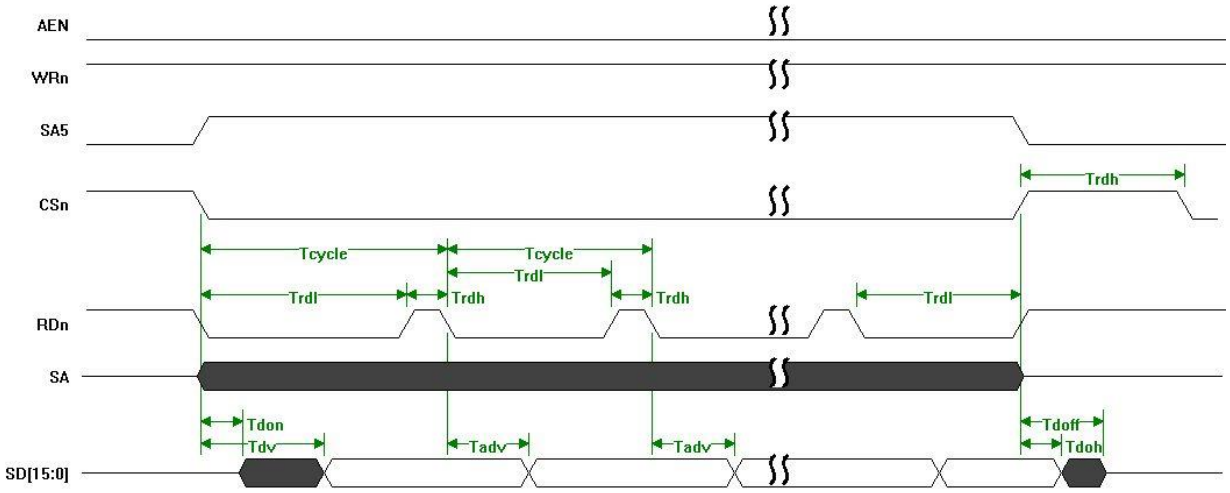
RDn stay low and SA1/0 toggle



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tadv	DATA VALID TIME FROM ADDRESS	-	-	43/45/50*	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

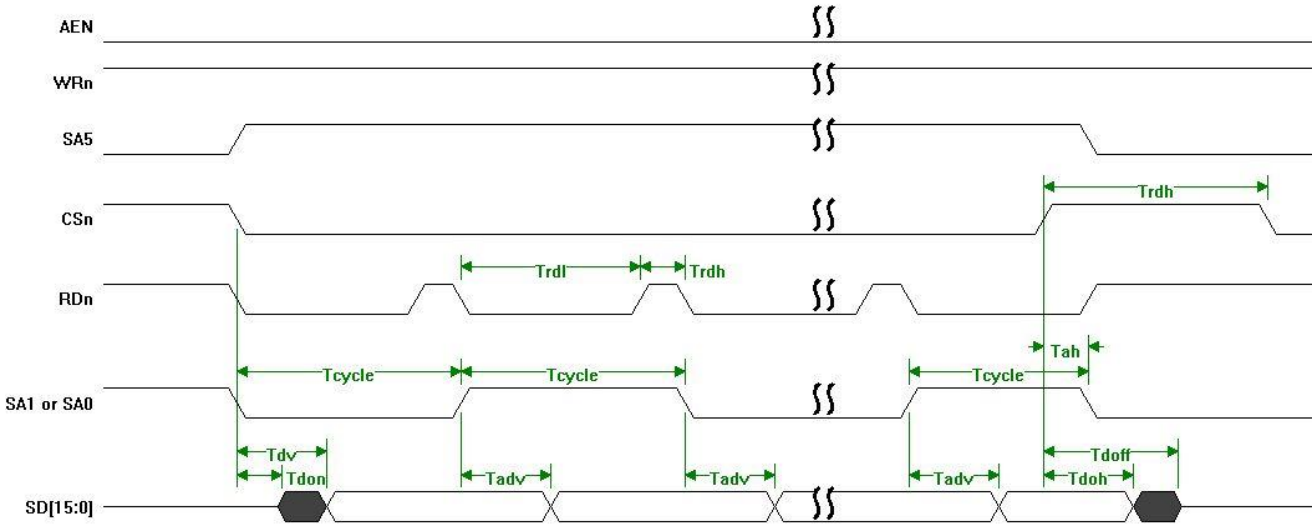
RDn toggle



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35/35/40*	-	-	ns
Tdv	DATA VALID TIME FROM RDN(1^{ST} CYCLE)	-	-	30/32/37*	ns
Tadv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*			ns
Tdoff	DATA BUFFER TURN OFF TIME			7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

RDn and SA0/1 both toggle

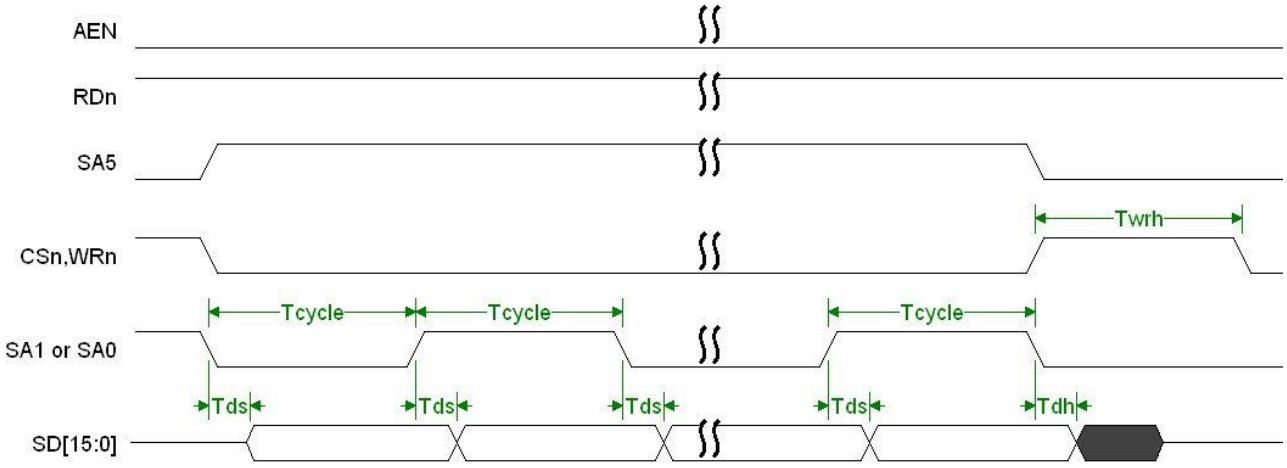


Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35/35/40*	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tadv	DATA VALID TIME FROM ADDRESS	-	-	30/32/378	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

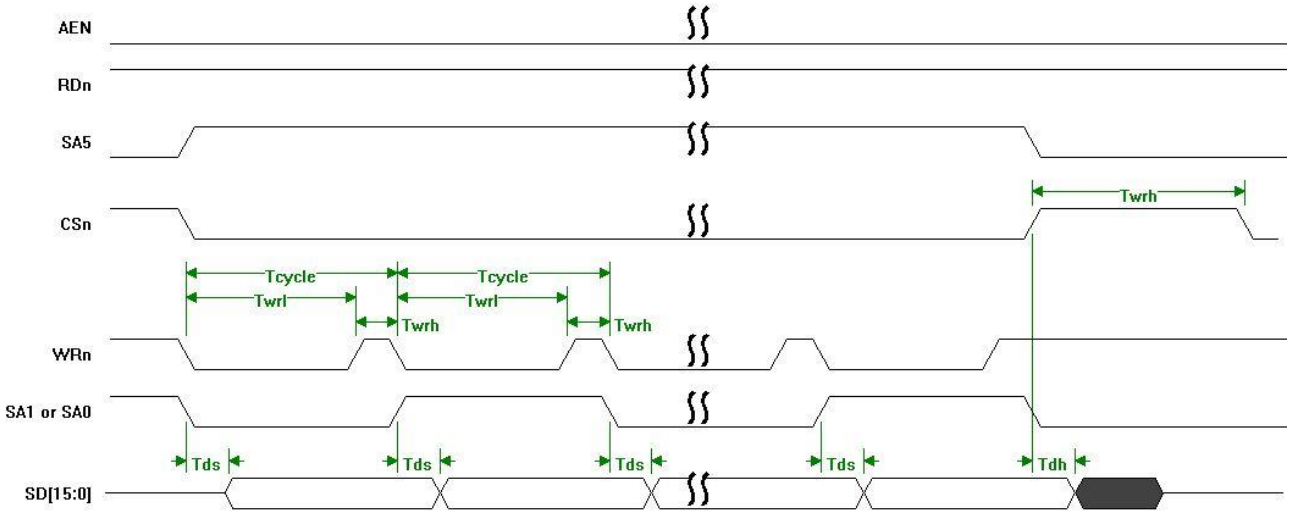
7.5.5.4 Burst Write Bus Timing

SA0/1 toggle



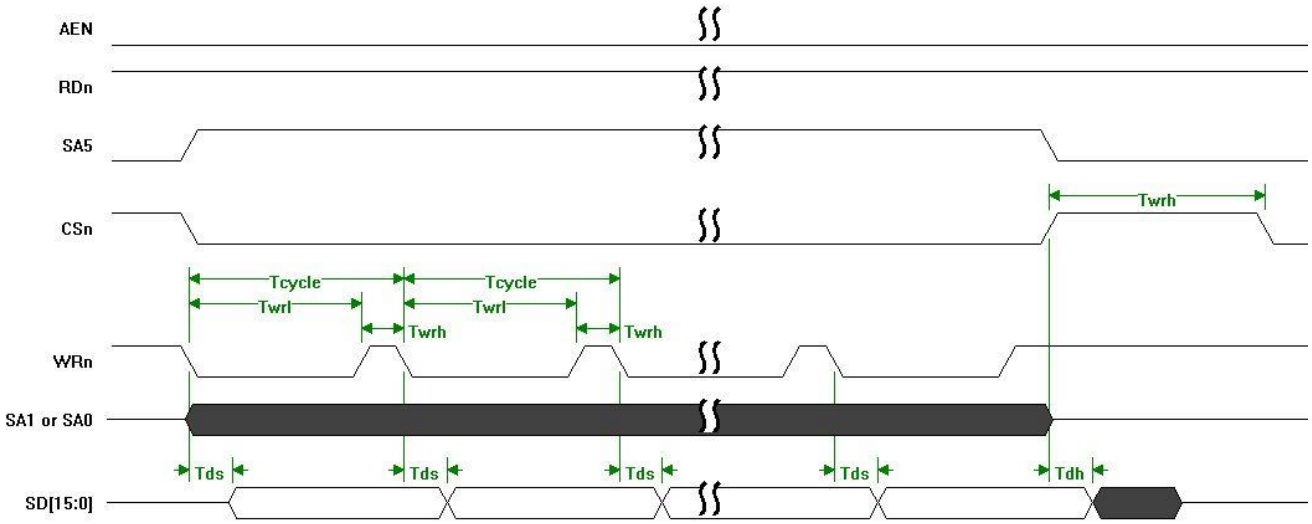
Symbol	Description	Min	Typ.	Max	Units
Tcycle	WRITE CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

WRn and SA0/1 toggle



Symbol	Description	Min	Typ.	Max	Units
Tcycle	WRITE CYCLE TIME	48	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

WRn toggle

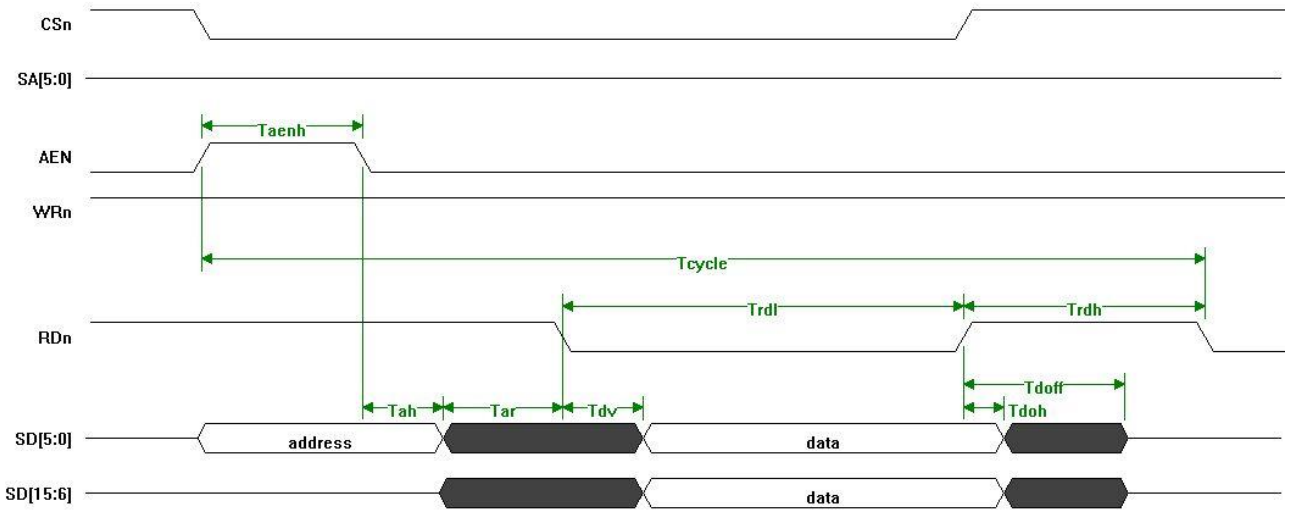


Symbol	Description	Min	Typ.	Max	Units
Tcycle	WRITE CYCLE TIME	48	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

7.5.6 8/16-Bit Address/Data Multiplex Bus Timing

The AX88796C 8-bit Address/Data multiplex bus mode only supports single read and single write data access mode.

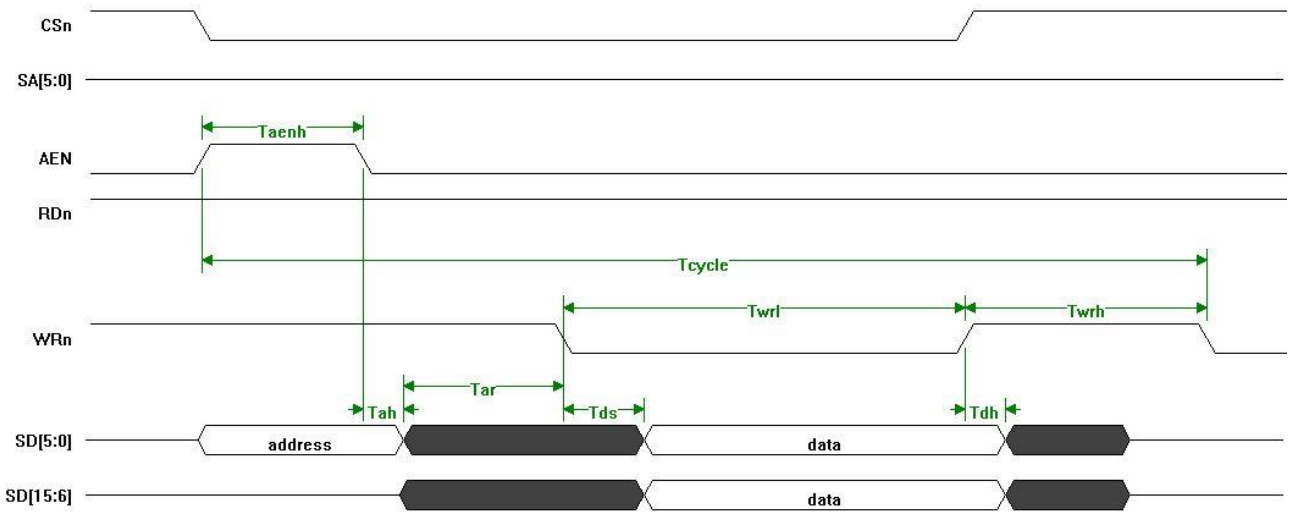
7.5.6.1 8/16-Bit Single Read Bus Timing



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	57/57/58*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35	-	-	ns
Taenh	AEN HI REQUIRE TIME	8	-	-	ns
Tar	ADDRESS SETUP TO RDN LOW TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	1/1/2*	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	20/22/27*	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

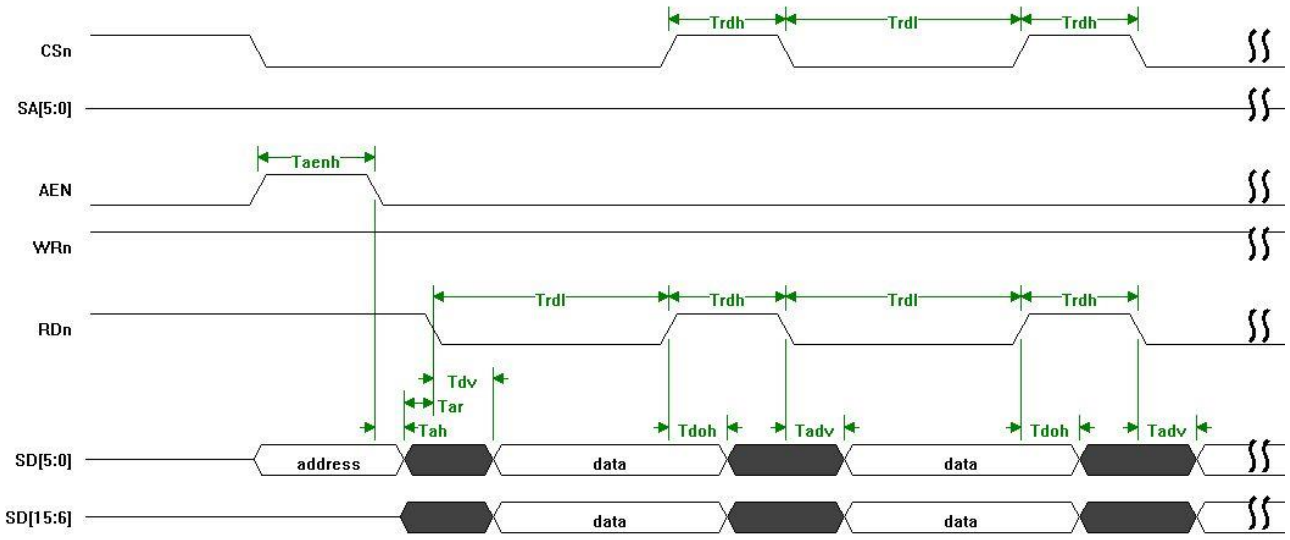
7.5.6.2 8/16-Bit Single Write Bus Timing



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	57/57/58*	-	-	ns
Twdh	WRN HI REQUIRE TIME	13	-	-	ns
Twdl	WRN LOW REQUIRE TIME	35	-	-	ns
Taenh	AEN HI REQUIRE TIME	8	-	-	ns
Tar	ADDRESS SETUP TO RDN LOW TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	1/1/2*	-	-	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

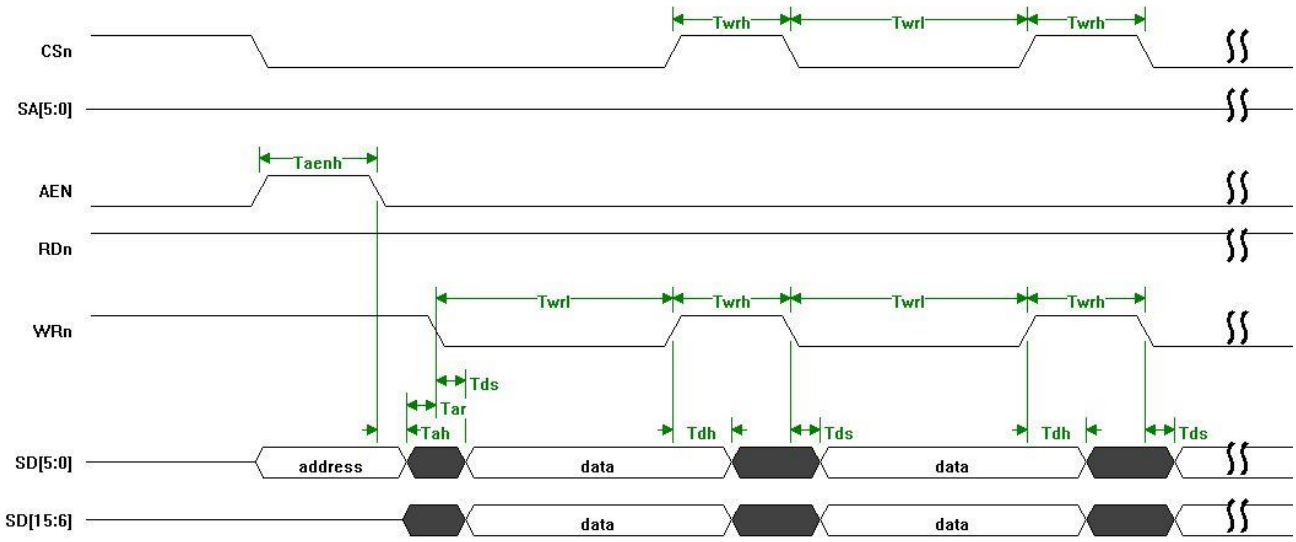
7.5.6.3 16-Bit Burst Read Bus Timing



Symbol	Description	Min	Typ.	Max	Units
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35/35/40*	-	-	ns
Taenh	AEN HI REQUIRE TIME	8	-	-	ns
Tar	ADDRESS SETUP TO RDN LOW TIME	0	-	-	ns
Tdv	DATA VALID TIME FROM RDN (1^{ST} CYCLE)	-	-	20/22/27*	ns
Tadv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tah	ADDRESS HOLD TIME	1/1/2*	-	-	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

7.5.6.4 16-Bit Burst Write Bus Timing

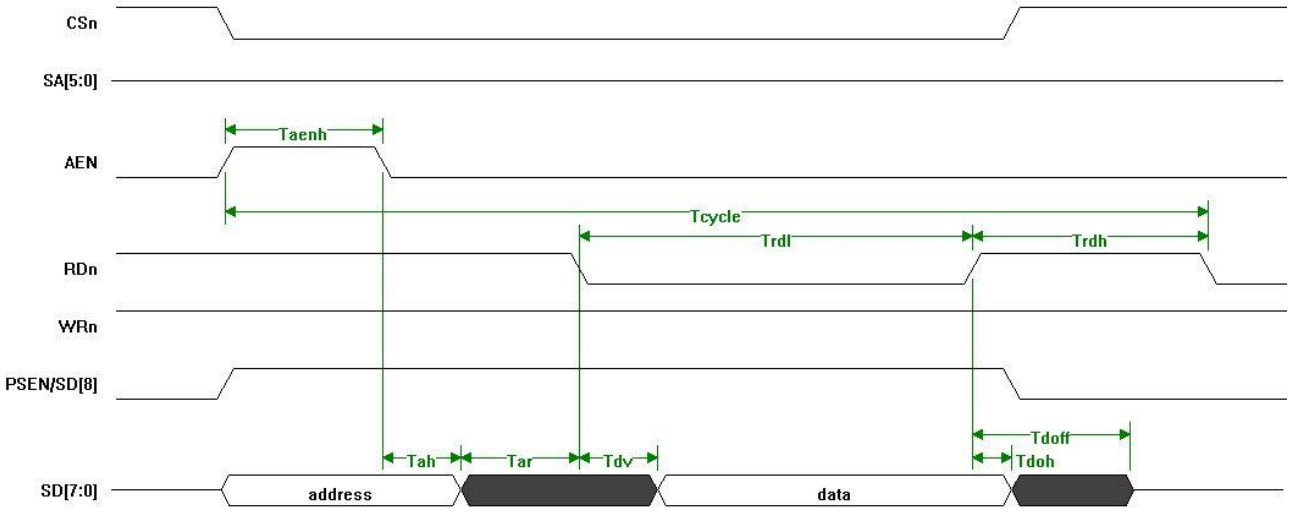


Symbol	Description	Min	Typ.	Max	Units
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Taenh	AEN HI REQUIRE TIME	8	-	-	ns
Tar	ADDRESS SETUP TO RDN LOW TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	1/1/2*	-	-	ns
Tdh	DATA HOLE TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

7.5.7 8051 Bus Timing

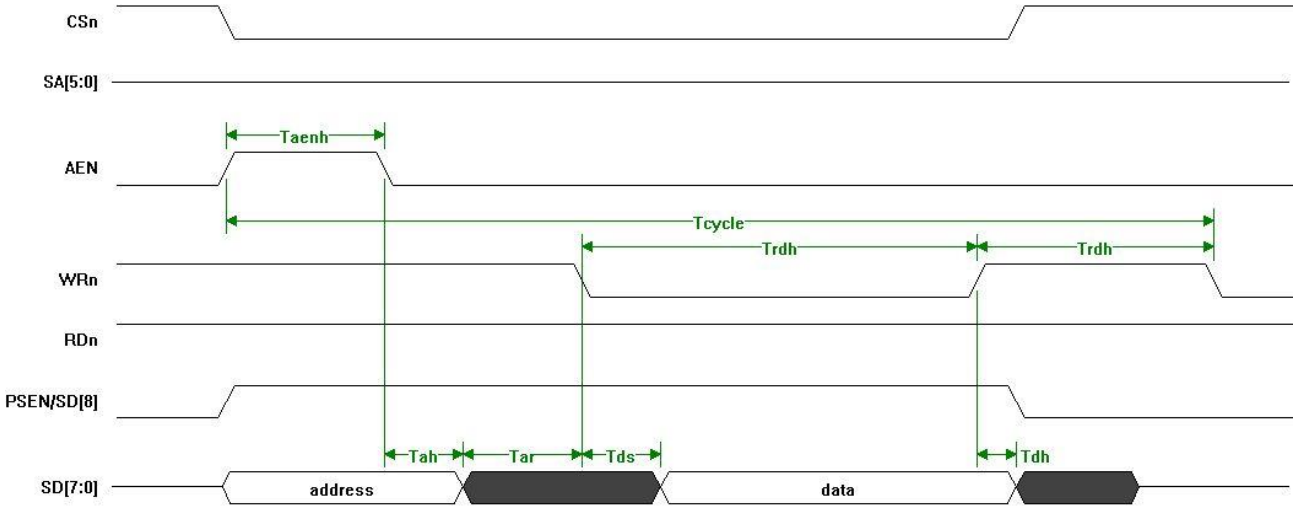
7.5.7.1 Single Read Bus Timing



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	57/57/58*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35	-	-	ns
Taenh	AEN HI REQUIRE TIME	8	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	20/22/27*	ns
Tar	ADDRESS SETUP TO RDN LOW TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	1/1/2*	-	-	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

7.5.7.2 Single Write Bus Timing

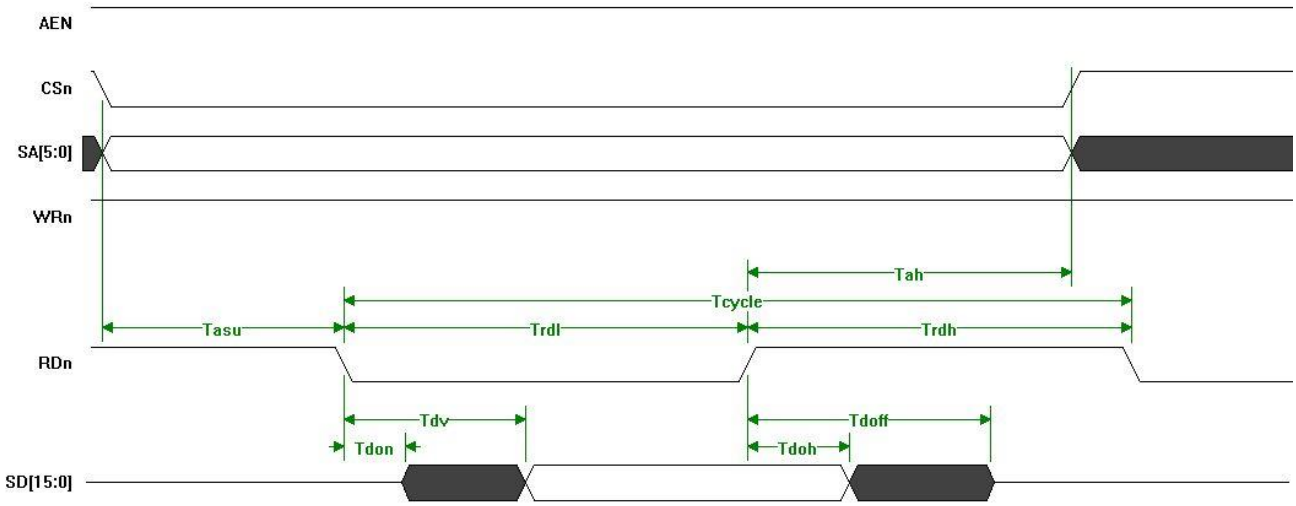


Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	57/57/58*	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Taenh	AEN HI REQUIRE TIME	8	-	-	ns
Tar	ADDRESS SETUP TO RDN LOW TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	1/1/2*	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tdh	DATA HOLD TIME	0	-	-	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

7.5.8 Renesas series CPU Bus Timing

7.5.8.1 Single Read Bus Timing

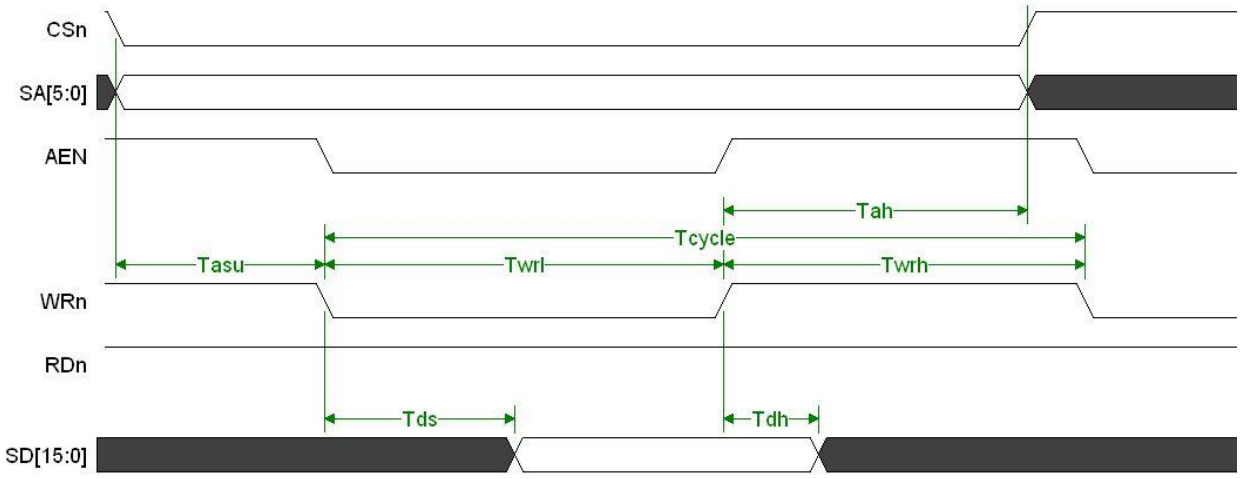


Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35/35/40*	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

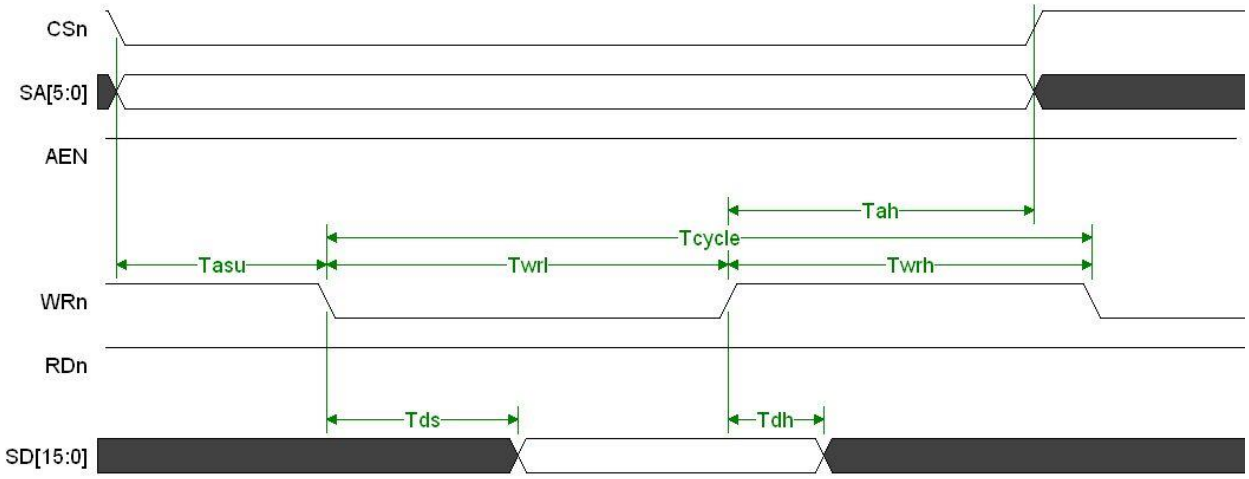
7.5.8.2 Single Write Bus Timing

16 Bit Write



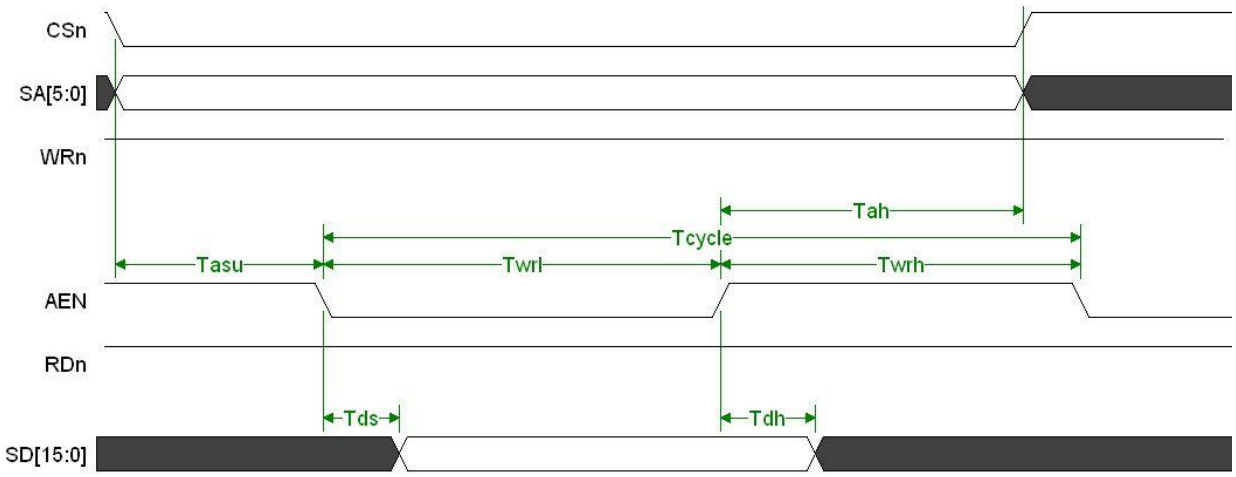
Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tdh	DATA HOLD TIME	0	-	-	ns

Write High Byte



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tdh	DATA HOLD TIME	0	-	-	ns

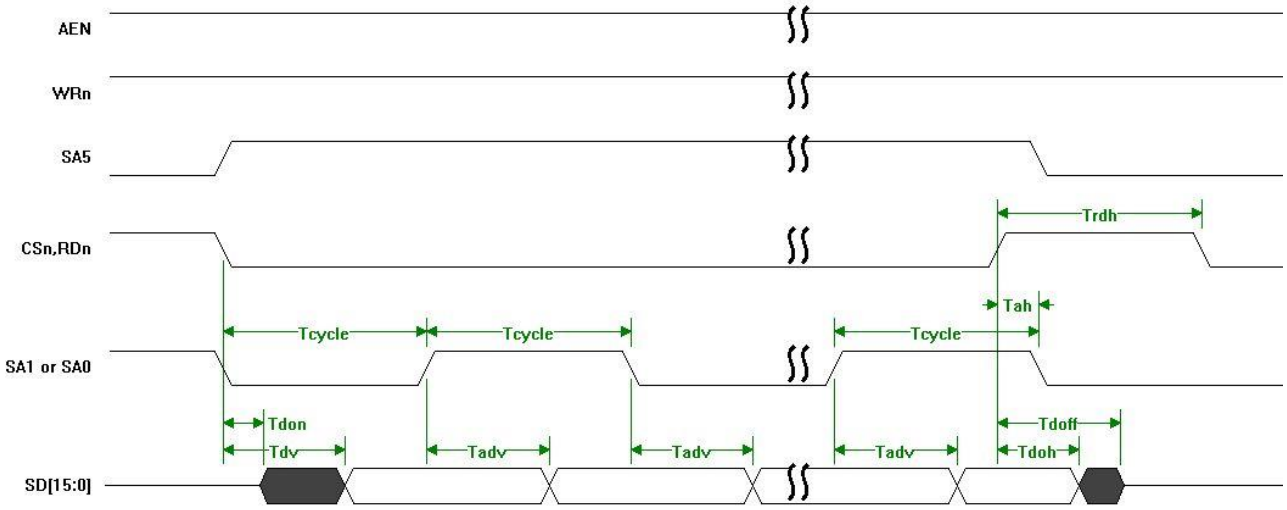
Write Low Byte



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Tasu	ADDRESS SETUP TIME	0	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns
Tdh	DATA HOLD TIME	0	-	-	ns

7.5.8.3 Burst Read Bus Timing

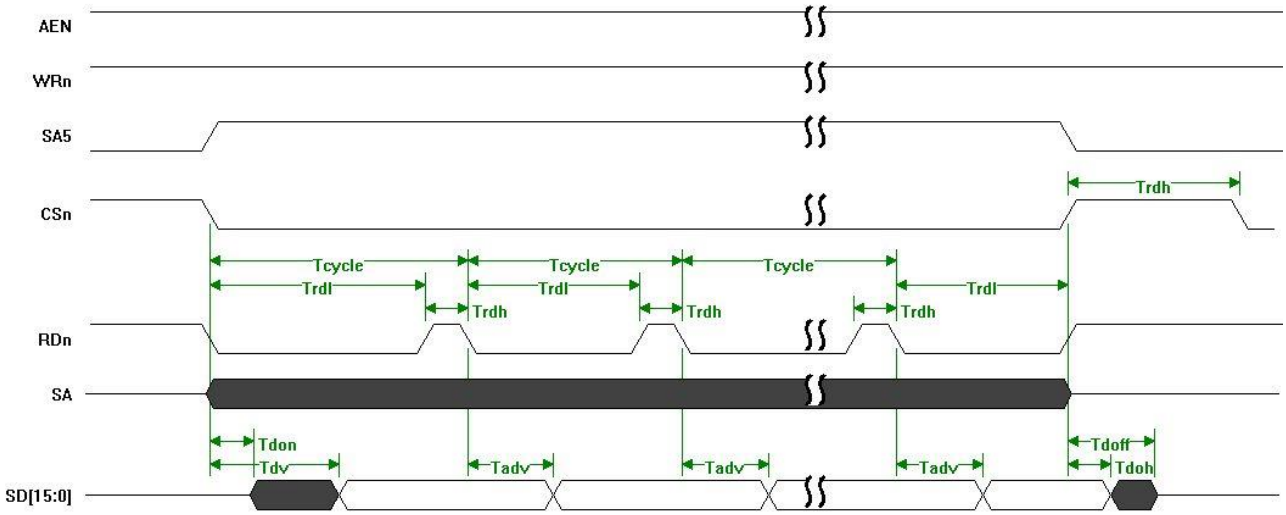
SA0/1 toggle



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tadv	DATA VALID TIME FROM ADDRESS	-	-	43/45/50*	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

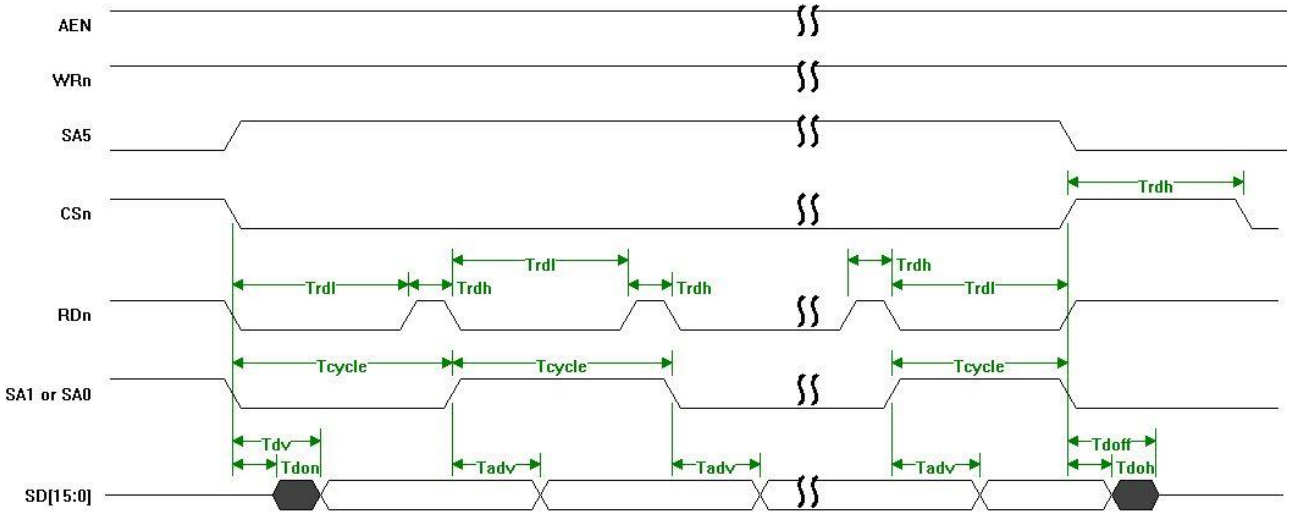
RDn toggle



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35/35/40*	-	-	ns
Tdv	DATA VALID TIME FROM RDN (1^{ST} CYCLE)	-	-	30/32/37*	ns
Tadv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*			ns
Tdoff	DATA BUFFER TURN OFF TIME			7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

RDn and SA0/1 toggle

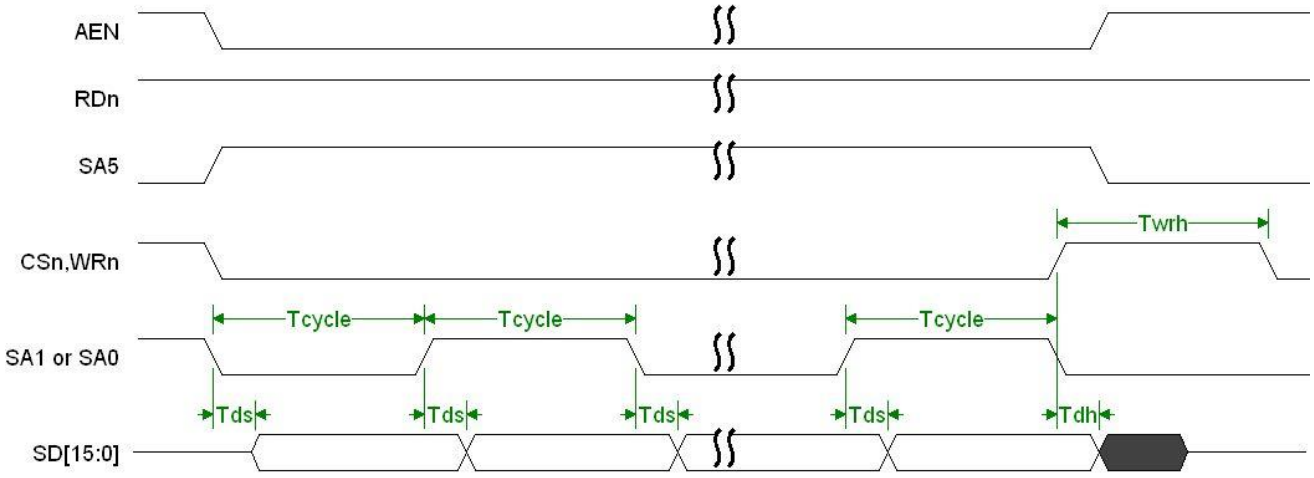


Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48/48/53*	-	-	ns
Trdh	RDN HI REQUIRE TIME	13	-	-	ns
Trdl	RDN LOW REQUIRE TIME	35/35/40*	-	-	ns
Tdv	DATA VALID TIME FROM RDN	-	-	30/32/37*	ns
Tadv	DATA VALID TIME FROM ADDRESS	-	-	30/32/37*	ns
Tdoh	DATA OUTPUT HOLD TIME	2/3/3*	-	-	ns
Tah	ADDRESS HOLD TIME	0	-	-	ns
Tdon	DATA BUFFER TURN ON TIME	4/5/7*	-	-	ns
Tdoff	DATA BUFFER TURN OFF TIME	-	-	7/8/9*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

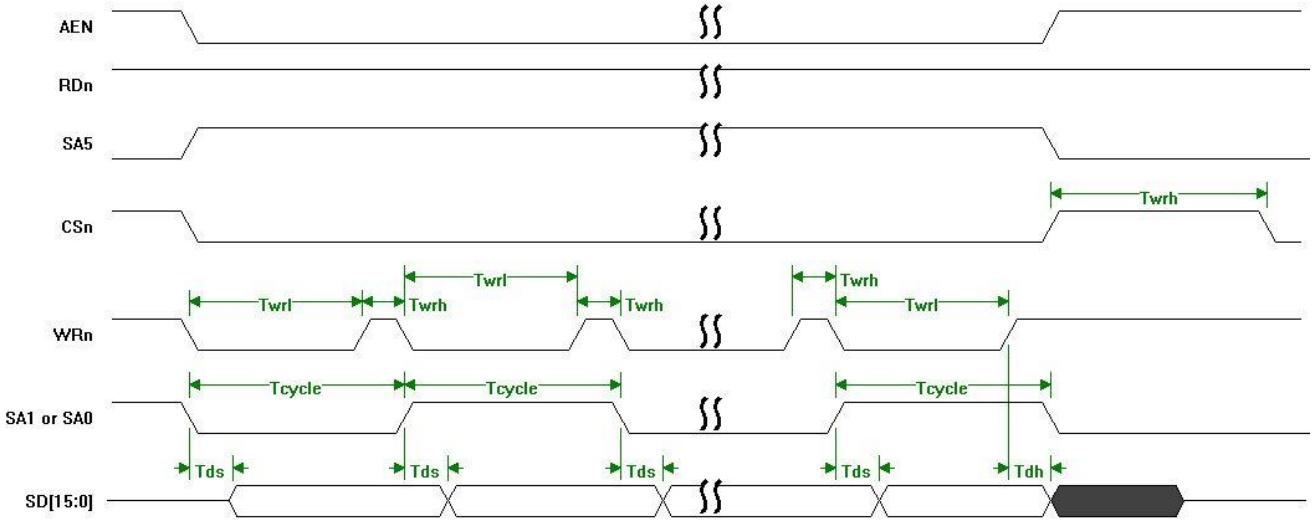
7.5.8.4 Burst Write Bus Timing

SA0/1 toggle



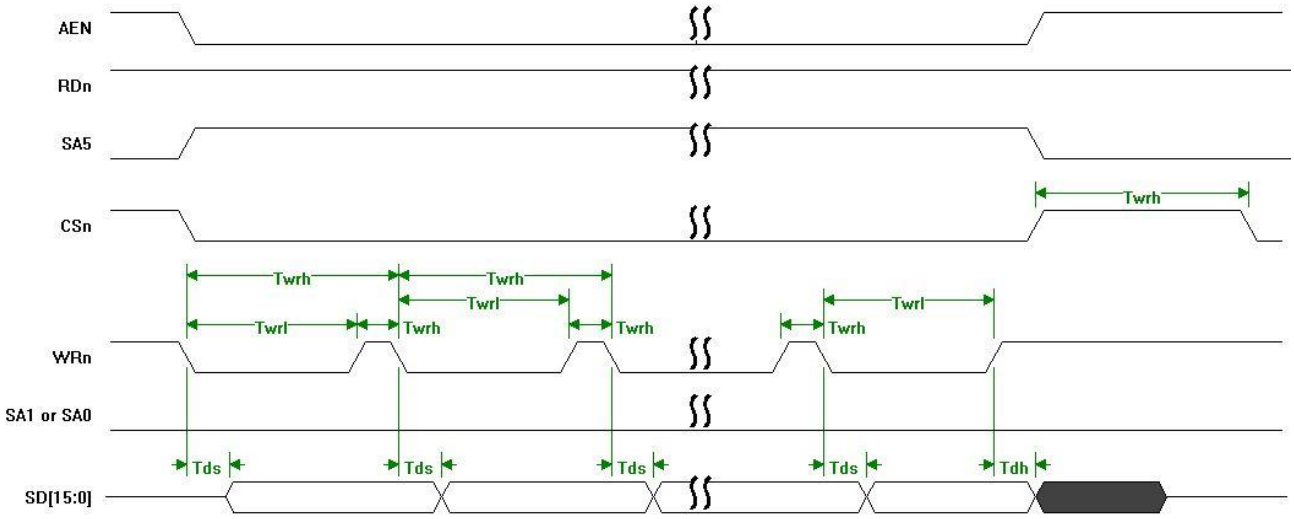
Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Tdh	DATA HOLD TIME	0	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

WRn and SA0/1 toggle



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

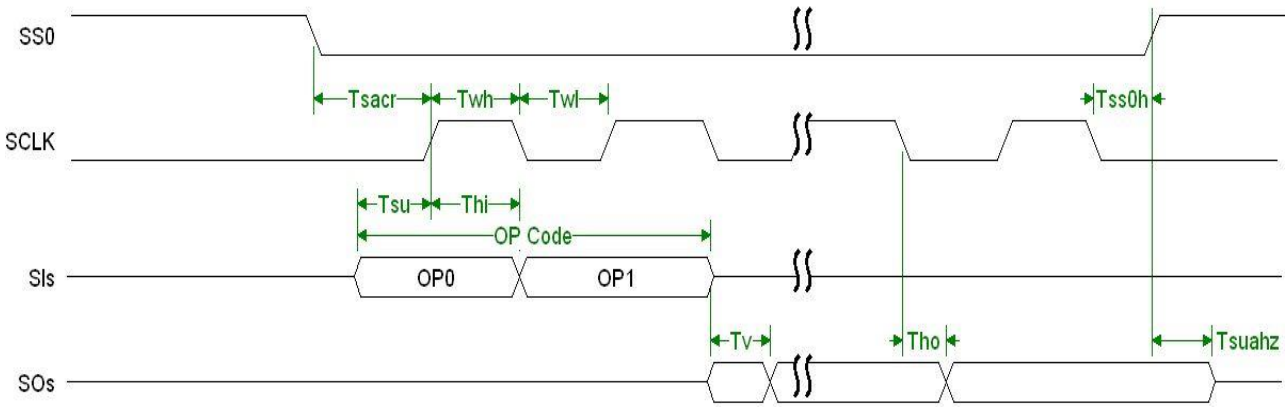
WRn toggle



Symbol	Description	Min	Typ.	Max	Units
Tcycle	READ CYCLE TIME	48	-	-	ns
Twrh	WRN HI REQUIRE TIME	13	-	-	ns
Twrl	WRN LOW REQUIRE TIME	35	-	-	ns
Tds	DATA STABLE TIME	-	-	15	ns

7.5.9 SPI Bus Timing

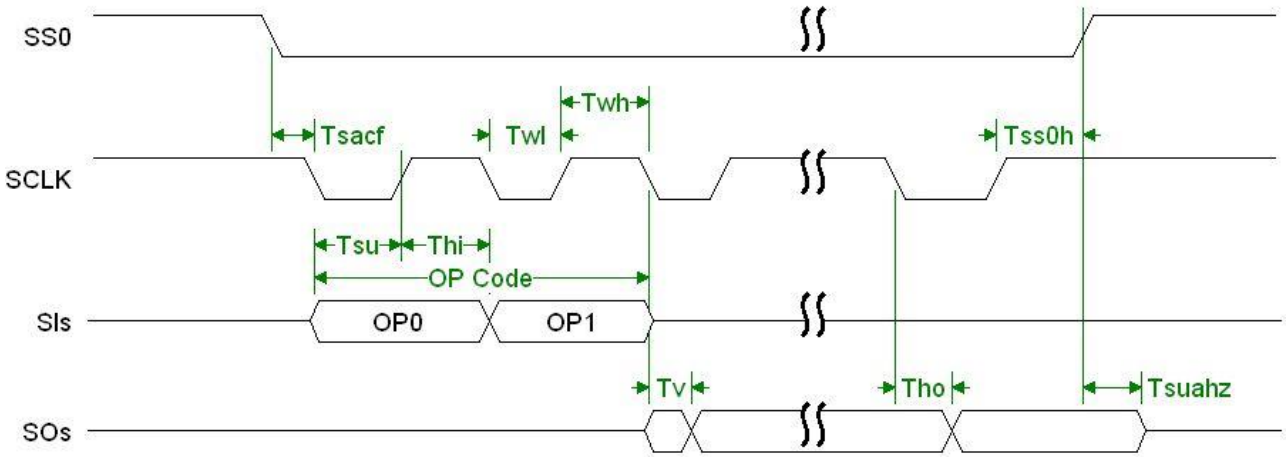
7.5.9.1 Mode 0 Timing



Symbol	Description	Min	Typ.	Max	Units
Tsacr	SS0 ACTIVE TO SCLK RISING TIME	4.5/5/6.5*	-	-	ns
Twh	SCLK HOLD HIGH TIME	10.5/12/17*	-	-	ns
Twl	SCLK HOLD LOW TIME	10.5/12/17*	-	-	ns
Tsu	INPUT DATA SET UP TIME	1.93/1.98/2.24*	-	-	ns
Thi	INPUT DATA HOLD TIME	0	-	-	ns
Tv	OUTPUT DATA VALID TIME	-	-	10.15/11.77/16.96*	ns
Tho	OUTPUT DATA HOLD TIME	-	-	10.15/11.77/16.96*	ns
Tss0h	SCLK FALLING TO SS0 GOES HIGH TIME	0	-	-	ns
Tsuahz	SS0 UN-ACTIVE TO OUTPUT CHANGE TO HI-Z TIME	2.93/3.09/3.35*	-	6.75/7.51/9.2*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

7.5.9.2 Mode 3 Timing

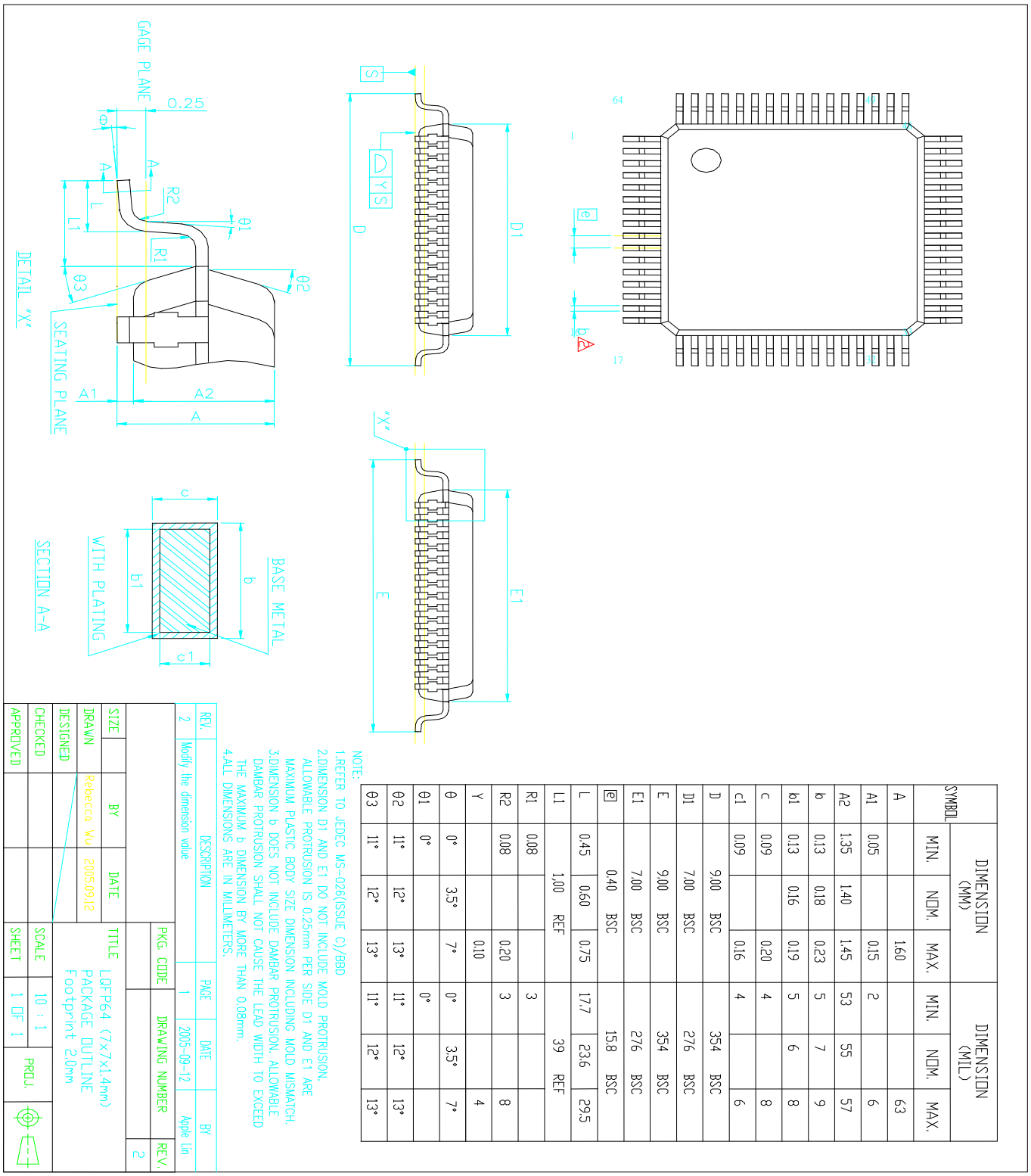


Symbol	Description	Min	Typ.	Max	Units
Tsacf	SS0 ACTIVE TO SCLK FALLING TIME	0	-	-	ns
Twh	SCLK HOLD HIGH TIME	10.5/12/17*	-	-	ns
Twl	SCLK HOLD LOW TIME	10.5/12/17*	-	-	ns
Tsu	INPUT DATA SET UP TIME	1.93/1.98/2.24*	-	-	ns
Thi	INPUT DATA HOLD TIME	0	-	-	ns
Tv	OUTPUT DATA VALID TIME	-	-	10.15/11.77/16.96*	ns
Tho	OUTPUT DATA HOLD TIME	-	-	10.15/11.77/16.96*	ns
Tss0h	SCLK RISING TO SS0 GOES HIGH TIME	10.5/12/17*	-	-	ns
Tsuahz	SS0 UN-ACTIVE TO OUTPUT CHANGE TO HI-Z TIME	2.93/3.09/3.35*	-	6.75/7.51/9.2*	ns

*:When VCCIO=(3.3V) / (2.5V) / (1.8V)

8.0 Package Information

8.1 64-pin LQFP package



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.60			63
A1	0.05		0.15	2		6
A2	1.35	1.40	1.45	53	55	57
b	0.13	0.18	0.23	5	7	9
b1	0.13	0.16	0.19	5	6	8
c	0.09		0.20	4		8
c1	0.09		0.16	4		6
D	9.00 BSC			354 BSC		
D1	7.00 BSC			276 BSC		
E	9.00 BSC			354 BSC		
E1	7.00 BSC			276 BSC		
e	0.40 BSC			15.8 BSC		
L	0.45	0.60	0.75	17.7	23.6	29.5
L1	1.00 REF			39 REF		
R1	0.08			3		
R2	0.08		0.20	3		8
Y			0.10			4
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°			0°		
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°

NOTE:
1.REFER TO JEDEC MS-026(ISSUE C)/BBD
2.DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
ALLOWABLE PROTRUSION IS 0.25mm PER SIDE D1 AND E1 ARE
MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE
DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED
THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
4.ALL DIMENSIONS ARE IN MILLIMETERS.

REV.	DESCRIPTION	PAGE	DATE	BY
2	Modify the dimension value	1	2005-09-12	Apple Lin

SIZE	BY	DATE	PKG. CODE
DRAWN	Rebecca Wu	2005.09.12	DRAWING NUMBER
DESIGNED			REV.
CHECKED			2
APPROVED			

TITLE: LQFP64 (7x7x1.4mm)
PACKAGE OUTLINE
Footprint 2.0mm

SCALE: 10 : 1
SHEET: 1 OF 1
PROJ.

9.0 Ordering Information

Part Number	Description
AX88796CLF	64 PIN, LQFP Package, Commercial grade 0°C to +70 °C (Green, Lead-Free)
AX88796CLI	64 PIN, LQFP Package, Industrial grade -40°C to +85 °C (Green, Lead-Free)

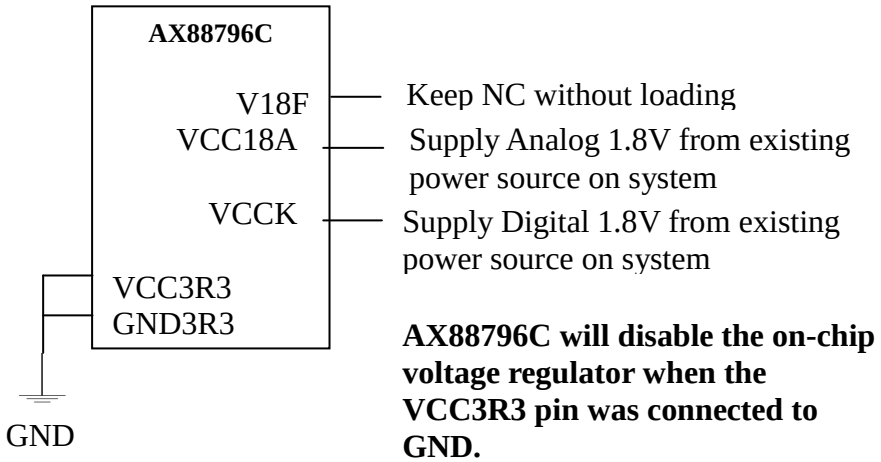
10.0 Revision History

Revision	Date	Comment
V1.00	2010/02/12	Initial Release.
V1.01	2010/03/11	1. Modified some descriptions in page 1 “Feature”. 2. Removed “Product Description” in page 2. 3. Added Section 1.2 “Block Diagram”. 4. Added Section 1.4 “Bus Interface Configuration Table and Application” and removed Appendix A1, A2. 5. Modified some descriptions in Section 2.4. 6. Corrected the MAC address setting descriptions in Section 3.1, 4.1.1, 6.1.37, 6.1.38, 6.1.39. 7. Removed the current information in Section 7.1.2. 8. Updated Thermal Resistance values in Section 7.2.
V1.10	2010/03/26	1. Modified some descriptions in Feature page, Section 1.1, 1.4.7, 4.5, 4.6. 2. Modified some pin name descriptions in Section 1.3.3. 3. Updated Fig 5, 6, 7, 8, 9, 10 in Section 1.4 to add the AEN signal connection. 4. Added “I” and “O” type descriptions in Section 2. 5. Modified some pin definition descriptions in Section 2. 6. Modified some SPI related descriptions in Section 5. 7. Modified some registers descriptions in Section 6.1.
V1.11	2010/04/15	1. Modified some descriptions in Section 6.1.22. 2. Corrected a typo in Section 6.1.26. 3. Added some descriptions in Section 6.2.1.
V1.12	2010/04/28	1. Modified power saving level descriptions in Section 2.6, 3.1, 4.12, 5.6, 6.1, 7.3. 2. Modified some descriptions in Section 4.12.3, 6.1.7, 6.1.26, 6.1.29, 6.1.30. 3. Modified SPI Interrupt related information in Section 6.1.55.
V1.13	2010/05/19	1. Added more GPIO1~GPIO3 pins information in Section 1.3. 2. Added detailed description of PS2 (Power Saving Mode 2) in Section 2.6. 3. Updated Fig 16 in Section 4.5. 4. Corrected the descriptions of RX Header fields in Fig 18. 5. Added more information in Section 4.10 “Mixed Endian Byte Ordering”. 6. Modified some descriptions in Section 4.11. 7. Modified some descriptions in Section 6.1.13.
V1.14	2011/04/15	1. Corrected some typos in Section 2.5, 2.6, 3.1, 5.4.1, 6.1, 6.1.7, 6.1.34. 2. Modified some descriptions in Section 4.12, 4.12.3, 5.4.1, 6.1.6, 6.1.14, 6.1.16.
V1.15	2013/03/08	1. Added copyright legal header information. 2. Corrected some typos in Section 3.1, 6.1.4. 3. Modified some descriptions in Section 3.1.

Revision	Date	Comment
V1.16	2013/08/13	1. Modified some descriptions in Section 2.1.
V1.17	2014/12/09	1. Modified some descriptions in Section 1.4.1, 1.4.4, 4.6, 4.12.2, 7.5.6.

Appendix A: Disable AX88796C voltage regulator

The AX88796C integrates an on-chip 3.3V to 1.8V voltage regulator for single-power supply system design. If the system have 1.8V power source already, user may like to disable AX88796C voltage regulator and use the existing 1.8V power source (probably a higher efficiency version). In that case, user can connect VCC3R3 (pin-10) and GND3R3 (pin-11) to ground, keep V18F (pin-9) open. Please refer to below picture for details.



4F, No. 8, Hsin Ann Rd., HsinChu Science Park,
HsinChu, Taiwan, R.O.C.

TEL: 886-3-5799500
FAX: 886-3-5799558

Email: support@asix.com.tw
Web: http://www.asix.com.tw