# NCP146

# Voltage Regulator - CMOS Low Dropout

## 300 mA

The NCP146 is 300 mA LDO that provides the engineer with a very stable, accurate voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCP146 employs the dynamic quiescent current adjustment for very low $I_Q$ consumption at no−load.

### Features

- Operating Input Voltage Range: 1.7 V to 5.5 V
- Available in Fixed Voltage Options: 1.8 V
- Very Low Quiescent Current of Typ. 50 μA
- Low Dropout: 280 mV Typical at 300 mA
- ±1% Accuracy at Room Temperature
- High Power Supply Ripple Rejection: 75 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Stable with a 1 μF Ceramic Output Capacitor
- Available in SOIC−8 Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applicaitons

- Home Automation, Factory Automation
- Portable Medical Equipment
- Other Battery Powered Applications

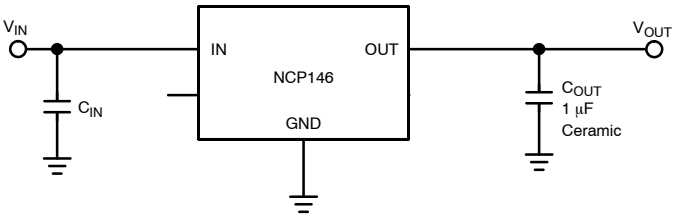
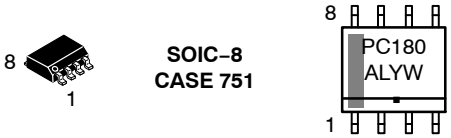



**Figure 1. Typical Application Schematic**

**ON Semiconductor®**

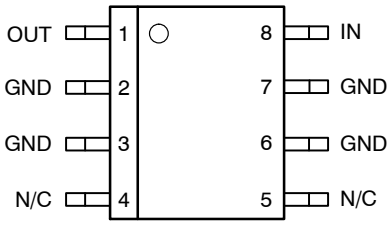
www.onsemi.com

**MARKING DIAGRAM**




| | |
|---|---|
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| ▪ | = Pb−Free Package |

**PIN CONNECTIONS**




SOIC−8
(Top View)

**ORDERING INFORMATION**

See detailed ordering, marking and shipping information on page 8 of this data sheet.

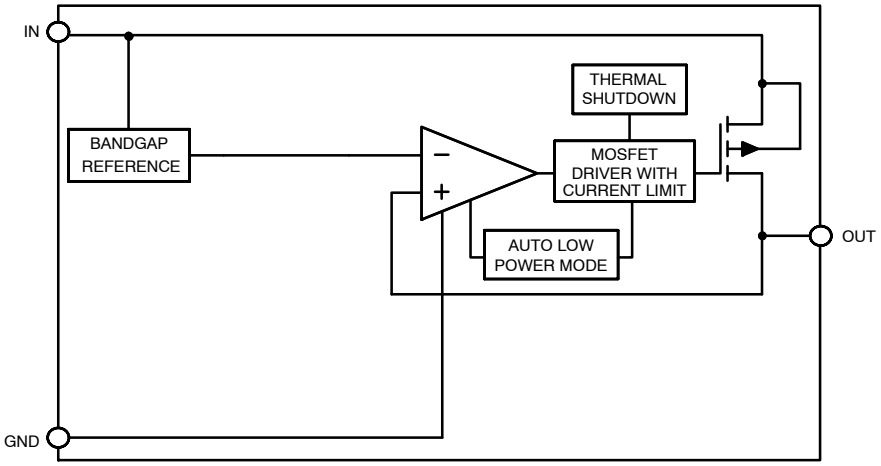



**Figure 2. Simplified Schematic Block Diagram**

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT | Regulated output voltage pin. A small ceramic capacitor with minimum value of 1 μF is needed from this pin to ground to assure stability. |
| 2, 3, 6, 7 | GND | Power supply ground. |
| 8 | IN | Input pin. A small capacitor is needed from this pin to ground to assure stability. |
| 4, 5 | N/C | Not connected. This pin can be tied to ground to improve thermal dissipation. |

## ABSOLUTE MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage (Note 1) | $V_{IN}$ | −0.3 V to 6 V | V |
| Output Voltage | $V_{OUT}$ | −0.3 V to $V_{IN}$ + 0.3 V or 6 V | V |
| Output Short Circuit Duration | $t_{SC}$ | ∞ | s |
| Maximum Junction Temperature | $T_{J(MAX)}$ | 150 | °C |
| Storage Temperature | $T_{STG}$ | −55 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | $ESD_{HBM}$ | 2000 | V |
| ESD Capability, Machine Model (Note 2) | $ESD_{MM}$ | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per EIA/JESD22−A114,
   ESD Machine Model tested per EIA/JESD22−A115,
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

## THERMAL CHARACTERISTICS (Note 3)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, SOIC−8<br>Thermal Resistance, Junction−to−Air | $R_{\theta JA}$ | 161 | °C/W |

3. Single component mounted on 1 oz, FR 4 PCB with 645 $mm^2$ Cu area.

## ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 85°C$; $V_{IN}$ = 2.8 V, $I_{OUT}$ = 1 mA, $C_{IN} = C_{OUT}$ = 1 μF. Typical values are at $T_J$ = +25°C. Min./Max. are for $T_J$ = −40°C and $T_J$ = +85°C respectively (Note 4).

| Parameter | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Operating Input Voltage | | $V_{IN}$ | 1.7 | | 5.5 | V |
| Output Voltage Accuracy | $-40°C \le T_J \le 85°C$ | $V_{OUT}$ | −2 | | +3 | % |
| Line Regulation | $V_{OUT}$ + 0.5 V ≤ $V_{IN}$ ≤ 5.5 V | $Reg_{LINE}$ | | 0.01 | 0.1 | %/V |
| Load Regulation | $I_{OUT}$ = 1 mA to 150 mA | $Reg_{LOAD}$ | | 15 | | mV |
| Load Regulation | $I_{OUT}$ = 1 mA to 300 mA | | | 30 | | |
| Load Transient | $I_{OUT}$ = 1 mA to 300 mA or 300 mA to 1 mA in 1 μs, $C_{OUT}$ = 1 μF | $Tran_{LOAD}$ | | −50/ +30 | | mV |
| Dropout Voltage (Note 5) | $I_{OUT}$ = 300 mA | $V_{DO}$ | | 280 | | mV |
| Output Current Limit | $V_{OUT}$ = 90% $V_{OUT(nom)}$ | $I_{CL}$ | 300 | 600 | | mA |
| Quiescent Current | $I_{OUT}$ = 0 mA | $I_Q$ | | 50 | 95 | μA |
| Power Supply Rejection Ratio | $V_{IN}$ = 2.8 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 150 mA, f = 1 kHz | PSRR | | 75 | | dB |
| Output Noise Voltage | $V_{IN}$ = 2.8 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 150 mA, f = 10 Hz to 100 kHz | $V_N$ | | 70 | | $\mu V_{rms}$ |
| Thermal Shutdown Temperature | Temperature increasing from $T_J$ = +25°C | $T_{SD}$ | | 160 | | °C |
| Thermal Shutdown Hysteresis | Temperature falling from $T_{SD}$ | $T_{SDH}$ | | 20 | | °C |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when $V_{OUT}$ falls 100 mV below the regulated voltage at $V_{IN} = V_{OUT(NOM)}$ + 1 V.

## TYPICAL CHARACTERISTICS

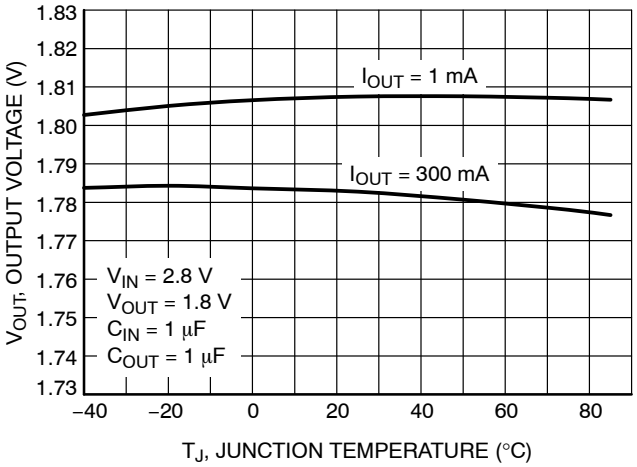



**Figure 3. Output Voltage vs. Temperature**

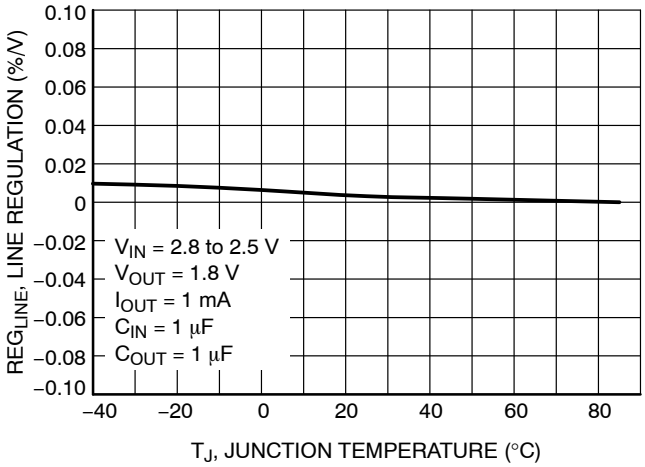



**Figure 4. Line Regulation vs. Temperature**

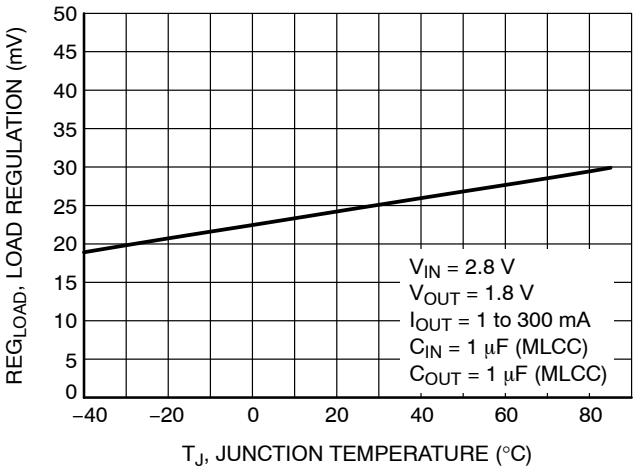



**Figure 5. Load Regulation vs. Temperature**

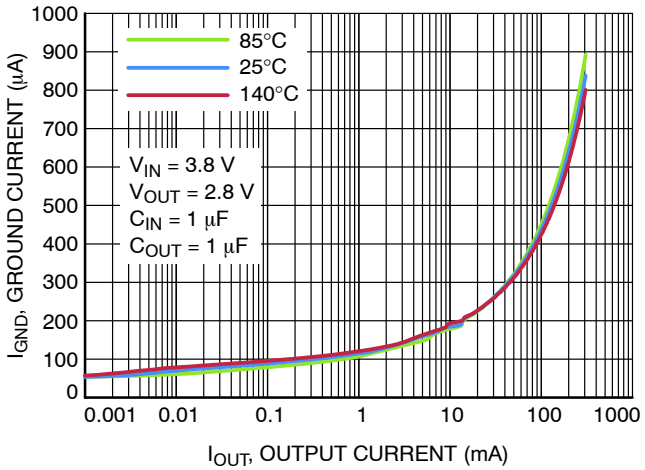



**Figure 6. Ground Current vs. Output Current**

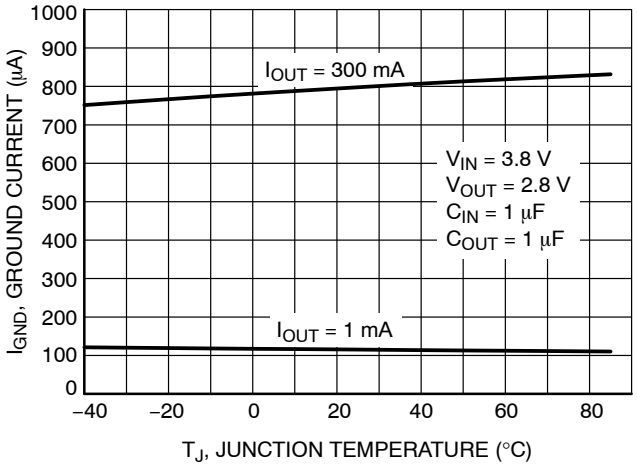



**Figure 7. Ground Current vs. Temperature**

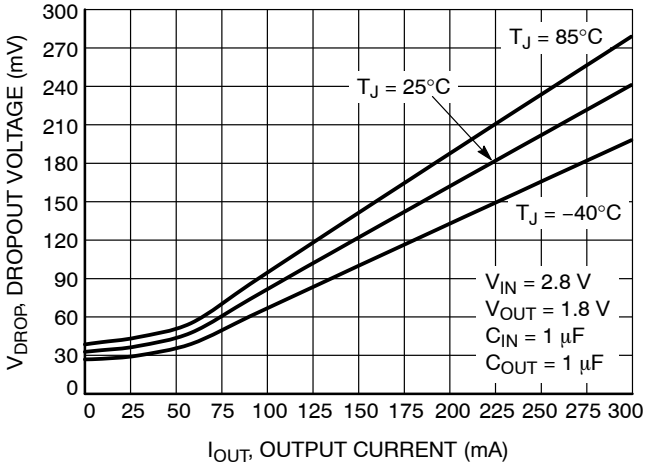



**Figure 8. Dropout Voltage vs. Output Current**

## TYPICAL CHARACTERISTICS

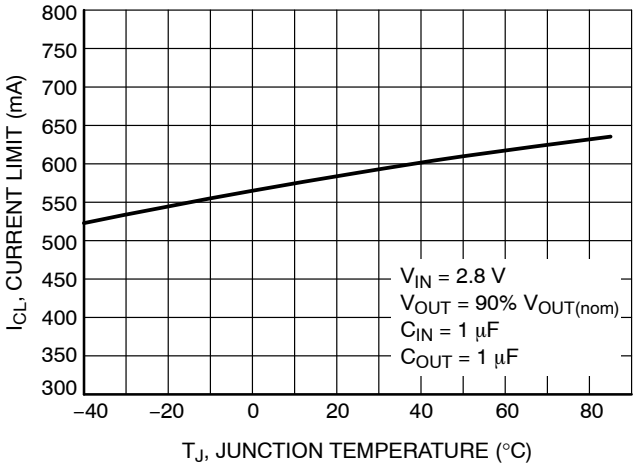



**Figure 9. Current Limit vs. Temperature**

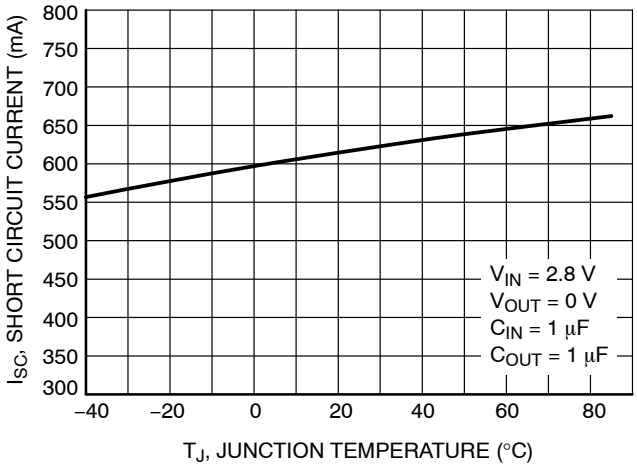



**Figure 10. Short Circuit Current vs. Temperature**

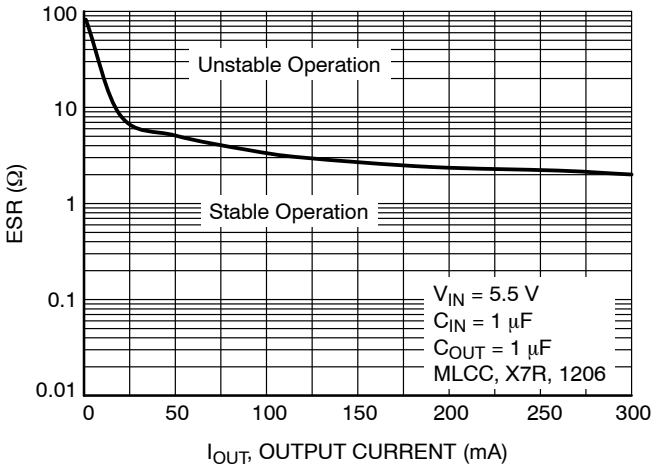



**Figure 11. Output Capacitor ESR vs. Output Current**

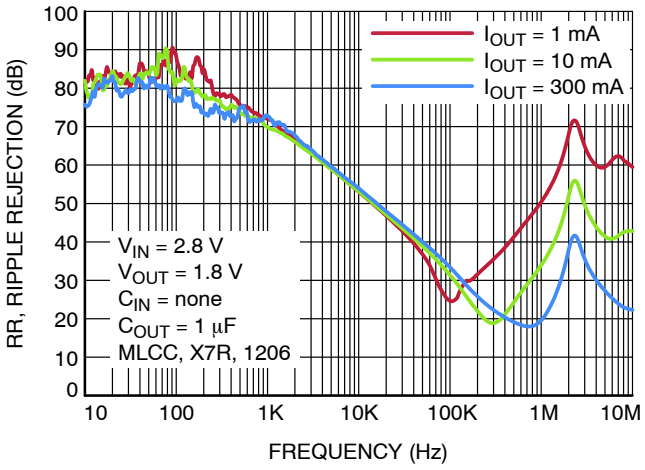



**Figure 12. Power Supply Rejection Ratio, $C_{OUT}$ = 1 μF**

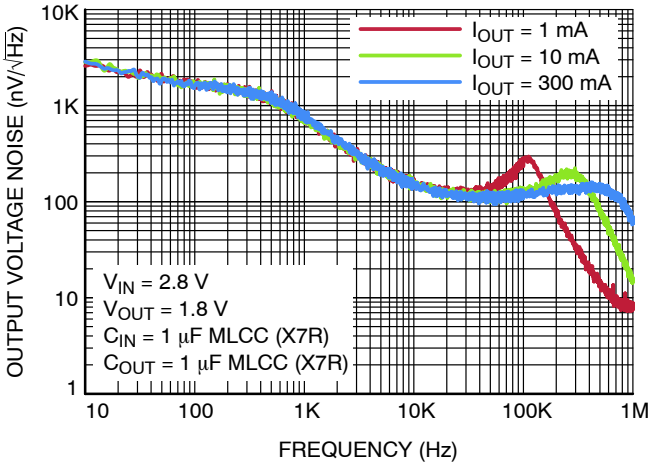



**Figure 13. Output Voltage Noise Spectral Density**

| $I_{OUT}$ | RMS Output Noise (μV) | |
|---|---|---|
| | 10 Hz – 100 kHz | 100 Hz – 100 kHz |
| 1 mA | 59.97 | 57.07 |
| 10 mA | 60.22 | 57.17 |
| 300 mA | 70.35 | 67.79 |

## TYPICAL CHARACTERISTICS

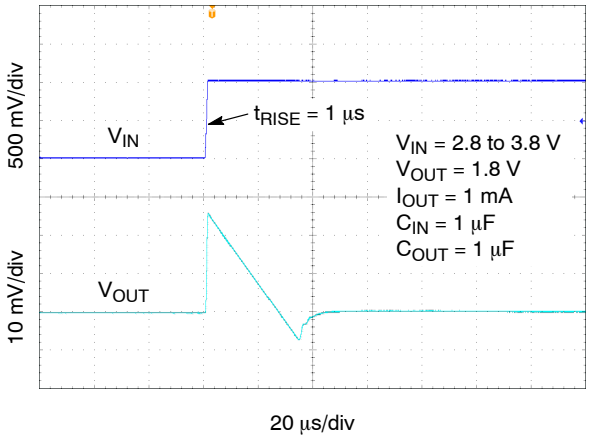



**Figure 14. Line Transient Response – Rising Edge**

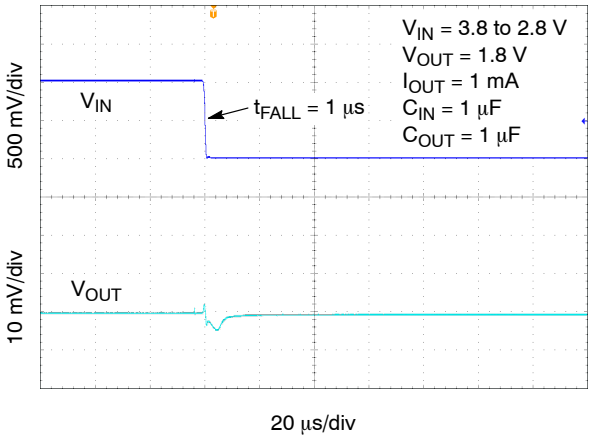



**Figure 15. Line Transient Response – Falling Edge**

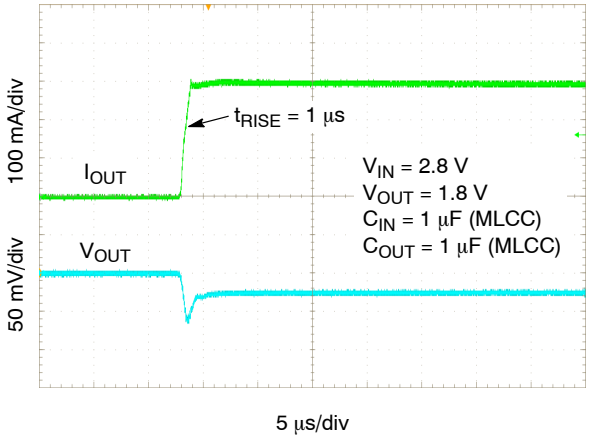



**Figure 16. Load Transient Response – Rising Edge**

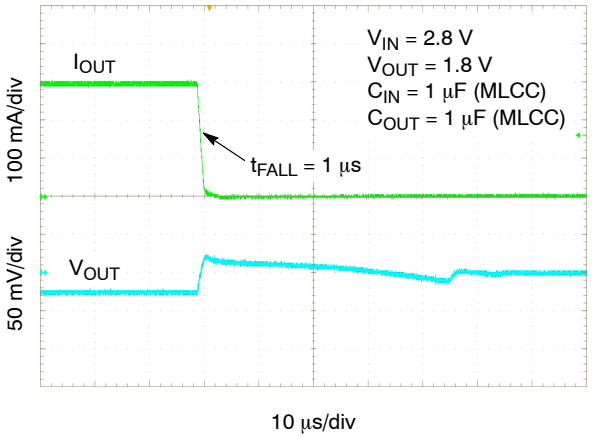



**Figure 17. Load Transient Response – Falling Edge**

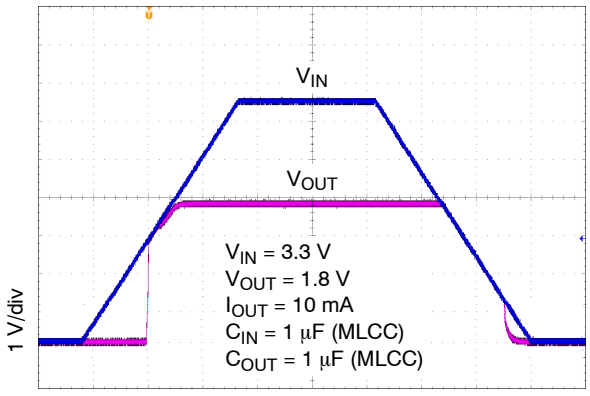



**Figure 18. Turn−on/off – Slow Rising $V_{IN}$**

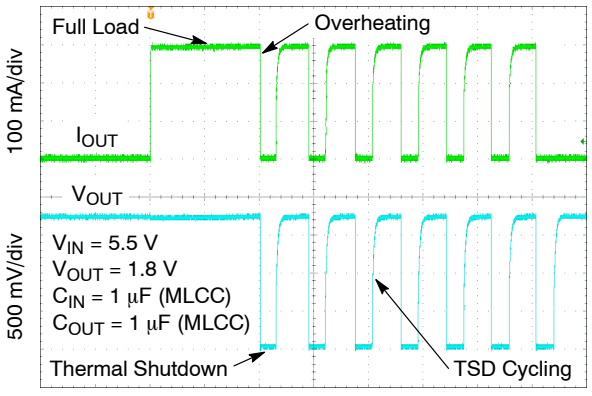



**Figure 19. Short Circuit and Thermal Shutdown**

## APPLICATIONS INFORMATION

### General

The NCP146 is a high performance 300 mA Low Dropout Linear Regulator. This device delivers very high PSRR (over 75 dB at 1 kHz) and excellent dynamic performance as load/line transients. In connection with very low quiescent current this device is very suitable for various battery powered applications such as tablets, cellular phones, wireless and many others. The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

### Input Capacitor Selection ($C_{IN}$)

It is recommended to connect at least a 1 μF Ceramic X5R or X7R capacitor as close as possible to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage. There is no requirement for the min. /max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes. Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

### Output Decoupling ($C_{OUT}$)

The NCP146 requires an output capacitor connected as close as possible to the output pin of the regulator. The recommended capacitor value is 1 μF and X7R or X5R dielectric due to its low capacitance variations over the specified temperature range. The NCP146 is designed to remain stable with minimum effective capacitance of 0.22 μF to account for changes with temperature, DC bias and package size. Especially for small package size capacitors such as 0402 the effective capacitance drops rapidly with the applied DC bias.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the $C_{OUT}$ but the maximum value of ESR should be less than 2 Ω. Larger output capacitors and lower ESR could improve the load transient response or high frequency PSRR. It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature.

### Output Current Limit

Output Current is internally limited within the IC to a typical 600 mA. The NCP146 will source this amount of current measured with a voltage drops on the 90% of the nominal $V_{OUT}$. If the Output Voltage is directly shorted to ground ($V_{OUT}$ = 0 V), the short circuit protection will limit the output current to 630 mA (typ). The current limit and short circuit protection will work properly over whole temperature range and also input voltage range. There is no limitation for the short circuit duration.

### Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold ($T_{SD}$ − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold ($T_{SDU}$ − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides the protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

### Power Dissipation

As power dissipated in the NCP146 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. For reliable operation junction temperature should be limited to +125°C

The maximum power dissipation the NCP146 can handle is given by:

$$P_{D(MAX)} = \frac{\left[125^{\circ}C - T_A\right]}{\theta_{JA}} \qquad \text{(eq. 1)}$$

The power dissipated by the NCP146 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}@I_{OUT}\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \qquad \text{(eq. 2)}$$

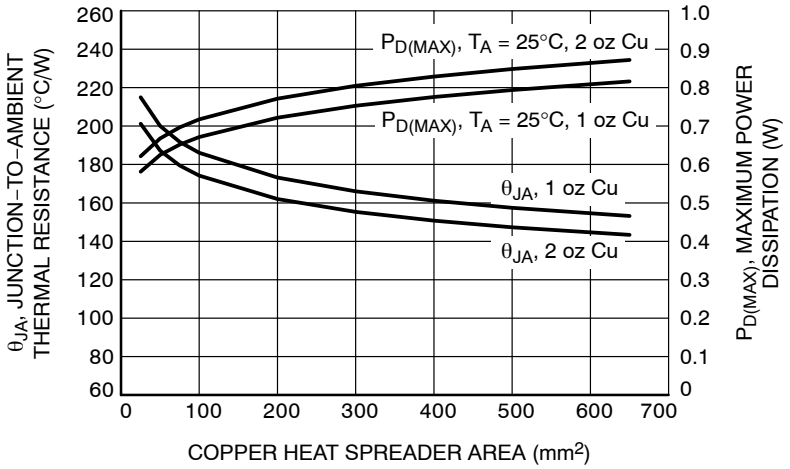



**Figure 20. $\theta_{JA}$ vs. Copper Area**

### Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases, where the extended reverse current condition can be anticipated the device may require additional external protection.

### Power Supply Rejection Ratio

The NCP146 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz − 10 MHz can be tuned by the selection of $C_{OUT}$ capacitor and proper PCB layout.

### PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place $C_{IN}$ and $C_{OUT}$ capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size, use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated from the equation above (Equation 2). Expose pad should be tied the shortest path to the GND pin.

## ORDERING INFORMATION

| Device | Voltage Option | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCP146CD180R2G | 1.8 V | PC180 | SOIC−8 (Pb−Free) | 3000 / Tape & Reel |

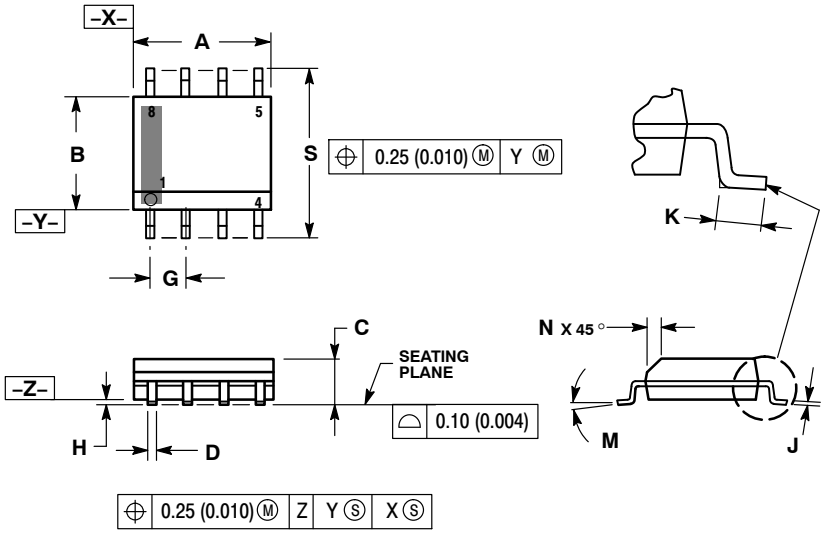
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

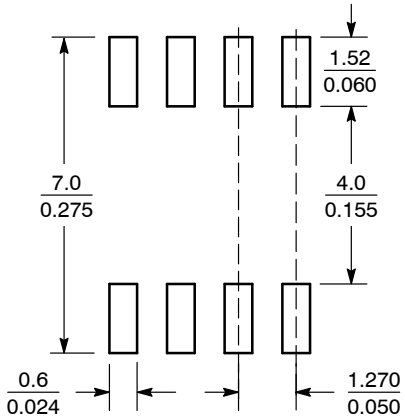
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

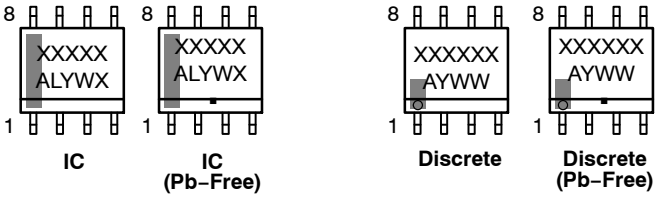
### SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42564B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **SOIC−8 NB** | **PAGE 1 OF 2** |

**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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