# NL3S22AH, NL3S22UH

# USB 2.0 + Audio Switch

The NL3S22AH/NL3S22UH is a double−pole/double−throw (DPDT) analog switch for routing high speed differential data and audio. The differential channels are compliant with High Speed USB 2.0, Full Speed USB 1.1, Low Speed USB 1.0 and any generic UART protocol. The multi−purpose audio path is capable of passing signals with negative voltages as low as 3 V below ground and features shunt resistors to reduce Pop and Click noise in the audio system.

For the NL3S22AH, the audio path (AUDP/AUDN) will be selected with SEL=0 with the device enabled (EN = 1). For the NL3S22UH, the high speed data path (HDP/HDN) will be selected with SEL=0 with the device enabled (EN = 1).

### Features

- $V_{CC}$ Range: 2.7 V to 3.7 V
- Control Pins Compatible with 1.8 V Interfaces
- $I_{CC}$: 60 μA (Typ)
- ESD Performance: 2 kV HBM
- Available in 1.4 mm x 1.8 mm UQFN10
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### High Speed Data Path

- Input Signal Range: 0 V to 4.5 V
- $R_{DS(on)}$: 5.4 Ω (Typ)
- $C_{ON}$: 8.7 pF (Typ)
- Data Rate: USB 2.0–Compliant – up to 480 Mbps
- Bandwidth: >811 MHz

### Audio Path

- Input Signal Range: −3.0 V to 3.0 V
- $R_{DSON}$: 0.56 Ω (Typ)
- $R_{ON(FLAT)}$: 0.004 Ω (Typ)
- THD+N:
  - − 113 dB ($R_L$ = 32 Ω / $V_{IS}$ = 1.0 $V_{RMS}$)
  - − 109 dB ($R_L$ = 16 Ω / $V_{IS}$ = 0.4 $V_{RMS}$)

### Applications

- Smartphones
- Tablets
- USB 2.0 Hosts/Peripherals
- Audio / High−Speeds Data Switching
- USB Type−C Switching

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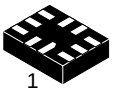
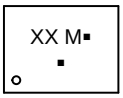
**MARKING DIAGRAM**




**UQFN10**
**CASE 488AT**




XX = AY for NL3S22AHMUTAG
= DW for NL3S22UHMUTAG
M = Date Code
▪ = Pb−Free Device
(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NL3S22AHMUTAG | UQFN10 (Pb−Free) | 3000 / Tape & Reel |
| NL3S22UHMUTAG | UQFN10 (Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

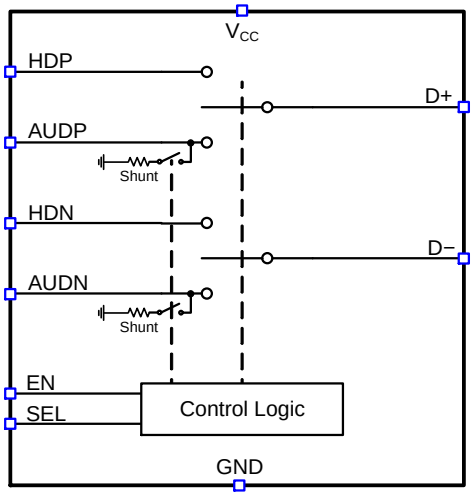



**Figure 1. Block Diagram**

**FUNCTION TABLE**

| EN | SEL | | Shunt Status | D+/D− Function |
|---|---|---|---|---|
| | NL3S22AH | NL3S22UH | | |
| 0 | X | X | ON | No Connect (Power Down) |
| 1 | 0 | 1 | OFF | AUDP/AUDN |
| 1 | 1 | 0 | ON | HDP/HDN |

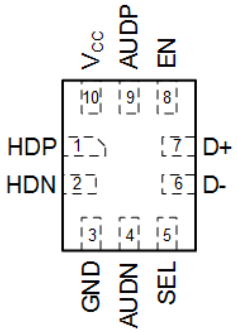



**Figure 2. UQFN10 – Top Through View**

**PIN DESCRIPTION**

| Pin Name | Pin | Description |
|---|---|---|
| HDP | 1 | High Speed Differential Data (+) |
| HDN | 2 | High Speed Differential Data (−) |
| GND | 3 | Ground |
| AUDN | 4 | Audio Signal (−) |
| SEL | 5 | Function Select |
| D− | 6 | Audio/Data Common I/O (−) |
| D+ | 7 | Audio/Data Common I/O (+) |
| EN | 8 | Chip Enable |
| AUDP | 9 | Audio Signal (+) |
| $V_{CC}$ | 10 | Power Supply |

## MAXIMUM RATINGS

| Rating | Symbol | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | −0.5 to +4.2 | V |
| $V_{IS}$ | Analog Input/Output Voltage | HDP, HDN | −0.5 to +5.5 | V |
| | | AUDP, AUDN | −3.5 to +4.2 | |
| | | D+, D− | −3.5 to +5.5 | |
| $V_{IN}$ | Digital Control Pin Voltage on EN, SEL | | −0.5 to $V_{CC}$ + 0.5 | V |
| $T_s$ | Storage Temperature | | −55 to +150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 seconds | | 260 | °C |
| $T_J$ | Junction Temperature Under Bias | | 150 | °C |
| MSL | Moisture Sensitivity (Note 1) | | Level 1 | |
| $I_{LU}$ | Latchup Current (Note 2) | | ±100 | mA |
| ESD | ESD Protection (Note 3) | Human Body Model<br>Charged Device Model | 2000<br>2000 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
2. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114 for all pins.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | 2.7 | 3.7 | V |
| $V_{IS}$ | Switch Input / Output Voltage (Note 4) | HDP, HDN | 0 | 4.5 | V |
| | | AUDP, AUDN | −3.0 | 3.0 | |
| | | D+, D− | −3.0 | 4.5 | |
| $V_{IN}$ | Digital Control Input Voltage | | GND | $V_{CC}$ | V |
| $T_A$ | Operating Temperature Range | | −40 | +85 | °C |

4. If the audio channel is not in use, it is recommended that no signals are applied on the audio inputs AUDN and AUDP.

**DC ELECTRICAL CHARACTERISTICS** (Typical values are at $V_{CC}$ = +3.6 V and $T_A$ = +25°C, unless otherwise specified)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | −40 °C to 85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **POWER SUPPLY** | | | | | | | |
| $I_{CC}$ | Supply Current | EN = 1, $I_{IS}$ = 0 mA | 3.6 | − | 60 | 100 | μA |
| | | EN = 0 (Power Down) | | − | − | 1.0 | |
| **Control Logic (EN, SEL)** | | | | | | | |
| $V_{IH}$ | Input High Voltage | | 3.6 | 1.4 | − | − | V |
| | | | 2.7 | 1.3 | − | − | |
| $V_{IL}$ | Input Low Voltage | | 3.6 | − | − | 0.4 | V |
| | | | 2.7 | − | − | 0.4 | |
| $V_{IHYS}$ | Input Hysteresis | | 2.7 – 3.6 | − | 250 | − | mV |
| $I_{IN}$ | Leakage Current | | 2.7 – 3.6 | − | − | ±100 | nA |
| **AUDIO SWITCH (AUDP/AUDN ↔ D+/D−)** | | | | | | | |
| $R_{ON}$ | ON−Resistance | $V_{IS}$ = −3.0 V to 3.0 V, $I_{IS}$ = 50 mA | 3.0 | − | 0.56 | 0.73 | Ω |
| $\Delta R_{ON}$ | ON−Resistance Matching Between Channels | $V_{IS}$ = −3.0 V to 3.0 V, $I_{IS}$ = 50 mA | 3.0 | − | 0.07 | − | Ω |
| $R_{FLAT(ON)}$ | ON Resistance Flatness | $V_{IS}$ = −3.0 V to 3.0 V, $I_{IS}$ = 50 mA | 3.0 | − | 0.004 | − | Ω |
| $R_{SH}$ | Shunt Resistance | | 3.6 | − | 110 | 200 | Ω |
| $I_{SW(OFF)}$ | OFF−State Leakage | EN = 0, $V_{IS}$ = 3.0 V at D+/D− | 3.6 | − | − | ±200 | nA |
| $I_{SW(ON)}$ | ON−State Leakage | $V_{IS}$ = 0 V to 3.0 at D+/D−, AUDP = AUDP = open | 3.6 | − | ±2.2 | ±3.0 | μA |
| **DATA SWITCH (HDP/HDN ↔ D+/D−)** | | | | | | | |
| $R_{ON}$ | ON−Resistance | $V_{IS}$ = 0 V to 1.7 V, $I_{IS}$ = 15 mA | 3.0 | − | 5.4 | 6.63 | Ω |
| $\Delta R_{ON}$ | ON−Resistance Matching Between Channels | $V_{IS}$ = 0 V to 1.7 V, $I_{IS}$ = 15 mA | 3.0 | − | 0.2 | − | Ω |
| $R_{FLAT(ON)}$ | ON Resistance Flatness | $V_{IS}$ = 0 V to 1.7 V, $I_{IS}$ = 15 mA | 3.0 | − | 0.002 | − | Ω |
| $I_{SW(OFF)}$ | OFF−State Leakage | EN = 0, $V_{IS}$ = 0 V to 3.6 V | 3.6 | − | − | ±200 | nA |
| $I_{SW(ON)}$ | ON−State Leakage | $V_{IS}$ = 0 V to 3.6 V | 3.6 | − | − | ±200 | nA |

**AC ELECTRICAL CHARACTERISTICS** (Typical values are at $V_{CC}$ = +3.6 V and $T_A$ = +25°C)

| Symbol | Parameter | Test Conditions | $V_{CC}$ (V) | −40 °C to 85 °C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | |
| **AUDIO SWITCH (AUDP/AUDN ↔ D+/D−)** | | | | | | | |
| THD | Audio THD | f = 20 Hz to 20 kHz,<br>$V_{IS}$ = 1.0 $V_{RMS}$, DC Bias = 0 V,<br>$R_L$ = 32 Ω<br>$V_{IS}$ = 0.4 $V_{RMS}$, DC Bias = 0 V,<br>$R_L$ = 16 Ω | 2.7 – 3.6 | − | <br><br>−113<br><br>−109 | − | dB |
| PSRR | Power Supply Ripple Rejection | From $V_{CC}$ unto AUDP/AUDN,<br>f = 217 Hz, $R_L$ = 16 Ω | 2.7 – 3.6 | − | 106 | − | dB |
| **DATA SWITCH (HDP/HDN ↔ D+/D−)** | | | | | | | |
| $C_{ON}$ | Equivalent ON−Capacitance | Switch ON, f = 1 MHz | 3.6 | − | 8.7 | 10 | pF |
| $C_{OFF}$ | Equivalent OFF−Capacitance | Switch OFF, f = 1 MHz | 3.6 | − | 1.8 | − | pF |
| $D_{IL}$ | Differential Insertion Loss | f = 10 MHz | 2.7 – 3.6 | − | −0.5 | − | dB |
| | | f = 800 MHz | 2.7 – 3.6 | − | −2.8 | − | |
| $D_{ISO}$ | Differential Off−Isolation | f = 10 MHz | 2.7 – 3.6 | − | −54 | − | dB |
| | | f = 800 MHz | 2.7 – 3.6 | − | −25 | − | |
| $D_{CTK}$ | Differential Crosstalk | f = 10 MHz | 2.7 – 3.6 | − | −62 | − | dB |
| | | f = 800 MHz | 2.7 – 3.6 | − | −28 | − | |
| PSRR | Power Supply Ripple Rejection | From $V_{CC}$ unto D+/D−,<br>f = 217 Hz, $R_L$ = 50 Ω | 2.7 – 3.6 | − | 111 | − | dB |
| **DYNAMIC TIMING** | | | | | | | |
| $t_{PD}$ | Propagation Delay (Notes 5 and 6) | $V_{NOn}$ or $V_{NCn}$ = 0V, $R_L$ = 50 Ω | 2.7 – 3.6 | − | 0.25 | − | ns |
| $t_{EN}$ | Enable Time,<br>EN to HDx<br>EN to AUDx | $V_{IS}$ = 1 V, $R_L$ = 50 Ω, $C_L$ = 7 pF<br>(fixture only) | 2.7 – 3.6 | <br>−<br>− | <br>2.1<br>5.1 | <br>−<br>− | µs |
| $t_{DIS}$ | Disable Time,<br>EN to HDx<br>EN to AUDx | $V_{IS}$ = 1 V, $R_L$ = 50 Ω, $C_L$ = 7 pF<br>(fixture only) | 2.7 – 3.6 | <br>−<br>− | <br>157<br>53 | <br>−<br>− | ns |
| $t_{ON}$ | Turn−On Time,<br>SEL to HDx<br>SEL to AUDx | $V_{IS}$ = 1 V, $R_L$ = 50 Ω, $C_L$ = 7 pF<br>(fixture only) | 2.7 – 3.6 | <br>−<br>− | <br>0.3<br>3.4 | <br>−<br>− | µs |
| $t_{OFF}$ | Turn−Off Time,<br>SEL to HDx<br>SEL to AUDx | $V_{IS}$ = 1 V, $R_L$ = 50 Ω, $C_L$ = 7 pF<br>(fixture only) | 2.7 – 3.6 | <br>−<br>− | <br>157<br>44 | <br>−<br>− | ns |
| $t_{INIT}$ | Initialization Time (Notes 5 and 7), $V_{CC}$ to D+/D− | $V_{IS}$ = 1 V, $R_L$ = 50 Ω, $C_L$ = 7 pF<br>(fixture only) | 2.7 – 3.6 | 150 | − | − | µs |
| $t_{sk(b-b)}$ | Bit to bit skew | Within the same differential channel | 2.7 – 3.6 | − | 5 | − | ps |
| $t_{sk(ch-ch)}$ | Channel to channel skew | Maximum skew between all channels | 2.7 – 3.6 | − | 5 | − | ps |

5. Guaranteed by design.
6. No other delays than the RC network formed by the load resistance and the load capacitance of the switch are added on the bus. For a 10 pF load, this delay is 5 ns which is much smaller than rise and fall time of typical driving systems. Propagation delays on the bus are determined by the driving circuit on the driving side and its interactions with the load of the driven side.
7. Wait time required after $V_{CC}$ power−up to operating level before data access is valid.

## PARAMETER MEASUREMENT INFORMATION

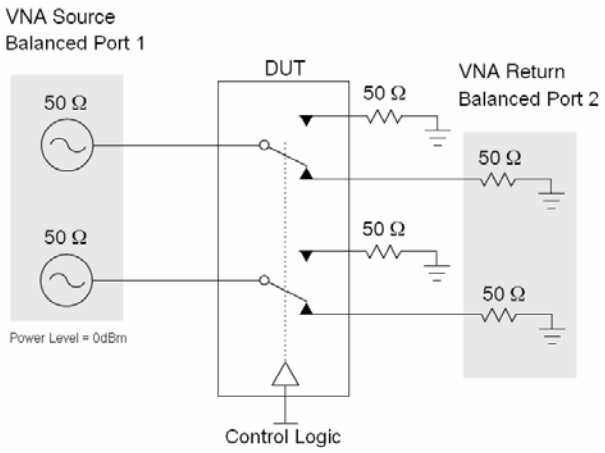



**Figure 3. Differential Insertion Loss ($S_{DD21}$)**

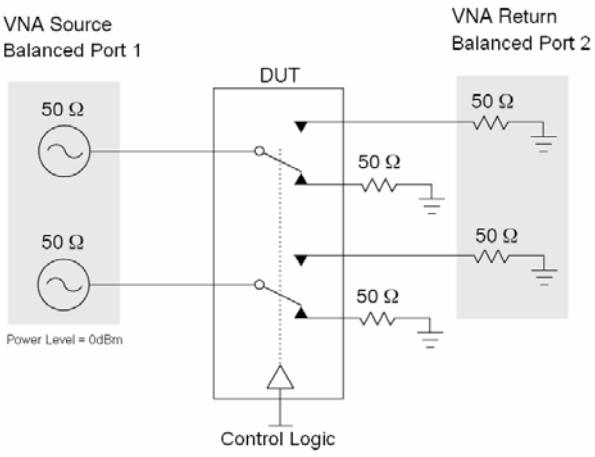



**Figure 4. Differential Off Isolation ($S_{DD21}$)**

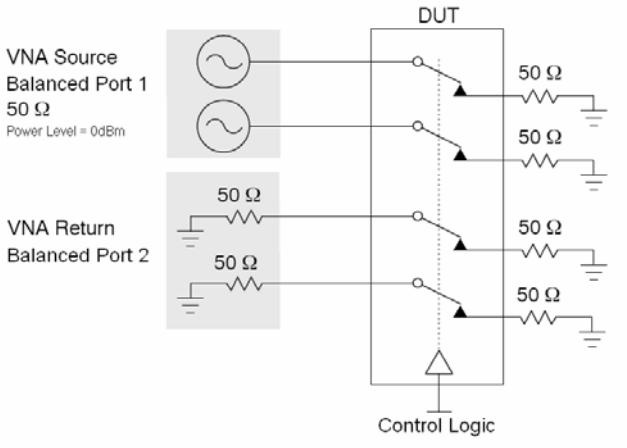
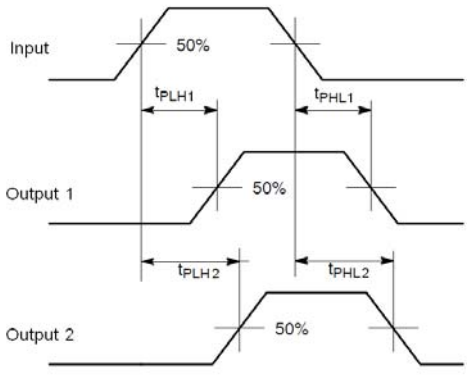
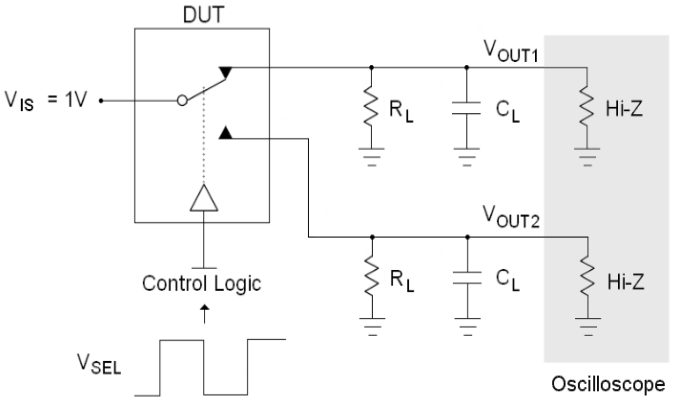



**Figure 5. Differential Crosstalk ($S_{DD21}$)**




$t_{skew} = |t_{PLH1}-t_{PLH2}|$ or $|t_{PHL1}-t_{PHL2}|$

**Figure 6. Bit−to−Bit and Channel−to−Channel Skew**



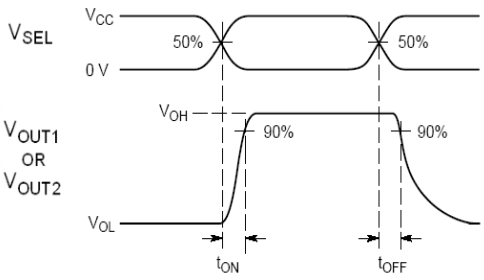




**Figure 7. $t_{ON}$ and $t_{OFF}$**

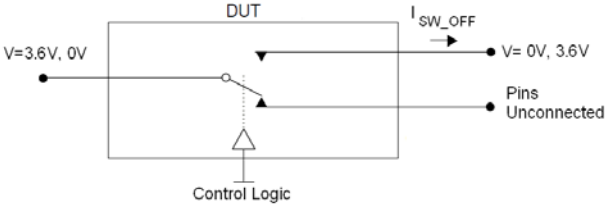



**Figure 8. Off State Leakage**

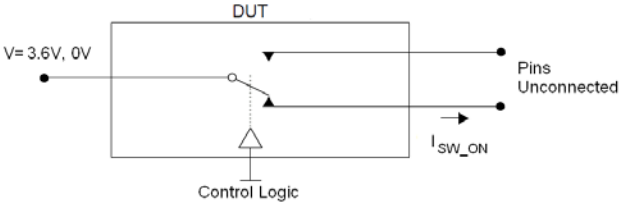



**Figure 9. On State Leakage**

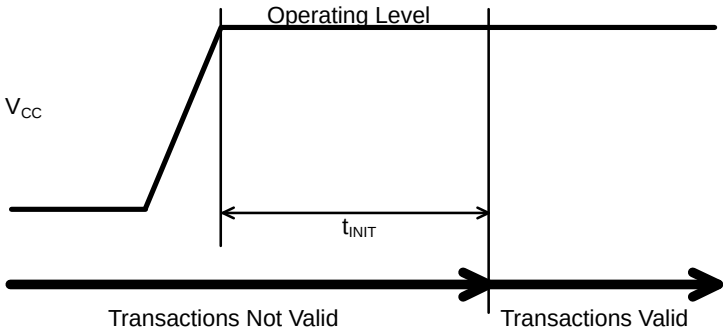



**Figure 10. $t_{INIT}$, Initialization Time**

## TYPICAL OPERATING CHARACTERISTICS

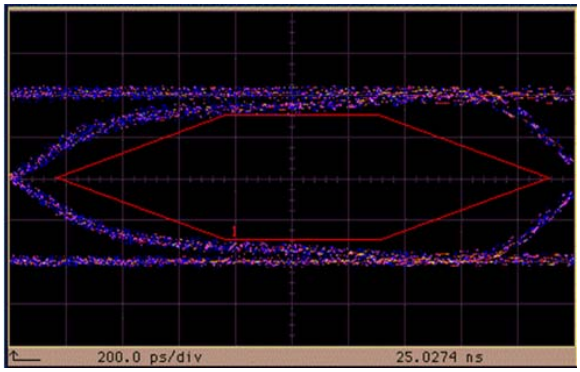



Figure 11. USB 2.0 High Speed Eye Diagram

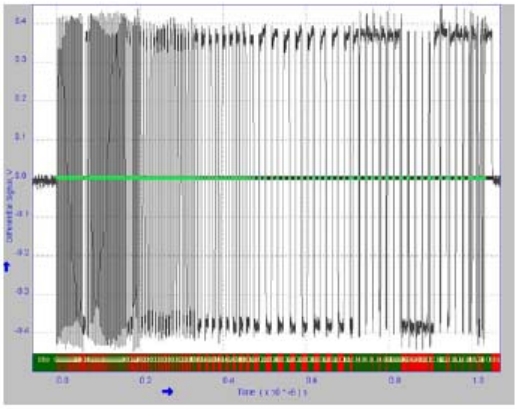


Figure 12. USB 2.0 High Speed Pattern

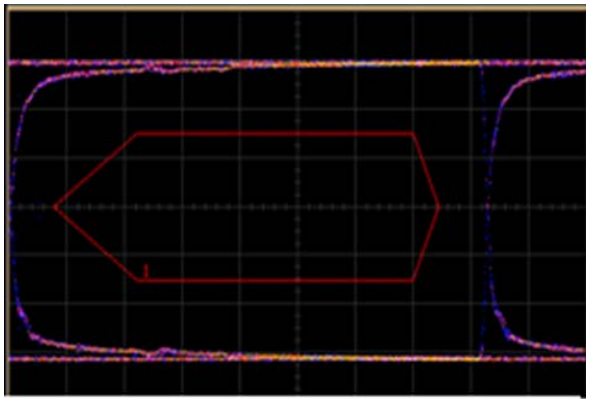


Figure 13. USB 1.1 Full Speed Eye Diagram

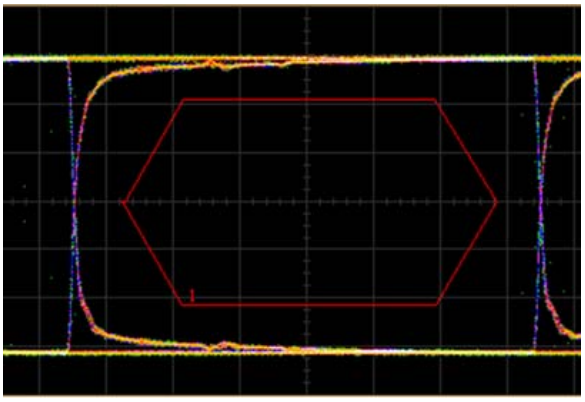


Figure 14. USB 1.0 Low Speed Eye Diagram

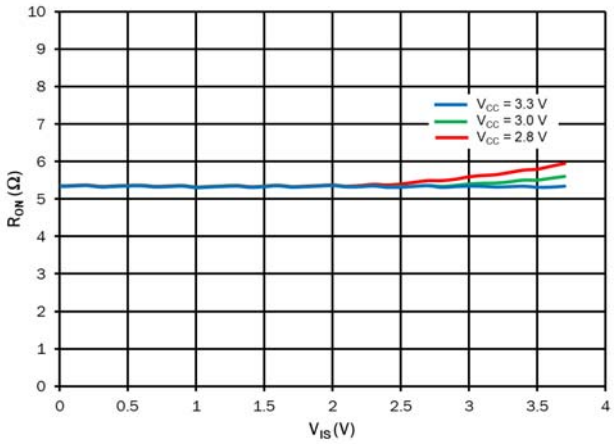



Figure 15. Data Path On Resistance

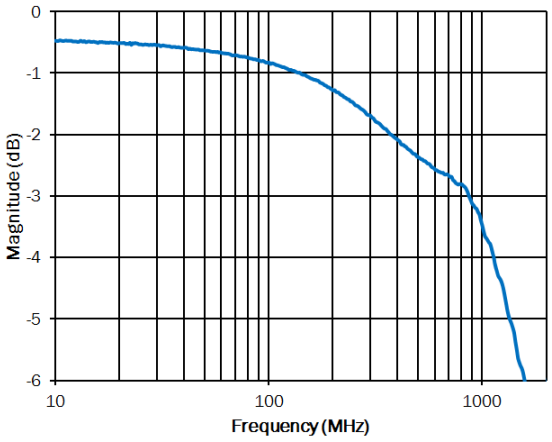



Figure 16. Data Switch Differential Insertion Loss

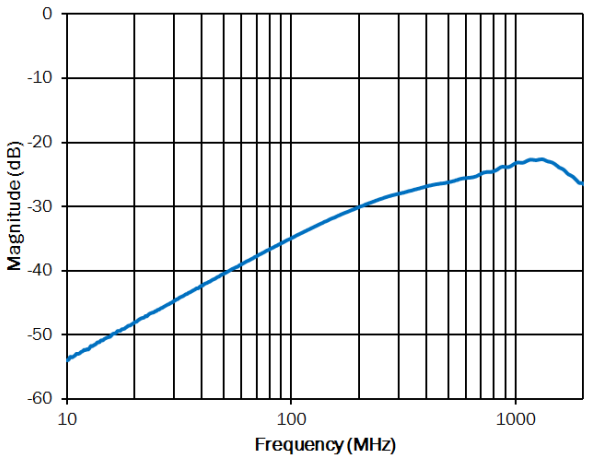



**Figure 17. Data Switch Differential Off−Isolation**

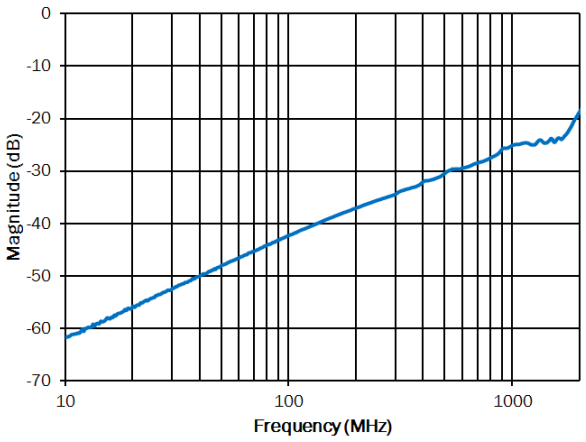



**Figure 18. Data Switch Differential Crosstalk**

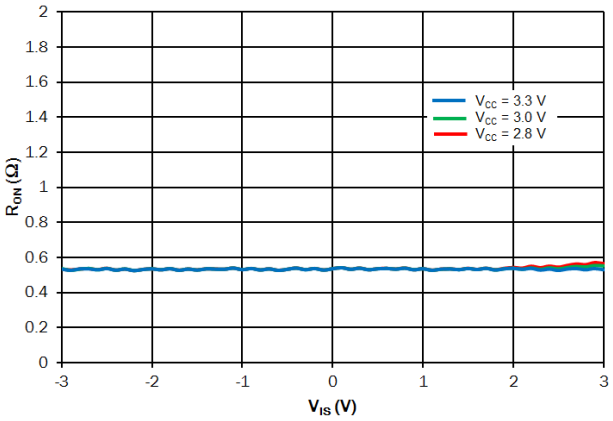



**Figure 19. Audio Path On Resistance**

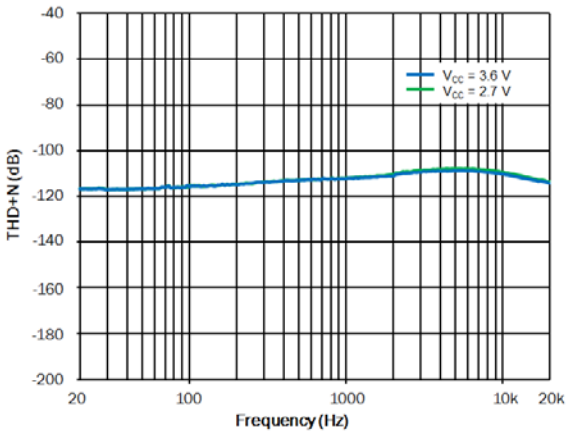



**Figure 20. Audio THD+N ($R_L$ = 32 Ω, $V_{IS}$ = 1.0 $V_{RMS}$)**

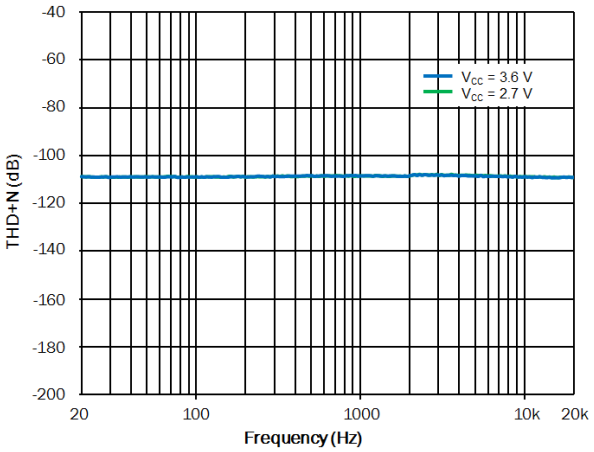


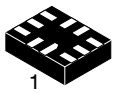

**Figure 21. Audio THD+N ($R_L$ = 16 Ω, $V_{IS}$ = 0.4 $V_{RMS}$)**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

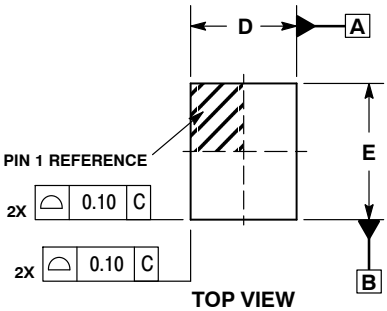
ON Semiconductor®

**UQFN10 1.4x1.8, 0.4P**
CASE 488AT−01
ISSUE A

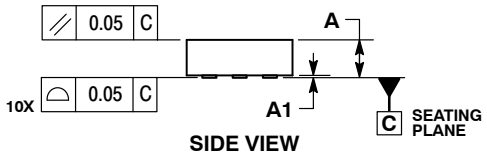
DATE 01 AUG 2007



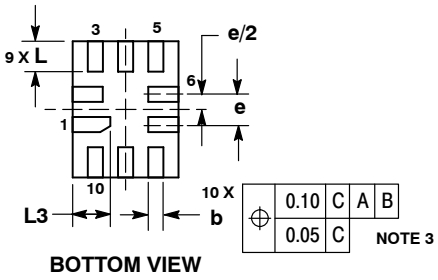
**SCALE 5:1**



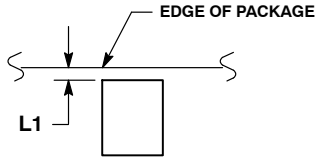

**TOP VIEW**



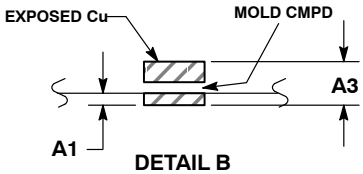

**SIDE VIEW**




**BOTTOM VIEW**




**DETAIL A**
**Bottom View**
**(Optional)**

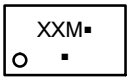



**DETAIL B**
**Side View**
**(Optional)**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.45 | 0.60 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 REF | |
| b | 0.15 | 0.25 |
| D | 1.40 BSC | |
| E | 1.80 BSC | |
| e | 0.40 BSC | |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |
| L3 | 0.40 | 0.60 |

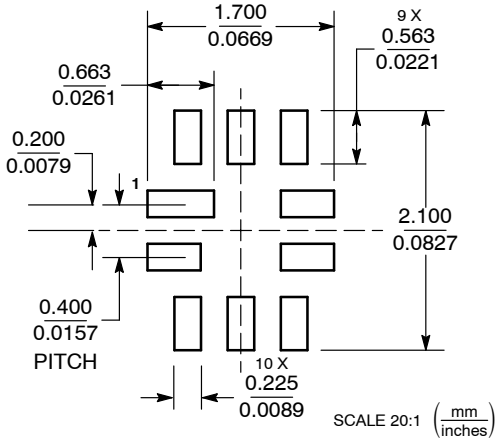
### GENERIC MARKING DIAGRAM*




XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

### MOUNTING FOOTPRINT




SCALE 20:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

| | | |
|---|---|---|
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| **DESCRIPTION:** | **10 PIN UQFN, 1.4 X 1.8, 0.4P** | **PAGE 1 OF 1** |

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