STEVAL-IDP004V1

Data brief

IO-Link master multi-port evaluation board based on L6360

Features

- Main supply voltage 32 V maximum
- 4 L6360 IO-Link master devices
- RS-485 serial interface
- CAN serial interface
- USB interface
- DC-DC converter
- On-board reverse polarity protection
- Designed to meet IEC requirement for industrial standards
- RoHS and WEEE compliant

Description

The STEVAL-IDP004V1 evaluation board with STM32 microcontroller has four separate L6360 ICs.

Communication with the ICs is via I²C in master mode and is managed by the STM32F205RB MCU; each L6360 has its own address and shares the bus with the other devices.

The STEVAL-IDP004V1 is developed to create a multi-port master d based on serial asynchronous communication to support the IO-Link protocol. Each node is equipped with an industrial M12 connector (as required by the standard) for connection with a single slave node using a cable 20 meter long; the wire is a normal three-pole: one for the IO-Link bus, one for the L+ line (positive supply voltage pole) and one for the L- line (negative supply voltage pole).

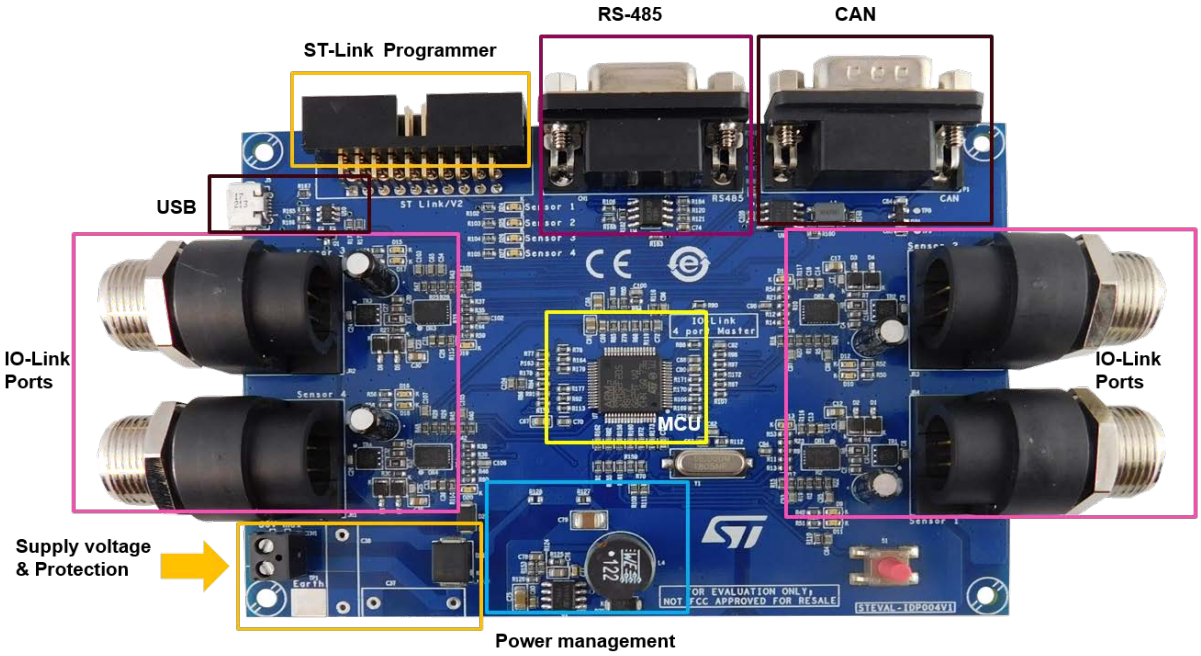
Beyond the IO-Link connection, the board includes RS-485 bus, CAN bus and USB hardware interfaces.

The layout is designed to meet the requirements for IEC61000-4-2/4/5 for industrial segment.

Product summary	
IO-Link master multi-port evaluation board based on L6360	STEVAL-IDP004V1
High-performance ARM Cortex-M3 MCU with 128 Kbytes Flash, 120 MHz CPU, ART Accelerator	STM32F205RB
IO-Link communication master transceiver IC	L6360

1 Block identification

Figure 1. **STEVAL-IDP004V1 block identification**



2 Schematic diagrams

Figure 2. **STEVAL-IDP004V1 circuit schematic (1 of 13)**

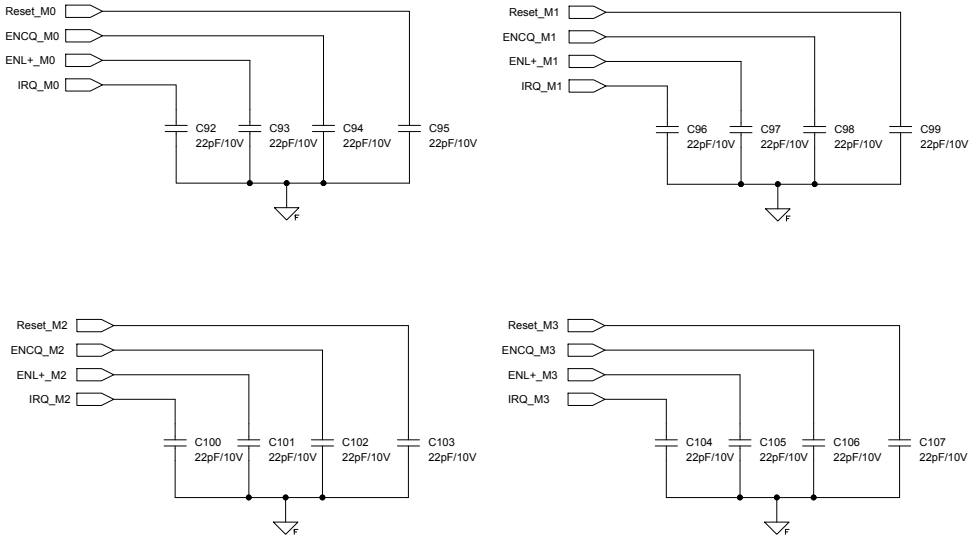


Figure 3. **STEVAL-IDP004V1 circuit schematic (2 of 13)**

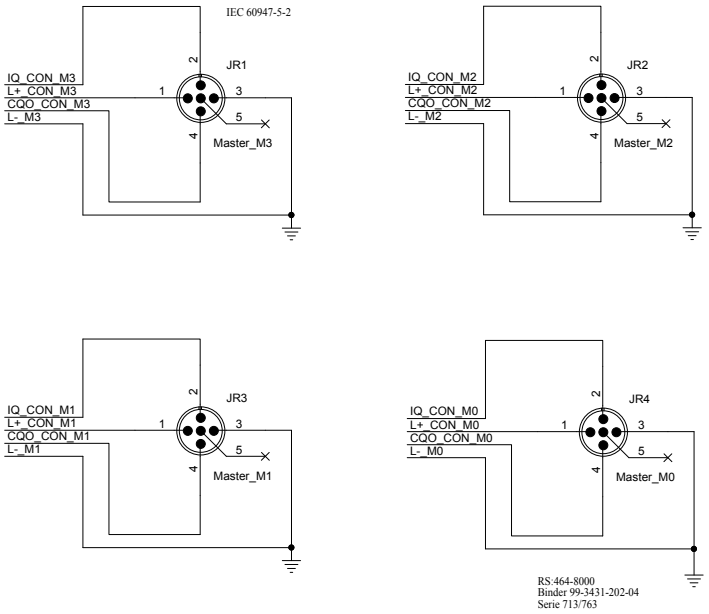


Figure 4. **STEVAL-IDP004V1 circuit schematic (3 of 13)**

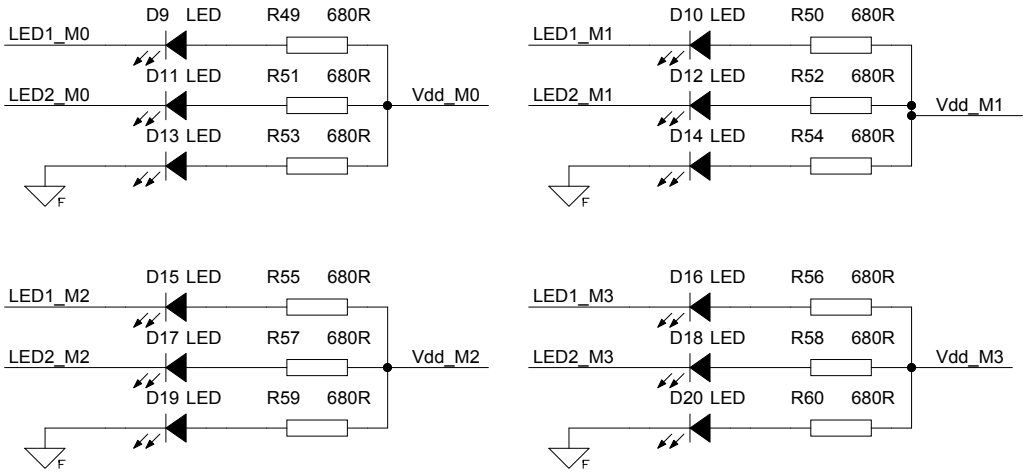


Figure 5. **STEVAL-IDP004V1 circuit schematic (4 of 13)**

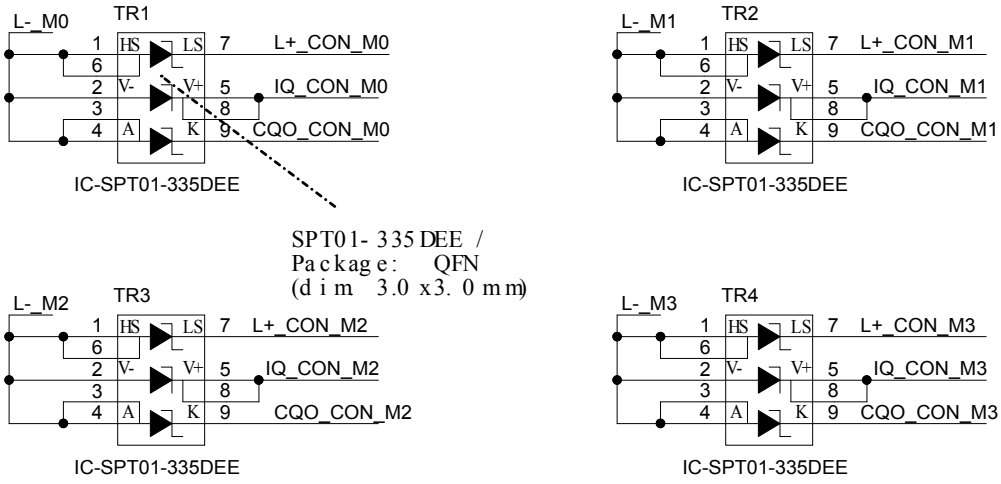


Figure 6. **STEVAL-IDP004V1 circuit schematic (5 of 13)**

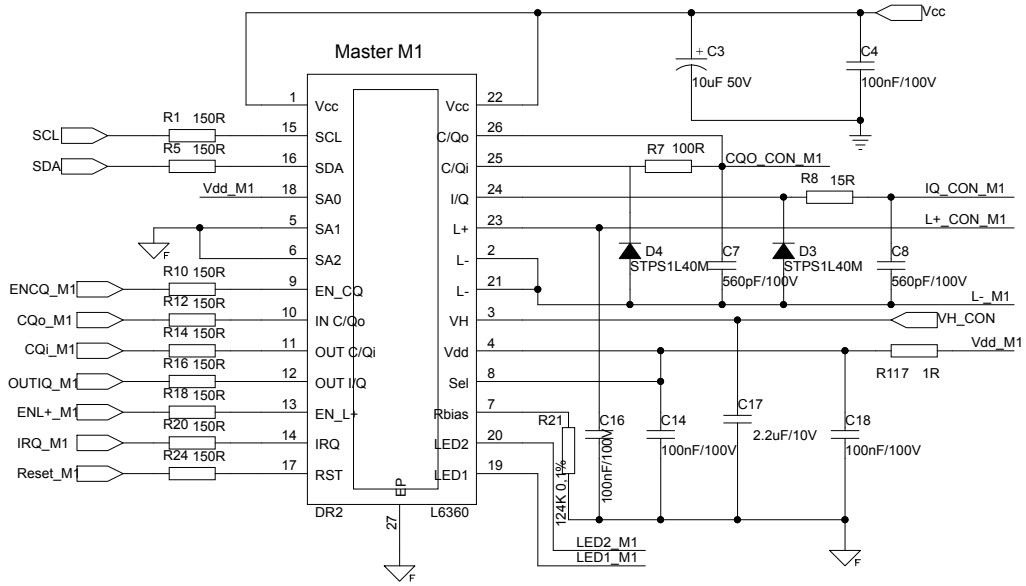


Figure 7. **STEVAL-IDP004V1 circuit schematic (6 of 13)**

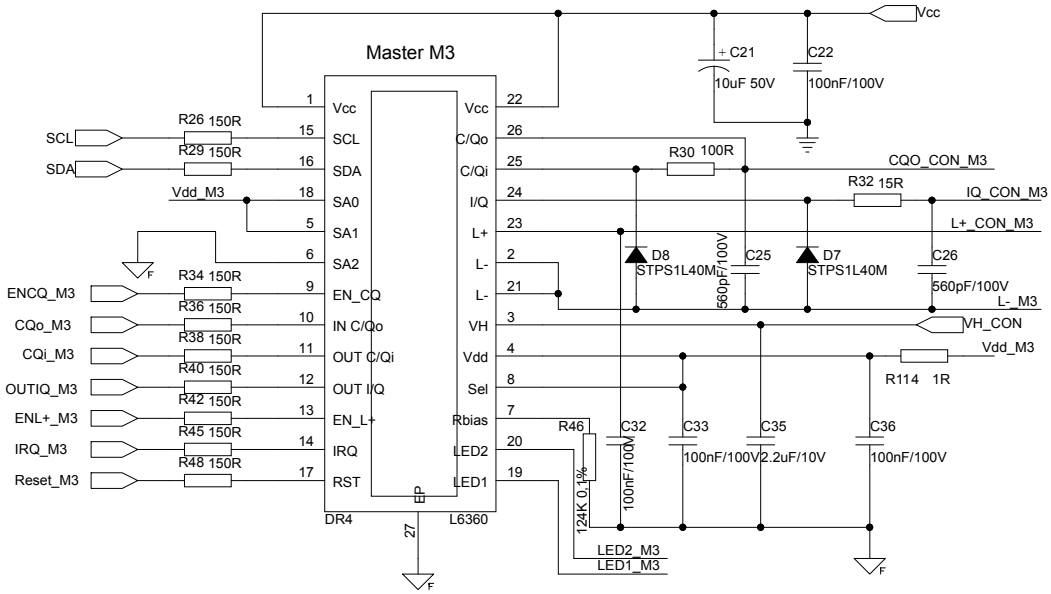


Figure 8. **STEVAL-IDP004V1 circuit schematic (7 of 13)**

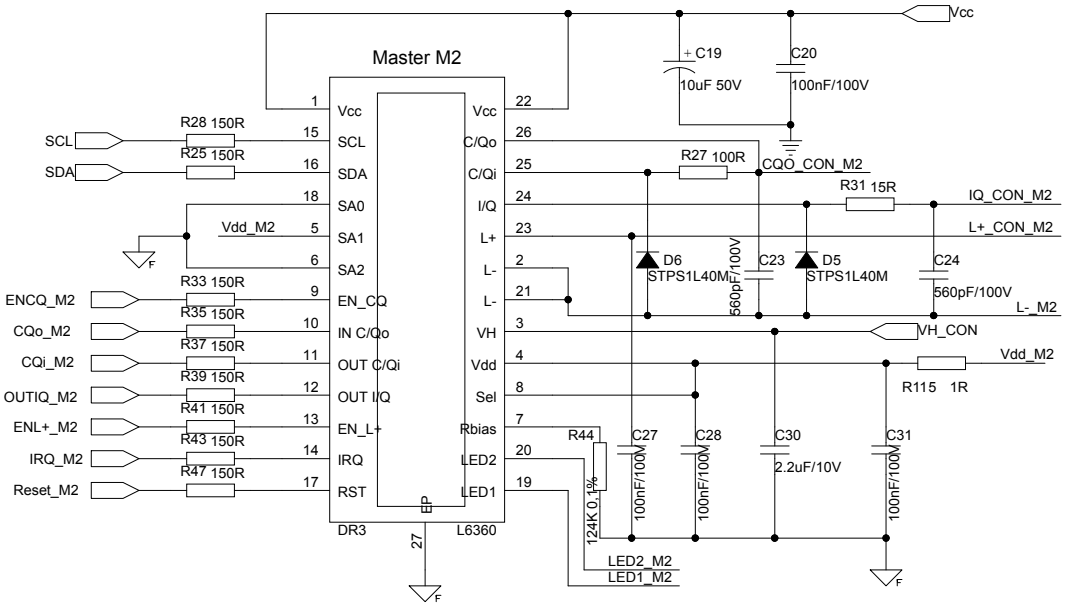


Figure 9. **STEVAL-IDP004V1 circuit schematic (8 of 13)**

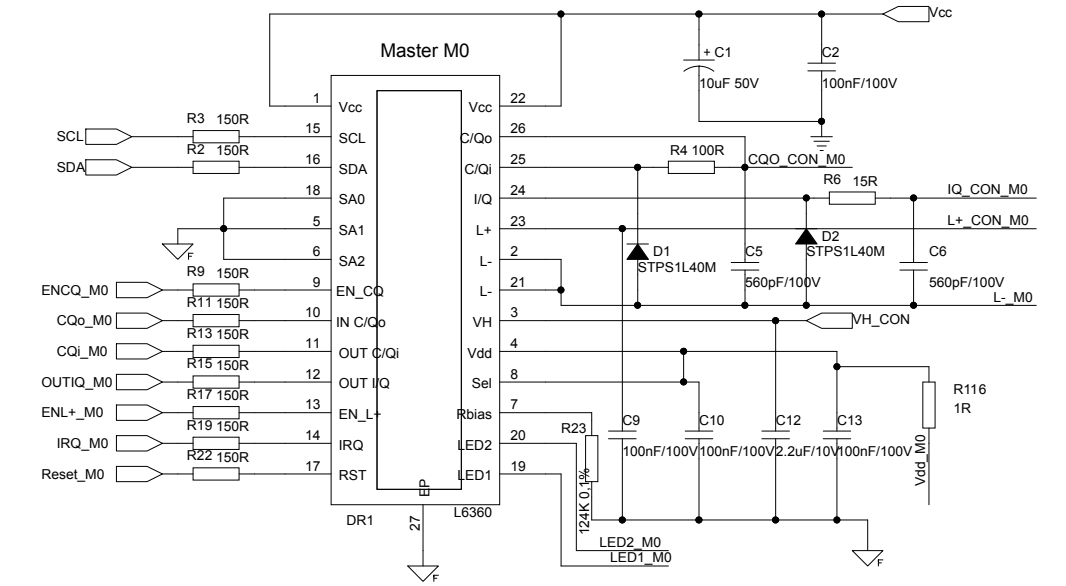


Figure 10. **STEVAL-IDP004V1 circuit schematic (9 of 13)**

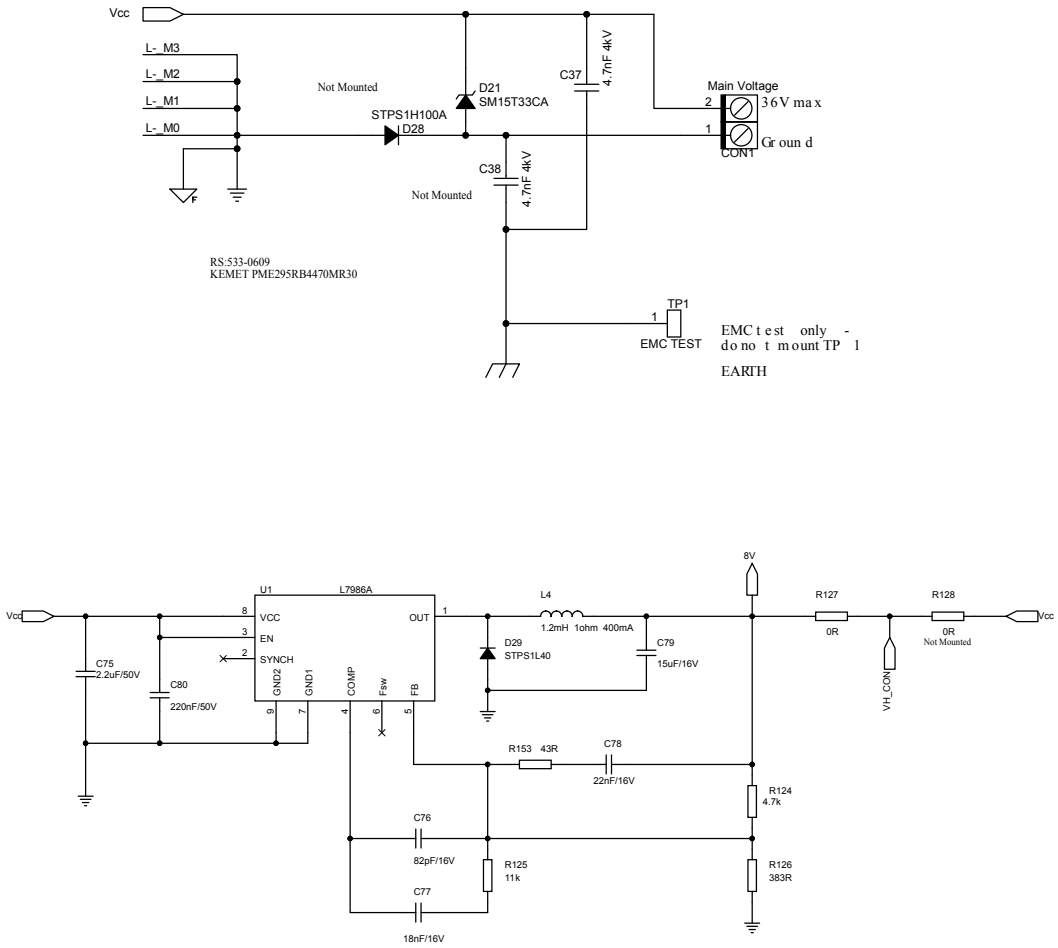


Figure 11. **STEVAL-IDP004V1 circuit schematic (10 of 13)**

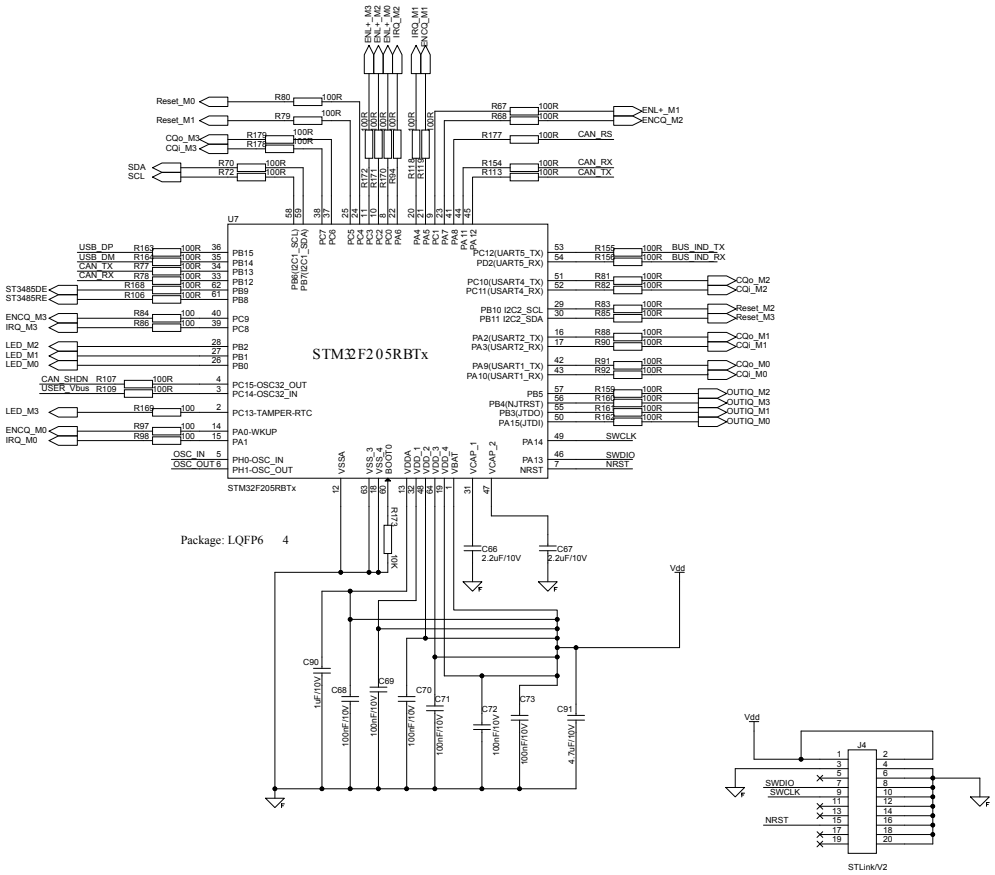


Figure 12. **STEVAL-IDP004V1 circuit schematic (11 of 13)**

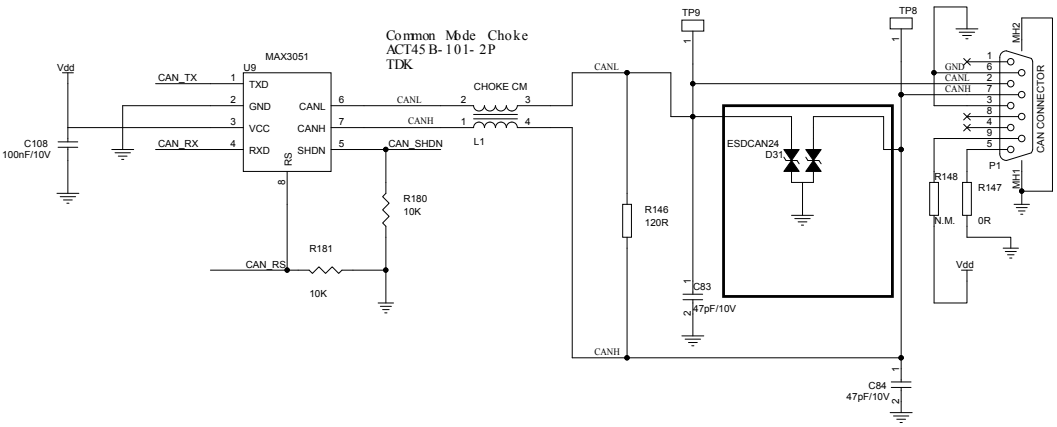


Figure 13. **STEVAL-IDP004V1 circuit schematic (12 of 13)**

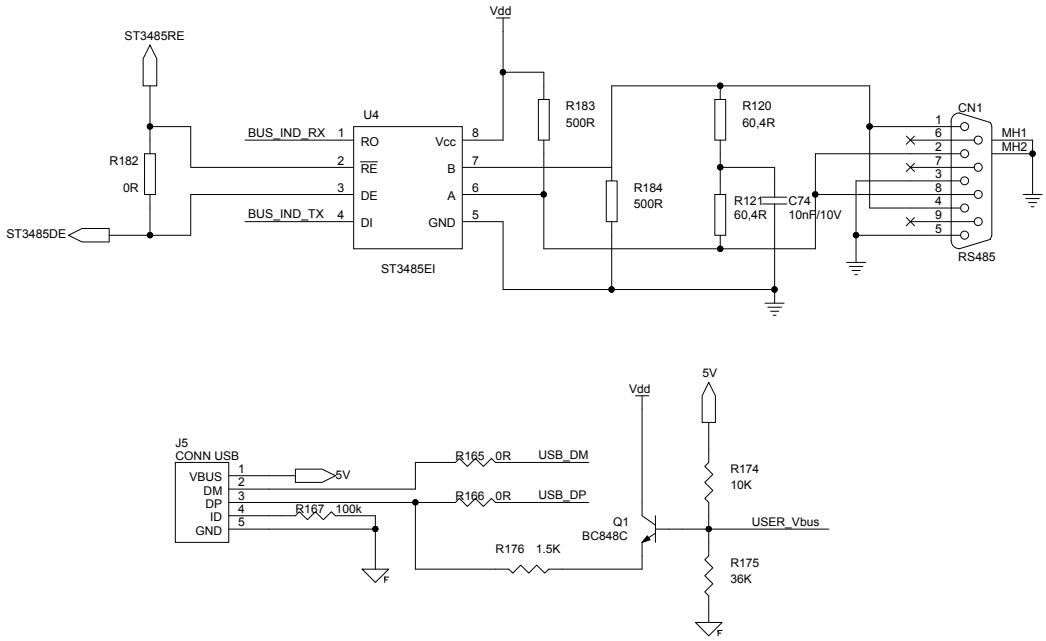
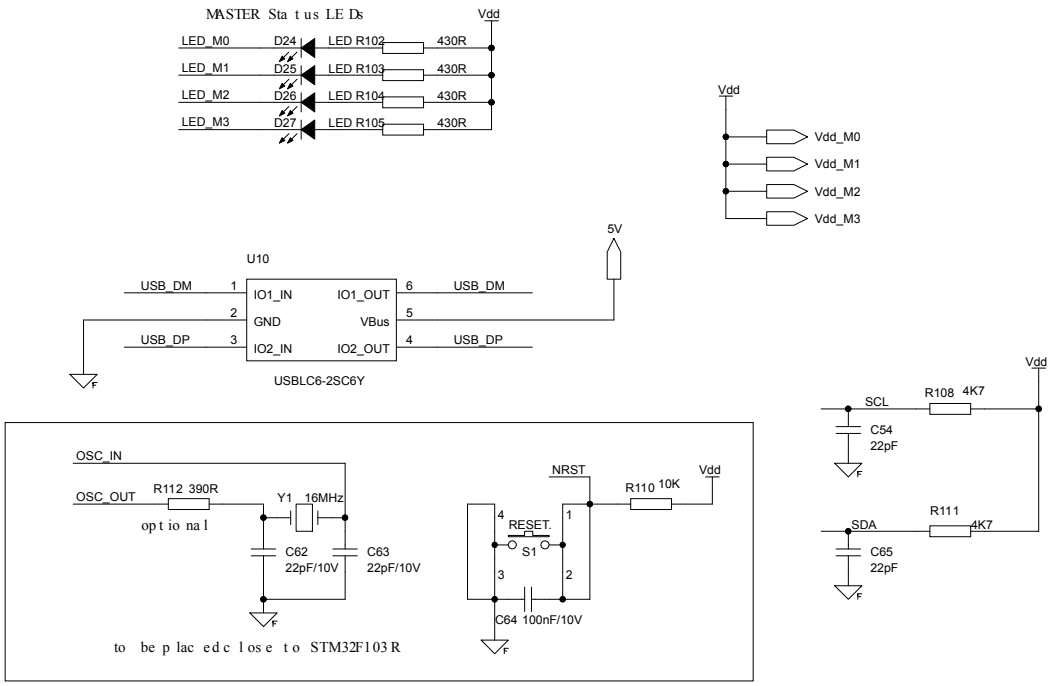


Figure 14. **STEVAL-IDP004V1 circuit schematic (12 of 13)**



Revision history

Table 1. Document revision history

Date	Version	Changes
17-May-2017	1	Initial release.
05-Jul-2017	2	Minor text changes.
27-Jun-2018	3	Updated cover image and Figure 1. STEVAL-IDP004V1 block identification.