

FQU13N06-VB Datasheet

N-Channel 60 V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	R _{DS(on)} (Ω)	I _D (A)	Q _g (Typ.)
60	0.032 at V _{GS} = 10 V	35 ^d	21.7
	0.037 at V _{GS} = 4.5 V	30 ^d	

FEATURES

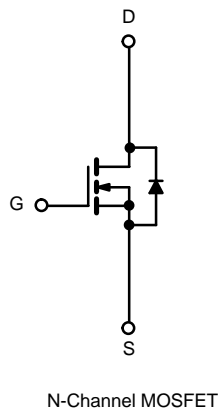
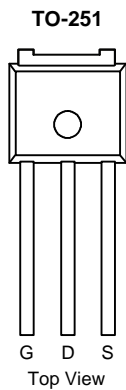
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET[®] Power MOSFET
- 100 % R_g and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Power Supply
- Secondary Synchronous Rectification
- DC/DC Converter



ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	60	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	35 ^d	
		T _C = 70 °C	30 ^d	
Pulsed Drain Current	I _{DM}	100	A	
Avalanche Current	I _{AS}	40		
Single Avalanche Energy ^a	L = 0.1 mH	E _{AS}	80	mJ
Maximum Power Dissipation ^a	P _D	T _C = 25 °C	59.5 ^b	W
		T _A = 25 °C ^c	2.7	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) ^c	R _{thJA}	46	°C/W
Junction-to-Case (Drain)	R _{thJC}	2.1	

Notes:

- Duty cycle ≤ 1 %.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).
- Package limited.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{DS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0		3.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 250	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$			250	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}, V_{GS} = 10\text{ V}$	50			A
Drain-Source On-State Resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 12\text{ A}$		0.032		Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		0.037		
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10\text{ A}$		110		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$		1100		μF
Output Capacitance	C_{oss}			281		
Reverse Transfer Capacitance	C_{rss}			130		
Total Gate Charge ^c	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		46		nC
		$V_{DS} = 30\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		28		
Q_{gs}			7			
Q_{gd}			6.7			
Gate Resistance	R_g	$f = 1\text{ MHz}$	0.4	2	4	Ω
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 1.5\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		8	16	ns
Rise Time ^c	t_r			9	18	
Turn-Off Delay Time ^c	$t_{d(off)}$			35	53	
Fall Time ^c	t_f			9	18	
Drain-Source Body Diode Ratings and Characteristics $T_C = 25\text{ }^\circ\text{C}^b$						
Continuous Current	I_S				50	A
Pulsed Current	I_{SM}				100	
Forward Voltage ^a	V_{SD}	$I_F = 10\text{ A}, V_{GS} = 0\text{ V}$		0.75	1.5	V
Reverse Recovery Time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		34	51	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			2	3	A
Reverse Recovery Charge	Q_{rr}			34	51	nC

Notes:

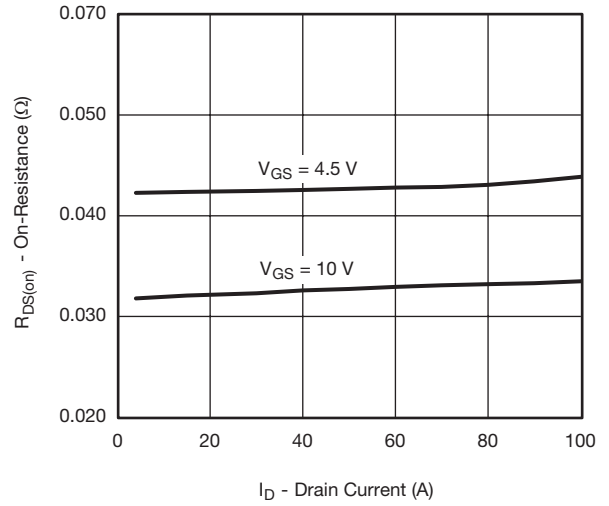
- Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

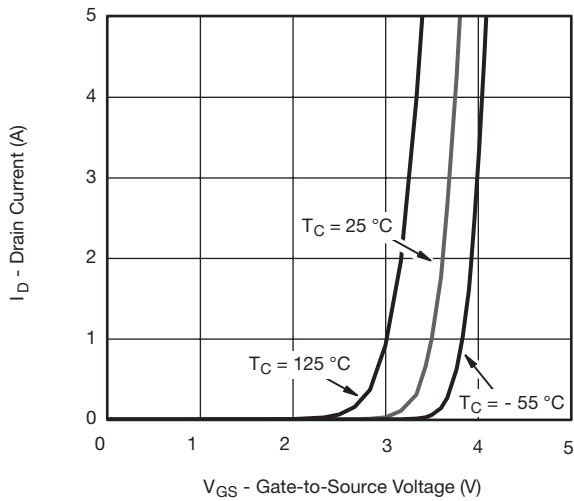
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



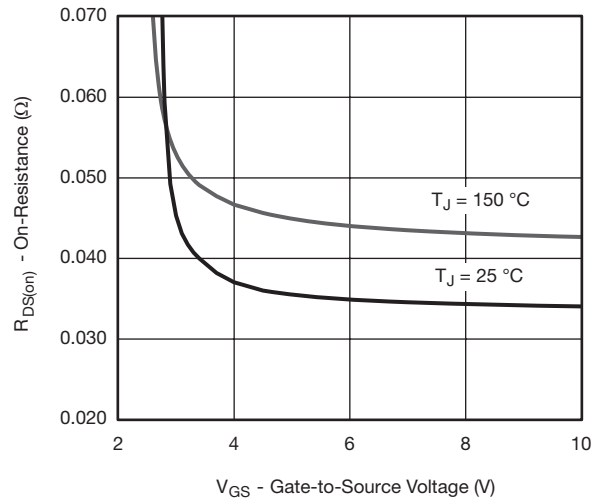
Drain to Source Voltage vs. I_D



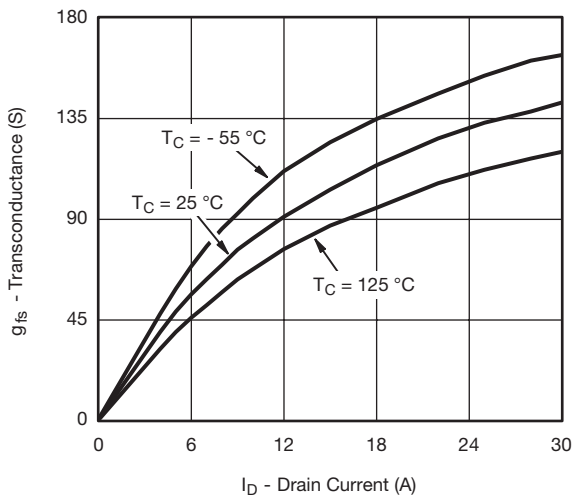
On-Resistance vs. Drain Current



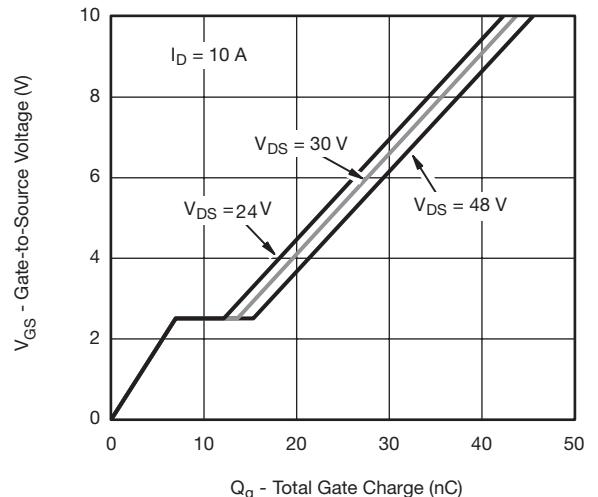
Transfer Characteristics



On-Resistance vs. Gate-to-Source Voltage

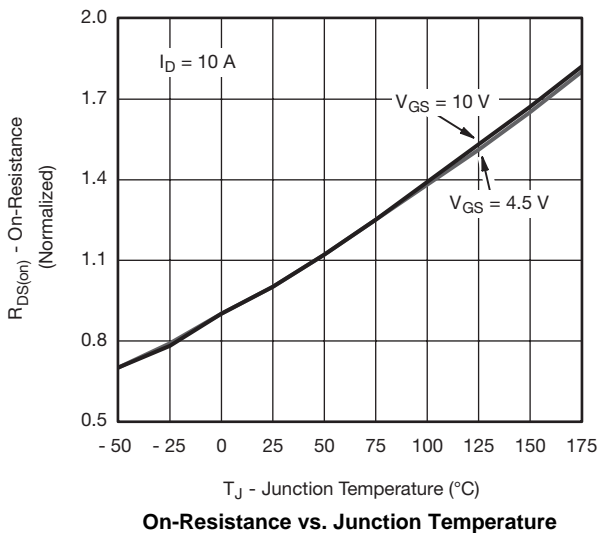
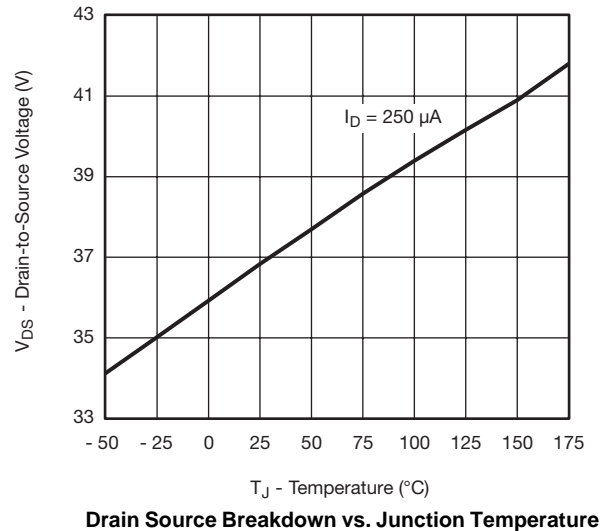
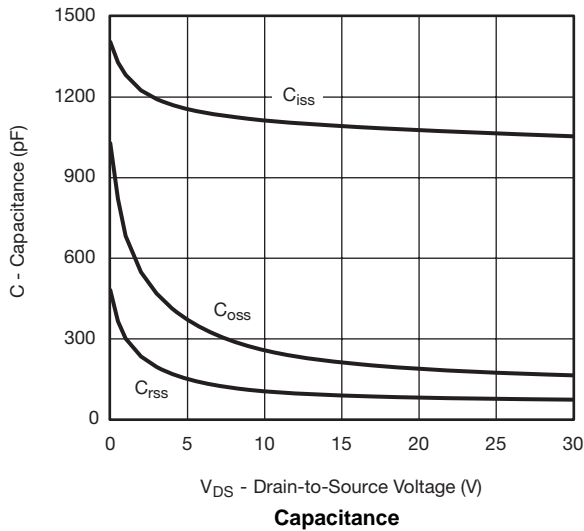
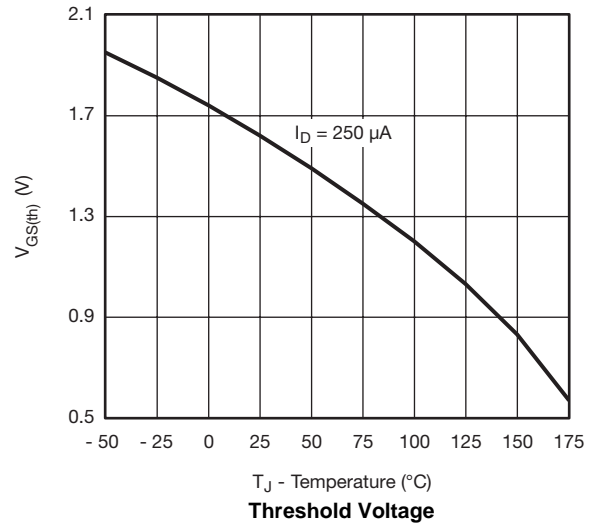
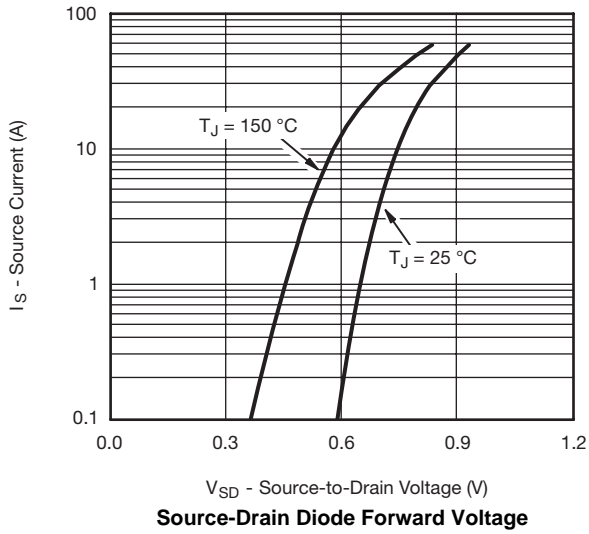


Transconductance

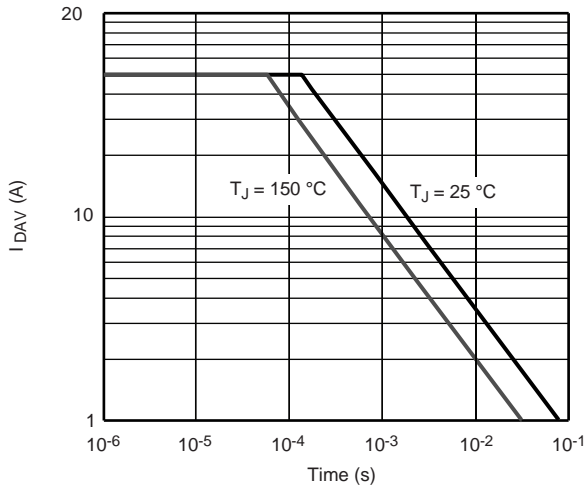


Gate Charge

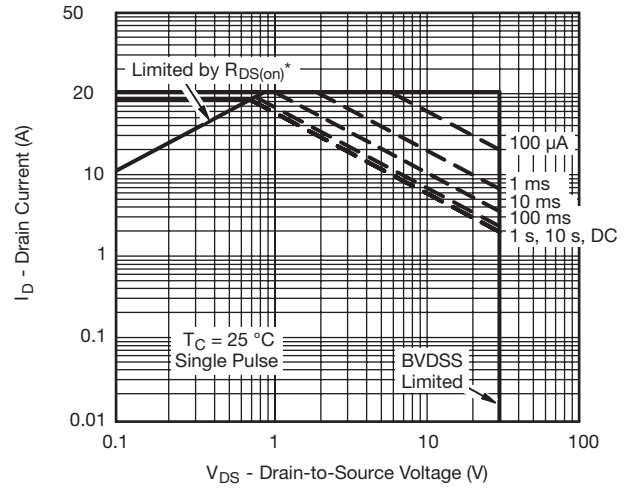
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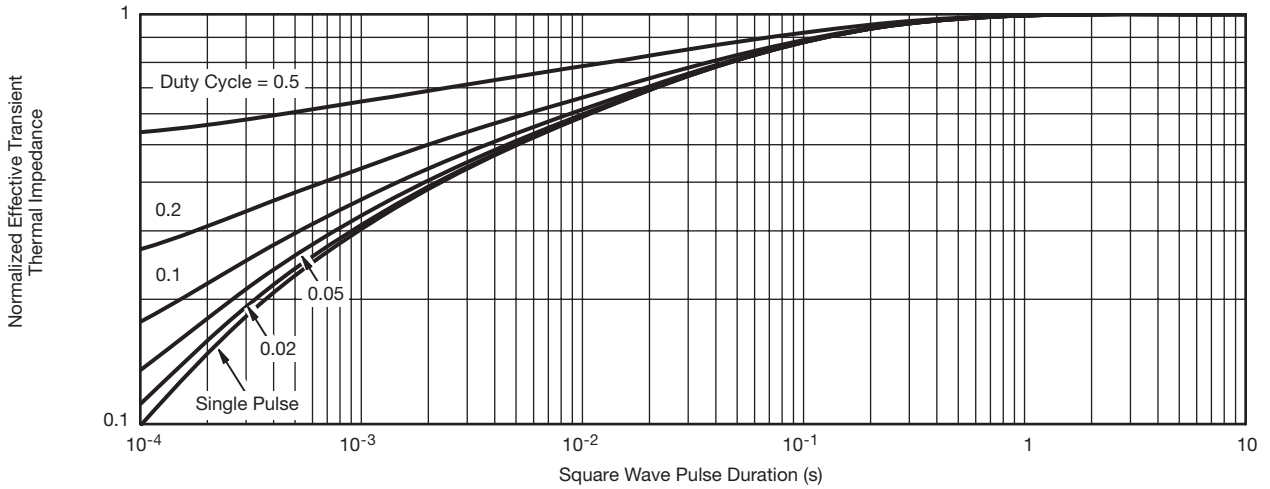
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Single Pulse Avalanche Current Capability vs. Time



Safe Operating Area
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



Normalized Thermal Transient Impedance, Junction-to-Case

TO-251AA (DPAK)



Note: Dimension L3 is for reference only.

Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	2.21	2.38	0.087	0.094
A1	0.89	1.14	0.035	0.045
b	0.71	0.89	0.028	0.035
b1	0.76	1.14	0.030	0.045
b2	5.23	5.43	0.206	0.214
c	0.46	0.58	0.018	0.023
c1	0.46	0.58	0.018	0.023
D	5.97	6.22	0.235	0.245
E	6.48	6.73	0.255	0.265
e	2.28 BSC		0.090 BSC	
L	8.89	9.53	0.350	0.375
L1	1.91	2.28	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.15	1.52	0.045	0.060
ECN: S-03946—Rev. E, 09-Jul-01 DWG: 5346				

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