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Product Brief
IGLOO2 FPGA

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Contents

1 Revision History . . . 1
1.1 Revision 15.0 . . . 1
1.2 Revision 14.0 . . . 1
1.3 Revision 13.0 . . . 1
1.4 Revision 12.0 . . . 1
1.5 Revision 11.0 . . . 1
1.6 Revision 10.0 . . . 1
1.7 Revision 9.0 . . . 1
1.8 Revision 8.0 . . . 1
1.9 Revision 7.0 . . . 2
1.10 Revision 6.0 . . . 2
1.11 Revision 5.0 . . . 2
1.12 Revision 4.0 . . . 2
1.13 Revision 3.0 . . . 2
1.14 Revision 2.0 . . . 2
1.15 Revision 1.0 . . . 2

2 IGLOO2 FPGAs Product Brief . . . 3
2.1 IGLOO2 Family . . . 3
2.1.1 High-Performance FPGA . . . 3
2.1.2 High-Speed Serial Interfaces . . . 3
2.1.3 High-Speed Memory Interfaces . . . 3
2.1.4 High-Performance Memory Subsystem . . . 3
2.1.5 Clocking Resources . . . 4
2.1.6 Operating Voltage and I/Os . . . 4
2.1.7 Security . . . 4
2.1.8 Reliability . . . 4
2.1.9 Low Power . . . 5
2.2 IGLOO2 FPGA Block Diagram . . . 5
2.3 I/Os Per Package . . . 7
2.4 Acronyms . . . 11
2.5 IGLOO2 Ordering Information . . . 11
2.5.1 IGLOO2 Commercial and Industrial Temperature Grade Devices . . . 12
2.5.2 IGLOO2 Military Temperature Grade Devices . . . 13
2.6 IGLOO2 Device Status . . . 13
2.7 IGLOO2 Datasheet and Pin Descriptions . . . 13
2.8 Marking Specification Details . . . 13
2.8.1 Description . . . 14

3 IGLOO2 Device Family Overview . . . 15
3.1 Reliability . . . 15
3.2 Highest Security Devices . . . 15
3.2.1 Design Security vs. Data Security . . . 15
3.2.2 Design Security . . . 15
3.2.3 Data Security . . . 16
3.3 Low Power . . . 17
3.4 High-Performance FPGA Fabric . . . 17
3.4.1 Dual-Port Large SRAM . . . 18

3.4.2 Three-Port Micro SRAM . . . 18
3.4.3 Mathblocks for DSP Applications . . . 18
3.5 High-Performance Memory Subsystem . . . 18
3.5.1 DDR Bridge . . . 18
3.5.2 AHB Bus Matrix . . . 19
3.5.3 Fabric Interface Controller . . . 19
3.5.4 Embedded SRAM . . . 19
3.5.5 Embedded NVM . . . 19
3.5.6 DMA Engines . . . 19
3.5.7 APB Configuration Bus . . . 19
3.5.8 Peripherals . . . 19
3.6 Clock Sources: On-Chip Oscillators, PLLs, and CCCs . . . 20
3.7 High-Speed Serial Interfaces . . . 20
3.7.1 SerDes Interface . . . 20
3.7.2 PCI Express . . . 20
3.7.3 XAUI/XGXS Extension . . . 20
3.8 High-Speed Memory Interfaces: DDRx Memory Controllers . . . 21
3.8.1 MDDR Subsystem . . . 21
3.8.2 FDDR Subsystem . . . 21
3.9 IGLOO2 Development Tools . . . 21
3.9.1 Design Software . . . 21
3.9.2 Design Hardware . . . 22
3.9.3 IP Cores . . . 22

Tables

Table 1 IGLOO2 FPGA Product Family 6
Table 2 Packaging Options 7
Table 3 I/Os per Package 7
Table 4 Features per Device/Package Combination 8
Table 5 Programming Interfaces 9
Table 6 Chip Resources Needed for Programming Modes 10
Table 7 IGLOO2 Devices without Data Security (All Speed Grades, C and I Temperature) 12
Table 8 IGLOO2 Data Security S Devices (All Speed Grades, C, and I Temperature) 12
Table 9 Design Security Features 16
Table 10 Data Security Features 17

Figures

Figure 1 IGLOO2 FPGA Block Diagram 5
Figure 2 IGLOO2 Evaluation Kit 22

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 15.0

Information about M2GL150 FCV484M was added. See IGLOO2 Military Temperature Grade Devices, page 13.

1.2 Revision 14.0

Name change from native SerDes interface to native EPCS SerDes interface in the High-Speed Serial Interfaces, page 20 in revision 14.0.

1.3 Revision 13.0

The following is a summary of changes made in revision 13.0:

- Updated Table 1, page 6 and Table 2, page 7 for grade 1 and 2 entries (SAR 80231).
- Updated the IGLOO2 Ordering Information, page 11 image for grade 1 and 2 entries (SAR 80231).
- Added the grade 1 and grade 2 references in IGLOO2 Datasheet and Pin Descriptions, page 13 (SAR 80231).
- Added grade 1 and 2 entries in Description, page 14 (SAR 80231).

1.4 Revision 12.0

The following is a summary of changes made in revision 12.0:

- Footnotes were inserted in Table 4, page 8 as required. (SAR 66079, SAR 77444, and SAR 73335)

1.5 Revision 11.0

The following is a summary of changes made in revision 11.0:

- Updated Table 1, page 6 (SAR 71995).
- Updated Marking Specification Details, page 13 (SAR 71995).
- Updated Low Power, page 5 (SAR 71995).

1.6 Revision 10.0

The following is a summary of changes made in revision 9.0:

- Updated Table 4, page 8 (SAR 69876).
- Added Table 6, page 10, Table 7, page 12, and Table 8, page 12 (SAR 69876).
- Updated Marking Specification Details, page 13 (SAR 69876).

1.7 Revision 9.0

The following is a summary of changes made in revision 9.0:

- Updated Table 1, page 6, Table 3, page 7, Table 4, page 8, Table 5, page 9, and Table 9, page 16.
- Removed all instances of and references to M2GL100. VQ144 is replaced with TQ144 (SAR 62858).
- Updated Table 9, page 16 and Table 10, page 17.
- Updated IGLOO2 Ordering Information, page 11.
- Added IGLOO2 Development Tools, page 21.

1.8 Revision 8.0

Updated Device Packages 005-VF256 and 150-FCS536 in Table 4, page 8–Table 5, page 9 in revision 8.0.

1.9 Revision 7.0

Table 2, page 7, Table 4, page 8, and Table 5, page 9 were updated in revision 7.0.

1.10 Revision 6.0

The following is a summary of changes made in revision 6.0:

- Table 1, page 6 to Table 5, page 9 and IGLOO2 Ordering Information, page 11 were update with Military device data.
- The Marking Specification Details, page 13 and the Programming Interfaces, page 9 were added.

1.11 Revision 5.0

The following is a summary of changes made in revision 5.0:

- Tables 3-6 were combined into Table 5, page 9.
- Fabric Interface Controller features were added to IGLOO2 FPGA Product Family, page 6.
- Packages VQ144 and FCV484 were added to Table 3, page 7 and Table 5, page 9.

1.12 Revision 4.0

The following is a summary of changes made in revision 4.0:

- The Data Security Features section, table and the Device Status table were removed.
- Figure 1, page 5 was updated.

1.13 Revision 3.0

The following is a summary of changes made in revision 3.0:

- Packages FCS325 and VF256 were added to I/Os Per Package, page 7.
- IGLOO2 Ordering Information, page 11 was updated.

1.14 Revision 2.0

The following was a summary of changes that were made in revision 2.0:

- LSRAM x32/36 widths added. Table 1, page 6 table note added referring to updates in Table 5, page 9 – Table 7, page 12.
- IGLOO2 Ordering Information, page 11 was updated. Part Numbers (tables 7 and 8) were removed. IGLOO2 Device Status, page 13 was updated.
- M2GL090-FG676 and M2GL005-VF400 package pinouts finalized.

1.15 Revision 1.0

Revision 1.0 was the initial release of this document.

2 IGLOO2 FPGAs Product Brief

Microsemi IGLOO®2 FPGAs integrate the fourth generation flash-based FPGA fabric and high-performance communication interfaces on a single chip. The IGLOO2 family is the industry's lowest power, most reliable, and highest security programmable logic solution. This next generation IGLOO2 architecture offers up to 3.6X gate count implemented with the 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and mathblocks for digital signal processing (DSP). High-speed serial interfaces include PCI express (PCIe), 10 Gbps attachment unit interface (XAUI) / XGMII extended sublayer (XGXS) plus native serialization/deserialization (SerDes) communication, while double data rate 2 (DDR2)/DDR3 memory controllers provide high-speed memory interfaces.

2.1 IGLOO2 Family

2.1.1 High-Performance FPGA

- Efficient 4-input LUTs with carry chains for high-performance and low power
- Up to 236 blocks of dual-port 18 Kbit SRAM (Large SRAM) with 400 MHz synchronous performance (512 × 36, 512 × 32, 1 Kbit × 18, 1 Kbit × 16, 2 Kbit × 9, 2 Kbit × 8, 4 Kbit × 4, 8 Kbit × 2, or 16 Kbit × 1)
- Up to 240 blocks of three-port 1 Kbit SRAM with 2 read ports and 1 write port (micro SRAM)
- High-performance DSP
  - Up to 240 fast mathblocks with 18 × 18 signed multiplication, 17 × 17 unsigned multiplication and 44-bit accumulator

2.1.2 High-Speed Serial Interfaces

- Up to 16 SerDes lanes, each supporting:
  - XGXS/XAUI extension (to implement a 10 Gbps (XGMII) Ethernet PHY interface)
  - Native EPCS SerDes interface facilitates implementation of serial rapidIO in fabric or an SGMII interface to a soft Ethernet MAC
  - PCI express (PCIe) endpoint controller
  - ×1, ×2, and ×4 lane PCI express core
  - Up to 2 Kbytes maximum payload size
  - 64-/32-bit AXI/AHB master and slave interfaces to the application layer

2.1.3 High-Speed Memory Interfaces

- Up to 2 high-speed DDRx memory controllers
  - HPMS DDR (MDDR) and fabric DDR (FDDR) controllers
  - Supports LPDDR/DDR2/DDR3
  - Maximum 333 MHz clock rate
  - SECDED enable/disable feature
  - Supports various DRAM bus width modes, ×8, ×9, ×16, ×18, ×32, and ×36
  - Supports command reordering to optimize memory efficiency
  - Supports data reordering, returning critical word first for each command
- SDRAM support through a soft SDRAM memory controller

2.1.4 High-Performance Memory Subsystem

- 64 KB embedded SRAM (eSRAM)
- Up to 512 KB embedded nonvolatile memory (eNVM)
- One SPI/COMM_BLK
- DDR bridge (2 port data R/W buffering bridge to DDR memory) with 64-bit AXI interface
- Non-blocking, multi-layer AHB bus matrix allowing multi-master scheme supporting 5 masters and 7 slaves
- Two AHB/APB interfaces to FPGA fabric (master/slave capable)

- Two DMA controllers to offload data transactions
  - 8-channel peripheral DMA (PDMA) for data transfer between HPMS peripherals and memory
- High-performance DMA (HPDMA) for data transfer between eSRAM and DDR memories

2.1.5 Clocking Resources

- Clock sources
  - High precision 32 kHz to 20 MHz main crystal oscillator
  - 1 MHz embedded RC oscillator
  - 50 MHz embedded RC oscillator
- Up to 8 clock conditioning circuits (CCCs) with up to 8 integrated analog PLLs
  - Output clock with 8 output phases and 45° phase difference (multiply/divide, and delay capabilities)
- Frequency: input 1 MHz to 200 MHz, output 20 MHz to 400 MHz

2.1.6 Operating Voltage and I/Os

- 1.2 V core voltage
- Multi-standard user I/Os (MSIO/MSIOD)
  - LVTTL/LVCMOS 3.3 V (MSIO only)
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, and 2.5 V
  - DDR (SSTL2_1and SSTL2_2)
  - LVDS, MLVDS, Mini-LVDS, and RSDS differential standards
  - PCI
  - LVPECL (receiver only)
- DDR I/Os (DDRIO)
  - DDR, DDR2, DDR3, LPDDR, SSTL2, SSTL18, and HSTL
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, and 2.5 V
- Market leading number of user I/Os with 5G SerDes

2.1.7 Security

- Design security features (available on all devices)
  - Intellectual property (IP) protection through unique security features and use models new to the PLD industry
  - Encrypted user key and bitstream loading, enabling programming in less-trusted locations
  - Supply-chain assurance device certificate
  - Enhanced anti-tamper features
  - Zeroization
- Data security features (available on premium devices)
  - Non-deterministic random bit generator (NRBG)
  - User cryptographic services (AES-256, SHA-256, elliptical curve cryptographic (ECC) engine)
  - User physically unclonable function (PUF) key enrollment and regeneration
  - CRI pass-through DPA patent portfolio license
  - Hardware firewalls protecting microcontroller subsystem (HPMS) memories

2.1.8 Reliability

- Single event upset (SEU) immune
  - Zero FIT FPGA configuration cells
- Junction Temperature
  - 125 °C—Military Temperature
  - 100 °C—Industrial Temperature
  - 85 °C—Commercial Temperature
- Single error correct double error detect (SECDED) protection on the following:
  - Embedded memories (eSRAMs)
  - PCIe buffer
  - DDR memory controllers with optional SECDED modes
- Buffers implemented with SEU resistant latches on the following:
  - DDR bridges (HPMS, MDDR, and FDDR)
  - SPI FIFO

- NVM integrity check at power-up and on-demand
- No external configuration memory required—instant-on, retains configuration when powered off

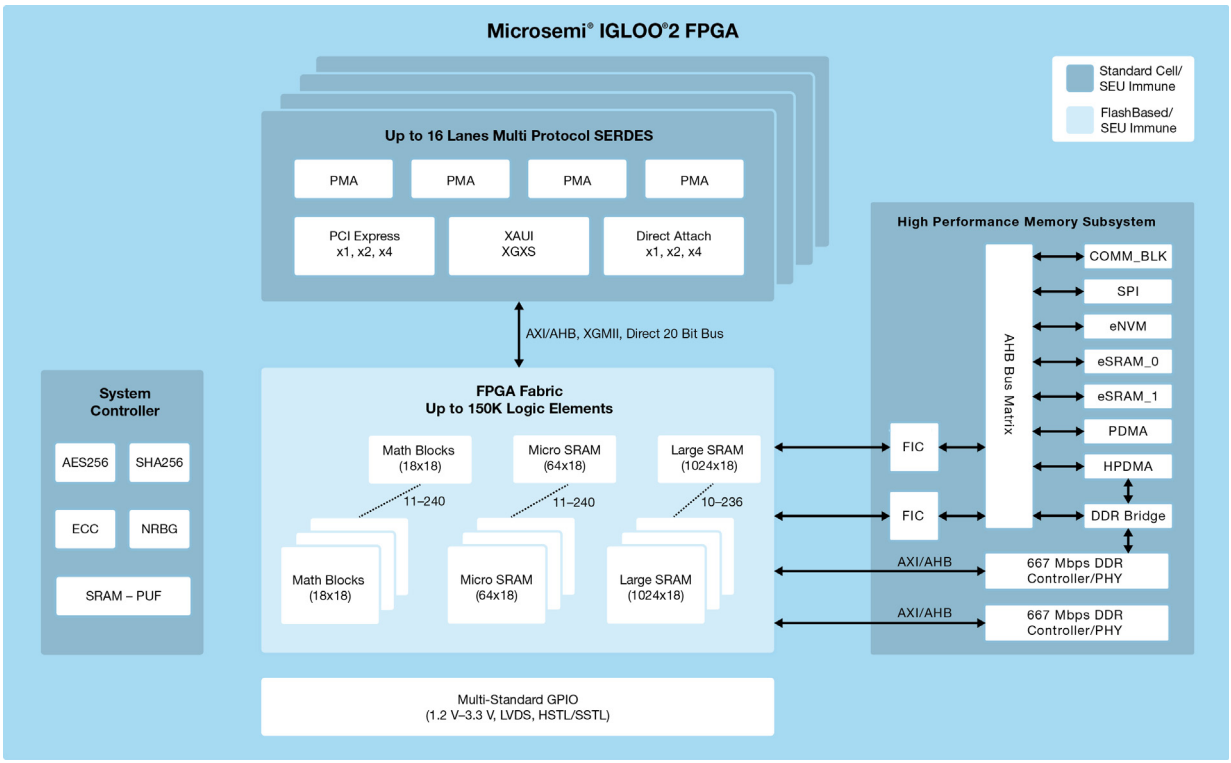
2.1.9 Low Power

- Low static and dynamic power
  - Flash*Freeze (F*F) mode for fabric
- Power as low as 13 mW/Gbps per lane for SerDes devices
- Up to 25% lower total power than competing devices

2.2 IGLOO2 FPGA Block Diagram

The following figure shows the various blocks available in IGLOO2 FPGA.

Figure 1 • **IGLOO2 FPGA Block Diagram**



The following table lists the features and device ranges of IGLOO2.

Table 1 • **IGLOO2 FPGA Product Family**

Peripherals	Features [1, 2]	M2GL005 (S)	M2GL010 (S/T/TS)	M2GL025 (T/TS)	M2GL050 (T/TS)	M2GL060 (T/TS)	M2GL090 (T/TS)	M2GL150 (T/TS)
Logic/DSP	Maximum Logic Elements (4LUT + DFF)[3]	6,060	12,084	27,696	56,340	56,520	86,184	146,124
	Math Blocks (18 × 18)	11	22	34	72	72	84	240
	PLLs and CCCs	2	2	6	6	6	6	8
	SPI/HPDMA/PDMA	1 each	1 each	1 each	1 each	1 each	1 each	1 each
	Fabric Interface Controllers	1	1	1	2	1	1	2
	Data Security	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, and RNG	AES256, SHA256, RNG, ECC, and PUF	AES256, SHA256, RNG, ECC, and PUF	AES256, SHA256, RNG, ECC, and PUF
Memory	eNVM (K Bytes)	128	256	256	256	256	512	512
	LSRAM 18K Blocks	10	21	31	69	69	109	236
	uSRAM1K Blocks	11	22	34	72	72	112	240
	eSRAM (K Bytes)	64	64	64	64	64	64	64
	Total RAM (K	703	912	1104	1826	1826	2586	5000
High Speed	DDR Controllers	1 × 18	1 × 18	1 × 18	2 × 36	1 × 18	1 × 18	2 × 36
	SerDes Lanes (T)	0	4	4	8	4	4	16
	PCIe End Points	0	1	1	2	2	2	4
User I/Os	MSIO (3.3 V)	119	123	157	139	271	309	292
	MSIOD (2.5 V)	28	40	40	62	40	40	106
	DDRIO (2.5 V)	66	70	70	176	76	76	176
	Total User I/O	209	233	267	377	387	425	574
Grades	Commercial (C), Industrial (I), Military (M), and Automotive (T1/T2)	C, I, T1, and T2	C, I, M, T1, and T2	C, I, M, T1, and T2	C, I, M, T1, and T2	C, I, M, T1, and T2	C, I, M, T1, and T2	C, I, and M

1. *Feature availability is package dependent.*
2. *Data security features are only available in S and TS devices.*
3. Total logic may vary based on utilization of DSP and memories in your design. See UG0445: IGLOO2 FPGA and SmartFusion2 SoC FPGA Fabric User Guide for more information about DSP and memories.

2.3 I/Os Per Package

The following tables list the packaging options and I/O details for IGLOO2 devices.

Table 2 • **Packaging Options**

Package Options[1]	Pitch (mm)	Length x Width (mm)
FCS(G)325[2]	0.5	11 × 11
VF(G)256[2, 3]	0.8	14 × 14
FCS(G)536[2]	0.5	16 × 16
VF(G)400[2, 3]	0.8	17 × 17
FCV(G)484[2, 3]	0.8	19 × 19
TQ(G)144[2, 4]	0.5	20 × 20
FG(G)484[2, 5]	1.0	23 × 23
FG(G)676[2, 3]	1.0	27 × 27
FG(G)896[2]	1.0	31 × 31
FC(G)1152[2]	1.0	35 × 35

1. *All the packages mentioned above are available with lead and lead free.*
2. *(G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*
3. *Automotive T2 grade devices are available in the VF(G)256, VF(G)400, FG(G)484, and FG(G)676 packages.*
4. *The TQ(G)144 package will be available in T2 grade by the end of February, 2017.*
5. Automotive T1 grade devices are available in the FG(G)484 package.

Table 3 • **I/Os per Package**

Devices		M2GL005 (S)	M2GL010 (T/TS)[1, 2]	M2GL025 (T/TS)[1]	M2GL050 (T/TS)[1]	M2GL060 (T/TS)[1]	M2GL090 (T/TS)[1, 3, 4]	M2GL150 (T/TS)[5]
FCS(G)325	I/Os			180	200	200	180	
	Lanes			2	2	2	4	
VF(G)256	I/Os	161	138	138				
	Lanes		2	2				
FCS(G)536	I/Os							293
	Lanes							4
VF(G)400	I/Os	171	195	207	207	207		
	Lanes		4	4	4	4		
FCV(G)484	I/Os							248
	Lanes							4
TQ(G)144	I/Os	84	84					
	Lanes							
FG(G)484	I/Os	209	233	267	267	267	267	
	Lanes		4	4	4	4	4	
FG(G)676	I/Os					387	425	
	Lanes					4	4	

Table 3 • **I/Os per Package *(continued)***

Devices		M2GL005 (S)	M2GL010 (T/TS)[1, 2]	M2GL025 (T/TS)[1]	M2GL050 (T/TS)[1]	M2GL060 (T/TS)[1]	M2GL090 (T/TS)[1, 3, 4]	M2GL150 (T/TS)[5]
FG(G)896	I/Os				377			
	Lanes				8			
FC(G)1152	I/Os							574
	Lanes							16

1. Mil Temp 010/025/050/060/090 devices are only available in the FG(G)484 package.
2. M2GL010 (S) device is only available in TQ(G)144 package. M2GL010 (T/TS) devices are not available in TQ(G)144 package.
3. 090 FCS(G)325 is 11x13.5 pkg dimension.
4. The M2GL090 (T/TS) device in the FCSG325 package is available with an ordering code of XZ48. The XZ48 ordering code pre-configures the device for Auto Update mode. Minimum Order quantities apply, contact your local Microsemi sales office for details.
5. Mil Temp 150 devices are only available in the FC(G)1152 package.

Note: Shaded cells indicate that the device packages have vertical migration capability.

The following table lists the features per device and its package combination.

Table 4 • **Features per Device/Package Combination**

Package	Devices	MDDR	FDDR	Crystal Oscillators	5G SerDes Lanes[1]	PCIe Endpoints	MSIO (3.3 V max) [2]	MSIOD (2.5 V max) [3]	DDRIO (2.5 V max)	Total User I/Os
TQ(G)144 [4]	M2GL005 (S)			1			52	9	23	84
	M2GL010 (S)			1			50	11	23	84
VF(G)256 [4]	M2GL005 (S)			1			119	12	30	161
	M2GL010 (T/TS)	×18[5]		1	2	1	66	8	64	138
	M2GL025 (T/TS)	×18[5]		1	2	1	66	8	64	138
FCS(G)325 [4]	M2GL025 (T/TS)	×18[5]		1	2	1	94	22	64	180
	M2GL050 (T/TS)	×18[6]		1	2	1	90	22	88	200
	M2GL060 (T/TS)	×18[5]		1	4	2	114	22	64	200
	M2GL090 (T/TS)	×18[5]		1	4	2	104	12	64	180
VF(G)400 [4]	M2GL005 (S)	×18[5]		1			79	28	64	171
	M2GL010 (T/TS)	×18[5]		1	4	1	99	32	64	195
	M2GL025 (T/TS)	×18[5]		1	4	1	111	32	64	207
	M2GL050 (T/TS)	×18[6]		1	4	1	87	32	88	207
	M2GL060 (T/TS)	×18[5]		1	4	2	111	32	64	207
FCV(G)484 [4]	M2GL150 (T/TS)	×18[5]	×18[5]	1	4	4[7]	91	34	123	248

Table 4 • **Features per Device/Package Combination *(continued)***

Package	Devices	MDDR	FDDR	Crystal Oscillators	5G SerDes Lanes[1]	PCIe Endpoints	MSIO (3.3 V max) [2]	MSIOD (2.5 V max) [3]	DDRIO (2.5 V max)	Total User I/Os
FG(G)484 [4]	M2GL005 (S)	×18[5]		1			115	28	66	209
	M2GL010 (T/TS)	×18[5]		1	4	1	123	40	70	233
	M2GL025 (T/TS)	×18[5]		1	4	1	157	40	70	267
	M2GL050 (T/TS)	×18[6]		1	4	1	105	40	122	267
	M2GL060 (T/TS)	×18[5]		1	4	2	157	40	70	267
	M2GL090 (T/TS)	×18[5]		1	4	2	157	40	70	267
FC(G)536 [4]	M2GL150 (T/TS)	×18[5]	×18[5]	1	4	4[7]	151	16	126	293
FG(G)676 [4]	M2GL060 (T/TS)	×18[5]		1	4	2	271	40	76	387
	M2GL090 (T/TS)	×18[5]		1	4	2	309	40	76	425
FG(G)896 [4, 8]	M2GL050 (T/TS)	×36[9]	×36[9]	1	8	2	139	62	176	377
FC(G)1152 [4]	M2GL150 (T/TS)	×36[10]	×36[10]	1	16	4	292	106	176	574

1. Maximum SerDes rate for military temperature devices is 3.125 Gbps
2. Number of differential MSIO is number of MSIOs/2 for even and number of MSIOs – 1/2 for odd.
3. Number of differential MSIOD is number of MSIODs/2 for even and number of MSIODs – 1/2 for odd.
4. All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant /Pb-free.
5. DDR supports ×18, ×16, ×9, and ×8 modes
6. DDR supports ×18 and ×16 modes
7. 4 PCIe Gen1/Gen2 endpoints ×1 lane configuration.
8. DDR3 is non-compliant. Call technical support for details.
9. DDR supports ×36, ×32, ×18, and ×16 modes.
10. DDR supports ×36, ×32, ×18, ×16, ×9, and ×8 modes.

Note: SerDes is not available in Automotive T1 grade.

The following table lists the programming interfaces that are available in IGLOO2 FPGA.

Table 5 • **Programming Interfaces**

Package	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
TQ(G)144 [1]	M2GL005 (S)	Yes	Yes	No	No
	M2GL010 (S)	Yes	Yes	No	No
VF(G)256 [1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	No
	M2GL025 (T/TS)	Yes	Yes	Yes	No
FCS(G)325 [1]	M2GL025 (T/TS)	Yes	Yes	No	No
	M2GL050 (T/TS)	Yes	Yes	No	No
	M2GL060 (T/TS)	Yes	Yes	No	No
	M2GL090 (T/TS)	Yes	Yes	No	No

Table 5 • **Programming Interfaces *(continued)***

Package	Devices	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
VF(G)400 [1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	Yes
	M2GL025 (T/TS)	Yes	Yes	Yes	Yes
	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
FCV(G)484 [1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)484 [1]	M2GL005 (S)	Yes	Yes	Yes	Yes
	M2GL010 (T/TS)	Yes	Yes	Yes	Yes
	M2GL025 (T/TS)	Yes	Yes	Yes	Yes
	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
	M2GL090 (T/TS)	Yes	Yes	Yes	Yes
FCS(G)536 [1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes
FG(G)676 [1]	M2GL060 (T/TS)	Yes	Yes	Yes	Yes
	M2GL090 (T/TS)	Yes	Yes	Yes	Yes
FG(G)896 [1]	M2GL050 (T/TS)	Yes	Yes	Yes	Yes
FC(G)1152 [1]	M2GL150 (T/TS)	Yes	Yes	Yes	Yes

1. All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

The following table lists the chip resources needed for programming modes.

Table 6 • **Chip Resources Needed for Programming Modes**

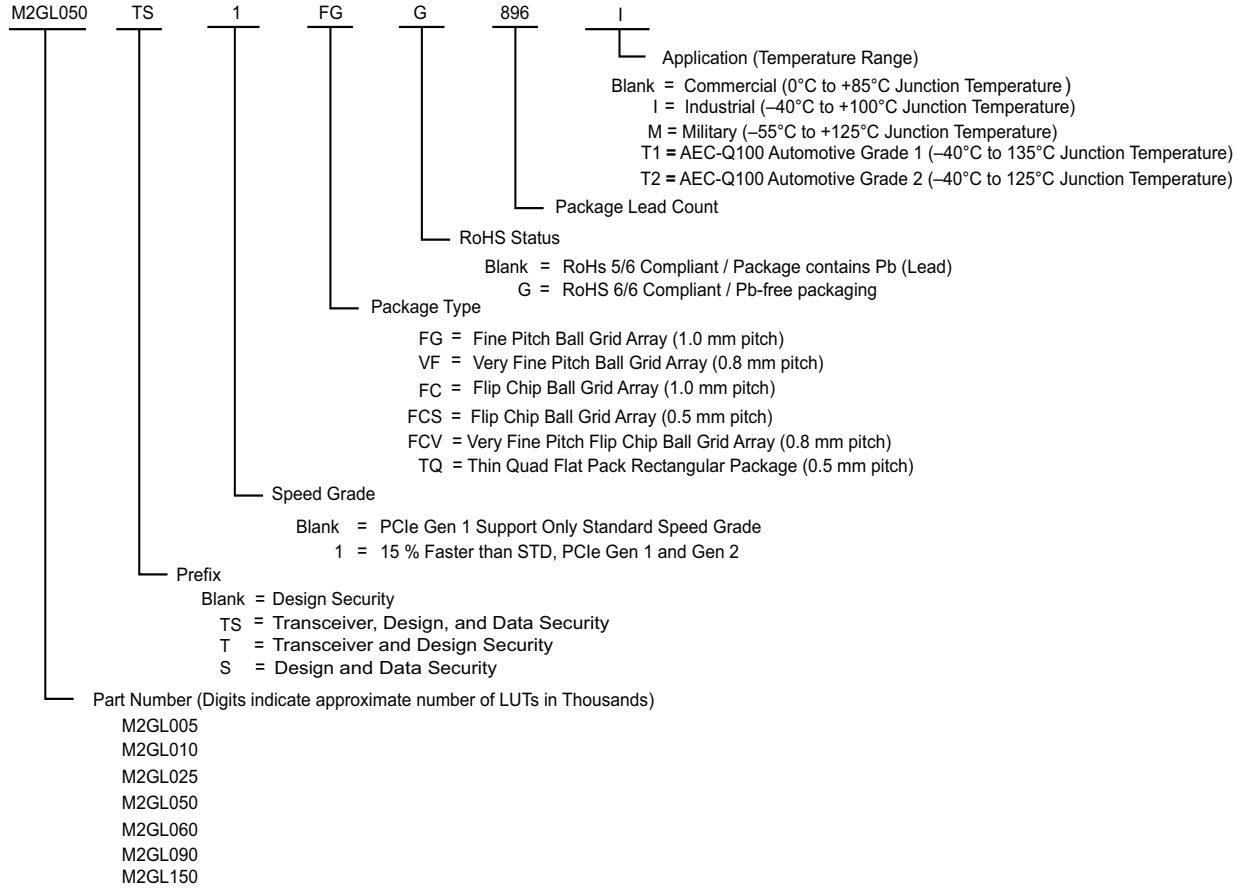
Programming Mode	JTAG	SPI_0	Flash_GOLDEN_N	System Controller SPI Port
External FlashPro4/5	Yes	No	No	No
External uP – JTAG slave	Yes	No	No	No
External uP – SPI Slave	No	No	No	Yes
Auto Programming	No	Yes	Yes	No
2-Step IAP	No	Yes	No	No
Programming Recovery	No	Yes	No	No

2.4 Acronyms

AES	advanced encryption standard
AHB	advanced high-performance bus
APB	advanced peripheral bus
AXI	advanced eXtensible interface
COMM_BLK	communication block
DDR	double data rate
DPA	differential power analysis
ECC	elliptical curve cryptography
EDAC	error detection and correction
FDDR	DDR2/3 controller in FPGA fabric
FIC	fabric interface controller
HPMS	high-performance memory subsystem
IAP	in-application programming
MACC	multiply accumulate
MDDR	DDR2/3 controller in HPMS
SECDED	single error correct double error detect
SEU	Single Event Upset
SHA	secure hashing algorithm
XAUI	10 Gbps attachment unit interface
XGMII	10 Gigabit media independent interface
XGXS	XGMII extended sublayer

2.5 IGLOO2 Ordering Information

The M2GL150 device is taken as an example and explains the various parts and their purposes.



Note: M2GL005 devices are not available with transceivers or in the military temperature grade.

Note: Automotive grade devices are available with S/TS.

2.5.1 IGLOO2 Commercial and Industrial Temperature Grade Devices

The following lists IGLOO2 commercial and industrial temperature grade devices.

Table 7 • **IGLOO2 Devices without Data Security (All Speed Grades, C and I Temperature)[1]**

M2GL	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
005										
010		T		T			T			
025	T	T		T			T			
050	T			T			T		T	
060	T			T			T	T		
090	T						T	T		
150			T		T					T

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

Note: *T indicates that the devices are available with Transceiver. Example ordering code: M2GL025T-FCSG325*

Note: *Shaded cells indicate that the devices are available without Transceiver. Example ordering code: M2GL025-FCSG325*

The following table lists IGLOO2 data security devices.

Table 8 • **IGLOO2 Data Security S Devices (All Speed Grades, C, and I Temperature)[1]**

M2GL	FCS(G)325	VF(G)256	FCS(G)536	VF(G)400	FCV(G)484	TQ(G)144	FG(G)484	FG(G)676	FG(G)896	FC(G)1152
005		S		S		S	S			
010		TS		TS		S	TS			
025	TS	TS		TS			TS			
050	TS			TS			TS		TS	
060	TS			TS			TS	TS		
090	TS						TS	TS		
150			TS		TS					TS

1. *All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.*

Note: *S indicates that the devices are available with Data Security. Example ordering code: M2GL005S-VFG400*

Note: *TS indicates that the devices are available with Transceiver and Data Security. Example ordering code: M2GL025TS-FCSG325*

2.5.2 IGLOO2 Military Temperature Grade Devices

Following are IGLOO2 military temperature devices:

- M2GL010 (T/TS)-1FG(G)484M
- M2GL025 (T/TS)-1FG(G)484M
- M2GL050 (T/TS)-1FG(G)484M
- M2GL060 (T/TS)-1FG(G)484M
- M2GL090 (T/TS)-1FG(G)484M
- M2GL150 (T/TS)-1FC(G)1152M
- M2GL150 (T/TS)-1FCV484M

Note: Gold Wire bonds are available for the FG484 package by appending X399 to the part number when ordering, for example: M2GL090 (T/TS)-1FG484MX399.

Note: All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

2.6 IGLOO2 Device Status

See *DS0128: IGLOO2 and SmartFusion2 Datasheet* for device status.

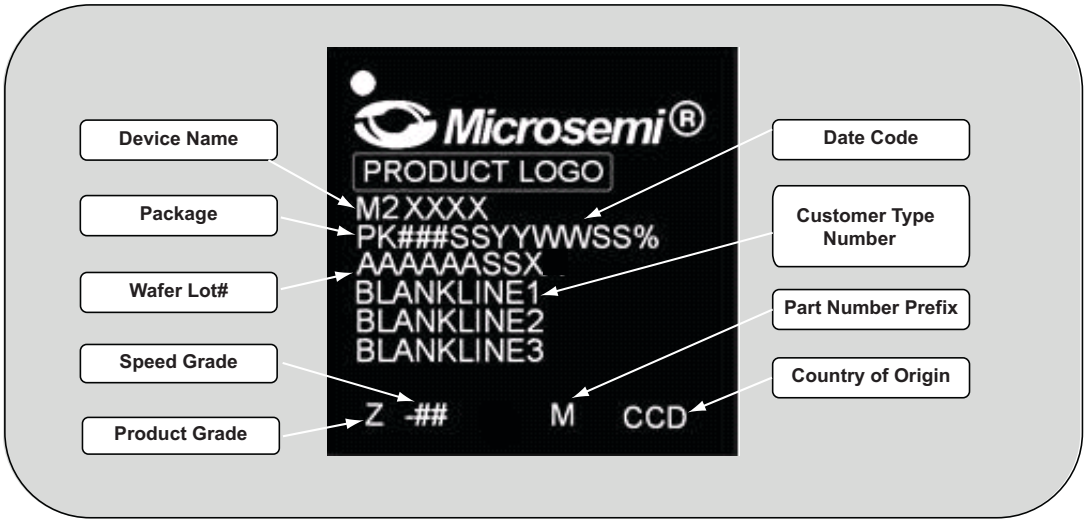
2.7 IGLOO2 Datasheet and Pin Descriptions

The datasheet and pin descriptions are published separately:

- *DS0128: IGLOO2 and SmartFusion2 Datasheet*
- *DS0124: IGLOO2 Pin Descriptions Datasheet*
- *DS0138: IGLOO2 Automotive Grade 1 Datasheet*
- *DS0134: SmartFusion2 and IGLOO2 Automotive Grade 2 Datasheet*
- *PB0135: Automotive Grade 2 IGLOO2 FPGAs Product Brief*

2.8 Marking Specification Details

Microsemi normally topside marks the full ordering part number on each device. The following figure provides the details for each character code present on Microsemi's IGLOO2 FPGA devices.



2.8.1 Description

- Device Name (M2XXXX): M2GL for IGLOO2 Devices
  - Example: M2GL050TS
- Package (PK###): Available Package as below
  - *PK: Package code*[1]*:*
  - FG(G): Fine Pitch BGA, 1.00 mm pitch
  - FC(G): Flip Chip Fine Pitch BGA with Metal LID on top, 1.00 mm pitch
  - FCV(G): Flip Chip Very Fine Pitch BGA with Metal LID on top, 0.8 mm pitch
  - FCS(G): Flip Chip Ultra Fine Pitch BGA with Metal LID on top, 0.5 mm pitch
  - VF(G): Very Fine Pitch BGA, 0.8 mm pitch
  - TQ(G): Ultra Fine Pitch Thin Quad Flat Pack Package, 0.5 mm pitch
  - ###: Number of Pins: Can be three or four digits. For example,144, 256, or 1152
- Wafer Lot (AAAAAASSX): Microsemi Wafer lot #
  - AAAAAA: Wafer lot number
  - SS: Two blank spaces
  - X: One digit die revision code
- Speed Grade (-##): Speed Binning Number
  - Blank: Standard speed grade
  - -1: -1 Speed grade
- Product grade (Z): Product Grade; assigned as follows
  - Blank/C: Commercial
  - ES: Engineering Samples
  - I: Industrial
  - M: Military Temperature
  - PP: Pre Production
  - T1: AEC-Q100 Automotive Grade 1
  - T2: AEC-Q100 Automotive Grade 2
- Date Code (YYWWSS%): Assembly Date Code
  - YY: Last two digits for seal year
  - WW: Work week the part was sealed
  - SS: Two blank spaces
  - %: Can be digital number or character for new product
- Customer Type Number: As specified on lot traveler
  - GW: Gold Wire bond
- Part number Prefix: Part number prefix, assigned as below
  - Blank: Design Security
  - T: Transceivers and Design Security
  - S: Design and Data Security
  - TS: Transceiver, Design, and Data Security
- Country of Origin (CCD): Assembly house country location
  - *Country name: Country Code*
  - China: CHN
  - Hong Kong: HKG
  - Japan: JPN
  - Korea, South: KOR
  - Philippines: PHL
  - Taiwan: TWN
  - Singapore: SGP
  - United States: USA
  - Malaysia: MYS

1. All the packages mentioned above are available with lead and lead free. (G) indicates that the package is RoHS 6/6 Compliant/Pb-free.

3 IGLOO2 Device Family Overview

Microsemi's IGLOO2 FPGAs integrate the fourth generation flash-based FPGA fabric and high-performance communication interfaces on a single chip. The IGLOO2 family is the industry's lowest power, highest reliability, and most secured programmable logic solution. This next generation IGLOO2 architecture offers up to 3.6X gate count, implemented with the 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and mathblocks for DSP. High-speed serial interfaces enable PCIe, XAUI / XGXS plus native SerDes communication while DDR2/DDR3 memory controllers provide high-speed memory interfaces.

3.1 Reliability

IGLOO2 flash-based fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. The flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, IGLOO2 devices add reliability to many other aspects of the device. Single error correct double error detect (SECDED) protection is implemented on the embedded SRAM (eSRAM), and is optional on the DDR memory controllers. This means that if a one-bit error is detected, it is corrected automatically. If more than one-bit errors are detected, they are not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are more resistant to SEUs. Therefore, no correction is needed in DDR bridges such as HPMS, MDDR, and FDDR, SPI, and PCIe FIFOs.

3.2 Highest Security Devices

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the IGLOO2 family incorporates essentially all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO®, and ProASIC®3 third-generation flash FPGAs and cSoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion2 and IGLOO2 FPGAs add many unique designs and data security features and use models new to the PLD industry.

3.2.1 Design Security vs. Data Security

When classifying security attributes of programmable logic devices (PLDs), a useful distinction is made between design security and data security.

3.2.2 Design Security

Design security helps protecting the intent of the owner of the design, such as keeping the design and associated bitstream keys confidential, preventing design changes (for example, insertion of Trojan Horses), and controlling the number of copies made throughout the device life cycle. Design security may also be known as IP protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security.

The following table lists the main design security features supported in IGLOO2.

Table 9 • **Design Security Features**

Features (all devices)	M2GL005, M2GL010, M2GL025, and M2GL050	M2GL060, M2GL090, and M2GL150
FlashLock® passcode security (256-bit)	•	•
Flexible security settings using flash lock-bits	•	•
Encrypted/authenticated design key loading	•	•
Symmetric key design security (256-bit)	•	•
Design key verification protocol	•	•
Encrypted/authenticated configuration loading	•	•
Certificate-of-Conformance (C-of-C)	•	•
Back-tracking prevention (also know as, Versioning)	•	•
Device certificate(s) (anti-counterfeiting)	•	•
Support for configuration variations	•	•
Fabric NVM and eNVM integrity tests	•	•
Information services (S/N, Cert., USERCODE, and others)	•	•
Tamper detection	•	•
Tamper response (includes Zeroization)	•	•
ECC public key design security (384-bit)		•
Hardware intrinsic design key (SRAM-PUF)		•

3.2.3 Data Security

Data security protects the information that IGLOO2 FPGA stores, processes, or communicates with the end application. If, for example, the configured design allows implementing the key management and encryption portion of a secure military radio, data security is entailed in encrypting and authenticating the radio traffic, and protecting the associated application-level cryptographic keys. Data security is closely related to the terms information assurance (IA) and information security. All IGLOO2 devices incorporate enhanced design security, making them the most secure programmable logic devices ever made. Select IGLOO2 models also include an advanced set of on-chip data security features that helps designing the most secure information assurance applications easier and better than ever before.

The following table lists the data security features of IGLOO2.

Table 10 • **Data Security Features**

Features (S devices)	M2GL005S, M2GL010S, M2GL010TS, M2GL025TS, and M2GL050TS	M2GL060TS, M2GL090TS, and M2GL150TS
CRI pass-through DPA patent license	●	●
Hardware firewalls protecting access to memories	●	●
Non-deterministic random bit generator service	●	●
AES-128/256 service (ECB, OFB, CTR, and CBC modes)	●	●
SHA-256 service	●	●
HMAC-SHA-256 service	●	●
Key tree service	●	●
PUF emulation (Pseudo-PUF)	●	
PUF emulation (SRAM-PUF)		●
ECC point-multiplication service		●
ECC point-addition service		●
User SRAM-PUF enrollment service		●
User SRAM-PUF activation code export service		●
SRAM-PUF intrinsic key gen. and enrollment service		●
SRAM-PUF key import and enrollment service		●
SRAM-PUF key regeneration service		●

3.3 Low Power

Microsemi's flash-based FPGA fabric results in extremely low-power design implementation with static power as low as 7.5 mW (for 6,060 LE device). Flash*Freeze (F*F) technology provides an ultra-low power static mode, also known as Flash*Freeze mode, for IGLOO2 devices, with power less than 11 mW for the largest device, which contains 146,124 LEs. Flash*Freeze mode entry retains all SRAMs and register information, and the exit from Flash*Freeze mode achieves rapid recovery to active mode.

3.4 High-Performance FPGA Fabric

Built on 65 nm process technology, the IGLOO2 FPGA fabric is composed of a logic module, a large SRAM (LSARM), a µSRAM, and a mathblock. The logic module is the basic logic element and has the following advanced features:

- A fully-permutable 4-input LUT optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT

The 4-input LUT can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with carry input to generate the sum output.

3.4.1 Dual-Port Large SRAM

Large SRAM(LSRAM) (RAM1K×18) is targeted for storing large memory for use with various operations. Each LSRAM block can store up to 18,432 bits. Each RAM1K×18 block contains Port A and Port B. The LSRAM is synchronous for both read and write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers, which have control signals that are independent of the SRAM's control signals.

3.4.2 Three-Port Micro SRAM

µSRAM (RAM64×18) is the second type of SRAM, which is embedded in the IGLOO2 FPGA fabric devices. The uSRAM block is approximately 1 KB (1,152 bits). uSRAM blocks are primarily targeted for building embedded FIFOs that can be used by any embedded fabric masters. RAM64×18 uSRAM is a 3-port SRAM; Port A and Port B are used for read operations and Port C is used for write operations. The two read ports are independent of each other and can perform read operations in both synchronous and asynchronous modes. The write port is always synchronous.

3.4.3 Mathblocks for DSP Applications

The fundamental building block in any digital signal processing algorithm is the multiply accumulate (MACC) function. The IGLOO2 device implements a custom 18 × 18 MACC block for efficient implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities:

- Supports 18 × 18 signed multiplications natively (A[17:0] × B[17:0])
- Supports dot product; the multiplier computes:
  - (A[8:0] × B[17:9] + A[17:9] × B[8:0]) × 2^9
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms typically need small amounts of RAM for coefficients and larger RAMs for data storage. IGLOO2 micro RAMs are ideally suited to serve the needs of coefficient storage while the large RAMs are used for data storage.

3.5 High-Performance Memory Subsystem

The high-performance memory subsystem (HPMS) embeds two separate 32 Kbyte SRAM blocks that have optional SECDED capabilities (32 Kbytes with SECDED enabled, 40 Kbytes with SECDED disabled), up to two separate 256 Kbyte eNVM (flash) blocks, and two separate DMA controllers for fast DMA user logic offloading. The HPMS provides multiple interfacing options to the FPGA fabric to facilitate tight integration between the HPMS and user logic in the fabric.

3.5.1 DDR Bridge

The DDR bridge is a data bridge between two AHB bus masters and a single AXI bus slave. The DDR bridge accumulates AHB writes into write combining buffers prior to bursting out to the external DDR memory. The DDR bridge also includes read combining buffers, allowing AHB masters to efficiently read data from the external DDR memory from a local buffer. The DDR bridge optimizes reads and writes from multiple masters to a single external DDR memory. Data coherency rules between the masters and the external DDR memory are implemented in hardware. The DDR bridge contains two write combining buffers and two read buffers. All buffers within the DDR bridge are implemented with single event upsets (SEU) tolerant latches and are not subject to SEUs that SRAM exhibits. IGLOO2 devices implement three DDR bridges in the HPMS, FDDR, and MDDR subsystems.

3.5.2 AHB Bus Matrix

The AHB bus matrix (ABM) is a non-blocking AHB-Lite multi-layer switch, supporting four master interfaces and eight slave interfaces. The switch decodes access is attempted by masters to various slaves, according to the memory map and security configurations. When multiple masters attempt to access a particular slave simultaneously, an arbiter associated with that slave decides which master gains access, according to a configurable set of arbitration rules. These rules can be configured by the user to provide different usage patterns to each slave. For example, a number of consecutive access opportunities to the slave can be allocated to one particular master, to increase the likelihood of the same type of accesses (all reads or all writes), which makes more efficient usage of the bandwidth to the slave.

3.5.3 Fabric Interface Controller

The fabric interface controller (FIC) block provides the HPMS master (MM) and fabric master (FM) interfaces between the HPMS and the FPGA fabric. Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks present in the HPMS (FIC_0 and FIC_1).

3.5.4 Embedded SRAM

The HPMS contains two blocks of 32 KB embedded SRAM (eSRAM), giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the parallelism that exists in the HPMS.

The eSRAM is designed for single error correct double error detect (SECDED) protection. When SECDED is disabled, the SRAM used to store SECDED data may be reused as an extra 16 KB of eSRAM.

3.5.5 Embedded NVM

The HPMS contains up to 512 KB of embedded NVM (eNVM), which is 64 bits wide.

3.5.6 DMA Engines

High-performance DMA and peripheral DMA engines are present in the HPMS.

3.5.6.1 High-Performance DMA

The high-performance DMA (HPDMA) engine provides efficient memory to memory data transfers between an external DDR memory and internal eSRAM. This engine has two separate AHB-Lite interfaces—one to the MDDR bridge and the other to the AHB bus matrix. All transfers by the HPDMA are full word transfers.

3.5.6.2 Peripheral DMA

The peripheral DMA (PDMA) engine is tuned for offloading byte-intensive operations, involving HPMS peripherals, to and from the internal eSRAMs. Data transfers can also be targeted to user logic/RAM in the FPGA fabric.

3.5.7 APB Configuration Bus

On every IGLOO2 device memory, an APB configuration bus is present to allow the user to initialize the SerDes ASIC blocks, the fabric DDR memory controller, and user instantiated peripherals in the FPGA fabric.

3.5.8 Peripherals

A large number of communications and general purpose peripherals are implemented in the HPMS.

3.5.8.1 Communication Block

The communication block (COMM_BLK) provides an UART-like communications channel between the HPMS and the system controller. System services are initiated through the COMM_BLK. System services such as *Enter Flash*Freeze Mode* are initiated through the COMM_BLK.

3.5.8.2 Serial Peripheral Interface

The serial peripheral interface (SPI) controller is compliant with the Motorola SPI, Texas Instruments synchronous serial, and National Semiconductor MICROWIRE™ formats. In addition, the SPI supports interfacing to large SPI flash and EEPROM devices by way of the slave protocol engine. The SPI controller supports both master and slave modes of operations.

The SPI controller embeds two 4 × 32 (depth × width) FIFOs for receive (RX) and transmit (TX). These FIFOs are accessible through RX data and TX data registers. Writing to the TX data register causes the data to be written to the transmit FIFO. This is emptied by the transmit logic. Similarly, reading from the RX data register causes data to be read from the receive FIFO.

3.6 Clock Sources: On-Chip Oscillators, PLLs, and CCCs

IGLOO2 devices have two on-chip RC oscillators—a 1 MHz RC oscillator and a 50 MHz RC oscillator—and the main crystal oscillator (32 KHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. These oscillators can be used in conjunction with the integrated user phase-locked loops (PLLs) and FAB_CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, power-on reset circuitry, and HPMS during the Flash*Freeze mode.

IGLOO2 devices have up to eight fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the eight PLLs and CCCs to generate the fabric clocks and the internal HPMS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the HPMS (HPMS_CCC) and an associated PLL (MPLL) for HPMS clocking and de-skewing the CLK_BASE clock. The fabric alignment clock controller (FACC), part of the HPMS CCC, is responsible for generating various aligned clocks required by the HPMS for correct operation of the HPMS blocks and synchronous communication with the user logic in the FPGA fabric.

3.7 High-Speed Serial Interfaces

3.7.1 SerDes Interface

IGLOO2 FPGA has up to four 5 Gbps SerDes transceivers, each supporting the following:

- Four SerDes/PCS lanes
- The native EPCS SerDes interface facilitates implementation of serial rapidIO (SRIO) in fabric or a SGMII interface for a soft Ethernet MAC. In EPCS modes, the maximum SerDes rate is 3.2 Gbps.

3.7.2 PCI Express

PCI express (PCIe) is a high speed, packet-based, point-to-point, low pin count, and serial interconnect bus. The IGLOO2 family has two hard high-speed serial interface blocks. Each SerDes block contains a PCIe system block. The PCIe system is connected to the SerDes block and following are the main features supported:

- Supports ×1, ×2, and ×4 lane configuration
- Endpoint configuration only
- PCI express base specification revision 2.0
- 2.5 and 5.0 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 Kbytes maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL master and slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 x 64 bit base address registers
- 1 virtual channel (VC)

3.7.3 XAUI/XGXS Extension

The XAUI/XGXS extension allows the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the XGMII fabric interface through an appropriate soft IP block in the fabric.

3.8 High-Speed Memory Interfaces: DDRx Memory Controllers

There are up to two DDR subsystems, MDDR (HPMS DDR), and FDDR (fabric DDR) present in IGLOO2 devices. Each subsystem consists of a DDR controller, PHY, and a wrapper. The MDDR has an interface to/from the HPMS and fabric, and FDDR provides an interface to/from the fabric.

The following are the main features supported by the FDDR and MDDR:

- Support for LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance
- Support 1, 2, or 4 ranks of memory
- Support different DRAM bus width modes: ×8, ×9, ×16, ×18, ×32, and ×36
- Support DRAM burst length of 2, 4, or 8 in full bus-width mode; supports DRAM burst length of 2, 4, 8, or 16 in half bus-width mode
- Support memory densities up to 4 GB
- Support a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and write buffers in fully associative CAMs, configurable in powers of 2, up to 64 reads plus 64 writes
- Support for dynamically changing clock frequency while in self-refresh
- Support command reordering to optimize memory efficiency
- Support data reordering, returning critical word first for each command

3.8.1 MDDR Subsystem

The MDDR subsystem has two interfaces to the DDR. One is an AXI 64-bit bus from the DDR bridge within the HPMS. The other is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the MDDR subsystem after reset. This APB configuration bus is mastered by a master in the FPGA fabric. Support for 3.3 V single data rate DRAMs (SDRAM) can be obtained by instantiating a soft AHB or AXI SDRAM memory controller in the FPGA fabric and connecting I/O ports to 3.3 V MSIO.

3.8.2 FDDR Subsystem

The FDDR subsystem has one interface to the DDR. This is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus can be mastered by a master in the FPGA fabric.

3.9 IGLOO2 Development Tools

3.9.1 Design Software

Microsemi's Libero® SoC is a comprehensive software toolset to design applications using the IGLOO2 device. Libero SoC manages the entire design flow from design entry, synthesis and simulation, place and route, timing, and power analysis, with the enhanced integration of the embedded design flow.

System designers can leverage the easy-to-use Libero SoC that includes the following features:

- System Builder for creation of system level architecture
- Synthesis, DSP, and debug support from Synopsys
- Simulation from Mentor Graphics
- Push-button design flow with power analysis and timing analysis
- SmartDebug for access to non-invasive probes within the IGLOO2 devices

See *Libero SoC* for more information.

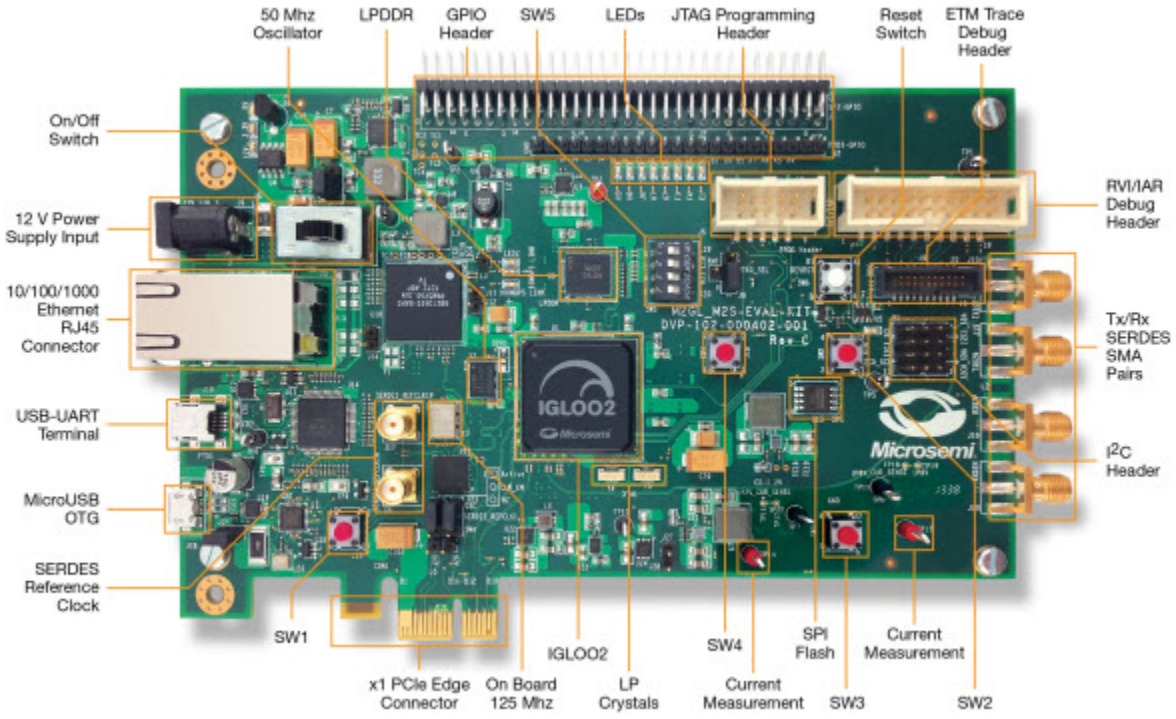
3.9.2 Design Hardware

Microsemi's IGLOO2 evaluation kit (M2GL-EVAL-KIT) is a low-cost platform to evaluate various features offered by IGLOO2 devices.

The kit includes a M2GL010T-1FGG484 device. The board includes an RJ45 interface to 10/100/1000 Ethernet, 512 Mb of LPDDR, 64 Mb SPI Flash, USB-UART connections as well as I^2C, SPI, and GPIO headers. The kit includes a 12 V power supply but can also be powered via the PCIe edge connector. The kit also includes a FlashPro4 JTAG programmer for programming and debugging.

The following figure shows the board image of the IGLOO2 evaluation kit.

Figure 2 • **IGLOO2 Evaluation Kit**



3.9.3 IP Cores

Microsemi offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core429, Core1553, CoreJESD204BRX/TX, CoreFRI, CoreFFT, and many other DirectCores. See *IP Cores* for more information.