Leadtrend

Preliminary Datasheet

LD7841K

10/20/2021

Single-Stage, High Power Factor, Constant Voltage Output Controller

Primary-Side Regulation with Integrated High Voltage Startup

REV: P00

The values contained in this preliminary datasheet are for reference only and not for approval. Users should verify for a current and complete document before placing orders

General Description

The LD7841K is a voltage mode controller for constant voltage output to LED drivers. Designed to support flyback or buck-boost topologies, its proprietary voltage mode control algorithm provides near−unity power factor and tightly regulates a constant output voltage from the primary side, thus eliminating the need for a secondary side feedback circuitry or an opticalcoupler.

The device is highly integrated with a minimum number of external components. A robust suite of safety protection is built in to simplify the design. This device is specifically intended for very compact space efficient designs and also provides a constant voltage regulation of the output if no load is connected to the LED drivers.

Feature

- Wide universal input range ($85V_{AC}$ ~ 305 V_{AC})
- Fast Startup time: ≦ 0.5 sec
- Low standby power
  - No load power saving : < 0.3W
  - Standby power consumption: < 0.5W
- Precise voltage regulation in the steady state : < ± 3 %
- Voltage regulation in the load transient: < ± 15%
- Total harmonic distortion current (THDi) optimization: <10%
- High Power Factor : PF > 0.9
- Robust Protection Features
  - Brown−In/Out Detection on HV pin
  - Cycle−by−cycle Peak Current Limit on CS pin
  - Over Load Protection on COMP pin
  - Secondary Diode short Protection on CS pin
  - Pin Short/Open Circuit Protection on CS and FB pin
  - Output Short Circuit Protection on FB pin
  - External OTP on CS pin
  - Internal Over Temperature Protection
- 250 mA / -700 mA Totem Pole Driving capability

Applications

- LED Driver Power Supplies
- Offline Appliances Requiring Power Factor Correction

Typical Application

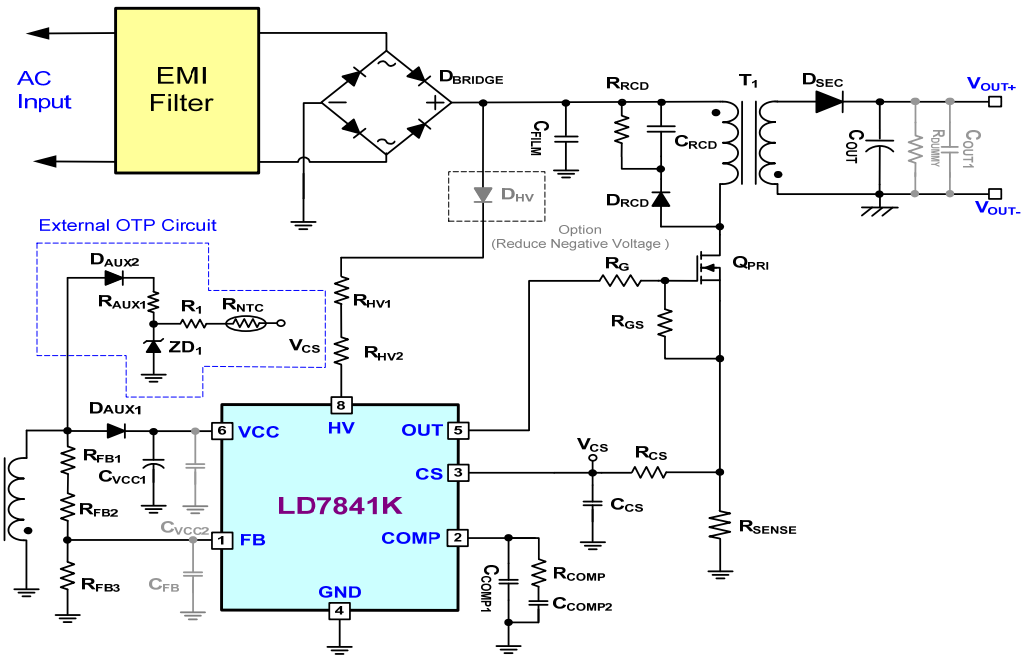


Fig. 1 Reference Circuit Design with CS_OTP Function

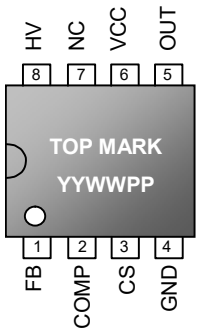
Note :

1) Due to the system design, it might cause the negative voltage on HV pin and over the maximum rating. Suggest to increase the related capacitance value of C_{FLIM} or add a diode as D_{HV} (Trr ≦ 50ns, max), the negative voltage over the maximum rating could be improved.

2) Once the OTP function is used, it is recommended to use the external OTP Circuit as Figure 1 to avoid the false trigger due to the slew rate of V_{FB} falling time.

Pin Configuration

SOP-8 (TOP VIEW)



YY: Year code
WW: Week code
PP: Production code

Ordering Information

Part number	Package		Top Mark	Shipping
LD7841KGS	SOP-8	Green package	LD7841KGS	2500 /tape & reel

The LD7841K GS is RoHS compliant/ green packaged.

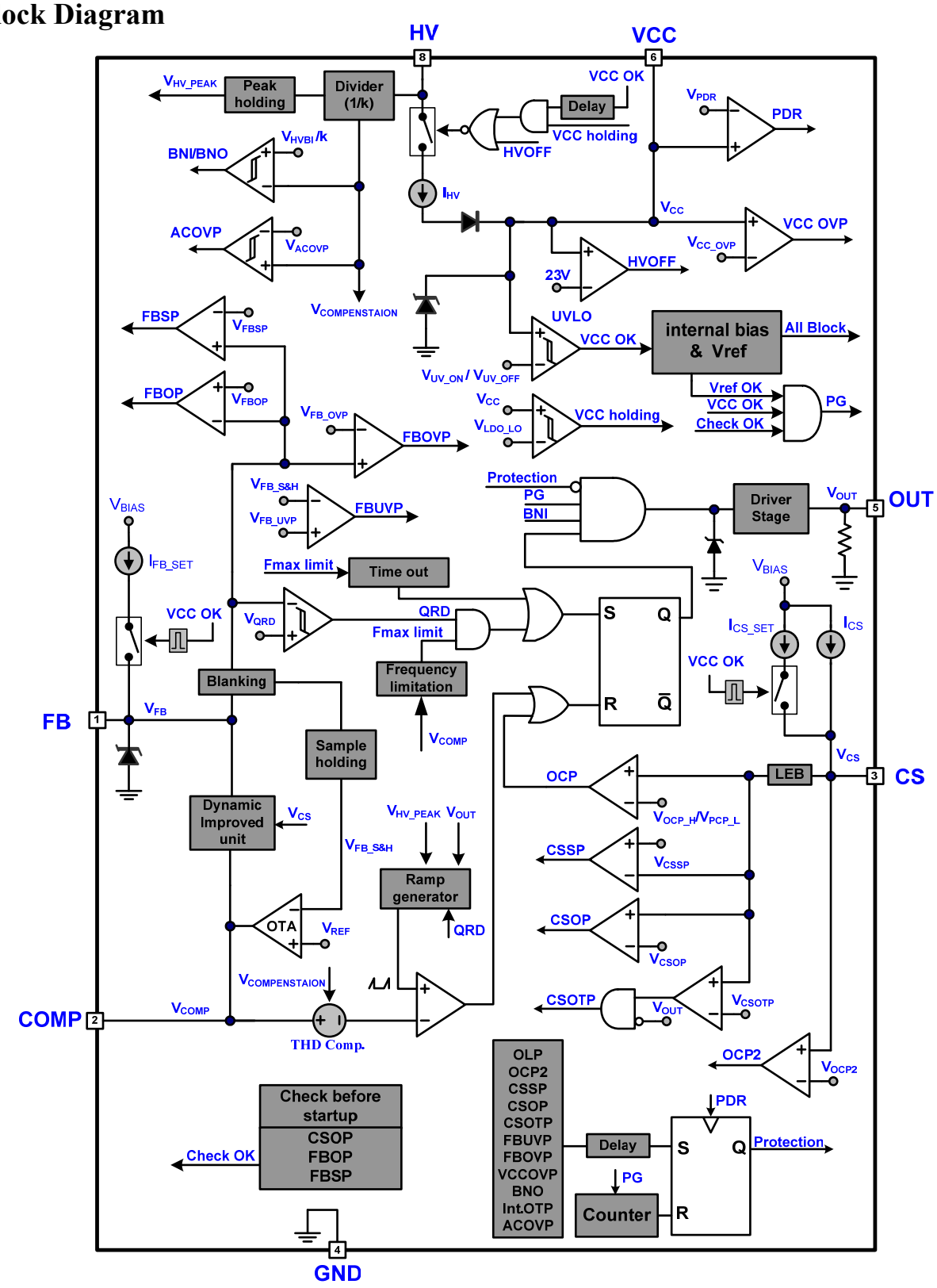
Protection Mode

ITEM	BNO	VCCOVP	FBOVP	SDSP	CSSP	CSOP	FBUVP (OSCP)	OLP	CSOTP	Int. OTP
LD7841K	Auto (1 hiccup)	Auto (1 hiccup)	Auto (1 hiccup)	Auto (8 hiccups)	Auto (1 hiccup)	Auto (1 hiccup)	Auto (4 hiccups)	Auto (4 hiccups)	Auto (1 hiccup)	Auto (1 hiccup)

Pin Descriptions

Pin No	NAME	FUNCTION
1	FB	This pin senses the auxiliary winding voltage for accurate output voltage control and detects the core reset event.
2	COMP	This pin receives a compensation network to stabilize the CV loop.
3	CS	This pin monitors the primary peak current for cycle by cycle limitation. It also provides the over temperature protection function by external NTC resistor during OUT is low.
4	GND	The controller ground.
5	OUT	Gate drive output to drive the external MOSFET.
6	VCC	IC's operating current and MOSFET driving current are supplied by this pin. This pin is connected to an external auxiliary voltage.
7	NC	No connection with chip internal.
8	HV	This pin connects to the bridge diode for providing the startup current and internal high voltage sensing function.

Block Diagram



Absolute Maximum Ratings

High voltage pin, HV	-0.3V ~ 700V
Supply Voltage VCC	-0.3V ~ 30V
OUT	-0.3V ~ VCC+0.3V
COMP, CS, FB	-0.3V ~ 6V
Source /Sink current on FB	3mA / -1.5mA
Storage Temperature Range	-65°C to 150°C
Package Thermal Resistance (SOP-8, θ_{JA})	160°C/W
Power Dissipation (SOP-8 at Ambient Temperature = 85 °C)	250mW
Lead temperature (Soldering, 10sec)	260°C
ESD Voltage Protection, Human Body Model (HV pin)	1.5 kV
ESD Voltage Protection, Human Body Model (except HV pin)	2.5 kV
ESD Voltage Protection, Machine Model	250 V
Gate Driving Current	250 mA / -700 mA

Caution:

Stresses beyond the ratings specified in “absolute maximum ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Item	Min.	Max.	Unit
Operating Junction Temperature	-40	125	°C
Supply Voltage of VCC	12	23	V
HV Pin Resistance (R_{HV1}+R_{HV2})	3.3	15	kΩ
HV Pin Bypass Capacitance	-	330	pF
VCC pin Capacitance (C_{VCC1})	22	47	μF
COMP pin Capacitance (C_{COMP1})	47	220	nF
COMP pin Capacitance (C_{COMP2})	0.47	1.0	μF
COMP pin Resistance (R_{COMP})	1	100	kΩ
CS pin Filter Capacitance (C_{CS})	-	220	pF
CS pin Filter Resistance (R_{CS})	0.1	1	kΩ
FB pin Source Current	-	1.5	mA
FB pin Sink Current	-	2.5	mA

Note :

1) Exceeding these ratings may damage the device.
2) This product guarantees robust performance from -20°C to 105°C ambit temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
3) When operation at harsh environment condition, as temperature and humidity or climate change …etc . Please pay attention to impedance variation between pin to pin or ground to avoid ripple remover closing loop and being failure.

Electrical Characteristics

V_{CC}=15V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
High voltage Supply (HV Pin)						
High voltage current source	V_{HV} ≥ 100V_{DC}, V_{VCC}= 0V	I_{HV1}		1.3	2.0	mA
	V_{HV}≥100V_{DC}, V_{VCC} =12V	I_{HV2}	3.0	3.6		mA
Off state leakage current	*;V_{VCC} > V_{UV_ON}, V_{HV} = 500 V_{DC}	I_{HV_OFF}			30	μA
Brown-in threshold voltage	V_{VCC} > V_{UV_ON}, V_{FB} = 0V	V_{HVBI}	95	100	105	V_{DC}
Brown-out threshold voltage		V_{HVBO}		85		V_{DC}
Brown-in de-bounce time	*;	T_{BNI}		15		ms
Brown-out de-bounce time	*; Enable this function after JFET is off	T_{BNO}		15		ms
High line threshold voltage	V_{HV_PEAK} is rising.	V_{HLINE}		230		V_{DC}
Low line threshold voltage	V_{HV_PEAK} is falling	V_{LLINE}		205		V_{DC}
ACOVP threshold voltage		V_{ACOVP}		445		V_{DC}
ACOVP de-bounce time	*;	T_{D_ACOVP}		150		μs
Supply Voltage (VCC Pin)						
Startup current	V_{VCC} < V_{UV_ON}	I_{ST}		75	100	μA
Operating current	3.45V ≦ V_{FB} ≦ 3.6V @ F_{MIN} , C_{OUT} ≦ 1nF, C_{COMP}=1μF	I_{OP_LO}		2.0		mA
	VCCOVP, OLP, CSSP, SDSP, CSOTP… etc.	I_{OP_PRO}		0.35		mA
UVLO (OFF)		V_{UV_OFF}	7.0	8.0	9.0	V
UVLO (ON)		V_{UV_ON}	16.0	17.5	19.0	V
Clamping threshold voltage		V_{CCH_CLAMP}	23	24.5	26	V
Clamping sink current	*;	I_{VCC_SINK}		3		mA
OVP threshold voltage	VCCOVP is triggered and 150us continuously.	V_{CC_OVP}	26	27.5	29	V
Self-biased current source threshold voltage	Keep holding current from HV to VCC	V_{LDO_LO}	8.5		11.5	V
Voltage Feedback (COMP Pin)						
Short circuit current	*; Source current when V_{COMP}=0.5V.	I_{COMP}		0.5		mA
Open loop voltage		V_{CMP_OPEN}	4.5	4.7	4.9	V
Over load protection threshold voltage		V_{OLP}	V_{CMP_OPEN} - 0.3			V
Over load protection de-bounce time	*; V_{COMP} ≧ V_{LOP} .	T_{DEB_OLP}		210		ms

V_{CC}=15.0V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Voltage Feedback (COMP Pin)						
Frequency limit reducing start threshold voltage	*; F_S=F_{S_MAX}	V_{CMP_FLH}		2.9		V
Frequency limit reducing end threshold voltage	F_S=F_{S_MIN}	V_{COMP_FLL}		0.35		V
Clamping low threshold voltage		V_{CMP_LOW}	0.30	0.35	0.40	V
Maximum turn on time setting	22kΩ ≧ R_{FB} ≧ 18kΩ, V_{HV}=100V_{DC}	T_{MAX_1}	21	27	33	μs
	10 kΩ ≧ R_{FB} ≧ 6kΩ, V_{HV}=100V_{DC}	T_{MAX_2}	13	17	21	μs
Minimum turn on time	V_{HV}=100V_{DC}, V_{COMP}=$V_{CMP\_TON\_MIN}$, Maximum on time setting=T_{MAX_1}	T_{MIN_L}	1.8	2.1	2.4	μs
Minimum on time threshold voltage	T_{ON} = T_{ON_MIN}	$V_{CMP\_TON\_MIN}$	0.95	1.0	1.05	V
Minimum frequency	V_{COMP} ≦ V_{COMP_FLL}	f_{MIN}	350	500	650	Hz
Maximum frequency	V_{COMP}≧V_{CMP_FLH}	f_{MAX}	78	90	105	kHz
Zero Current Detector and Feedback (FB Pin)						
Upper clamp voltage	I_{FB} = 0.2mA	V_{ZH}	4.4	4.7	5.0	V
Lower clamp voltage	I_{FB} = -2mA	V_{ZL}	0		-0.6	V
Input voltage rising threshold voltage	Detect at T_{BLA} during gate off.	V_{FBR}		0.52		V
Minimum blanking time of FB pin	*;	T_{BLA_ALL}		1.25		μs
QRD threshold voltage		V_{QRD}		0.3		V
FBOVP threshold voltage for SET0	R_{CS} ≦ 500Ω; Detect gate off after about 750ns.	$V_{FB\_OVP\_0}$	3.88	4.0	4.12	V
FBOVP threshold voltage for SET1	R_{CS} ≧ 800Ω; Detect gate off after about 750ns.	$V_{FB\_OVP\_1}$	4.08	4.2	4.32	V
FBOVP de-bounce	* ;	T_{DEB_FBOV}		4		Cycle
FBUVP threshold		$V_{FB\_UVP\_H}$	0.7	0.83	0.95	V
Output short protection de-bounce time	*; Enable this function after JFET is off	T_{DEB_OSCP}		56		ms
Internal reference voltage	Steady state ; Tj=25 ℃	V_{REF}	3.44	3.50	3.56	V
	Steady state ; Tj=--40~125 ℃			3.50		

V_{CC}=15.0V, T_A = 25°C unless otherwise specified.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Current Sensing (CS Pin)						
Soft start time	*; After T_{CCMP} end	T_{SS1}		39		ms
Soft start 1 mode	*; After T_{CCMP} end. During T_{SS11}, Fsw=22kHz and V_{CS} limit = 0.2V	T_{SS11}		5		ms
Soft start 2 mode	*; After T_{SS11} end, V_{CS} limit rising from 0.2 to 0.7V and ~100mV/step	T_{SS12}		34		ms
Leading edge blanking time	*; Including programming delay time.	T_{LEB_CS}	310	460	610	ns
Over current limitation threshold voltage		V_{CS_MIN}	0.75	0.83	0.91	V
		V_{CS_MAX}	0.93	1.00	1.07	V
Current limitation threshold voltage for secondary diode short protection		V_{OCP2}	0.9	1.0	1.1	V
Secondary diode short protection de-bounce	* ;	T_{OCP2}		7		Cycle
CSOTP threshold voltage	Detect gate off after about T_{BLA_CSOTP}.	V_{CS_OTP}	0.45	0.50	0.55	V
CSOTP blanking time	*; After gate off condition	T_{BLA_CSOTP}		1.5		μs
CSSP Threshold Voltage		V_{CSSP}	75	100	125	mV
CSSP de-bounce time	*; Enable this function after JFET is off and V_{COMP} ≧ 2V continuous.	T_{CSSP}		56		ms
Gate Drive Output (OUT Pin)						
Output low level		V_{G_LO}			0.5	V
Output high level		V_{G_HI}		10.6	13	V
Rising time	*; C_L=1000pF	T_{G_RISE}		250		ns
Falling time	*; C_L=1000pF	T_{G_FALL}		35		ns
Internal OTP (Over Temp. Protection)						
OTP tripping point	*; No switching	OTP		140		°C
OTP hysteresis	*;	ΔOTP		20		°C

*: Guaranteed by design.

Application Information

Operation Overview

LD7841K is an excellent active PFC single-stage flyback controller with constant voltage output and primary side regulation (PSR) control algorithm for LED lighting applications. It drives converter operating in quasi-resonant or discontinuous mode to achieve high efficiency, high power factor and lower harmonic current performance. By PSR, LD7841K is feedback accurately with primary side auxiliary winding without the shunt regulator and optocoupler at secondary side. By voltage mode control, the turn-on time of the switch is fixed while the turn-off time is varied in steady state. Therefore, the switching frequency varies in accordance with the input voltage or output loading variation. The maximum switching frequency is limited about 90kHz and minimum switching frequency is limited about 500Hz. LD7841K provides robust protections as over load protection, over voltage protection, over current protection, under voltage lockout and LEB of the current sensing. Its major features are described as below.

Internal High-Voltage Startup Circuit and Under Voltage Lockout (UVLO)

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes significant power to meet the power saving requirement. In most cases, startup resistors carry large resistance. It will take longer time to start up.

To achieve optimized topology, as shown in Fig. 2, LD7841K is implemented with a high-voltage startup circuit to enhance it. During startup, a high-voltage current source sinks current (I_{HV}) from the full-bridge rectifier to provide the startup current and charge VCC capacitor (C_{VCC}) at the same time. If the voltage of VCC pin (V_{VCC}) is lower than V_{PDR} (V_{UV_OFF}-1.5V, typ.), I_{HV} is limited about 1.3mA (typ.). Once V_{VCC} is higher than V_{PDR}, I_{HV} increases to 3.6mA (typ.) around to speed up startup sequence. Meanwhile, the VCC supply current (I_{ST}) consumes only 75μA (typ.), that most of the I_{HV} is reserved to charge C_{VCC}. In using such configuration, the turn on delay time will be almost no difference either in low line or high line conditions. Add the D_{HV} (Trr $\leqq$ 50ns) to avoid the negative voltage over the rating for some of application.

Once the V_{VCC} is higher than V_{UV_ON} (17.5V, typ.) and all of condition are checked (BNI, setting and CSSP…etc.), LD7841K powers on and further to deliver the gate drive signal, I_{HV} will not disabled right away and keeping provide current about 65ms (typ.) around for smaller C_{VCC} application. During this period, if V_{VCC} is higher than 23V (typ.), I_{HV} is off immediately.

The supply current is provided from the auxiliary winding of the transformer. Therefore, it would eliminate the power loss on the startup circuit and perform highly power saving.

An UVLO comparator is embedded to detect V_{CC} to ensure the supply voltage enough to power on and in addition to drive the power MOSFET. As shown in Fig. 3, a hysteresis is provided to prevent the shutdown from the voltage dip during startup.

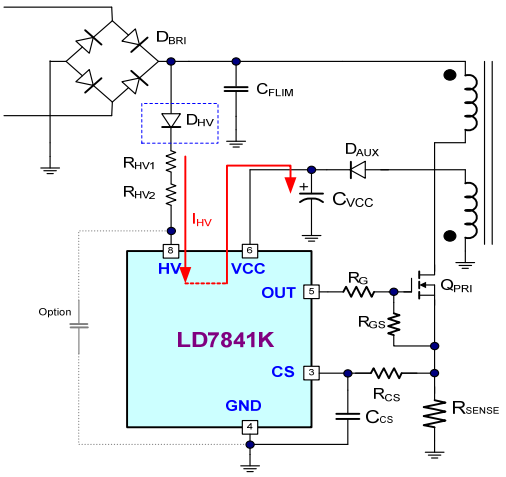


Fig. 2 Startup Circuit

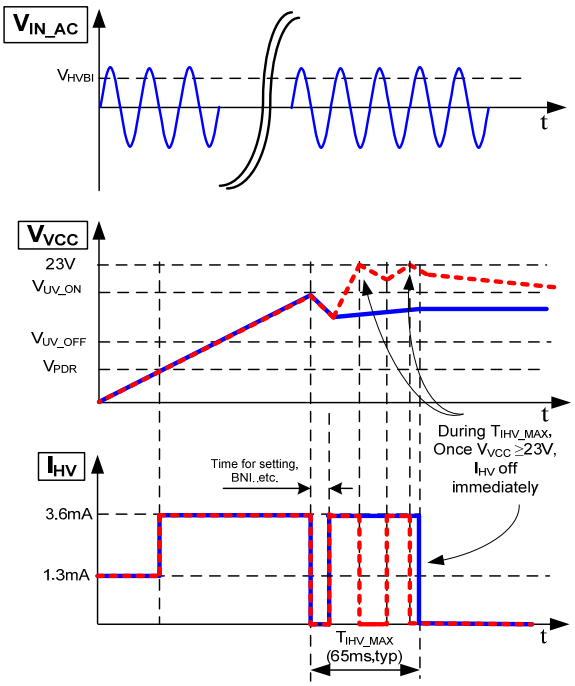


Fig. 3 I_{HV} Typically Waveform

After brown in condition is triggered, once V_{HV} is always lower than V_{HVBO} and longer than de-bounce time (T_{BNO}, 15ms, typ.), LD7841K will shut off to prevent from any damage.

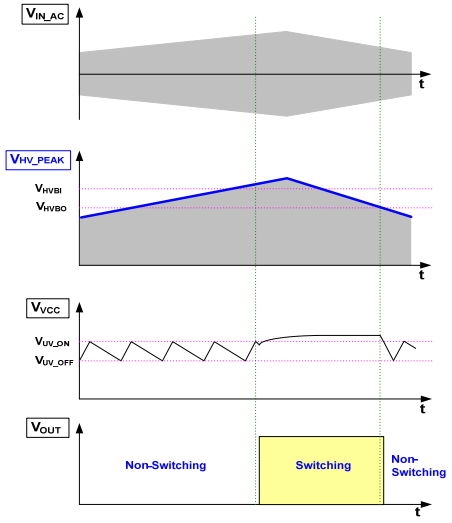


Fig. 5 BNI/BNO Function Sequence

Brown-In/Out on HV Pin

LD7841K provides brown-in/out function on HV pin. Fig. 4 and Fig. 5 show the operation. When V_{HV} is always lower than V_{HVBI} (100V_{DC}, typ.) during each period of 15ms around, the gate output will remain off even when the V_{VCC} already reaches V_{UV_ON}. It therefore forces the V_{VCC} hiccup between V_{UV_ON} and V_{UV_OFF} until V_{HV} is higher than V_{HVBI}. A hysteresis ($\triangle V_{HV}$, 15V_{DC}, typ.) is implemented to prevent the false-triggering during turn-on and turn off.

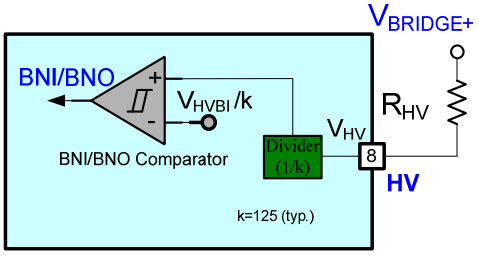


Fig. 4 BNI/BNO Function Block

Maximum On-Time Setting on FB Pin

LD7841K provides the maximum on time (T_{ON_MAX}) programmable function on FB pin. T_{ON_MAX} should be set according to the condition of the transformer, lowest AC line voltage, and maximum output power. A choice of optimum T_{ON_MAX} would result in best performance. As Fig.6, after V_{VCC} is higher than V_{UV_ON}, and BNI is triggered, the internal current source provides a constant current (I_{FB_SET}, 90 μA, typ.) about 450 μs (typ.) passed thought R_{FB_T} to check this voltage then set T_{MAX_N}.

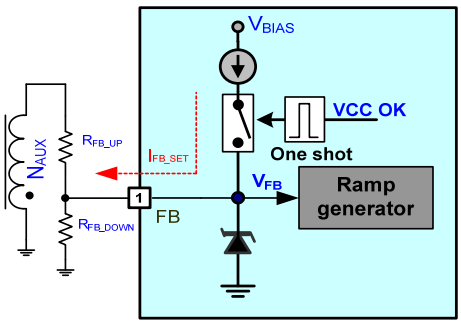


Fig. 6 Maximum on time Setting Block

Where:

$$R_{FB\_T} = \frac{(R_{FB\_UP} \times R_{FB\_DOWN})}{(R_{FB\_UP} + R_{FB\_DOWN})} \quad \text{(eq.1)}$$

The following table is the resistance suggestion for maximum on-time setting.

T_{MAX_N}	Condition	Max. on Time @V_{HV}=100V_{DC}	R_{FB_T} suggestion
T_{MAX_1}	22kΩ ≧ R_{FB_T} ≧ 18kΩ	~27μs	20kΩ
T_{MAX_2}	10kΩ ≧ R_{FB_T} ≧ 6kΩ	~17μs	8kΩ

Table1. Maximum on Time Setting

LD7841K implements the compensation of on time by monitor HV pin, as shown in below,

$$T_{ON\_MAX} = T_{MAX\_N} \times K_{TON} \quad \text{(eq.2)}$$

$$K_{TON} = \frac{100V}{V_{HV\_PEAK}} \quad \text{(eq.3)}$$

Where: V_{HV_PEAK} is from 100V_{DC} to 400V_{DC}. For abnormal condition, if FB pin is shorted to GND or floating (badly soldered), LD7841K will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

FB Short / Open Circuit Protection Before Startup

For abnormal condition, if the FB pin is opened condition, I_{FB_SET} will pull the V_{FB} into high level. Once V_{FB} is higher than 2.7V (typ.). LD7841K will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

If the FB pin is shorted to GND, V_{FB} will be pulled low, once V_{FB} is lower than 0.35V (typ.). LD7841K will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

Dynamic Improved Threshold Level Setting

LD7841K provides the dynamic improved threshold level programmable function. As Fig.7, after VCC is higher than V_{UV_ON}, and BNI is triggered, the internal current source provides a constant current (I_{CS_SET}, 270 μA, typ.) about 600 μs (typ.) passed thought R_{CS} to set threshold level.

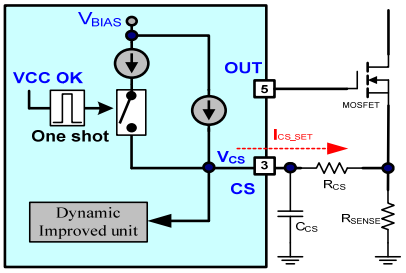


Fig. 7 Dynamic improved threshold level setting block

Table2 is the parameter setting of dynamic improvement as resistance suggestion on CS pin and dynamic trigger threshold level.

ITEM	R_{CS} (Ω)	USD	OSD1	OSD2	OSD3	V_{FB_OVP} (V)
		Percentage to V_{REF} (%)				
SET0	≦ 500	-4.2%	+5.7%	+8.6%	+11.4%	4.0V
Hysteresis		+100mV	-60mV	-120mV	-120mV	
SET1	≧ 800	-7.7%	+8.6%	+11.4%	+14.3%	4.2V
Hysteresis		+200mV	-120mV	-120mV	-120mV	

Table2. Dynamic and Over Voltage Setting Table

For abnormal condition, if the CS pin is floating, I_{CS_SET} will pull high the V_{CS}, once V_{CS} is higher than 2V (typ.) LD7841K will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

Consideration the tolerance of output capacitance and dynamic trigger level of LD7841K, the minimum output capacitance recommend is as below.

$$C_{OUT\_SET0\_MIN} = \frac{I_{OUTPUT\_MAX}}{2\times\pi\times f_{LINE}\times(2\times 3.5\%\times V_{OUT\_TYP.})} \quad \text{(eq.4)}$$

$$C_{OUT\_SET1\_MIN} = \frac{I_{OUTPUT\_MAX}}{2\times\pi\times f_{LINE}\times(2\times 8.5\%\times V_{OUT\_TYP.})} \quad \text{(eq.5)}$$

Where f_{LINE} is the AC input minimum frequency.

Current Sense Short Circuit Protection Before Startup

After settings are done, LD7841K delivers one pulse gate drive signal to turn on the MOSFET and check the condition of CS pin. This pulse width is given by the following equation.

$$T_{ON\_CSSP} \approx 0.3 \times (K_{TON}) \times T_{MAX\_N} \quad \text{(eq.6)}$$

If V_{CS} is higher than V_{CSSP} (100mV, typ.) during T_{ON_CSSP}, it means the function of current sense is normally, LD7841K will operate into soft start after T_{CCMP} (3ms, typ.). If V_{CS} is higher than 200mV, gate off immediately to avoid the saturation of transformer. Once V_{CS} is lower than V_{CSSP}, the protection of current sense short circuit before startup triggered, LD7841K will interrupt startup sequence and operate into hiccup mode until the fault condition is removed.

Soft Start

LD7841K provides soft start function by steps current sense limitation. At startup, the output voltage is lower, system will operate into CCM and cause higher stress. So, V_{CS} is limited at 0.2V (typ.) and the switching frequency (F_{SW}) is fixed at 22kHz (typ.) in first 5ms (typ.) during soft start (T_{SS1}). After T_{SS1}, V_{CS} is rising from 0.2V to 0.7V step by step about 34ms (T_{SS2}, typ.) for limited power deliver. F_{SW} is controlled by the voltage of COMP pin (V_{COMP}) during T_{SS2}. Fig. 8 is shown typical waveforms.

Primary Side Regulation

LD7841K detects the auxiliary winding to achieve constant voltage regulation. The typically waveform is shown in Fig.9. When the current of secondary side discharging to zero, the primary side V_{FB} is at knee point, then LD7841K samples the voltage at knee point and holds it until next switching cycle. This signal ($V_{FB\_S\&H}$) is compared to V_{REF} by the internal error amplifier. As shown in Fig.10. In order to keep the system is stable, place the compensation network at COMP pin to GND as closed as possible.

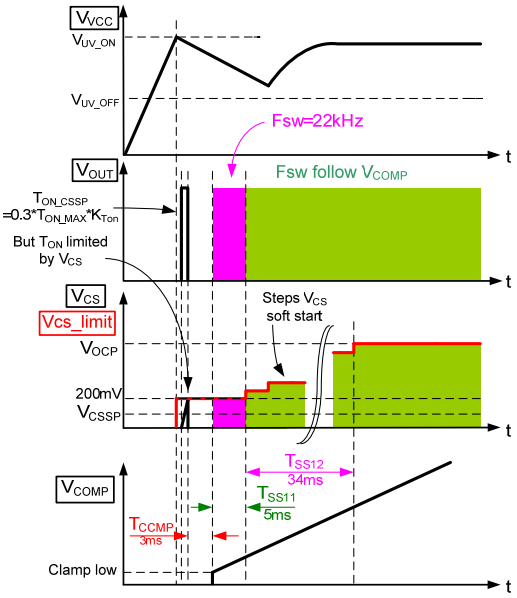


Fig. 8 current Sense Limitation Steps Function

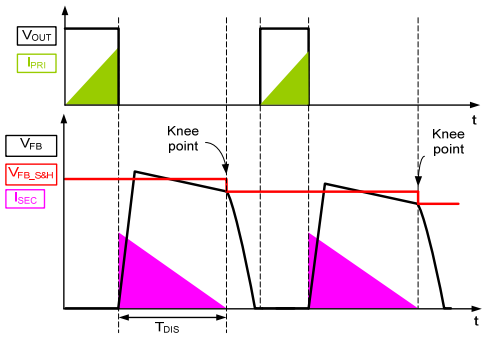


Fig. 9 V_{FB} Typically Waveform

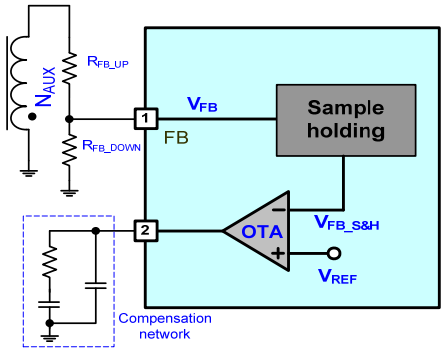


Fig. 10 Feedback Function Block

Principle of Constant Voltage Operation

The output voltage is given by the following equation.

$$V_{OUT} = (V_{REF} \times \frac{N_{SEC}}{N_{AUX}} \times \frac{R_{FB\_UP}+R_{FB\_DOWN}}{R_{FB\_DOWN}}) - V_F \quad \text{(eq.7)}$$

Where:

N_{SEC} is the turns of secondary main output winding.

N_{AUX} is the turns of auxiliary winding voltage to supply for VCC.

V_{REF} is the reference voltage of constant voltage feedback.

V_F is forward voltage of secondary rectifier diode.

Frequency Limitation

LD7841K implements the frequency limitation function to improve efficiency at light load. As shown in Fig.11, the maximum switching frequency is controlled by V_{COMP}.

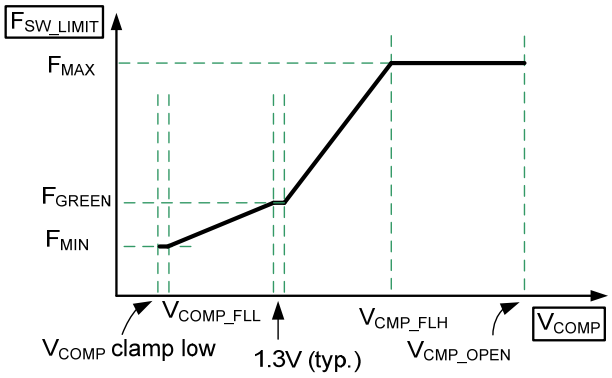


Fig. 11 Frequency Limitation Curve

Ramp Generator Block and Zero Current Detection (ZCD)

Fig. 12 shows typical function block. V_{COMP} and the output of the ramp generator block are compared to determine the MOSFET on-time.

A greater V_{COMP} produces more on-time. Using an external resistor connected to FB pin to set the desired slope of the internal ramp, the user may program the T_{ON_MAX}. Alternatively, the on-time will also achieve its maximum when V_{COMP} trip to V_{CMP_OPEN} (4.7V, typ.).

As shown in Fig.13, The block of zero current detection will detect auxiliary winding signal to drive MOSFET. If V_{FB} rises over V_{FBR} (0.52V, typ.) after T_{BLA} then drops under V_{QRD} (0.3V, typ.), the QRD signal is triggered and turn on MOSFET. As V_{FB} first drops to V_{QRD}, the current through the transformer is below zero. This feature enables transition-mode operation.

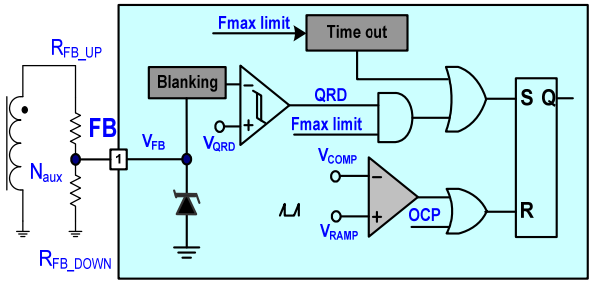


Fig. 12 QRD Function Block

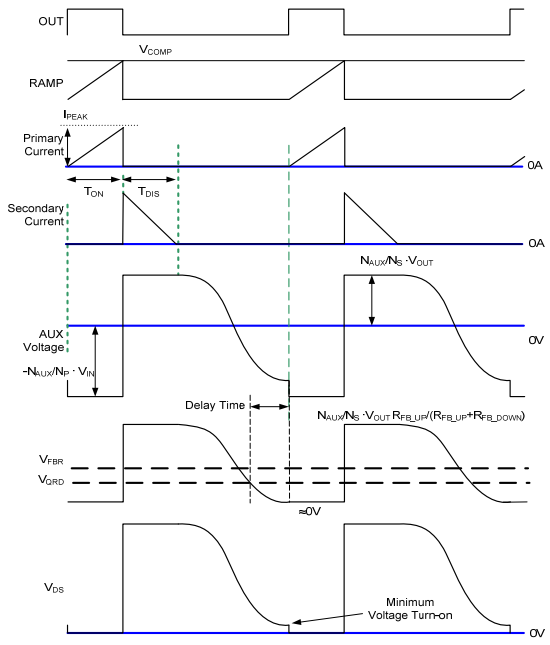


Fig. 13 QRD Detection on FB pin Waveform

Quasi-Resonant and DCM Operation

According to the difference of V_{FB}, LD7841K could operate at quasi-resonant mode or DCM mode. As

shown in Fig. 14. If QRD signal is triggered after the end of TO1 but before TO2, LD7841K operates at quasi-resonant mode.

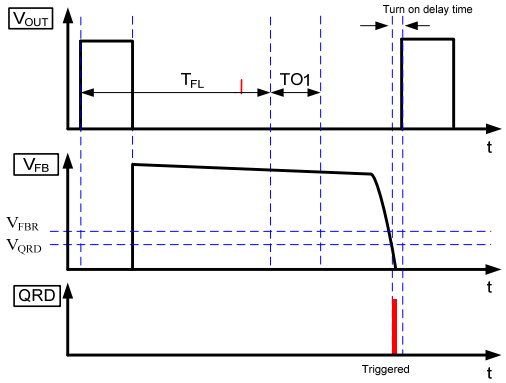


Fig. 14 QR Mode

As shown in Fig. 15. If QRD signal is triggered before the end of T_{FL}, the QRD signal is triggered but blanked to turn on MOSFET. After T_{FL}, QRD signal is triggered again and turn on the MOSFET during TO1 (5μs, typ.), LD7841K operates at DCM mode with valley switching. Where:

$$T_{FL} = \frac{1}{F_{SW\_LIMIT}} \quad \text{(eq.8)}$$

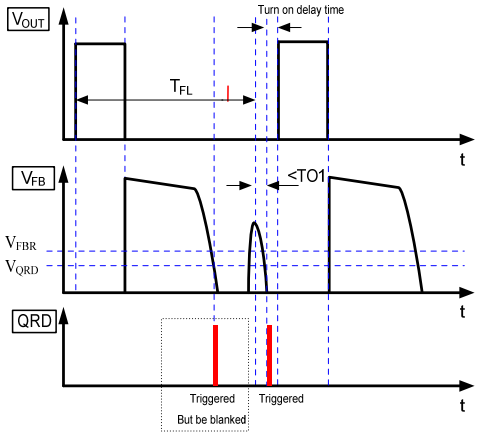


Fig. 15 DCM mode with valley switch

Same as previous condition but If QRD signal is not triggered again, the MOSFET will be turn on at the end of TO1 directly. LD7841K operates at DCM mode. As shown in Fig. 16.

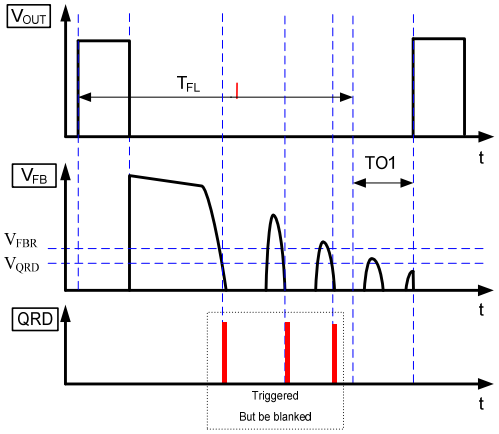


Fig. 16 DCM Mode

VCC Holding Mode

After UVLO (ON), if the V_{VCC} is lower than V_{LDO_LO}, internal high voltage source current will charge the C_{VCC}. Under the no load condition, VCC holding mode will keep the V_{VCC} higher than UVLO_OFF to avoid re-startup of system.

Output Drive Stage

With typical 250mA/-700mA peak driving capability, an output stage of a CMOS buffer is incorporated to drive a power MOSFET directly. The output voltage is clamped at 10.6V (typ.) to protect the MOSFET gate, even when the V_{CC} voltage is higher than 12V.

Leading-Edge Blanking and Cycle by Cycle limitation

A 460ns (typ.) leading-edge blanking time (T_{LEB_CS}) is included in the input of CS pin to prevent the false-trigger from the current spike. In the different rated power application, if the total pulse width of the turn-on spikes is lower than and the negative spike on the CS pin doesn't exceed -0.3V, it could eliminated the R-C filter.

However, the total pulse width of the turn-on spike is determined by the output power, circuit design and PCB

layout. It is strongly recommended to adopt a smaller R-C filter for higher power application to avoid the CS pin being damaged by the negative turn-on spike.

LD7841K detects the primary side peak current from the CS pin, which is used for cycle by cycle peak current limit. The maximum voltage threshold of the CS pin sets as V_{CS_MAX} (1.0V, typ.) or V_{CS_MIN} (0.83V, typ.) which are dependent on input voltage, once V_{CS} is higher than V_{CS_MAX} or V_{CS_MIN}, gate off immediately.

Protection Function

VCC Overvoltage Protection (VCCOVP)

The maximum rating of the VCC pin is limited below 30V. To prevent VCC from the fault condition, LD7841K is implemented with OVP function on VCC pin. When V_{VCC} higher than V_{CCH_CLAMP} (24.5V, typ.), LD7841K will sink a current about 3mA (typ.) first from VCC pin. But if supplier voltage keeps rising and higher than V_{CC_OVP} (27.5V, typ.) and de-bounce about 150μs continuously, LD7841K will enforce the gate off until the 1st cycle of VCC hiccup is tripped and the fault condition is removed.

FB Overvoltage Protection (FBOVP) - 1 Hiccup

If R_{FB_UP} is shorted or R_{FB_DOWN} is opened during operating, the feedback signal is incorrect. LD7841K is implemented with OVP function on FB pin. Once V_{FB} which is detected after gate off about 750ns and higher than $V_{FB\_OVP\_0}$ (4.0V, typ.) or $V_{FB\_OVP\_1}$ (4.2V, typ.), de-bounce about 4 switching cycles continuously, LD7841K will enforce the gate off until the 1st cycle of VCC hiccup is tripped and the fault condition is removed.

Under Voltage Protection (FBUVP/OSCP)

When the output short circuit occurs, the reflected output voltage of auxiliary winding will cause V_{FB} down. If V_{FB} is lower than V_{FB_UVP} (0.83V, typ.) and de-bounce about 56ms, LD7841K will enforce the gate off until the 4th cycle of VCC hiccup is tripped. For abnormal condition, if R_{FB_UP} is opened or R_{FB_DOWN} is shorted, FB under voltage protection is triggered too.

CS Short Circuit Protection (CSSP)

To avoid the damaged which is caused by CS pin short circuit during operating, LD7841K implemented a smart and robust CS short circuit protection function. If such fault condition occurs and V_{CS} is lower than V_{CSS} (100mV, typ.) then V_{COMP} is higher than 2V (typ.), after de-bounce about 56ms (T_{CSSP}), LD7841K will enforce the gate off until the 8th cycle of VCC hiccup is tripped and the fault condition is removed. As shown in Fig. 17.

CS Open Protection (CSOP)

If R_{CS} is opened during operating, The internal current source (I_{CS}, 10 μA, typ.) from CS pin to output , once V_{CS} is higher than V_{OCP_X}, LD7841K will enforce the gate off until the 1ST cycle of VCC hiccup is tripped and the fault condition is removed.

Over Load or Open Loop Protection (OLP)

LD7841K implemented the over loading protection, once V_{COMP} is higher than V_{OLP} (V_{CMP_OPEN}-0.3V, typ.) and after de-bounce about 210ms (T_{DEB_OLP}, typ.), LD7841K will enforce the gate off until the 4th cycle of VCC hiccup is tripped.

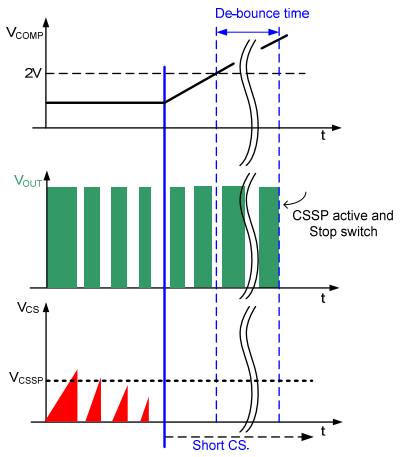


Fig. 17 Current Sense Short Circuit Protection

Secondary Diode Short Protection (SDSP)

The circuit detects output diode short condition if 7 consecutive switching cycles occur within which the CS pin voltage exceeds V_{OCP2} (1.0V, typ) within leading-edge blanking time (T_{LEB_CS}), the LD7841K will enforce the gate off until the 8th cycle of VCC hiccup is tripped.

External Over Temperature Protection (CSOTP)

During gate off, once V_{CS} is higher than V_{CS_OTP} (0.5V, typ) which is detected after gate off about 1.5us (typ.) delay from gate off and continuously for 32 switching cycles (typ.), CSOTP function is active. LD7841K will enforce the gate off until the 1st cycle of VCC hiccup is tripped.

Internal Over Temperature Protection (int. OTP)

When the junction temperature reaches 140°C approximately, the thermal sensor signals would stop IC's switching. If the IC's junction temperature cools by 20°C or VCC restart again.

Over Current Protection (OCP)

When input is AC mode, if the V_{CS} is equal to or higher than V_{CS_MAX} (for low line) / V_{CS_MIN} (for high line) once during entire haversine, the internal OCP's counter will mark and count until 28 haversine cycle continuously, OCP is triggered. The LD7841K will force the gate off until 8th cycle of VCC hiccup is tripped. As shown in Fig. 18.

Over Voltage Protection on HV Pin (ACOVP)

When $V_{HV} \geqq V_{ACOVP}$ and after de-bounce time (T_{D_ACOVP}) about 150us, ACOVP is triggered. The LD7841K will force the gate off until 1st cycle of VCC hiccup is tripped and the fault condition is removed. As shown in Fig. 19.

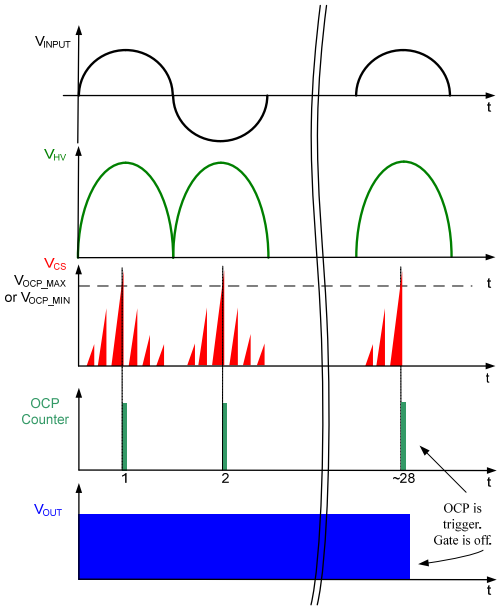


Fig. 18 Over Current Protection

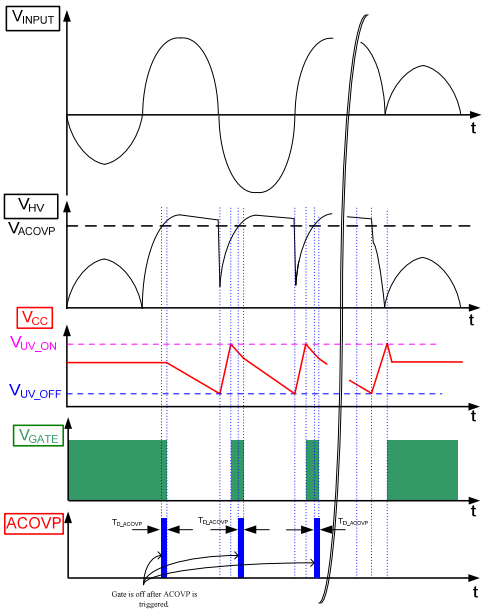
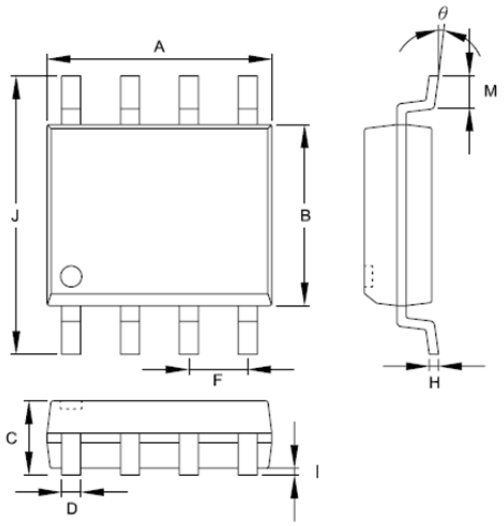


Fig. 19 ACOVP Function

Package Information

SOP-8



Symbol	Dimensions in Millimeters		Dimensions in Inch	
	MIN	MAX	MIN	MAX
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
θ	0°	8°	0°	8°

Revision History

REV.	Date	Change Notice
P00	10/20/2021	Original Specification.