PTR6100

2.4GHz 2Mbps Super MiNi Embedded Transceiver Module

Features:

- 2.4GHz ISM Band
- Power supply range:1.9~3.6 V
- 5V tolerant input signal pads
- Digital interface (SPI)speed :0~8Mbps
- 100% RF tested
- **High Speed:** Data rate 250kbps/1Mbps/2Mbps
- **Ultra-Low Cost:** High Hardware Integration, Need Few external components
- **Ultra-low Power:** The fast data rate and little time on the air reduced communications current
- **Minitype:** Size about 34x16mm with Antenna
- Range about 30-60 meters in open space
- **Enhanced ShockBurst™:**
  - MultiCeiver™-6 data pipes
  - Auto acknowledgement
  - Auto re-transmission
  - Packet identity
  - Carrier sense-stationary disturbance
  - Packet error counter
  - Three level deep RX FIFO and three level deep TX FIFO

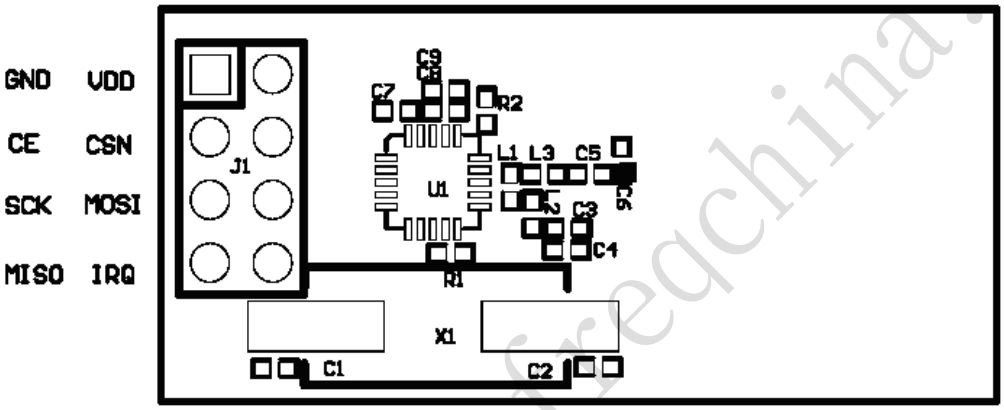
Typical Applications:

- RFID
- Security Applications
- Vehicle alarm systems
- Remote meter reading
- Remote data acquisition
- Alarm and Security System
- Authorization / Access control
- Automatic Meter Reading (AMR)
- High integrity wireless Fire / Security alarms
- Building environment control / monitoring
- Wireless mouse/keyboard and PC peripherals
- Wireless hands free
- Sports and leisure equipment
- Game pads
- Wireless Communication

Performance Data:

Parameter	Value	Unit
Minimum supply voltage	1.9	V
Maximum output power	0	dBm
Maximum data rate	2000	kbps
Supply current in TX mode@0dBm output power	11.3	mA
Supply current in RX mode@2000 kbps	13.5	mA
Sensitivity @250kbps	-94	dBm
Supply current in Power Down mode	900	nA

Pin Description（Top View）:



Pin		function	direct
Pin1	GND	Ground	
Pin2	VCC	Power supply :1.9~3.6V	
Pin3	CE	Chip enable control RX or TX mode	I
Pin4	CSN	SPI Chip Select	I
Pin5	SCK	SPI Clock	I
Pin6	MOSI	SPI Slave Data Input	I
Pin7	MISO	SPI Slave Data Output	O
Pin8	IRQ	interrupt pin	O

1、Mode Control:

PTR6100M module can work in following modes depending on CE pin and register PWR_UP, PRIM_RX

Control Level				
PWR_UP (register)	PRIM_RX (register)	CE	Mode	FIFO State
1	1	1	RX mode	-
1	0	1	TX mode	Data in TX FIFO
1	0	1->0	TX mode	Stays in TX mode until packet transmission is finished
1	0	1	Standby-II	TX FIFO empty
1	-	0	Standby-I	No ongoing packet transmission

0	-	-	Power Down	-

Application Note:

1. SPI Interface:

SPI is composed of SCK, MISO, MOSI and CSN.

（1） Under standby or power down mode, MCU set register's parameters though SPI

（2） Under receive/transmit mode, MCU read out or write on data though SPI

（3） The SPI interface is a standard SPI interface, maximum data rate is 8Mbps

2. Interrupt Output Interface (IRQ)

PTR6100M provide an active low interrupt pin (IRQ). It can active when Transmit Data Sent or Receive Data Ready or Maximum number of TX retries.

PTR6100M SPI Instruction Set

SPI Instruction For PTR6100M		
Instruction Name	**Instruction Format**	**Operation**
R_REGISTER	000A AAAA	Read registers. AAAAA = 5 bit Memory Map Address
W_REGISTER	001A AAAA	Write registers. AAAAA = 5 bit Memory Map Address *Executable in power down or standby modes only.*
R_RX_PAYLOAD	0110 0001	Read RX-payload: 1 – 32 bytes. A read operation will always start at byte 0. Payload will be deleted from FIFO after it is read. Used in RX mode.
W_RX_PAYLOAD	1010 0000	Used in TX mode. Write TX-payload: 1 – 32 bytes. A write operation will always start at byte 0.
FLUSH_TX	1110 0001	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, i.e. acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	Used for a PTX device Reuse last sent payload. Packets will be repeatedly resent as long as CE is high. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission
NOP	1111 1111	No Operation. Might be used to read the STATUS register

Configuration Register Description

Address (Hex)	register	Bit	Reset Value	Type	Description
00	*CONFIG*				Configuration Register
	reserved	7	0	R/W	Only '0' allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_RD 1: Interrupt not reflected on the IRQ pin 0:Reflect RX_DR as active low interrupt on the IRQ pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the IRQ pin 0: Reflect TX_DS as active low interrupt on the IRQ pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the IRQ pin 0: Reflect MAX_RT as active low interrupt on the IRQ pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' – 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	1: PRX, 0: PTX
01	*EN_AA* *Enhanced ShockBurst™*				Enable 'Auto Acknowledgment' Function Disable this functionality to be compatible with nRF2401
	Reserved	7:6	00	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto ack. data pipe 5
	ENAA_P4	4	1	R/W	Enable auto ack. data pipe 4
	ENAA_P3	3	1	R/W	Enable auto ack. data pipe 3
	ENAA_P2	2	1	R/W	Enable auto ack. data pipe 2
	ENAA_P1	1	1	R/W	Enable auto ack. data pipe 1
	ENAA_P0	0	1	R/W	Enable auto ack. data pipe 0
02	*EN_RXADDR*				Enabled RX Addresses
	Reserved	7:6	00	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4
	ERX_P3	3	0	R/W	Enable data pipe 3

	ERX_P2	2	0	R/W	Enable data pipe 2
	ERX_P1	1	1	R/W	Enable data pipe 1
	ERX_P0	0	1	R/W	Enable data pipe 0
03	***SETUP_AW***				Setup of Address Widths (common for all data pipes)
	Reserved	7:2	00000	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' – 5 bytes LSByte will be used if address width below 5 bytes
04	***SETUP_RETR***				Setup of Automatic Retransmission
	ARD	7:4	0000	R/W	Auto Re-transmit Delay ‘0000’ – Wait 250+86uS ‘0001’ – Wait 500+86uS ‘0010’ – Wait 750+86uS …….. ‘1111’ – Wait 4000+86uS (Delay defined from end of transmission to start of next transmission)
	ARC	3:0	0011	R/W	Auto Retransmit Count ‘0000’ –Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmit on fail of AA …… ‘1111’ – Up to 15 Re-Transmit on fail of AA
05	***RF_CH***				RF Channel
	Reserved	7	0	R/W	Only '0' allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel PTR6100M operates on
06	***RF_SETUP***			***R/W***	RF Setup Register
	CONT_WAVE	7	0	R/W	Enables continuous carrier transmit when high.
	Reserved	6	0	R/W	Only '0' allowed
	RF_DR_Low	5	0	R/W	Set RF Data Rate to 250kbps. See RF_DR_HIGH for encoding.
	PLL_LOCK	4	0	R/W	Force PLL lock signal
	RF_DR_High	3	1	R/W	Select between the high speed data rates. This bit is don’t care if RF_DR_LOW is set. Encoding:

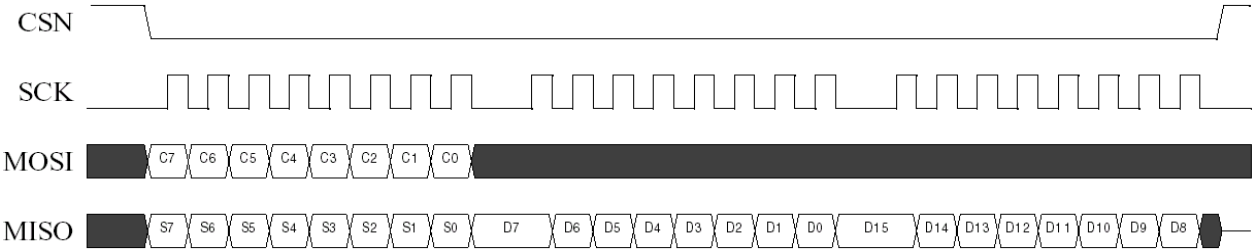
					[RF_DR_LOW, RF_DR_HIGH]: ‘00’ – 1Mbps ‘01’ – 2Mbps ‘10’ – 250kbps ‘11’ – Reserved
	RF_PWR	2:1	11	R/W	Set RF output power in TX mode '00' – -18 dBm '01' – -12 dBm '10' – -6 dBm '11' – 0 dBm
	LNA_HCURR	0	1	R/W	Setup LNA gain
07	***STATUS***				Status Register (In parallel to the SPI instruction word applied on the MOSI pin, the STATUS register is shifted serially out on the MISO pin)
	Reserved	7	0	R/W	Only '0' allowed
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Set high when new data arrives RX FIFO13. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt. Set high when packet sent on TX. If AUTO_ACK is activated, this bit will be set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retries interrupt Write 1 to clear bit. If MAX_RT is set it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: Not Used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
08	***OBSERVE_TX***				Transmit observe register
	PLOS_CNT	7:4	0	R	Packet Loss Counter. The register is reset by writing to RF_CH. The counter restarts after 15 lost packets. See page 14 and 16.
	ARC_CNT	3:0	0	R	Current value on resent counter. The counter is reset when transmission of a new packet starts.

09	*RPD*				
	Reserved	7:1	000000	R	
	RPD	0	0	R	Received Power Detector.
0A	*RX_ADDR_P0*	*39:0*	*0xE7E7 E7E7E7*	*R/W*	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first)
0B	*RX_ADDR_P1*	*39:0*	*0xC2C2 C2C2C2*	*R/W*	Receive address data pipe 1. 5 Bytes maximum length. (LSByte is written first)
0C	*RX_ADDR_P2*	*7:0*	*0xC3*	*R/W*	Receive address data pipe 2. Only LSB. MSBytes will be equal to RX_ADDR_P1[39:8]
0D	*RX_ADDR_P3*	*7:0*	*0xC4*	*R/W*	Receive address data pipe 3. Only LSB. MSBytes will be equal to RX_ADDR_P1[39:8]
0E	*RX_ADDR_P4*	*7:0*	*0xC5*	*R/W*	Receive address data pipe 4. Only LSB. MSBytes will be equal to RX_ADDR_P1[39:8]
0F	*RX_ADDR_P5*	*7:0*	*0xC6*	*R/W*	Receive address data pipe 5. Only LSB. MSBytes will be equal to RX_ADDR_P1[39:8]
10	*TX_ADDR*	*39:0*	*0xE7E7 E7E7E7*	*R/W*	Transmit address. Used for a PTX device only. (LSByte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with Enhanced ShockBurst™ enabled.
11	*RX_PW_P0*				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes). 0 Not Legal 1 = 1 byte … 32 = 32 bytes
12	*RX_PW_P1*				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes). 0 Not Legal 1 = 1 byte … 32 = 32 bytes
13	*RX_PW_P2*				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes).

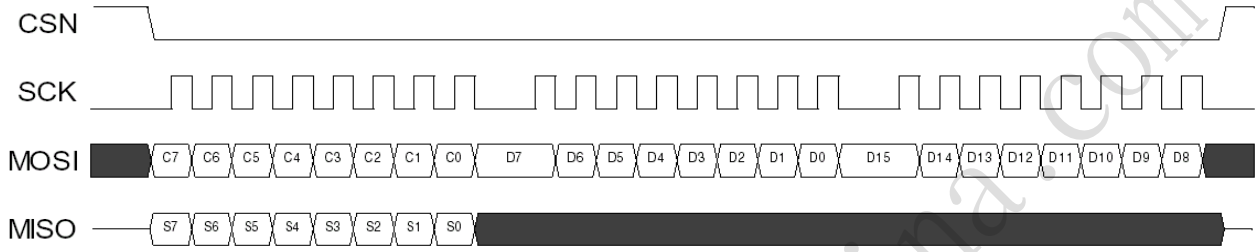
					0 Not Legal 1 = 1 byte … 32 = 32 bytes
14	*RX_PW_P3*				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes). 0 Not Legal 1 = 1 byte … 32 = 32 bytes
15	*RX_PW_P4*				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4(1 to 32 bytes). 0 Not Legal 1 = 1 byte … 32 = 32 bytes
16	*RX_PW_P5*				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes). 0 Not Legal 1 = 1 byte … 32 = 32 bytes
17	*FIFO_STATUS*				FIFO Status Register
	Reserved	7	0	R/W	Only '0' allowed
	TX_REUSE	6	0	R	Reuse last sent data packet if set high. The packet will be repeatedly resent as long as CE is high. TX_REUSE is set by the SPI instruction REUSE_TX_PL, and is reset by the SPI instructions W_TX_PAYLOAD or FLUSH TX
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1: TX FIFO empty. 0: Data in TX FIFO.
	Reserved	3:2	00	R/W	Only '00' allowed

	RX_FULL	1	0	R	RX FIFO full flag. 1: RX FIFO full. 0: Available locations in RX FIFO.
	RX_EMPTY	0	1	R	RX FIFO full flag. 1: RX FIFO empty. 0: Data in RX FIFO.
N/A	**TX_PLD**	255:0		W	Written by separate SPI command TX data payload register 1 - 32 bytes. This register is implemented as a FIFO with 3 levels. Used in TX mode only
N/A	**RX_PLD**	255:0		R	Written by separate SPI command RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with 3 levels. All receive channels share the same FIFO
1C	***DYNPD***				Enable dynamic payload length
	Reserved	**7:6**		R/W	Written by separate SPI command RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with 3 levels. All receive channels share the same FIFO
	DPL_P5	5		R/W	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4		R/W	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3		R/W	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P4)
	DPL_P2	2		R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P4)
	DPL_P1	1		R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P4)
	DPL_P0	0		R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P4)
1D	***FEATURE***				Feature Register
	Reserved	**7:3**		R/W	Only ‘00000’ allowed
	EN_DPL	2		R/W	Enables Dynamic Payload Length
	EN_ACK_PAY	1		R/W	Enables Payload with ACK
	EN_DYN_ACK	0		R/W	Enables the W_TX_PAYLOAD_NOACK command
	DPL_P2	2		R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P4)
	DPL_P1	1		R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P4)
	DPL_P0	0		R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P4)

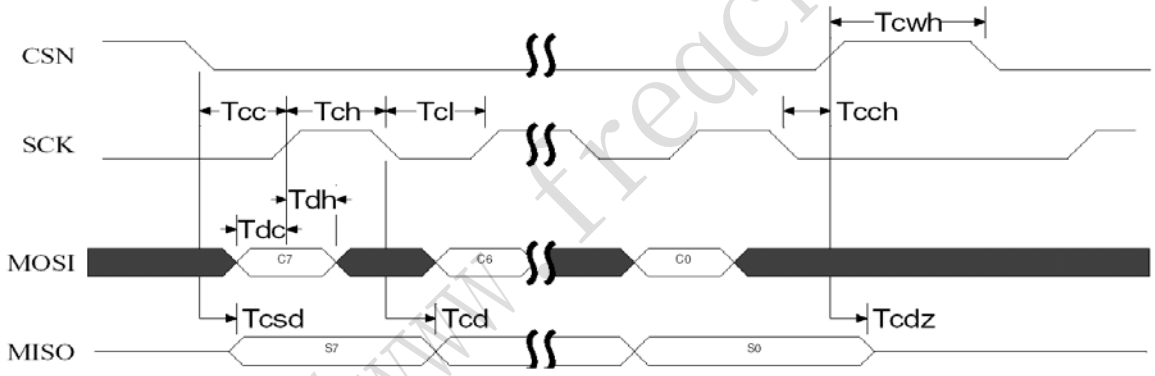
SPI Timing



SPI read operation



SPI write operation



SPI NOP timing diagram

Note:

Cn – SPI Instruction Bit
Sn – Status Register Bit
Dn – Data Bit (note: LSByte to MSByte, MSBit in each byte first)

PARAMETER	SYMBOL	MIN	MAX	UNITS
Data to SCK Setup	Tdc	2		ns
SCK to Data Hold	Tdh	2		ns
CSN to Data Valid	Tcsd		42	ns
SCK to Data Valid	Tcd		58	ns
SCK Low Time	Tcl	40		ns
SCK High Time	Tch	40		ns
SCK Frequency	Fsck	0	8	MHz
SCK Rise and Fall	Tr,Tf		100	ns
CSN to SCK Setup	Tcc	2		ns
SCK to CSN Hold	Tcch	2		ns
CSN Inactive time	Tcwh	50		ns
CSN to Output High Z	Tcdz		42	ns

SPI timing parameters

Programming of PTR6100M

By placing all high speed signal processing related to RF protocol on-chip, PTR6100M can connect with most kinds of cheap micro controller (MCU), and also can use high-speed processor as DSP etc. PTR6100M offers a simple SPI interface to application micro controller, which the data rate is 0~8Mbps, decided by the micro controller.

The PTR6100M module is embedded baseband protocol engine (Enhanced ShockBurst™), The embedded baseband protocol engine (Enhanced ShockBurst™) is supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced Shock- Burst™ reduces system cost by handling all the high-speed link layer operations.

Enhanced ShockBurst™ enables the implementation of ultra low power, high performance communication with low cost host microcontrollers.

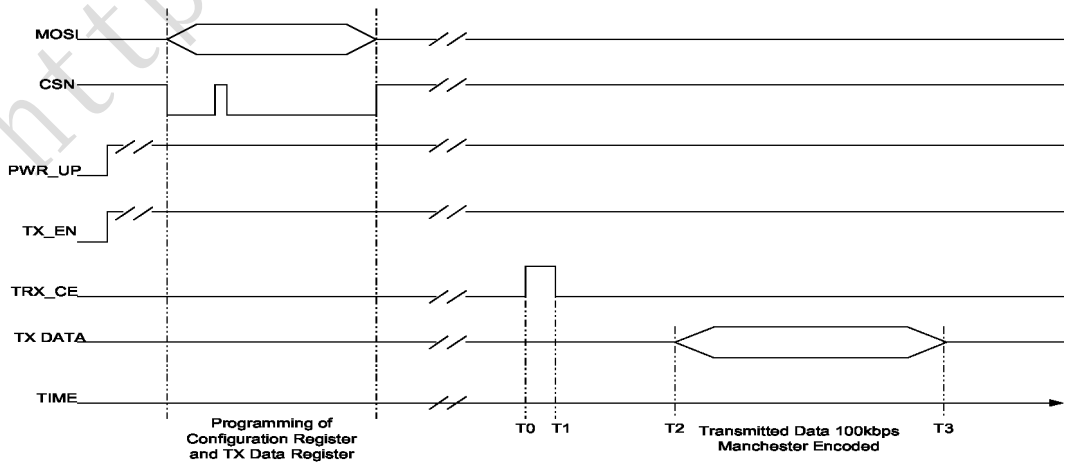
1、Configuration

In power down or standby modes, MCU select the useful registers to configuration via SPI interface.

2、Enhanced ShockBurst™ Transmitting Payload:

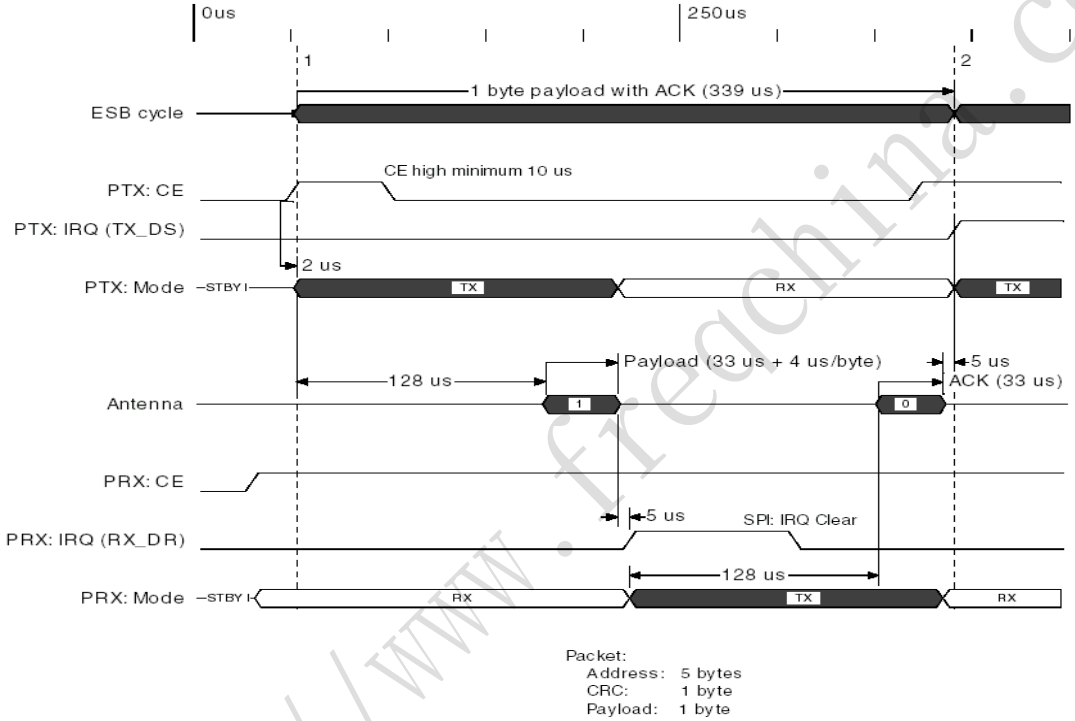
1. The configuration bit PRIM_RX has to be low.
2. When the application MCU has data to send, the address for receiving node (TX_ADDR) and payload data (TX_PLD) has to be clocked into PTR6100M via the SPI interface. TX_ADDR does not have to be rewritten if it is unchanged from last transmit. If the PTX device shall receive acknowledge, data pipe 0 has to be configured to receive the acknowledge. The receive address for data pipe 0 (RX_ADDR_P0) has to be equal to the transmit address (TX_ADDR) in the PTX device.
3. A high pulse on CE starts the transmission. The minimum pulse width on CE is 10 µs.
4. If auto acknowledgement is activated (Auto retransmit counter not equal zero, ENAA_P0=1) the radio goes into RX mode immediately.
5. The device goes into Standby-I mode if CE is low. Otherwise next payload in TX FIFO will be sent. If TX FIFO is empty and CE is still high, the device will enter Standby-II mode.
6. If the device is in Standby-II mode, it will go to Standby-I mode immediately if CE is set low.

TX timing

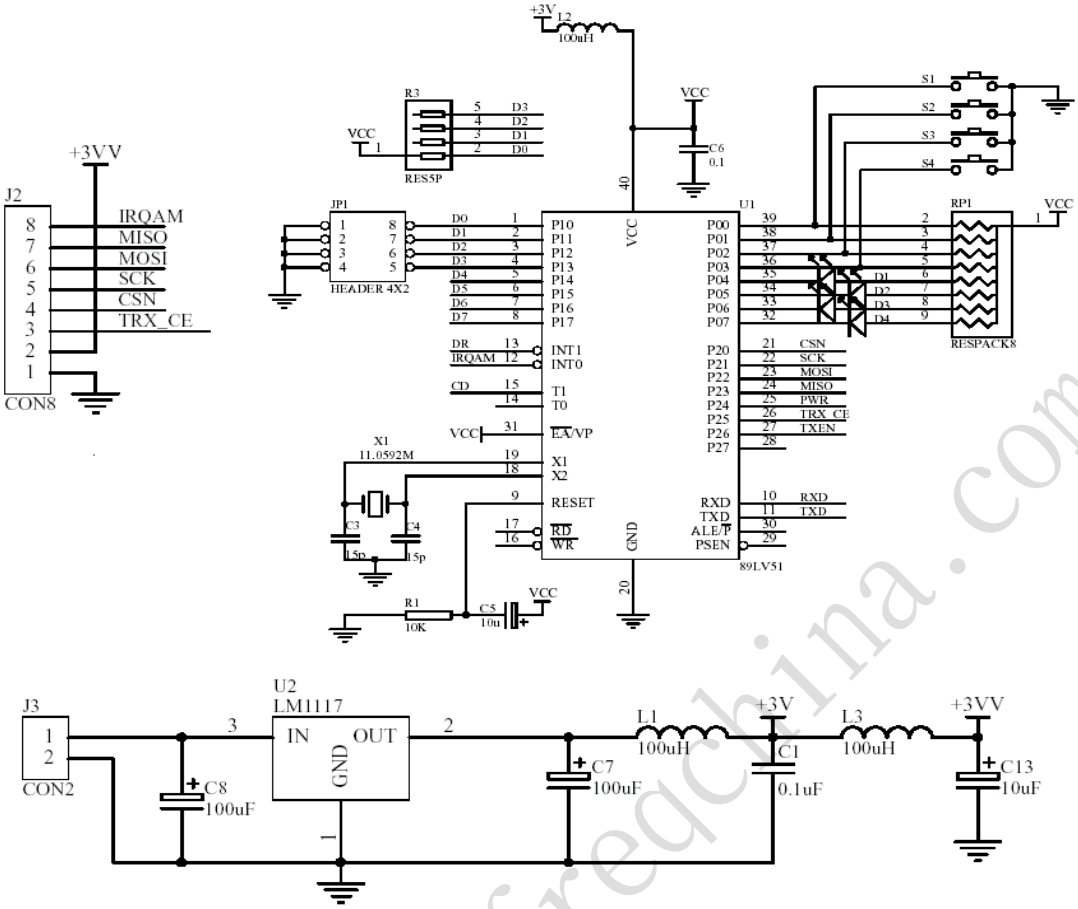


3、Enhanced ShockBurst™ Receive Payload:

1. The configuration bit PRIM_RX has to be high.
2. MCU sets the CE pin high.
3. After 130μs PTR6100M module is monitoring the air for incoming communication.
4. When a valid packet has been received (matching address and correct CRC), the payload is stored in the RX-FIFO, and the RX_DR bit in status register is set high. The IRQ pin will be active when RX_DR is high. RX_P_NO in status register will indicate what data pipe the payload has been received in.
5. If auto acknowledgement is enabled, an acknowledgement is sent back.
6. MCU sets the CE pin low to enter Standby-I mode (low current mode).
7. MCU can clock out the payload data at a suitable rate via the SPI interface.
8. The device is now ready for entering TX or RX mode or power down mode.

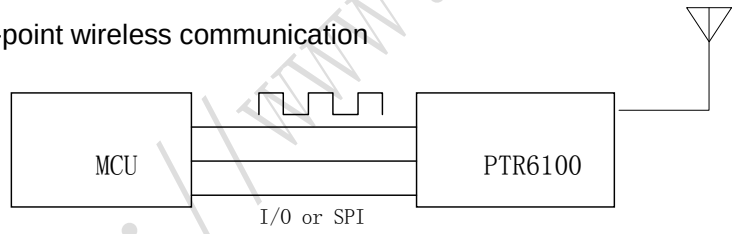


PTR6100M Hardware interface to MCU:

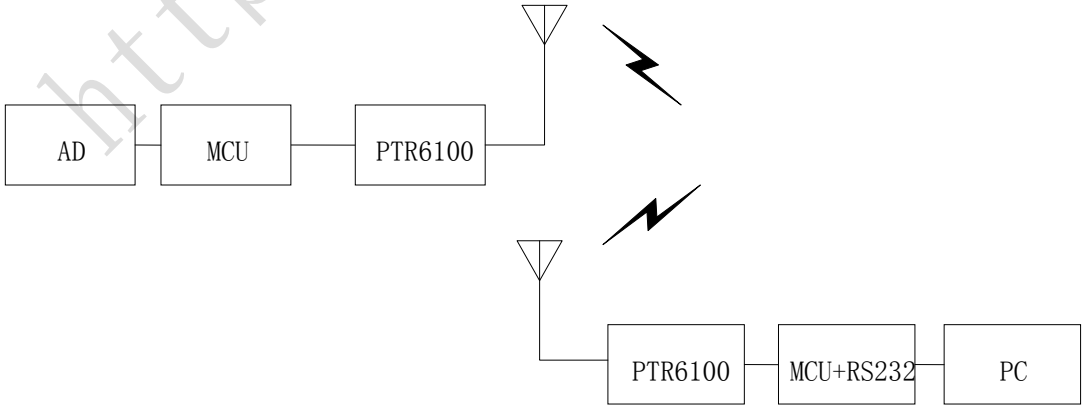


Application:

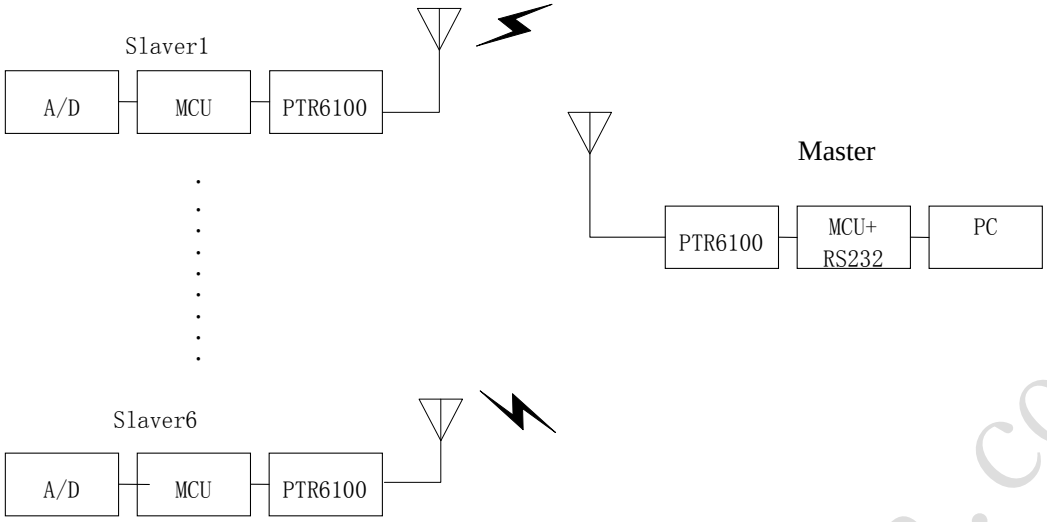
1)：Point-to-point wireless communication



2)：In data acquisition system point to point data transmitting,



3) point to multi-points bi-directional data transmission.



ATTENTION!

Electrostatic Sensitive Device

Observe Precaution for handling.