NSi1312

High Reliability Reinforced Isolated Amplifier

Datasheet (EN) 1.2

Product Overview

NSI1312 is a cost-effective isolated amplifier with output separated from input based on the NOVOSENSE capacitive isolation technology Adaptive OOK®. The device has a linear differential input signal range of ±1.2V (±1.5V full-scale). The high input impedance of NSI1312 makes it highly suitable for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

The device has a fixed gain of 1 and provides differential analog output version(NSI1312D) and single-ended analog output version(NSI1312S) option.

The low offset and gain drift ensure the accuracy over the entire temperature range. The high common-mode transient immunity ensures that the device is able to provide accurate and reliable measurements even in the presence of high-power switching such as in motor control applications.

The fail-safe function (missing VDD1 detection) simplifies system-level design and diagnostics.

Key Features

- Up to 5000V_{RMS} Insulation Voltage
- ±1.2V Linear Input Voltage Range
- Fixed Gain : 1
- Excellent DC Performance:
  - Offset Error: ±5mV (Max)
  - Offset Drift: ±20μV/℃ (Typ)
  - Gain Error: ±1% (Max)
  - Gain Drift: ±30ppm/℃ (Typ)
  - Nonlinearity: ±0.3% (Max)
  - Nonlinearity Drift: ±10ppm/℃ (Typ)
- SNR: 72dB (Typ)
- High CMTI: 100kV/μs (Typ)
- System-Level Diagnostic Features:
  - VDD1 monitoring
- Operation Temperature: -40℃~125℃
- RoHS-Compliant Packages:
  - SOW8 wide body (SOP8 300mil)
  - SOP8 narrow body (SOP 150mil)

Safety Regulatory Approvals

- UL recognition:
  - SOW8: 5000V_{rms} for 1 minute per UL1577
  - SOP8: 3000V_{rms} for 1 minute per UL1577
- CQC certification per GB4943.1-2011
- CSA component notice 5A approval IEC60950-1 standard
- DIN VDE V 0884-11:2017-01

Applications

- AC motor controls
- Power and solar inverters
- Uninterruptible Power Suppliers
- Automotive onboard chargers

Device Information

Part Number	*Package*	*Body Size*
NSI1312x-DSWVR	SOW8(300mil)	5.85mm × 7.50mm
NSI1312x-DSPR	SOP8(150mil)	4.90mm × 3.90mm

Functional Block Diagrams

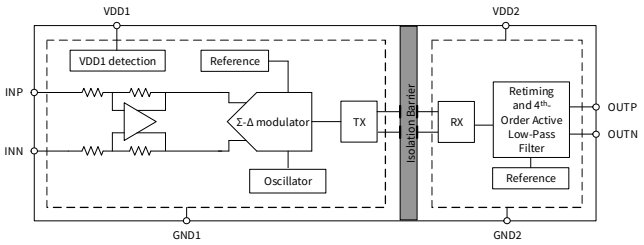

Figure 1. NSi1312D Block Diagram

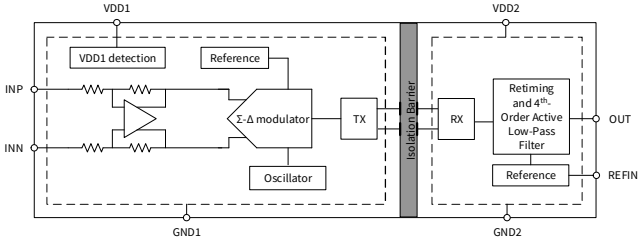

Figure 2. NSi1312S Block Diagram

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1. Pin Configuration and Functions

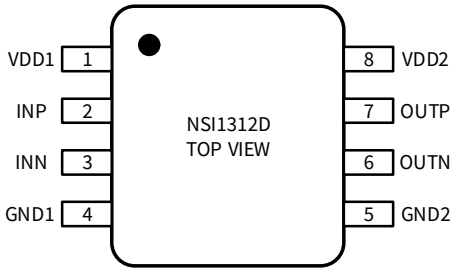


Figure 1.1 NSi1312D Package (SOW8 and SOP8)

Table 1.1 NSi1312D Pin Configuration and Description

NSi1312D PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power supply for isolator input side (4.5V to 5.5V)
2	INP	Positive analog input
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	OUTN	Negative output
7	OUTP	Positive output
8	VDD2	Power supply for isolator output side (3.0V to 5.5V)

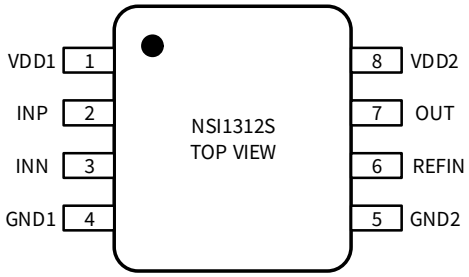


Figure 1.2 NSi1312S Package (SOW8 and SOP8)

Table 1.2 NSi1312S Pin Configuration and Description

NSi1312S PIN NO.	*SYMBOL*	*FUNCTION*
1	VDD1	Power supply for input side (4.5V to 5.5V)
2	INP	Positive analog input
3	INN	Negative analog input
4	GND1	Ground 1, the ground reference for input side
5	GND2	Ground 2, the ground reference for output side
6	REFIN	External Reference Input
7	OUT	Output
8	VDD2	Power supply for output side (3.0V to 5.5V)

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	VDD1, VDD2	-0.3		6.5	V
Input Voltage	INP, INN	GND1-6		VDD1+0.5	V
	REFIN	GND2-0.5		VDD2+0.5	V
Output Voltage	OUTP, OUTN, OUT	GND2-0.5		VDD2+0.5	V
Output current per Output Pin	Io	-10		10	mA
Operating Temperature	T_{OPR}	-40		125	℃
Junction Temperature	T_J	-40		150	℃
Storage Temperature	T_{STG}	-55		150	℃
Electrostatic discharge	HBM (1)	±2000			V
	CDM (2)	±1000			V

(1) Human body model (HBM), per AEC-Q100-002-RevD

(2) Charged device model (CDM), per AEC-Q100-011-RevB

3. Recommended Operating Conditions

Parameters	Symbol	Min	Typ	Max	Unit
Input side Power Supply	VDD1	3.0	5.0	5.5	V
Output side Power Supply	VDD2	3.0	3.3	5.5	V
Differential input voltage before clipping output	$V_{Clipping}$		±1.5		V
Linear differential input full scale voltage	V_{FSR}	-1.2		1.2	V
Operating common-mode input voltage	V_{CM}	-0.8		0.8	V
Operating Ambient Temperature	T_A	-40		125	℃

4. Thermal Information

Parameters	Symbol	SOW8	SOP8	Unit
Junction–to-ambient thermal resistance	$R_{\theta JA}$	86	137.7	℃/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	28	54.9	℃/W
Junction-to-board thermal resistance	$R_{\theta JB}$	42	71.7	℃/W
Junction–to-top characterization parameter	Ψ_{JT}	4	12	℃/W
Junction-to-board characterization parameter	Ψ_{JB}	42	46	℃/W

5. Specifications

5.1. Electrical Characteristics

(AVDD = 3.0V ~ 5.5V, DVDD = 3.0V ~ 5.5V, INP = -1.2V to +1.2V, and INN = AGND = 0V, T_A = -40℃ to 125℃. Unless otherwise noted, Typical values are at VDD1 = 5V, VDD2 = 3.3V, T_A = 25℃.Output characteristics is based on OUTP-OUTN for NSI1312D, is based on OUT-REFIN for NSI1312S.)

Parameters	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Comments*
Power Supply						
Input side supply voltage	VDD1	3.0	5.0	5.5	V	
Output side supply voltage	VDD2	3.0	5.0	5.5	V	
Input side supply current	IDD1		7.2	9	mA	
Output side supply current	IDD2		4.7	6.2	mA	
VDD1 undervoltage detection threshold voltage	$VDD1_{UV}$	1.8	2.3	2.7	V	VDD1 falling
Analog Input						
Input offset voltage	V_{OS}	-5	±1	5	mV	INP = INN = GND1, at T_A =25℃
Input offset drift	TCV_{OS}	-25	0.5	25	μV/°C	
Common-mode rejection ratio	$CMRR_{dc}$		-80		dB	INP = INN, f_{IN} = 0 Hz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
	$CMRR_{ac}$		-82		dB	INP = INN, f_{IN} = 10 kHz, $V_{CM\ min} \le VIN \le V_{CM\ max}$
Single-ended input resistance	R_{IN}		1		MΩ	INN = GND1
Differential input resistance	R_{IND}		1.6		MΩ	
Input capacitance	C_I		2		pF	
Input bias current	I_{IB}	-0.7	-0.6	-0.5	uA	INP = INN = GND1, at T_A =25℃, $I_{IB} = (I_{IBP} + I_{IBN}) / 2$
Input bias current drift	TCI_{IB}		-1		nA/°C	
Analog Output						
Nominal Gain			1		V/V	
Gain error	E_G	-0.4%	±0.1%	0.4%		at T_A =25℃
Gain error thermal drift	TCE_G	-50	-10	50	ppm/°C	
Nonlinearity		-0.05%	±0.01%	0.05%		at T_A =25℃
Nonlinearity drift			±1		ppm/°C	
Total harmonic distortion	THD		-70		dB	V_{IN} =±1.2V, f_{IN} = 10kHz, BW = 50kHz
Output noise			100		μV_{RMS}	INP = INN = GND1, BW = 50kHz
Signal to noise ratio	SNR		78		dB	V_{IN} =±1.2V, f_{IN} = 10kHz, BW = 50kHz
Common-mode output voltage	V_{CMout}	1.39	1.44	1.49	V	Only for NSI1312D

Differential fail-safe output voltage	$V_{FAILSAFE}$		-1.8	-1.7	V	NSI1312D VDD1 missing
Single-ended fail-safe output voltage	$V_{FAILSAFE}$		0		V	NSI1312S VDD1 missing, REFIN<1.8V
			REFIN-1.8			NSI1312S VDD1 missing, REFIN>1.8V
Single end reference input	REFIN	0.5	VDD2/2	VDD2-1.5	V	Only for NSI1312S. See application description for more details.
Single end reference input impedance	$REFIN_{IN}$		1		GΩ	Only for NSI1312S
Output bandwidth	BW	50	100		kHz	
Power supply rejection ratio	$PSRR_{dc}$		-95		dB	PSRR vs VDD1, at DC
	$PSRR_{ac}$		-95		dB	PSRR vs VDD1, 100mV and 10kHz ripple
	$PSRR_{dc}$		-90		dB	PSRR vs VDD2, at DC
	$PSRR_{ac}$		-80		dB	PSRR vs VDD2 for NSI1312D, 100mV and 10kHz ripple
	$PSRR_{ac}$		-72		dB	PSRR vs VDD2 for NSI1312S, 100mV and 1kHz ripple
Output resistance	R_{OUT}		< 0.2		Ω	
Output limit current	I_{LIM}		±13		mA	
Common-mode transient immunity	CMTI	100	150		kV/μs	Common-mode transient immunity
Timing						
Rising time of OUTP, OUTN	t_r		3.6		μs	
Falling time of OUTP, OUTN	t_f		3.6		μs	
INP, INN to OUTP, OUTN signal delay (50% - 50%)	t_{PD}		3.5	4	μs	
Analog setting time	t_{AS}		0.5		ms	VDD1 step to 5.0 V with VDD2 ≥ 3.0 V, to OUTP, OUTN valid, 0.1% settling

5.2. Power Rating Characteristics

Parameters	*Symbol*	*Max*	*Unit*	*Comments*
Total Power dissipation	P_D	83.6	mW	VDD1=VDD2=5.5V
Power dissipation of high side	P_{D1}	49.5	mW	VDD1=5.5V
Power dissipation of low side	P_{D2}	34.1	mW	VDD2=5.5V

5.3. Typical Performance Characteristics

Unless otherwise noted, test at NSI1312D VDD1 = 5V, VDD2 = 3.3V, INN=GND1=0V, INP = -1.2V to 1.2V, f_{IN} = 1kHz, BW = 10kHz. Characteristics of NSI1312S may be related to REFIN accuracy.

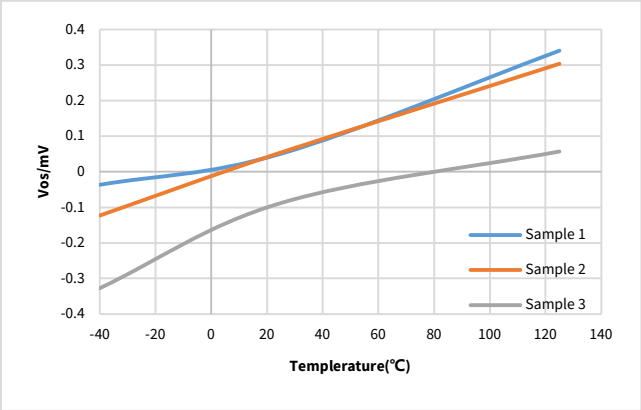


Figure 5. 1 Input Offset Voltage vs Temperature

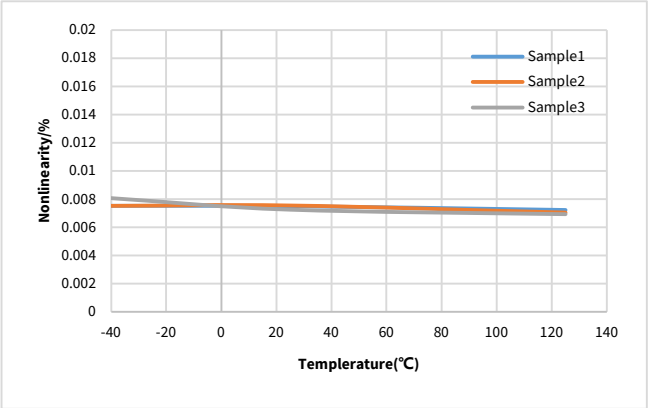


Figure 5. 3 Nonlinearity vs Temperature

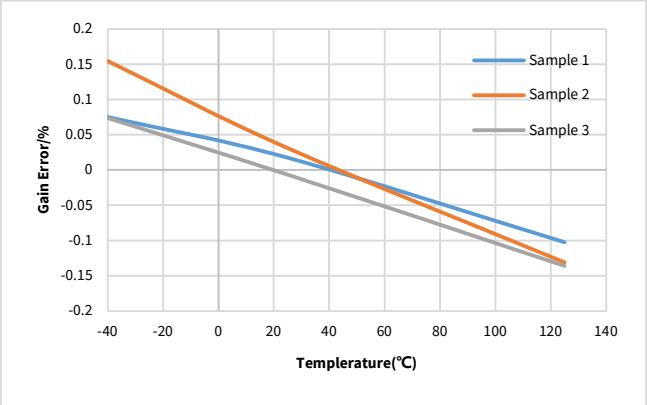


Figure 5. 2 Gain Error vs Temperature

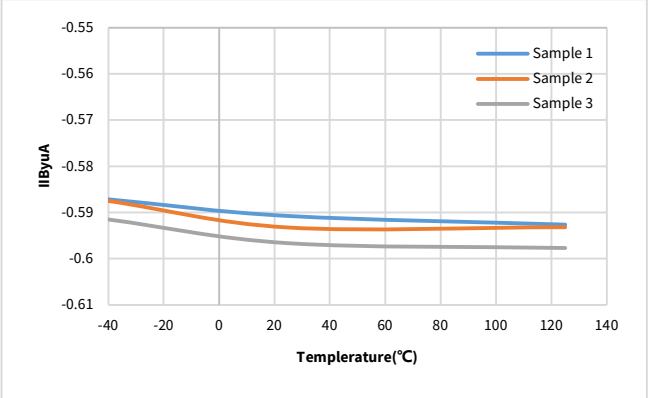


Figure 5. 4 Input Bias Current vs Temperature

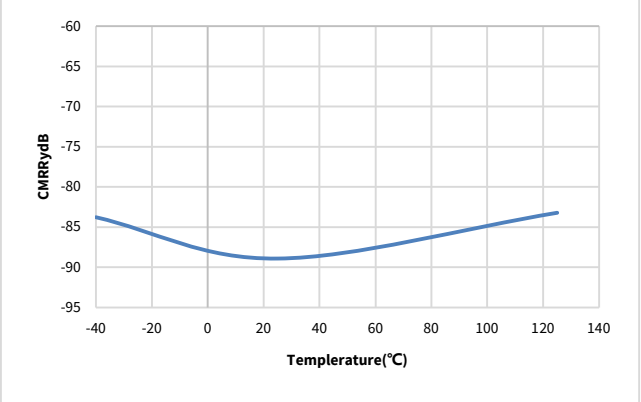


Figure 5. 5 Common-Mode Rejection Ratio vs Temperature

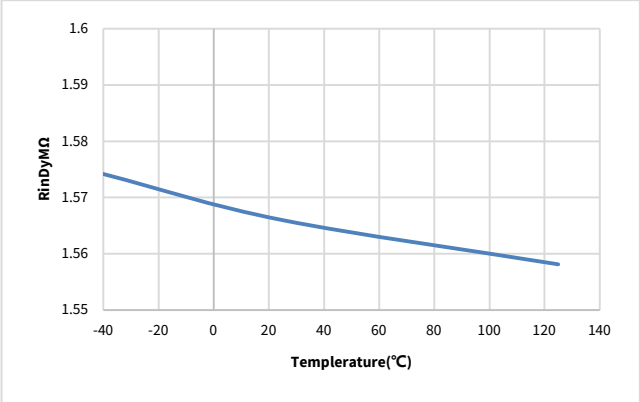


Figure 5. 6 Differential Input Resistance vs Temperature

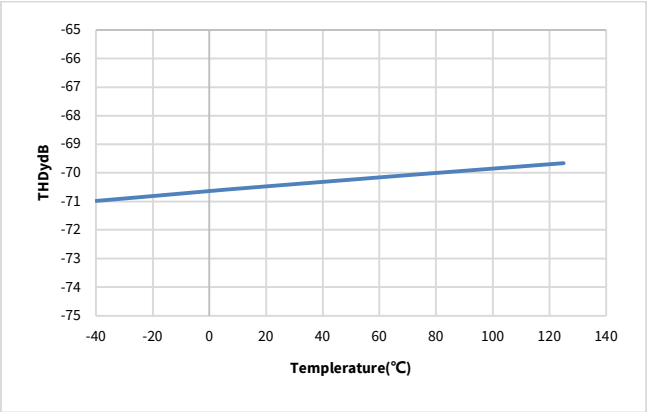


Figure 5. 7 THD vs Temperature

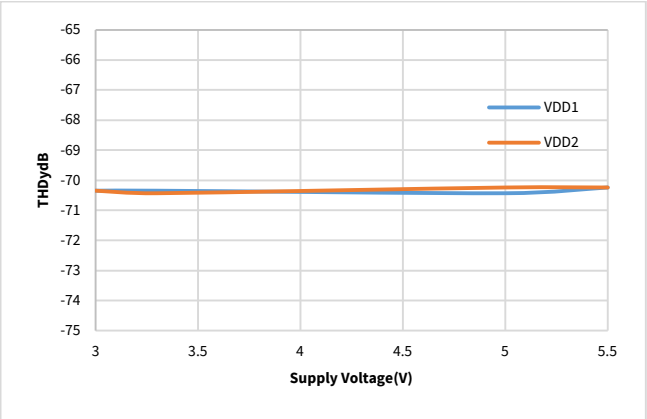


Figure 5. 8 THD vs Supply Voltage

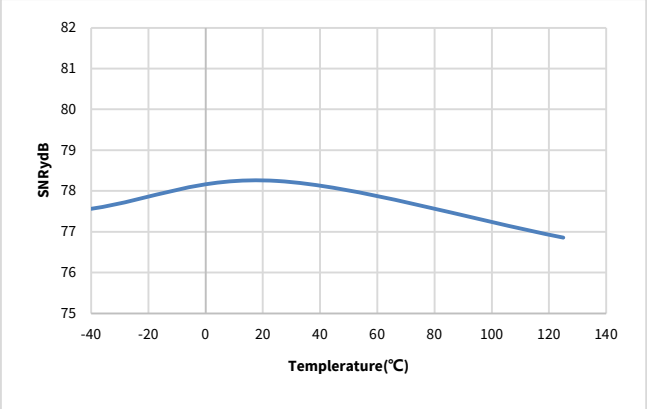


Figure 5. 9 SNR vs Temperature

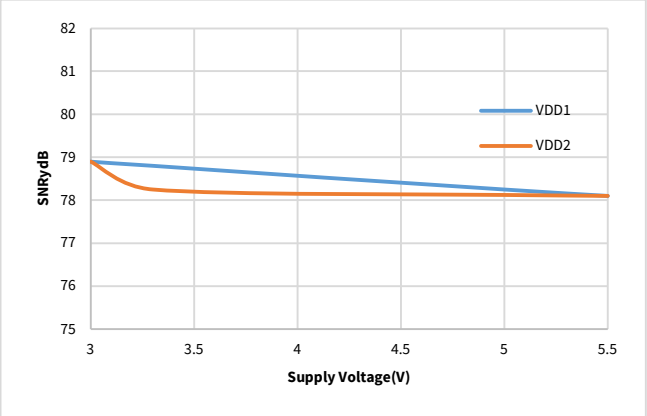


Figure 5. 10 SNR vs Supply Voltage

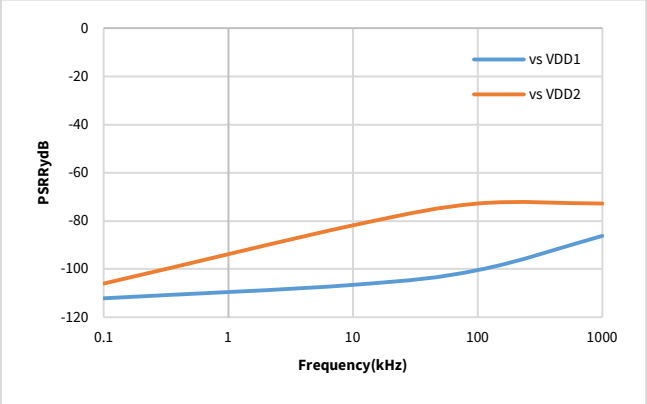


Figure 5. 11 Power-Supply Rejection Ratio vs Ripple Frequency (NSI1312D)

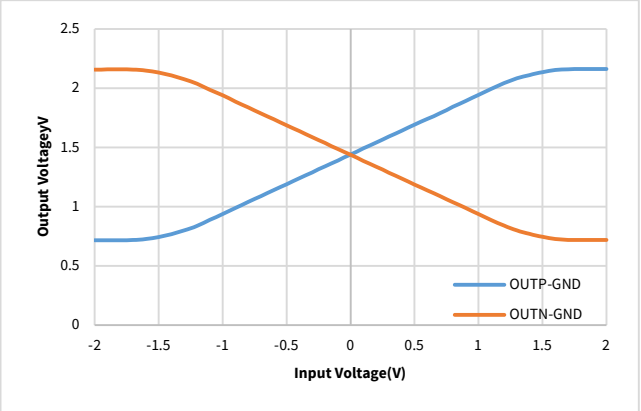


Figure 5. 12 Output Voltage vs Input Voltage (NSI1312D)

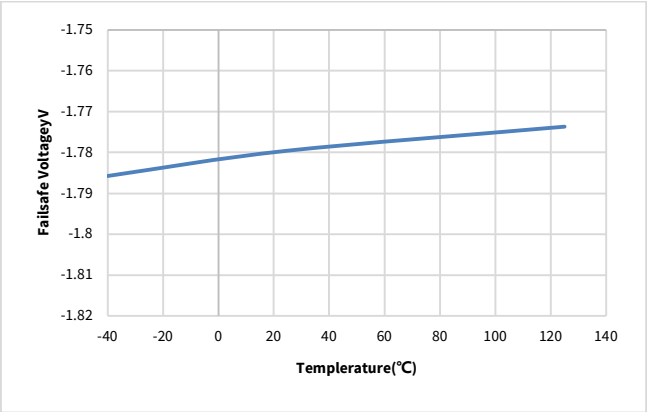


Figure 5. 13 Fail-Safe Output Voltage vs Temperature(NSI1312D)

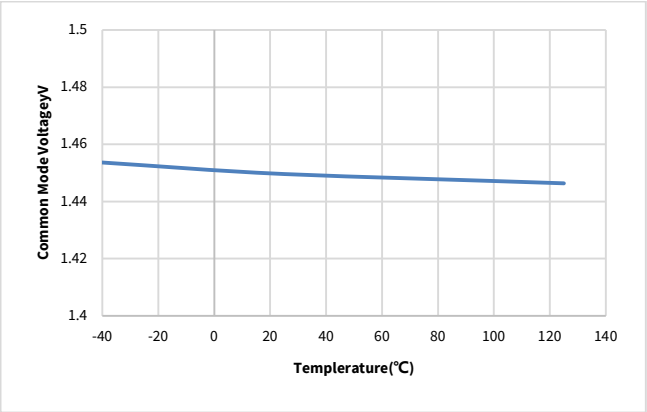


Figure 5. 14 Output Common-Mode Voltage vs Temperature(NSI1312D)

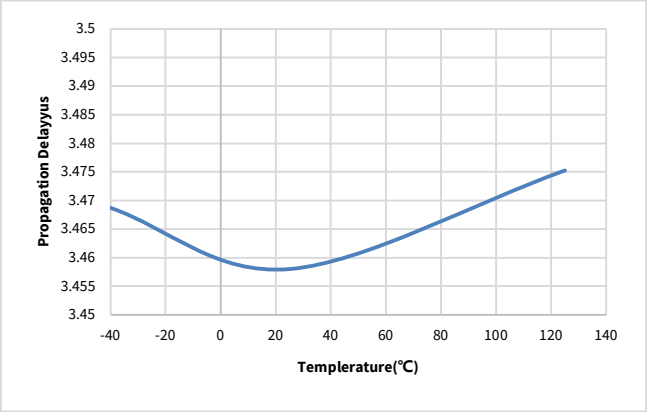


Figure 5. 15 Vin to Vout Delay vs Temperature

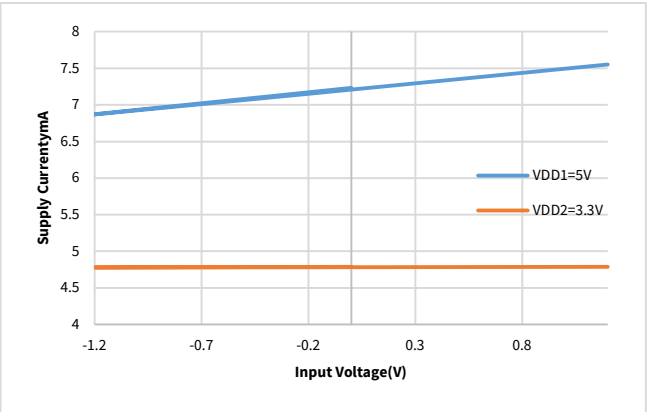


Figure 5. 16 Supply Current vs Input Voltage

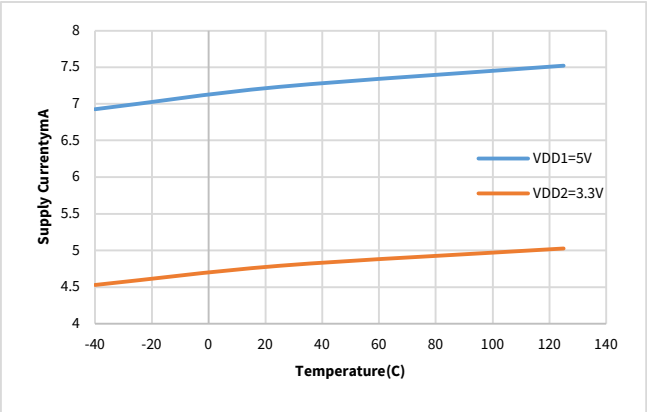


Figure 5. 17 Supply Current vs Temperature

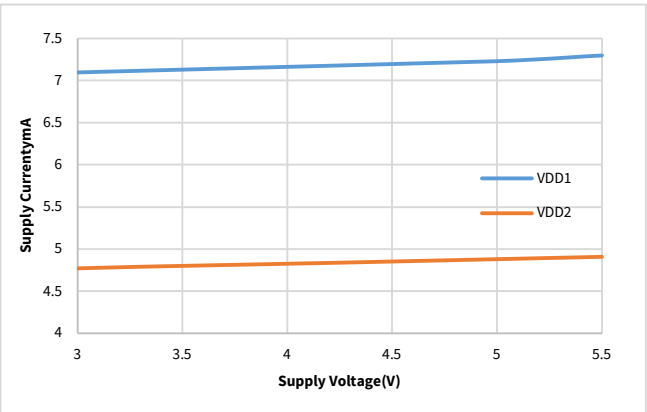


Figure 5. 18 Supply Current vs Supply Voltage

5.4. Parameter Measurement Information

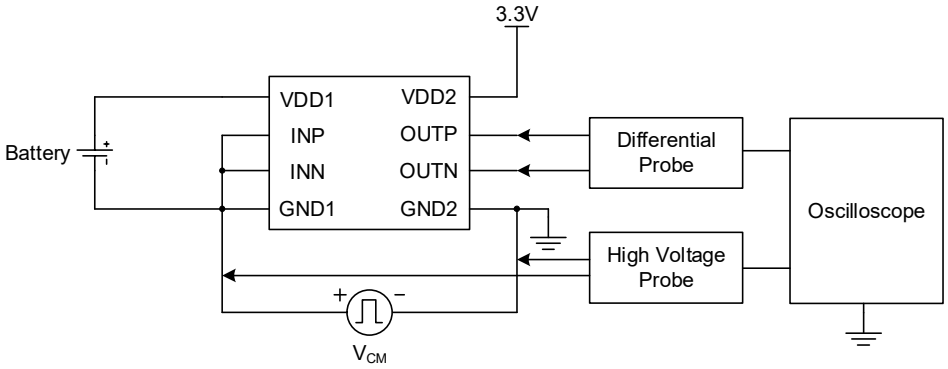


Figure 5.19 Common-Mode Transient Immunity Test Circuit

6. High Voltage Feature Description

6.1. Insulation and Safety Related Specifications

Parameters	*Symbol*	*Value*		*Unit*	*Comments*
		SOW8	*SOP8*		
Minimum External Air Gap (Clearance)	CLR	8	4	mm	Shortest terminal-to-terminal distance through air
Minimum External Tracking (Creepage)	CPG	8	4	mm	Shortest terminal-to-terminal distance across the package surface
Minimum internal gap	DTI	28		µm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600		V	DIN EN 60112 (VDE 0303-11); IEC 60112
Material Group		I			IEC 60664-1

6.2. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
DIN VDE 0110			SOP8	SOW8	
For Rated Mains Voltage ≤ 150Vrms			I to IV	I to IV	
For Rated Mains Voltage ≤ 300Vrms			I to III	I to IV	
For Rated Mains Voltage ≤ 600Vrms			I to II	I to IV	
Climatic Classification			40/125/21	40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	2	
Maximum repetitive isolation voltage		V_{IORM}	990	2121	V_{PEAK}
Maximum working isolation voltage	AC Voltage	V_{IOWM}	700	1500	V_{RMS}
	DC Voltage		990	2121	V_{DC}

Description	Test Condition	Symbol	Value		Unit
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.5 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1485	/	V_{PEAK}
	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	/	3977	V_{PEAK}
Input to Output Test Voltage, Method A. After Environmental Tests Subgroup 1	$V_{IORM} \times 1.3 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1287	/	V_{PEAK}
	$V_{IORM} \times 1.6 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	/	3394	V_{PEAK}
Input to Output Test Voltage, Method A. After Input and /or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1188	2545	V_{PEAK}
Maximum transient isolation voltage	t = 60 sec	V_{IOTM}	4242	7000	V_{PEAK}
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST}=V_{IOSM}\times1.3$	V_{IOSM}	6000	/	V_{PEAK}
	Test method per IEC62368-1, 1.2/50us waveform, $V_{TEST}=V_{IOSM}\times1.6$	V_{IOSM}	/	6250	V_{PEAK}
Isolation resistance	VIO =500V, $T_{amb}=T_s$	R_{IO}	$>10^9$	$>10^9$	Ω
	VIO =500V, 100℃ ≤ T_{amb} ≤ 125℃	R_{IO}	$>10^{11}$	$>10^{11}$	Ω
Isolation capacitance	f = 1MHz	C_{IO}	0.8	0.8	pF
Safety total power dissipation	V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Ps	907	1453	mW
Safety input, output, or supply current	θ_{JA} = 137.7℃/W for SOP8, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃	Is	165	/	mA
	θ_{JA} = 86℃/W for SOW8, V_I = 5.5V, T_J = 150 ℃, T_A = 25 ℃		/	264	mA
Maximum safety temperature		Ts	150	150	℃
UL1577					
Insulation voltage per UL	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	V_{ISO}	3000	5000	V_{RMS}

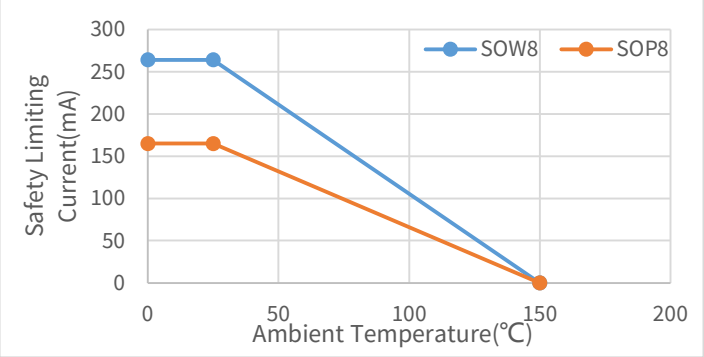


Figure 6.1 NSi1312x Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN VDE V 0884-11

6.3. Regulatory Information

The NSi1312x-DSWVR are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 5000V_{rms} Isolation voltage	Single Protection, 5000V_{rms} Isolation voltage	Reinforce Insulation 2121Vpeak, V_{IOSM}=6250Vpeak	Reinforced insulation
Certificate No.E500602	Certificate No.E500602	File (pending)	CQC20001264940

The NSi1312x-DSPR are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	DIN VDE V 0884-11(VDE V 0884-11):2017-01	Certified by CQC11-471543-2012 GB4943.1-2011
Single Protection, 3000V_{rms} Isolation voltage	Single Protection, 3000V_{rms} Isolation voltage	Basic Insulation 990Vpeak, V_{IOSM}=6000Vpeak	Basic insulation
Certificate No.E500602	Certificate No.E500602	File (pending)	CQC20001264940

7. Function Description

7.1. Overview

The NSI1312 is a cost-effective isolated amplifier with a high input impedance that accept wide range fully-differential input. The fully-differential input is suited to AC or bus voltage monitoring in high voltage applications where isolation is required. The analog input is continuously sampled by a second-order Σ-Δ modulator in the device. With the internal voltage reference and clock generator, the modulator converts the analog input signal to a digital bitstream, as shown in the Figure 7.1. The output of the modulator is transferred by the drivers (called TX in the Functional Block Diagram) across the isolation barrier that separates the isolated input side and output side voltage. The received bitstream and clock are synchronized and processed, as shown in the Functional Block Diagram, by a fourth-order analog filter on the output side and has a differential output. NSI1312 also has single-ended output version, as shown in the Figure 7.2, the received bitstream are processed and presented as a single-ended output with external voltage reference from REFIN pin.

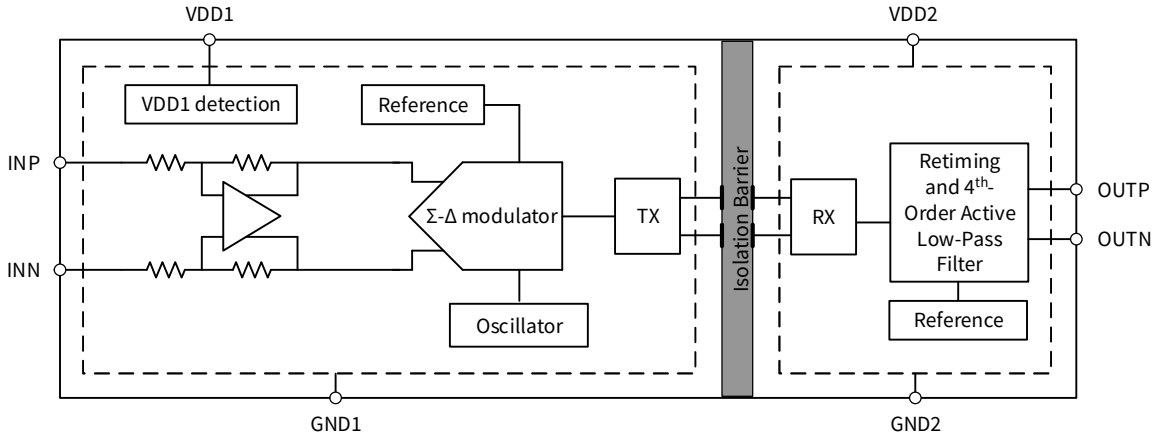


Figure 7.1 Function Block Diagram of Differential Output Version

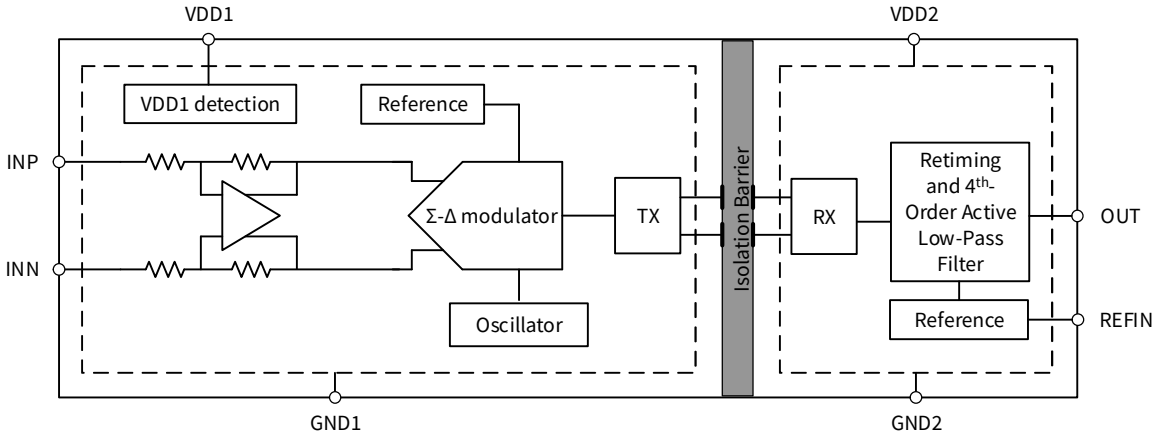


Figure 7.2 Function Block Diagram of Single-ended Output Version

7.2. Analog Input

There are two restrictions on the analog input signals (VINP and VINN).

- If the input voltage exceeds the range AGND – 6 V to AVDD + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turn on.
- The linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

7.3. Analog Output

For linear input range, the analog output of NSI1312 has a fixed gain of 1. If a full-scale input signal is applied to the NSI1312 ($V_{IN} \geq V_{Clipping}$), the differential analog output (V_{OUTP} -V_{OUTN} for NSI1312D and V_{OUT} -REFIN for NSI1312S) will be clipped (typically, 1.44V for positive clipping and -1.44V for negative clipping). The negative clipping differential output waveform is shown in Figure 7.3.

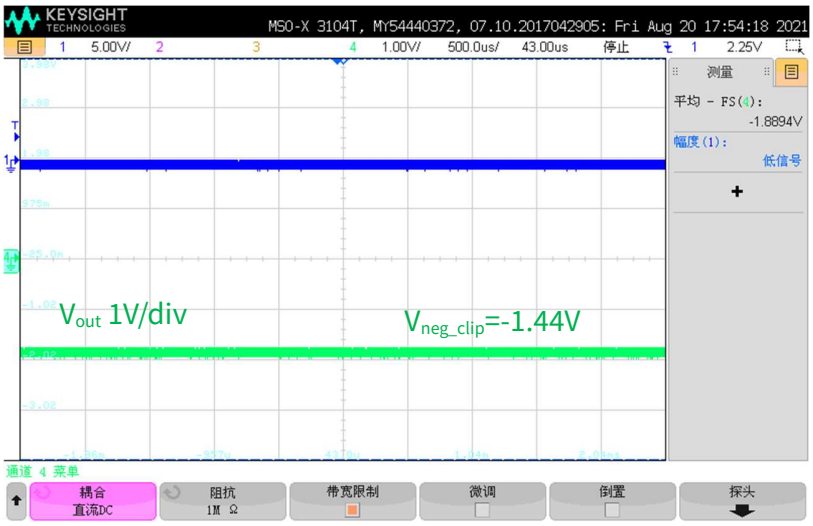


Figure 7.3 Typical negative clipping output

For differential output version (NSI1312D), the differential output pins have a common-mode voltage of 1.44V (typ). The differential output Vout of the NSI1312D is expressed as:

$$Vout = Gain * (V_{INP} - V_{INN})$$

For single-ended output version (NSI1312S), the REFIN pin with high input impedance needs external reference input. The output voltage Vout of the NSI1312S is expressed as:

$$Vout = Gain * (V_{INP} - V_{INN}) + REFIN$$

In addition, NSI1312 integrates some diagnostic measures and offers a fail-safe output to simplify system-level design. The fail-safe output is a negative differential output voltage that does not occur under normal device operation, and it will only be activated when the undervoltage of VDD1 is detected (VDD1< $VDD1_{UV}$). For NSI1312D, the typical failsafe output is -1.8V when VDD1 undervoltage, as is shown in Figure 7.4. For NSI1312S, the typical failsafe output is $V_{failsafe}$= 0V if V_{REF}<1.8V and $V_{failsafe}$= V_{REF}-1.8V if VREF<1.8V when VDD1 undervoltage, as is shown in Figure 7.5.

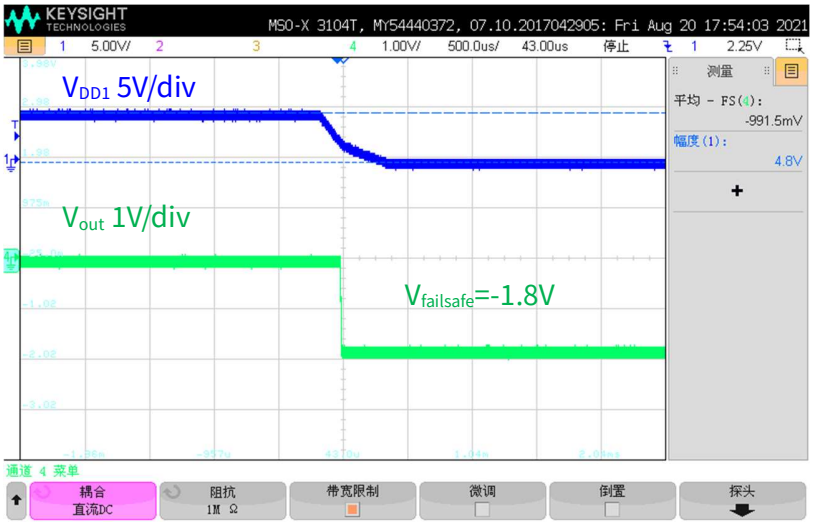
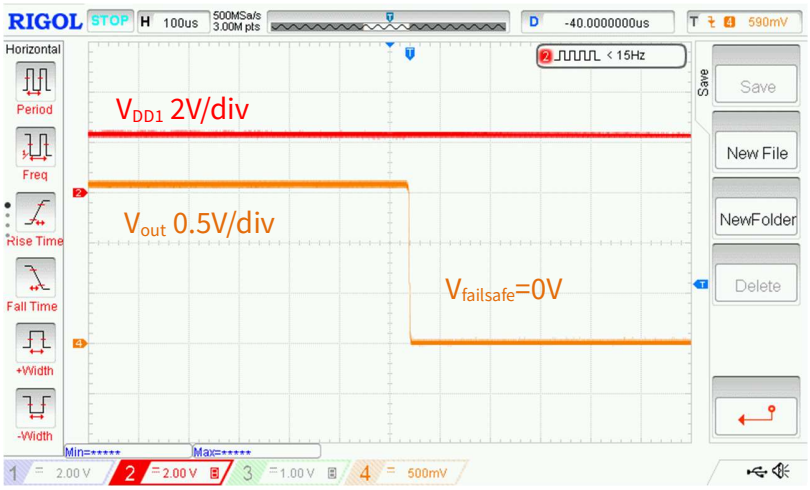
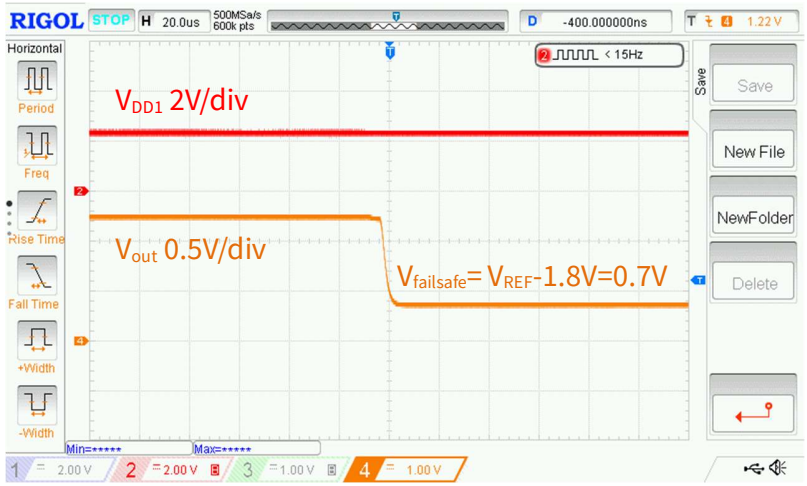


Figure 7.4 Typical Failsafe output when VDD1 undervoltage for NSI1312D



(a) V_{REF}=1.6V (V_{REF}<1.8V)



(b) V_{REF}=2.5V (V_{REF}>1.8V)

Figure 7.5 Typical failsafe output when VDD1 undervoltage for NSI1312S

8. Application Note

8.1. Typical Application Circuit

NSI1312 has an input impedance of up to 1MΩ, and has a wide bidirectional input voltage range as well. These features make NSI1312 ideally suitable for isolated AC and DC voltage sensing applications such as frequency inverters. The typical application circuit is shown in Figure 8.1.

For high voltage side design, the voltage of the frequency inverter is divided by a resistance network, and the divided voltage is applied to the input of NSI1312 through a RC filter to ensure best performance. The characteristics of this filter are dictated by the input topology and sampling frequency of the ADC, customer can adjust the filter design by demand. To reduce extra offset voltage caused by input bias current flowing through R_{sense}, suggest to add R_{FLTP} as below. To reduce extra gain error caused by input resistance of NSI1312, suggest customer to choose smaller resistance, such as R_{sense}≤10kΩ.

About controller side design, for differential output version (NSI1312D), the differential output of the isolated amplifier is converted to a single-ended analog output with an operational-amplifier-based circuit. Suggest to add >1kΩ resistor on the OUTP and OUTN pin to prevent output over-current protection.

For single-ended output version (NSI1312S), REFIN needs external reference input, such as accurate reference IC, LDO and resistor divider network. The single-ended output swing range is GND2+0.3V~VDD2-0.3V. To avoid OUT clamp, REFIN is recommended to be taken as VDD2/2 if need to support ±1.2V analog input range. If the reference is noisy, customer need to add RC filter and adjust the value by demand. The output can be connected to an analog-to-digital converter without signal conditioning. An analog-to-digital converter usually receives the analog output and converts to digital signal for controller processing.

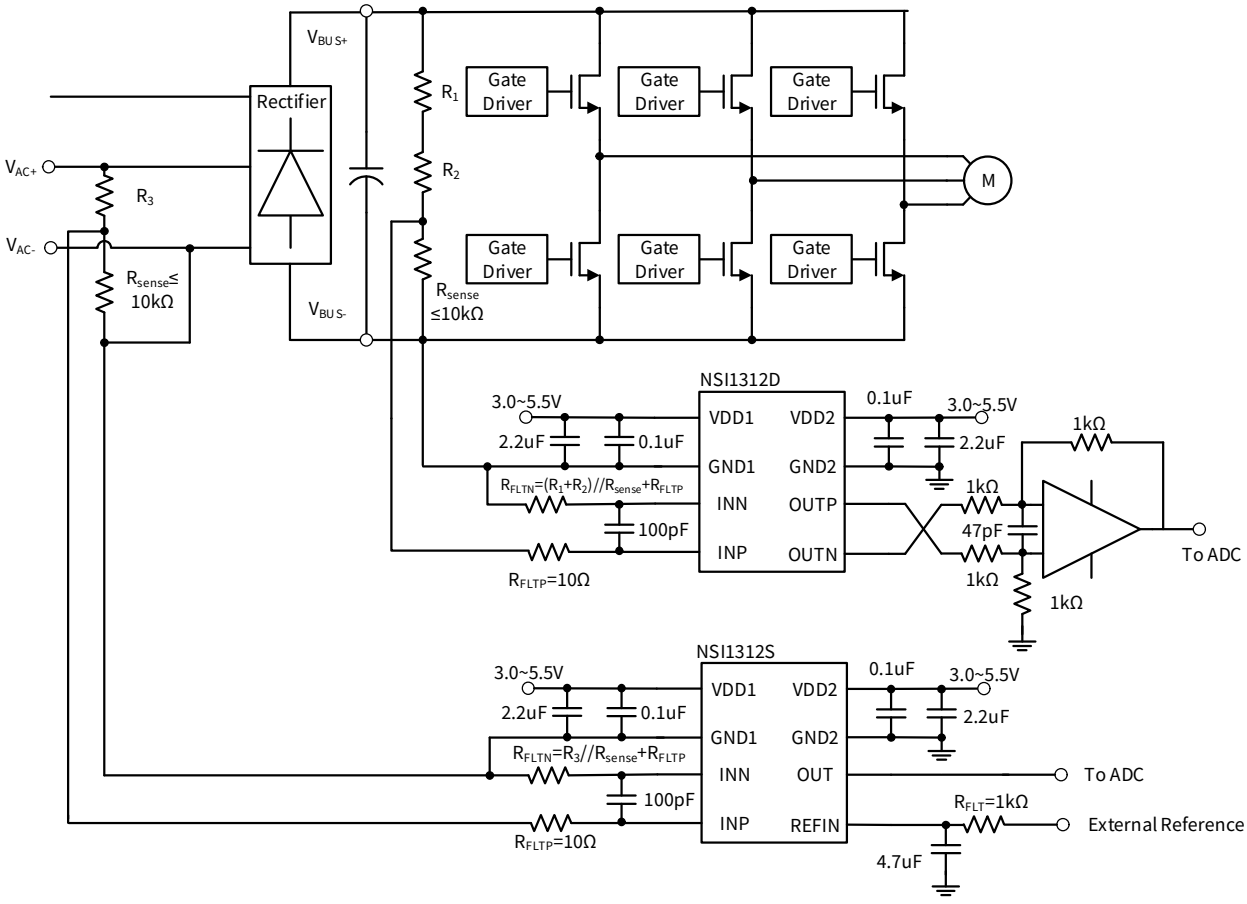


Figure 8.1 Typical application circuit in voltage sensing

8.2. Sense Resistor Selection

There are two other factors should be considered when selecting the sense resistor:

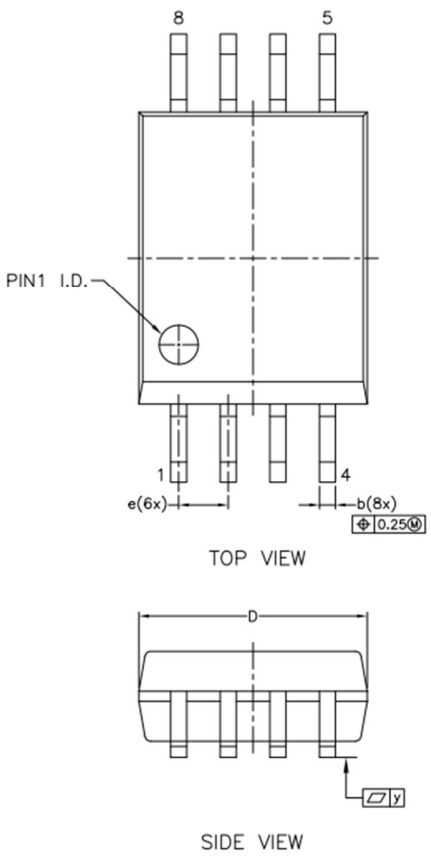
- The voltage-drop on R_{sense} divided by nominal V_{BUS} or V_{AC} must not exceed the recommended linear input voltage range: $V_{IN} \leq$ FSR.
- The voltage-drop on R_{sense} divided by V_{BUS} or V_{AC} in maximum allowed overvoltage condition must not exceed the input voltage that causes a clipping output: $V_{IN} \leq V_{Clipping}$.

8.3. PCB Layout

There are some key guidelines or considerations for optimizing performance in PCB layout:

- NSI1312 requires a 0.1μF bypass capacitor between VDD1 and GND1, VDD2 and GND2. The capacitor should be placed as close as possible to the VDD pin. If better filtering is required, an additional 1~10μF capacitor may be used.
- Kelvin rules is recommended for the connection between shunt resistor to NSI1312. Because of the Kelvin connection, any voltage drops across the trace and leads should have no impact on the measured voltage.
- Place the shunt resistor close to the INP and INN inputs and keep the layout of both connections symmetrical and run very close to each other to the input of the NSI1312. This minimizes the loop area of the connection and reduces the possibility of stray magnetic fields from interfering with the measured signal.

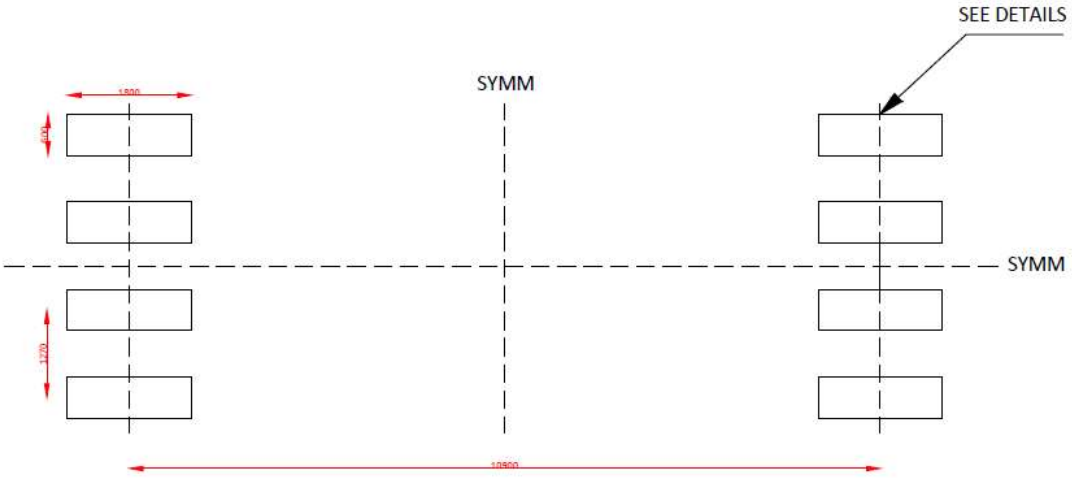
9. Package Information



* CONTROLLING DIMENSION : MM

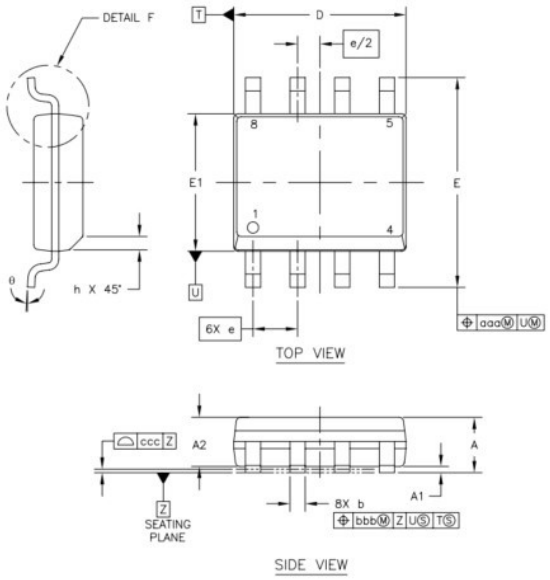
SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

Figure 9.1 SOW8 Package Shape and Dimension in millimeters



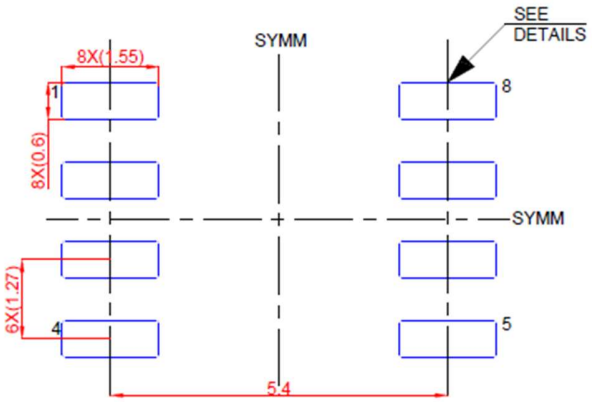
LAND PATTERN EXAMPLE(um)

Figure 9.2 SOW8 Package Board Layout Example

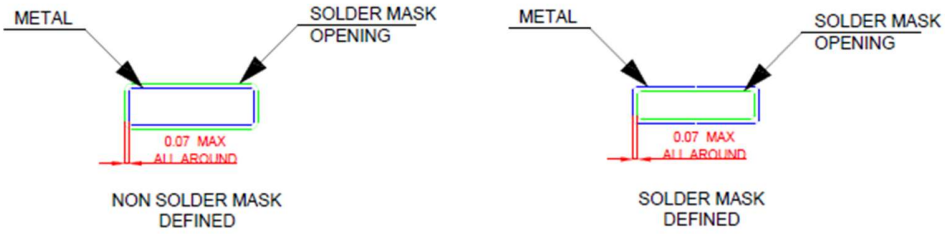


DESCRIPTION	SYMBOL	INCH			MILLIMETER		
		MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	.053		.069	1.35		1.75
STAND OFF	A1	.004		.010	0.10		0.25
MOLD THICKNESS	A2	.049		---	1.25		---
LEAD WIDTH	b	.014		.019	0.35		0.49
L/F THICKNESS	c	.007		.010	0.19		0.25
BODY SIZE	D	.189		.197	4.80		5.00
	E1	.150		.157	3.80		4.00
	E	.228		.244	5.80		6.20
LEAD PITCH	e	.050 BSC			1.27 BSC		
	L	.016		.049	0.40		1.25
	h	.010		.020	0.25		0.50
	θ	0°		7°	0°		7°
	θ1	5°		15°	5°		15°
	θ2	2°	7°	12°	2°	7°	12°
LEAD EDGE OFFSET	aaa	.010			0.25		
LEAD OFFSET	bbb	.010			0.25		
COPLANARITY	ccc	.004			0.10		

Figure 9.3 SOP8 package shape and dimension in millimeters



LAND PATTERN EXAMPLE(mm)



SOLDER MASK DETAILS

Figure 9.4 SOP8 Package Board Layout Example

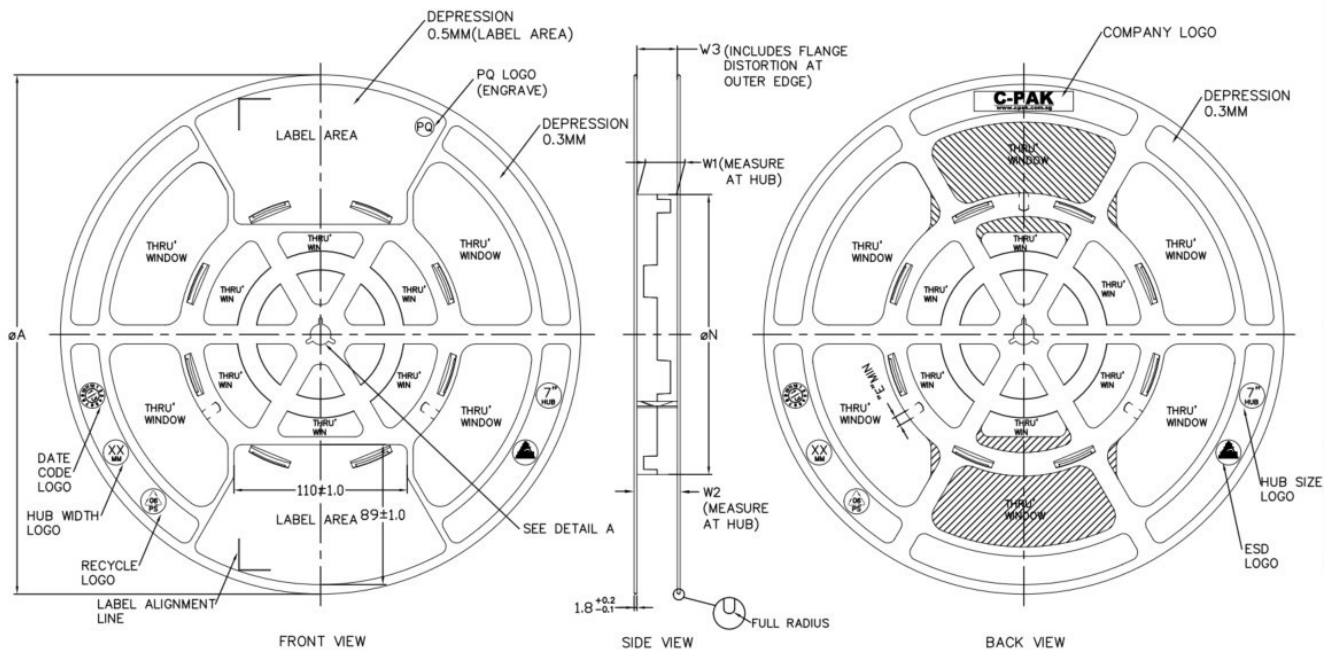
10. Ordering Information

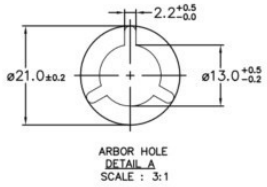
Part No.	*Isolation Rating(kV)*	*Linear Input Range(V)*	*Moisture Sensitivity Level*	*Temperature*	*Automotive*	*Package Type*	*Package Drawing*	*SPQ*
NSI1312D-DSPR	3	-1.2 ~ 1.2	Level-3	-40 to 125℃	NO	SOP8 (150mil)	SOP8	2500
NSI1312S-DSPR	3	-1.2 ~ 1.2	Level-3	-40 to 125℃	NO	SOP8 (150mil)	SOP8	2500
NSI1312D -DSWVR	5	-1.2 ~ 1.2	Level-3	-40 to 125℃	NO	SOP8 (300mil)	SOW8	1000
NSI1312S -DSWVR	5	-1.2 ~ 1.2	Level-3	-40 to 125℃	NO	SOP8 (300mil)	SOW8	1000

11. Documentation Support

Part Number	*Product Folder*	*Datasheet*	*Technical Documents*	*Isolator selection guide*
NSi1312	Click here	Click here	Click here	Click here

12. Tape and Reel Information





PRODUCT SPECIFICATION						
TAPE WIDTH	øA ±2.0	øN ±2.0	W1	W2 (MAX)	W3	E (MIN)
08MM	330	178	8.4	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT INTERFERENCE	5.5
12MM	330	178	12.4	18.4		5.5
16MM	330	178	16.4	22.4		5.5
24MM	330	178	24.4	30.4		5.5
32MM	330	178	32.4	38.4		5.5

SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{9}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{6}	CONDUCTIVE (GENERIC)	BLACK ONLY
E	10^{9} TO 10^{12}	ANTISTATIC (COATED)	ALL TYPES

Figure 12.1 Tape Information

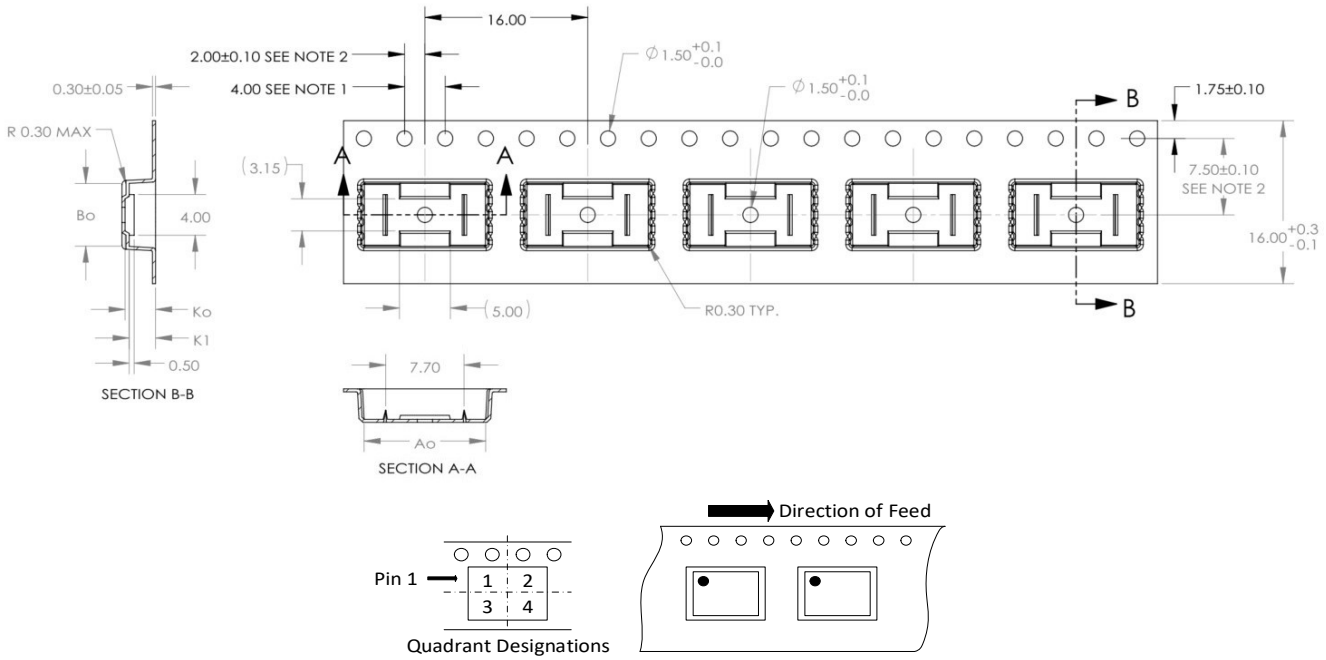
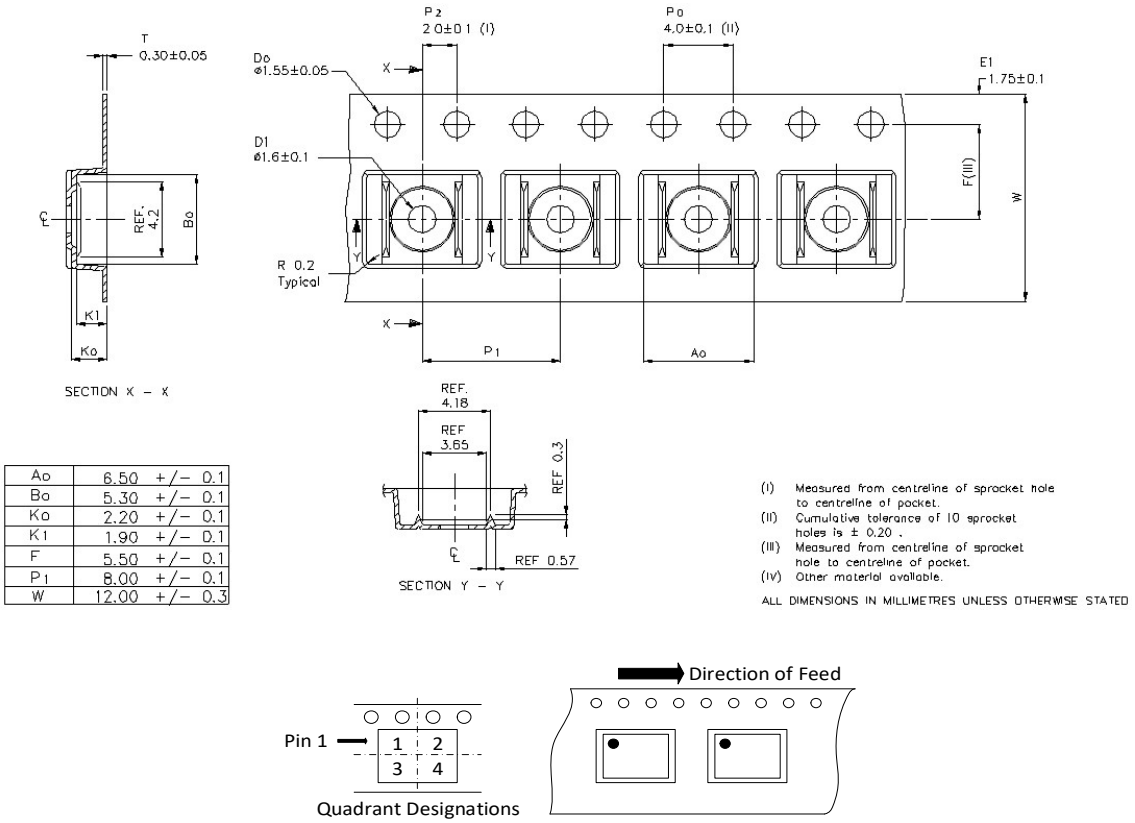


Figure 12.2 Reel Information of SOP8(300mil)



Ao	6.50	+/– 0.1
Bo	5.30	+/– 0.1
Ko	2.20	+/– 0.1
K1	1.90	+/– 0.1
F	5.50	+/– 0.1
P1	8.00	+/– 0.1
W	12.00	+/– 0.3

Figure 12.3 Reel Information of SOP8(150mil)

13. Revision History

Revision	Description	Date
1.0	Initial Release	2022/3/23
1.1	Update REFIN specification in 5.2 and UL certificate number in 6.3 and input filter resistance in Fig 8.1	2022/6/27
1.2	Update V_{CM} range in part 3, $V_{FAILSAFE}$ and $PSRR_{AC}$ specifications in 5.1, the comments of V_{OS}, I_{IB}, E_G and Nonlinearity in 5.1, Figure 5.11~5.14 in 5.3, the standard on which V_{IOSM} test method is based in 6.2, CQC certificate number in 6.3, description for analog output of NSI1312S in 7.3 and input filter resistance in Fig 8.1. Update typeface to Source Sans Pro.	2022/12/24

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