CJC4344

Stereo DAC with 24-Bit, 192 kHz Stereo D/A Converter

Edition	Author	Date	Description
V1.0	By ZN	2015.10	The first draft
V2.0	By TF	2016.8	Parametric change

DESCRIPTION

The CJC4344 is a high quality stereo DAC designed for portable multimedia applications. The CJC4344 is a complete, stereo digital-to-analog output systems including interpolation, multi-bit D/A conversion and output analog filtering in a 10-pin package.

The CS4344 support all major audio data interface formats, and the individual devices differ only in the supported interface format. The device including digital interpolation, third-order multi-bit delta-sigma digital-to-analog conversion, digital de-emphasis filter, analog filters. The CJC4344 is available in a 10-pin TSSOP package in Commercial (-40°C to +85°C) grade.

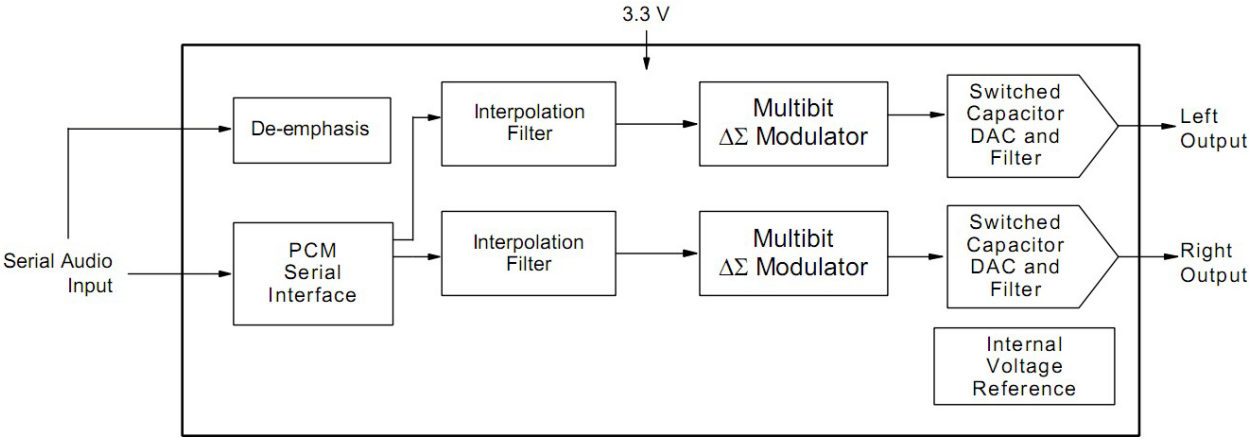
FEATURES

- DAC SNR 92dB (A-weighted)
- THD –87dB
- Architecture
  – Filtered Line-level Outputs
- VCC/2 common mode
- Supports sample rates up to 192 kHz
- 24-bit I²S input
- Small 10-pin TSSOP package

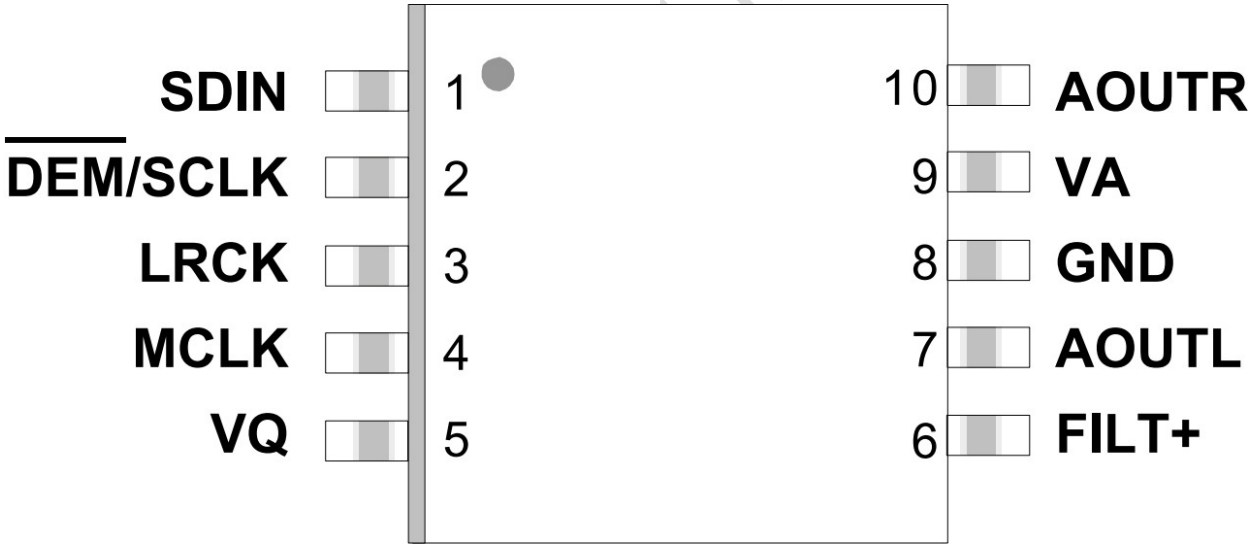
APPLICATIONS

- Handheld gaming
- Mobile multimedia
- DVD players
- digital TVs

BLOCK DIAGRAM



PIN CONFIGURATION



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PIN DESCRIPTION

PIN NO	NAME	I/O	DESCRIPTION
1	SDIN	I	Serial Audio Data Input - Input for two's complement serial audio data.
2	SCLK	I	Serial Clock - Serial clock for the serial audio interface.
3	LRCK	I	Left / Right Clock - Determines which channel, Left or Right, is currently active on the serial audio data line.
4	MCLK	I	Master Clock - Clock source for the delta-sigma modulator and digital filters.
5	VQ	O	Quiescent Voltage - Filter connection for internal quiescent voltage.
6	FILT+	O	Positive Voltage Reference - Positive reference voltage for the internal sampling circuits.
7	AOUTL	O	Analog L Outputs - The full-scale analog line output level is specified in the Analog Characters.
8	GND	I	Ground - Ground reference.
9	VA	O	Analog Power - Positive power supply for the analog and regulator for the digital core logic sections.
10	AOUTR	O	Analog R Outputs - The full-scale analog line output level is specified in the Analog Characters.

CHARACTERISTICS AND SPECIFICATIONS

GND = 0 V; all voltages with respect to ground.(Note1)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DC power supply Analog power	VA	3.0	3.3.	3.6	V
Ambient operating temperature (power applied) -CSZ	TA	-40	-	+85	℃

Note 1: Device functional operation is guaranteed within these limits. Functionality is not guaranteed or implied outside of these limits. Operation outside of these limits may adversely affect device reliability.

ABSOLUTE MAXIMUM RATINGS

GND = 0 V; all voltages with respect to ground.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
DC power supply Low voltage analog power	VA	-0.3		3.6	V
Input current, any pin except supplies	Iin	-		±10	mA
Digital input voltage (Note2) Digital interface	VIN-L	-0.3		VL+0.4	V

Normal operation is not guaranteed at these extremes.

Note 2: The maximum over/under voltage is limited by the input current except on the power supply pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

VA =3.3V, GND=0V, TA=+25ºC, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output						
Output Level		0dBFS	2.7	2.8	2.9	VPP
Master Clock Frequency	fCLK		2		50	MHz
Duty Cycle	dCLK		45		55	%
Input Sample Rate All MCLK/LRCK ratios combined		Fs	30		200	KHz
Load Impedance				3		KΩ
Load Capacitance				100		pF
DAC to Line-Out						
Signal to Noise Ratio	SNR	RL = 10kΩ A-weighted	87	91	92	dB
		RL = 10kΩ Un-weighted	85	89	90	dB
Total Harmonic Distortion Plus Noise	THD+N	RL = 10kΩ	83	85	87	dB
Channel Separation		1kHz	100	114	-	dB
Power Supply Rejection Ratio	PSRR	1kHz	-	44.2	-	dB
Digital Logic Levels						
Input HIGH Level	VIH		0.9VA			V
Input LOW Level	VIL				0.3VA	V
Output HIGH Level	VOH	IOH = 1mA	0.9VA			V
Output LOW Level	VOL	IOL = -1mA			0.1VA	V
Input Capacitance						pF
Input Leakage					+/-0.9	A

FILTER CHARACTERISTICS

(1) (Ta=Tmin~Tmax;VA=3.3V， fs=48kHz)

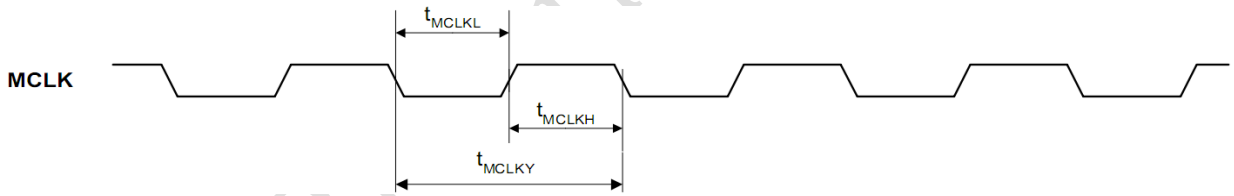
Parameter		Symbol	Min	Typ	Max	Units
DAC Digital Filter:						
Passband (Note3)	±0.01dB −6.0dB	PB	0 -	 22.05	20.0 -	kHz kHz
Stopband (Note3)		SB	24.1			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note4)		GD	-	24.0	-	1/fs
Digital Filter + SCF + CTF:						
Frequency	0~20 kHz	FR	-	±0.02	-	dB
Response	~40 kHz (Note5)		-	±1.0	-	dB

Note 3. The passband and stopband frequencies is proportional to fs.

Note 4. The delay occurred by digital counter, this time is the time from setting the 16/24bit data of input register to analog signal outputting from both channels.

Note 5. fs=96kHz.

SYSTEM CLOCK TIMING

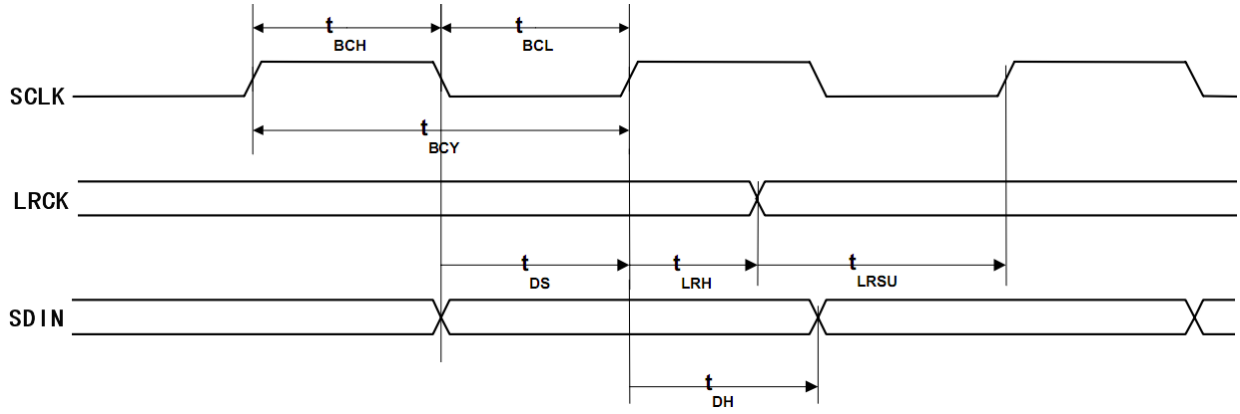


System Clock Timing Requirements

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	TMCLKL	21			ns
MCLK System clock pulse width low	TMCLKH	21			ns
MCLK System clock cycle time	TMCLKY	54			ns
MCLK duty cycle	TMCLKDS	60:40		40:60	ns

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	TMCLKL	10			ns
MCLK System clock pulse width low	TMCLKH	10			ns
MCLK System clock cycle time	TMCLKY	27			ns

AUDIO INTERFACE TIMING



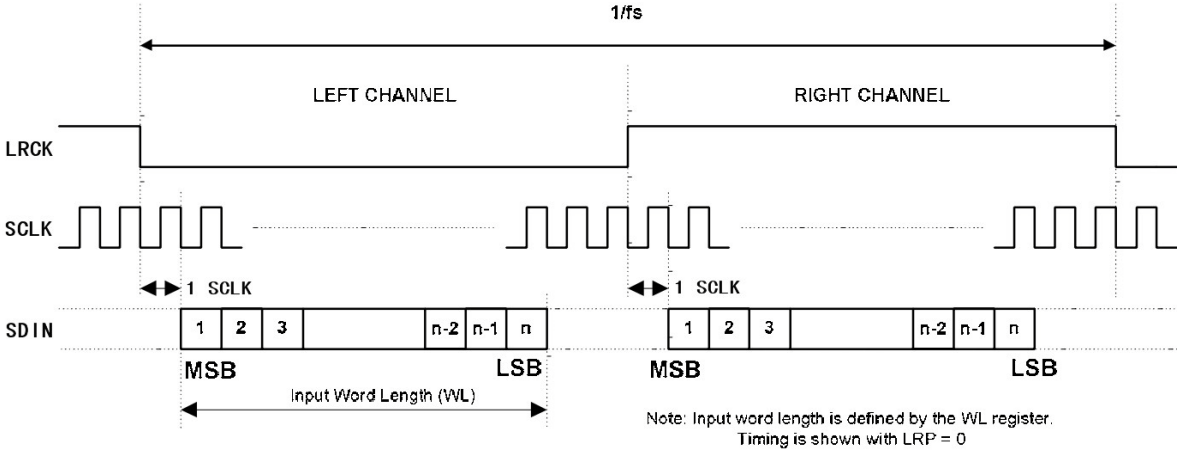
Digital Audio Data Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
SCLK cycle time	tBCY	50			ns
SCLK pulse width high	tBCH	20			ns
SCLK pulse width low	tBCL	20			ns
LRCK set-up time to SCLK rising edge	tLRSU	10			ns
LRCK hold time from SCLK rising edge	tLRH	10			ns
SDIN hold time from SCLK rising edge	tDH	10			ns

Note: SCLK period should always be greater than or equal to MCLK period.

AUDIO INTERFACE FORMAT

In I2S mode, the MSB is available on the second rising edge of SCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, SCLK frequency and sample rate, there may be unused SCLK cycles between the LSB of one sample and the MSB of the next.



I2S Justified Audio Interface (assuming n-bit word length)

SYSTEM CLOCKING

The external clocks, which are required to operate the CJC4344, are MCLK, BICK and LRCK. The master clock (MCLK) should be synchronized with LRCK, but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the Delta-Sigma modulator.

The system clocking have two operate MODE,are AUTO detect MODE and I2C Setting MODE.

The MCLK frequency is detected from the relation between MCLK and LRCK automatically.

AUTO detect MODE

LRCK	MCLK (MHz)									
(kHz)	64x	96x	128x	192x	256x	384x	512x	768x	1024x	1152x
32	-	-	-	-	8.1920	12.2880	-	-	32.7680	36.8640
44.1	-	-	-	-	11.2896	16.9344	22.5792	33.8688	45.1580	-
48	-	-	-	-	12.2880	18.4320	24.5760	36.8640	49.1520	-
64	-	-	8.1920	12.2880-	-	-	32.7680	49.1520	-	-
88.2	-	-	11.2896	16.9344	22.5792	33.8688	-	-	-	-
96	-	-	12.2880	18.4320	24.5760	36.8640	-	-	-	-
128	8.1920	12.2880	-	-	32.7680	49.1520	-	-	-	-
176.4	11.2896	16.9344	22.5792	33.8688	-	-	-	-	-	-
192	12.2880	18.4320	24.5760	36.8640	-	-	-	-	-	-

EXTERNAL SERIAL CLOCK MODE

The CJC4344 will enter the External Serial Clock Mode when 16 low to high transitions are detected on the DEM/SCLK pin during any phase of the LRCK period. When this mode is enabled, the Internal Serial Clock Mode and de-emphasis filter are disabled.

In the External Serial Clock Mode, the CJC4344 will support I²S data up to 24-bit, with data valid on the rising edge of SCLK.

DE-EMPHASIS CONTROL

The device includes on-chip digital de-emphasis. The frequency response of the de-emphasis curve scales with changes in the sample rate, Fs. The de-emphasis error will increase for sample rates other than 44.1 kHz.

When the SCLK/DEM pin is connected to VL (internal SCLK mode), the 44.1 kHz de-emphasis filter is activated. When the SCLK/DEM pin is connected to GND, the de-emphasis filter is disabled.

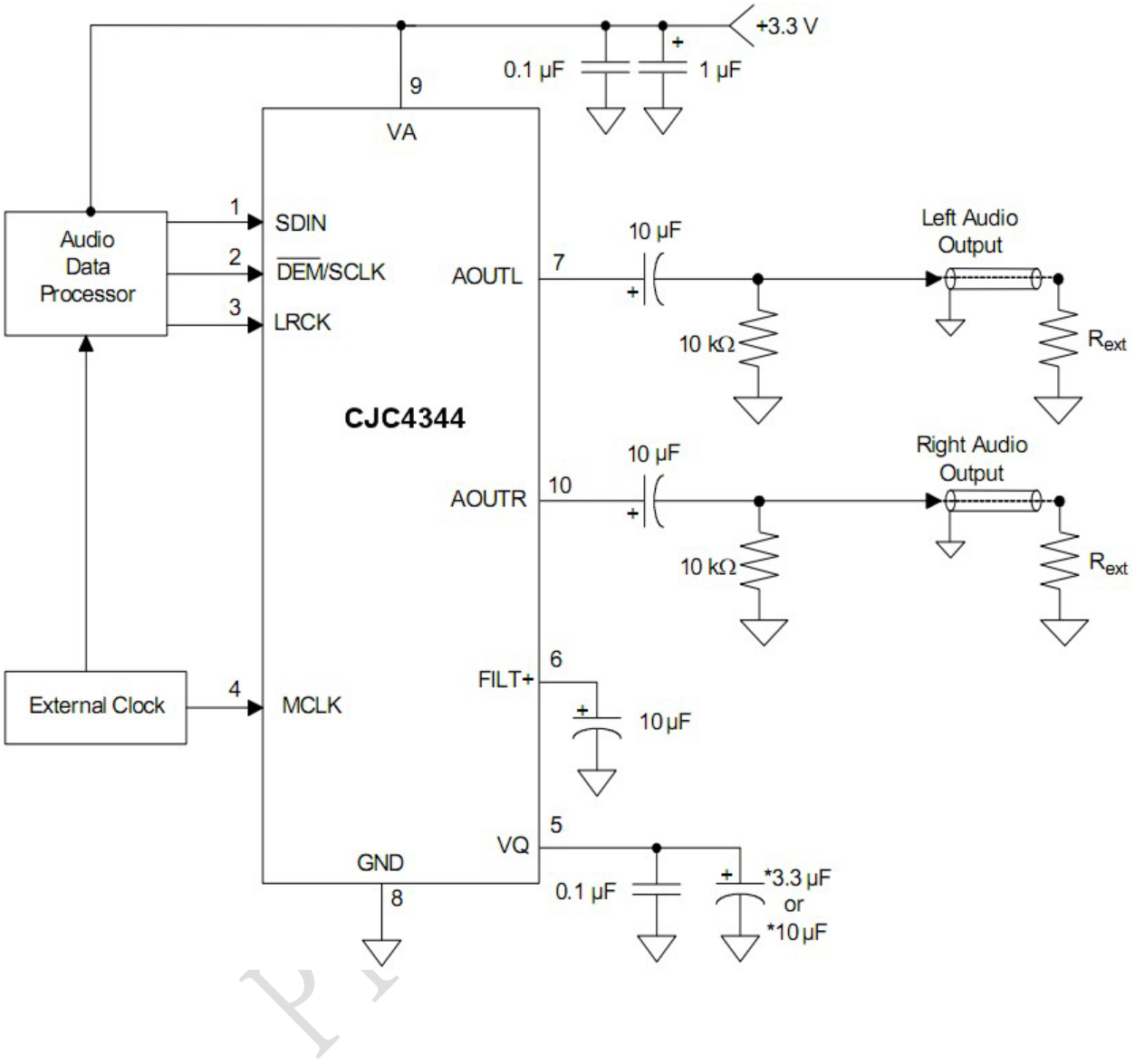
POWER-DOWN SEQUENCE

Follow the power-down sequence below:

1. For minimal pops, set the input digital data (SDIN) to zero for at least 8192 consecutive samples.
2. Remove the MCLK signal without applying any glitched pulses to the MCLK pin.
3. Remove the power supply voltages.

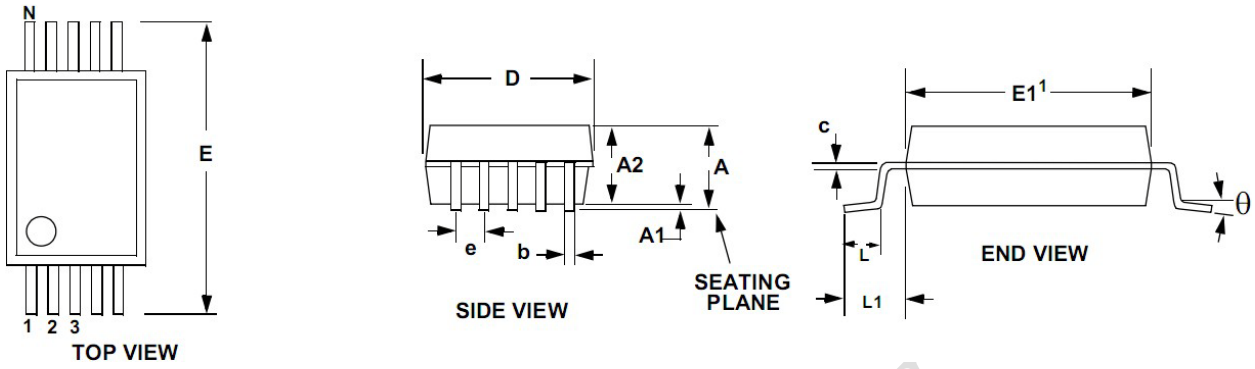
Note: A glitched pulse is any pulse that is shorter than the period defined by the minimum/maximum MCLK signal duty cycle specification and the nominal frequency of the input MCLK signal. A transient may occur on the analog outputs if the MCLK signal duty cycle specification is violated when the MCLK signal is removed during normal operation.

ABSOLUTE MAXIMUM RATINGS SYSTEM DESIGN



PACKAGE INFORMATION

Dimensions 10LD TSSOP (3mm BODY) PACKAGE DRAWING



		INCHES			MILLIMETERS	
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.0433	-	-	1.10
A1	0	-	0.0059	0	-	0.15
A2	0.0295	-	0.0374	0.75	-	0.95
b	0.0059	-	0.0118	0.15	-	0.30
c	0.0031	-	0.0091	0.08	-	0.23
D	-	0.1181BSC	-	-	3.00BSC	-
E	-	0.1929BSC	-	-	4.90BSC	-
E1	-	0.1181BSC	-	-	3.00BSC	-
e	-	0.0197BSC	-	-	0.50BSC	-
L	0.0157	0.0236	0.0315	0.40	0.60	0.80
L1	-	0.0374 REF	-	-	0.95 REF	-
θ	0°	-	8°	0°	-	8°

Controling Dimension is Millimeters

Notes:

1. Reference document: JEDEC MO-187
2. D does not include mold flash or protrusions which is 0.15 mm max. per side.
3. E1 does not include inter-lead flash or protrusions which is 0.15 mm max per side.
4. Dimension b does not include a total allowable dambar protrusion of 0.08 mm max.
5. Exceptions to JEDEC dimension.