WPM9435

P-Channel Enhancement Mode MOSFET

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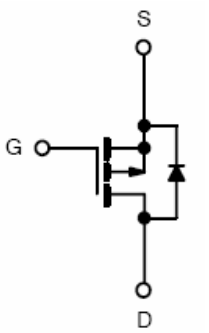
Description

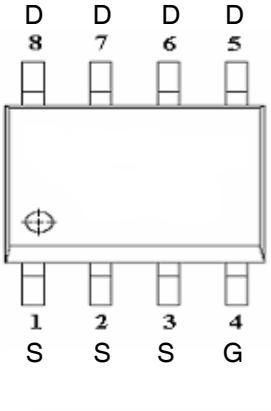
The WPM9435 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density, DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, notebook computer power management and other battery powered circuits where high-side switching.



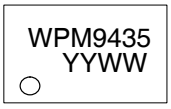
Features

- -30V/-5A,RDS(ON)= 36mΩ@VGS=- 10V
- -30V/-4A,RDS(ON)= 53mΩ@VGS=-4.5V
- Super high density cell design for extremely low RDS (ON)
- Exceptional on-resistance and maximum DC current capability
- SOP – 8P package design



Application

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch



YYWW = Date Code

WPM9435= Specific Device Code

Order information

Part Number	Part Number	Shipping
WPM9435-8/TR	SOP-8P	4000/ Tape&Reel

PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

Absolute Maximum Ratings (TA=25 unless otherwise specified)

Parameter	Symbol			Value	Units
V_{DS}	Drain-Source voltage			-30	V
V_{GS}	Gate-Source Voltage			±20	V
I_D	Continuous Drain Current	Steady-State	TA=25℃	-5.5	A
		Steady-State	TA=70℃	-4.4	
I_{DM}	Pulse Drain Current			-25	A
P_D	Power Dissipation	TA=25℃		2.0	W
		TA=70℃		1.2	
T_J	Operating Junction Temperature Range			-55~150	℃
Tstg	Storage Temperature Range				
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient			62.5	℃/W

Electrical Characteristics

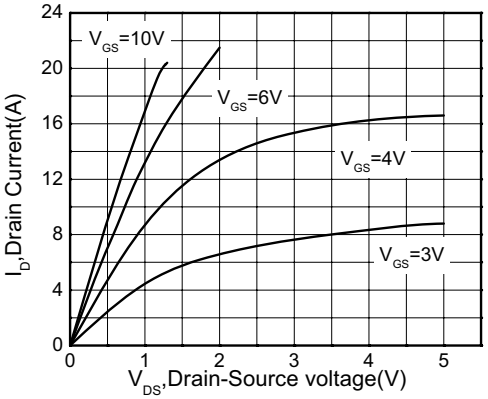
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=-250uA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=-250uA	-1.0	-2.0	-3.0	
Gate Leakage Current	I_{GSS}	V_{DS}=0V,V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-24V,V_{GS}=0V			-1	uA
		V_{DS}=-24V,V_{GS}=0V T_J=85℃			-10	
On-State Drain Current	$I_{D(on)}$	V_{DS}= -5V,V_{GS} =-4.5V	-10			A
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=-10V,I_D=-5.0A		0.036	0.046	Ω
		V_{GS}=-4.5V,I_D=-4.0A		0.053	0.066	
Forward Transconductance	gfs	V_{DS}=- 5V,I_D=-5A		8		S
Diode Forward Voltage	V_{SD}	I_S=-1.3A,V_{GS} =0V		-0.79	-1.5	V

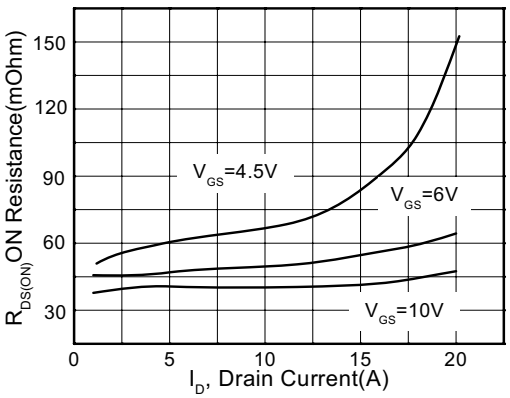
Dynamic

Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V I_D= -3.5A		10	18	nC
Gate-Source Charge	Q_{gs}			1.6		
Gate-Drain Charge	Q_{gd}			3.0		
Input Capacitance	C_{iss}	V_{DS}=-15V,V_{GS}=0V f=1MHz		710		pF
Output Capacitance	C_{oss}			115		
Reverse Transfer Capacitance	C_{rss}			100		
Turn-On Time	$t_{d(on)}$	V_{DD}=-15V,R_L=15Ω I_D≡-1.0A,V_{GEN}=-10V R_G=6Ω		8	18	nS
	t_r			8	18	
Turn-Off Time	$t_{d(off)}$			25	50	
	t_f			25	35	

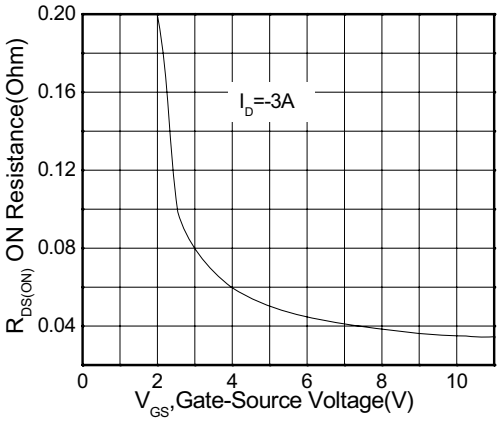
Typical Performance Characteristis



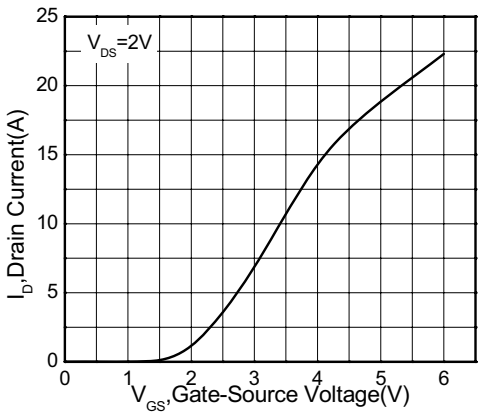
Drain Current VS Drain-Source voltage



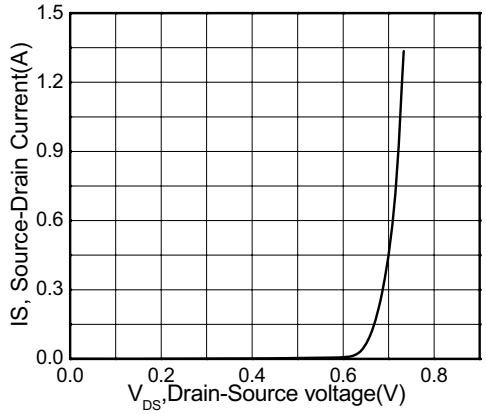
Drain Current vs ON Resistance



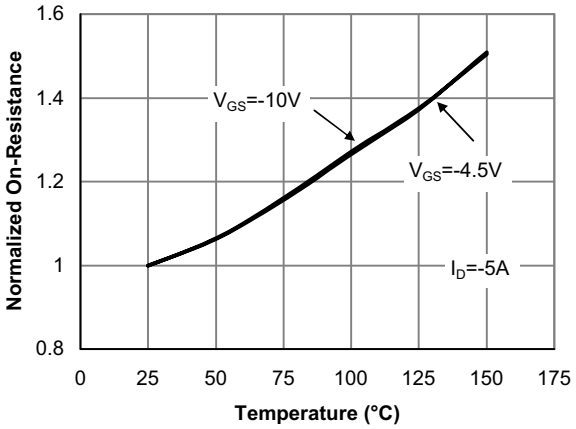
Gate-Source Voltage vs ON Resistance



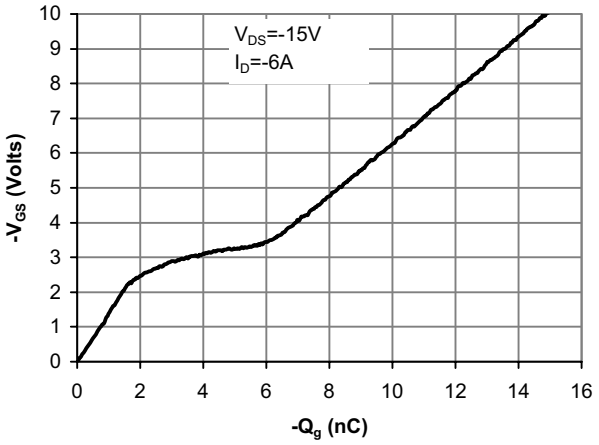
Drain Current VS Gate-Source Voltage



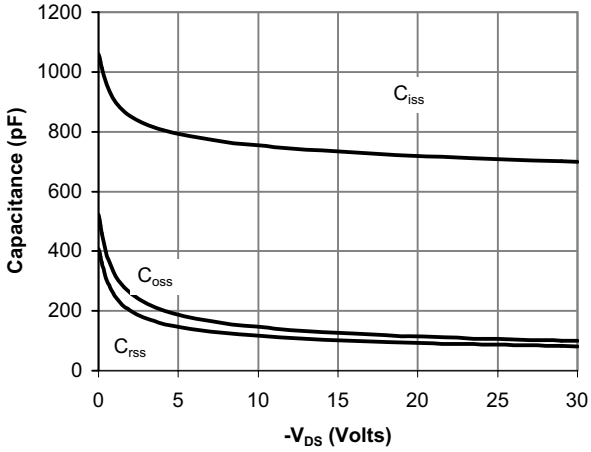
Drain Current VS Source-Drain Current



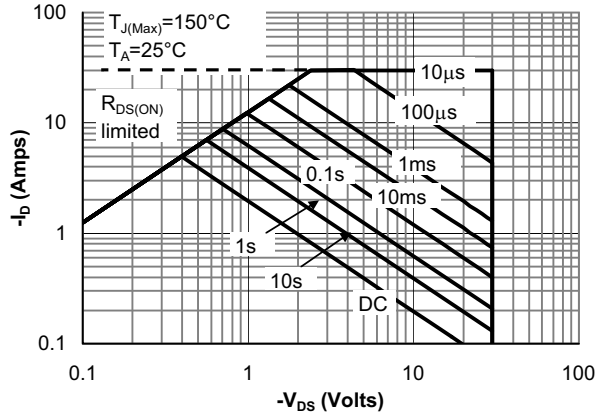
On-Resistance vs. Junction



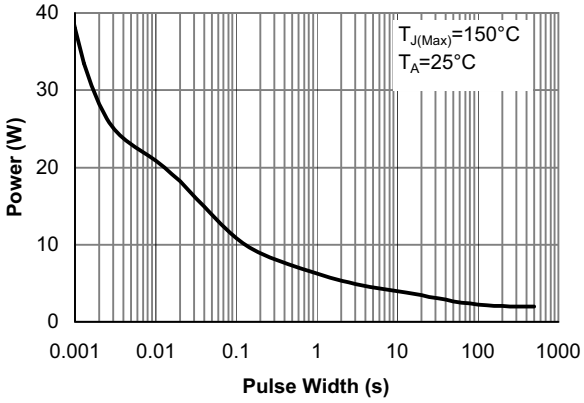
Gate-Charge Characteristics



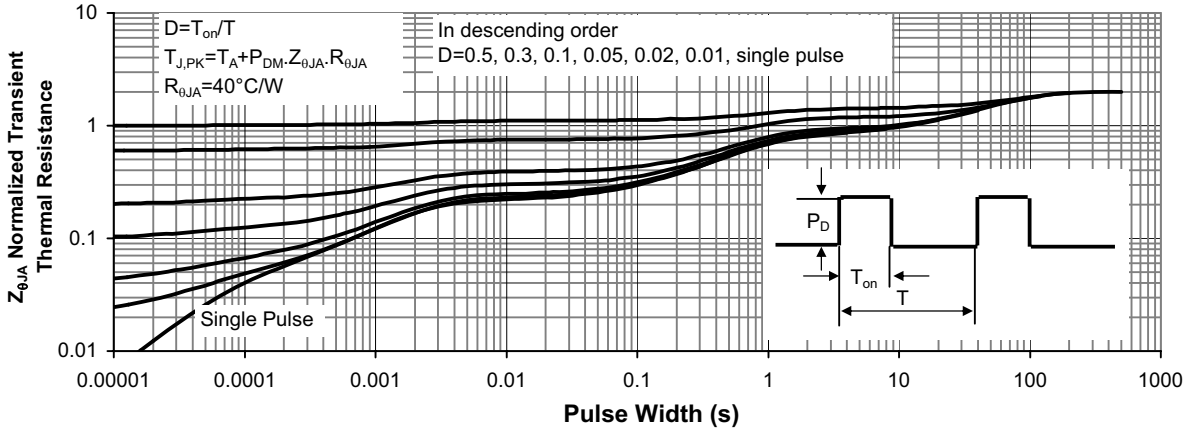
Capacitance Characteristics



Maximum Forward Biased Safe Operating Area (Note E)



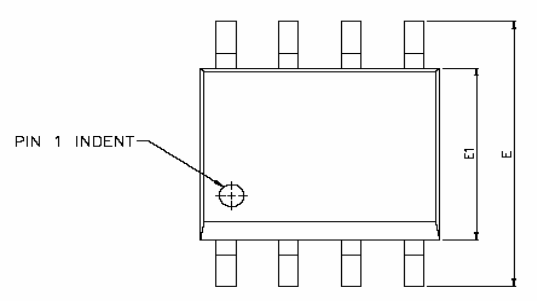
Single Pulse Power Rating Junction-to-Ambient (Note E)

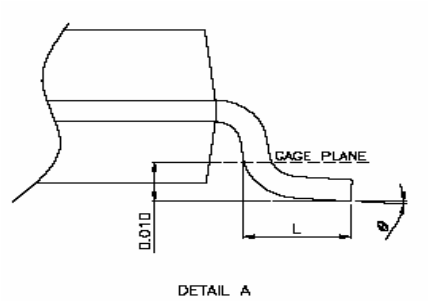


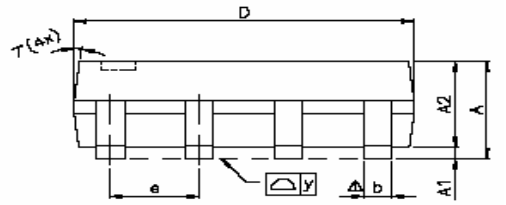
Normalized Maximum Transient Thermal Impedance

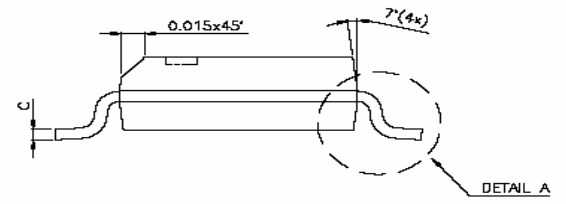
Packaging Information

SOP-8P Package Outline Dimension









SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	——	0.25	0.004	——	0.010
A2	——	1.45	——	——	0.057	——
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	——	1.27	——	——	0.050	——
L	0.38	0.71	1.27	0.015	0.028	0.050
② y	——	——	0.076	——	——	0.003
θ	0°	——	8°	0°	——	8°