NC-Cap/PSR (Primary Side Regulation) CV/CC Power Switch

Features

- ▲ Built-in 650V Power MOSFET
- ▲ NC-Cap/PSR Control
  - ■±4% CC and CV Precision
  - ■Audio Noise Cancellation Control
  - ■Output Short Protection
  - ■Without External Compensation/Filtering capacitor Needed
- ▲ Cable Drop Compensation
- ▲ Multi-Mode Control
- ▲ Low Standby Power Under 70mW
- ▲ Wide VDD Operating Range
- ▲ Cycle-by-Cycle Current Limiting
- ▲ Leading Edge Blanking(LEB)
- ▲ Built-in Soft Start
- ▲ VDD Under Voltage Lockout(UVLO)
- ▲ VDD OVP & Clamp

Applications

- ■ Battery Chargers for cellular phones, cordless phone, PDA, digital cameras, etc.
- ■ Replaces linear transformer and RCC SMPS
- ■ Small power adapter
- ■ AC/DC LED lighting

General Description

ZS292XDM is a high performance, highly integrated DCM(Discontinuous Conduction Mode) Primary Side Regulation (PSR) power switch for offline small power converter applications. It can achieve less than ±4% CV/CC precision.

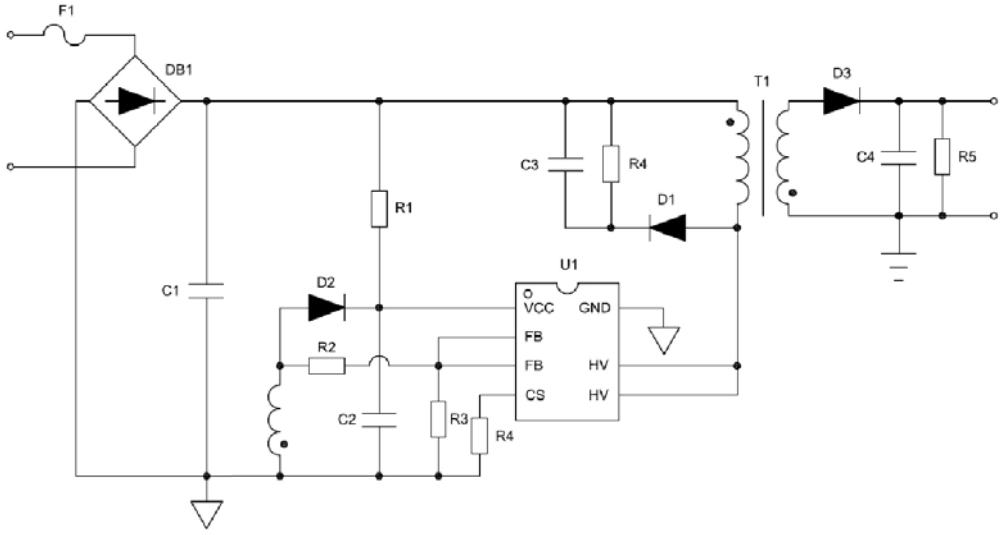
ZS292XDM has built-in NC-Cap/PSR control for CV control, which eliminates external compensation or filtering capacitor. It has built-in cable drop compensation function, which can provide excellent CV performance. The IC uses Multi Mode Control to improve efficiency and reliability and to decrease audio noise energy at light loadings. The IC can achieve less than 70mW standby power.

ZS292XDM has “Output Short Protection”, which can protect the system with large leakage inductance when output is short circuit.

ZS292XDM integrates functions and protections of FB Short Protection, Under voltage Lockout (UVLO), VDD Over voltage Protection (VDD OVP), Soft Start, Cycle-by-cycle Current Limiting (OCP), Pin Floating Protection, VDD Clamping.

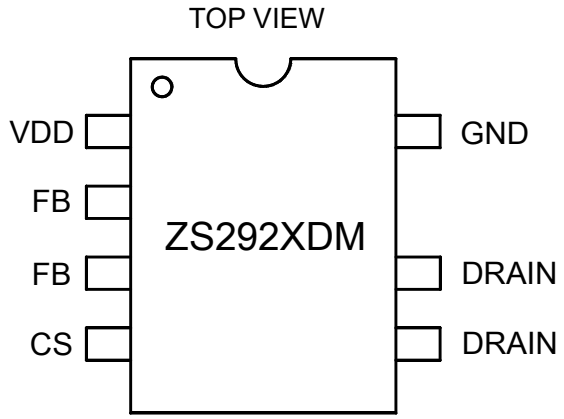
ZS292XDM is available in DIP-7 package.

Typical Application Information



General Information

Pin Configuration



DIP-7

Absolute Maximum Ratings

Parameter	Value
VDD DC Supply Voltage	30V
VDD DC Clamp Current	10mA
Drain Pin	-0.3~650V
FB, CS voltage range	-0.3~7V
Package Thermal Resistance	84℃/W
Maximum Junction Temperature	150℃
Operating Temperature Range	-40~85℃
Storage Temperature Range	-55~150℃
Lead Temperature(Soldering, 10sec)	260℃
ESD Capability, HBM	2KV
ESD Capability, MM	200V

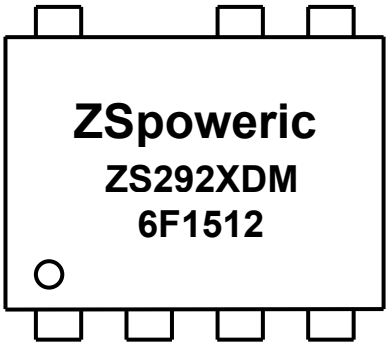
Recommended Operating Conditions

Parameter	Value	Unit
Supply Voltage, VDD	14~24	V
Operating ambient temperature	-40~85	℃
Maximum Switching Frequency	100K	Hz

Pin Description

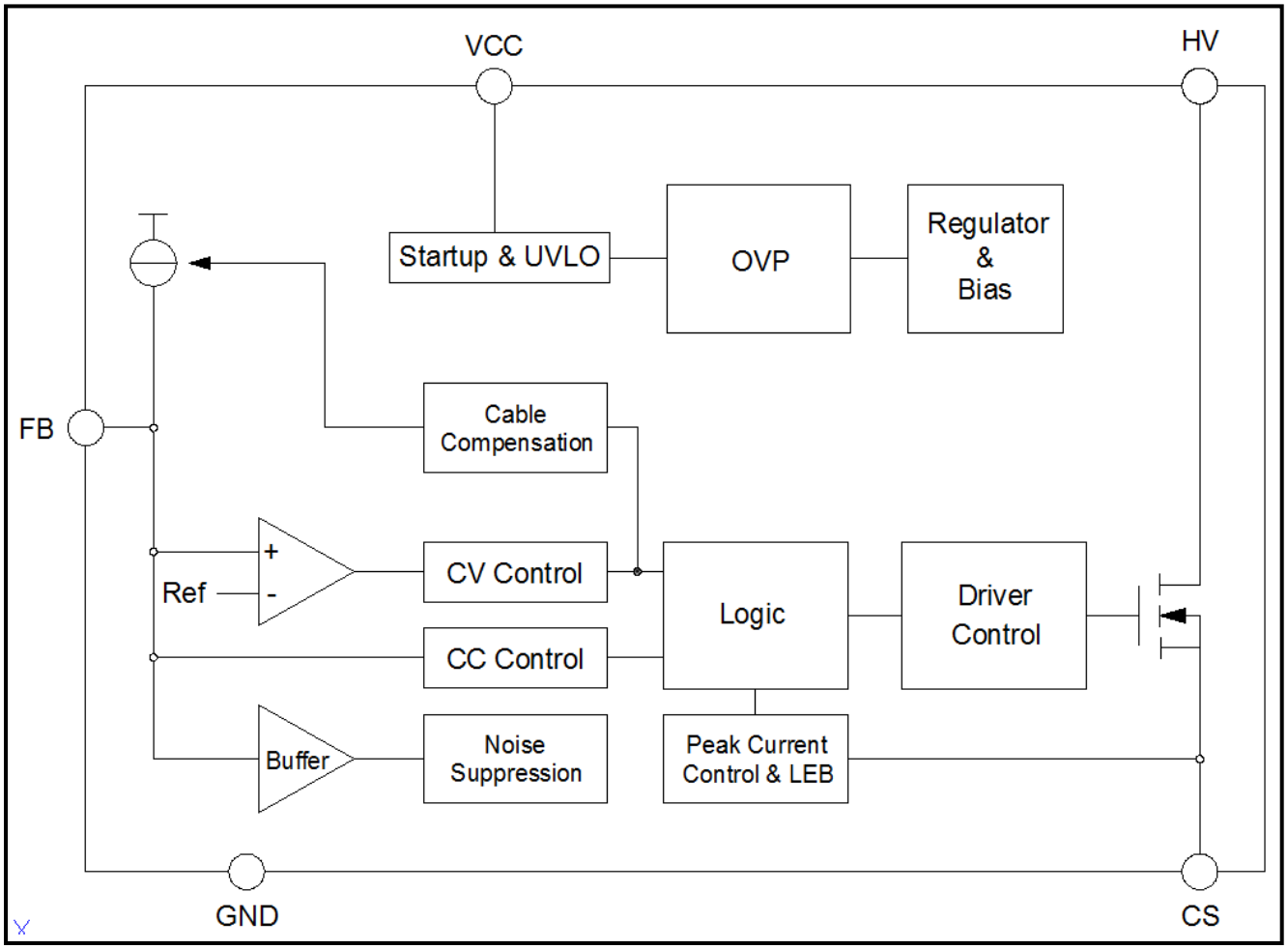
Pin No.	Name	I/O	Function
1	VDD	P	Power supply PIN
2,3	FB	I	System feedback pin. This control input regulates both the output voltage in CV mode and output current in CC mode based on the flyback voltage of the auxiliary winding.
4	CS	I	Current sense pin, connected to sense resistor the MOSFET current signal
5,6	DRAIN	O	Drain of HV MOSFET
7	GND	P	Ground reference pin

Ordering and Marking Information



ZSpoweric：Company Logo
ZS292X：Product name
D：DIP-7
M：Product Version
6F：Internal Code
15：Year Code
12：Week Code

BLOCK DIAGRAM

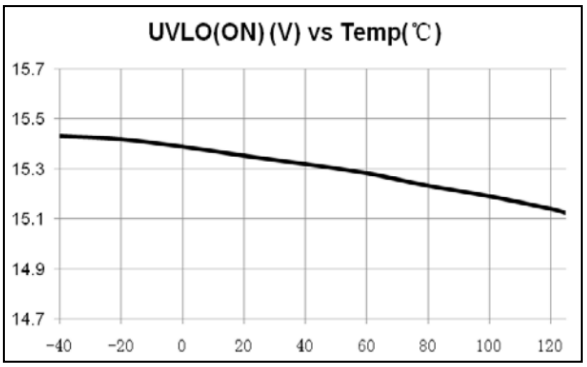


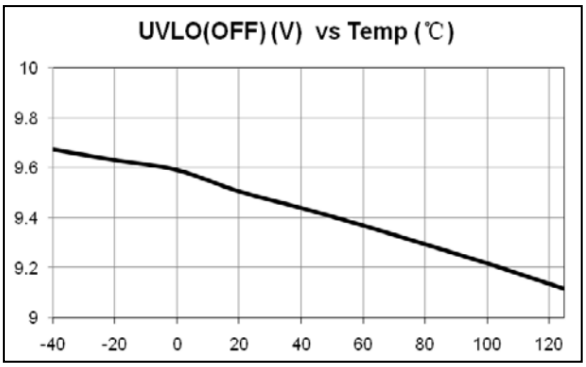
Electrical Characteristics

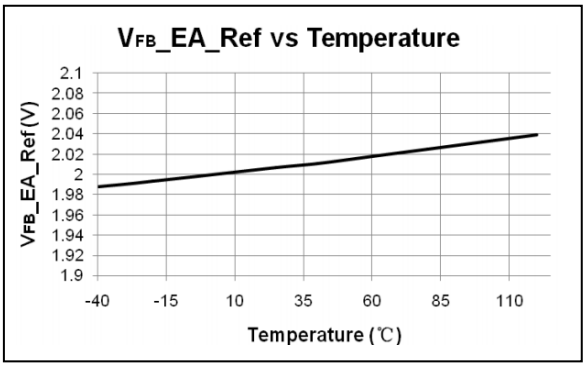
(T_A=25℃, unless otherwise stated, VDD=16.0V)

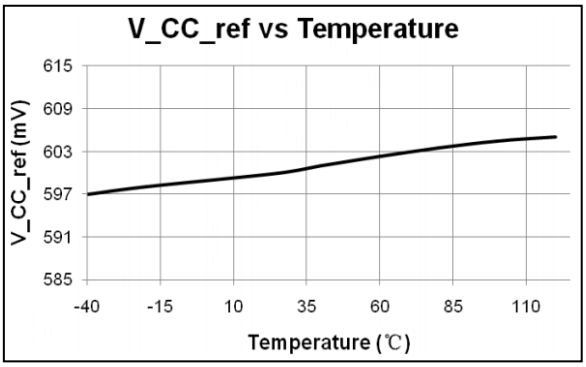
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE (VDD PIN)						
I_Startup	VDD Start up Current	VDD=UVLO(ON)-1V, Measure current into VDD		3	20	uA
I_VDD_OP	Operation Current	VDD=20V		0.8	1.5	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)			17.5		V
UVLO(OFF)	VDD Under Voltage Lockout Enter			7.0		V
V_{DD}_Clamp	VDD Over Voltage Protection trigger	I(V_{DD})=10mA	25	27	29	V
T_Softstart	Soft Start Time			2		mS
Feedback Input Section(FB Pin)						
V_{FB}_EA_Ref	Internal Error Amplifier(EA) reference input		1.97	2.00	2.03	V
V_{FB}_DEM	Demagnetization Comparator threshold			25		mV
T_{min}_OFF	Minimum OFF time			2		uS
T_{max}_OFF	Maximum OFF time			5		mS
T_{FB}_Short	Output Short Circuit Debounce Time			13		mS
T_{CC}/T_{DEM}	Ratio between switching period in CC mode and demagnetization time			2		
I_{Cable}_max	Max Cable compensation current			10		uA
Current Sense Input Section (CS Pin)						
T_blanking	CS Input Leading Edge Blanking Time			500		nS
Vth_OC	Current Limiting Threshold		480	500	520	mV
T_D_OC	Over Current Detection and Control Delay			100		nS
Power MOSFET Section						
BVdss	Drain Source Breakdown Voltage		650			V
Rdson	Static Drain-Source on Resistance	ZS2922DM		4.0		Ω
		ZS2923DM		2.3		
		ZS2924DM		1.5		
Idss	Zero Gate Voltage Drain Current				1	uA
$Td_{(on)}$	Turn-on delay time			9		nS
$Td_{(off)}$	Turn-off delay time			24		nS

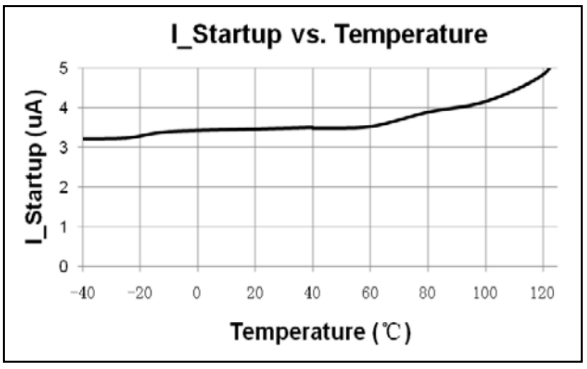
Characterization Plots











Operation Description

ZS292XDM is a high performance, highly integrated DCM (Discontinuous Conduction Mode) Primary Side Regulation (PSR) controller. The built-in high precision CV/CC control makes it very suitable for offline small power converter applications.

PSR Technology Introduction

Assuming the system works in DCM mode, the power transfer function is given by

$$P = \frac{\eta}{2} \times L_m \times I_{pk}^2 \times f_s = V_o \times I_o \qquad \text{(Eq.1)}$$

In the equation above, P is output power, Vo and Io are system output voltage and current respectively, η is system power transfer efficiency, Lm is transformer primary inductance, fs is system switching frequency, Ipk is primary peak current in a switching cycle. The following figure illustrates the waveform in a switching cycle.

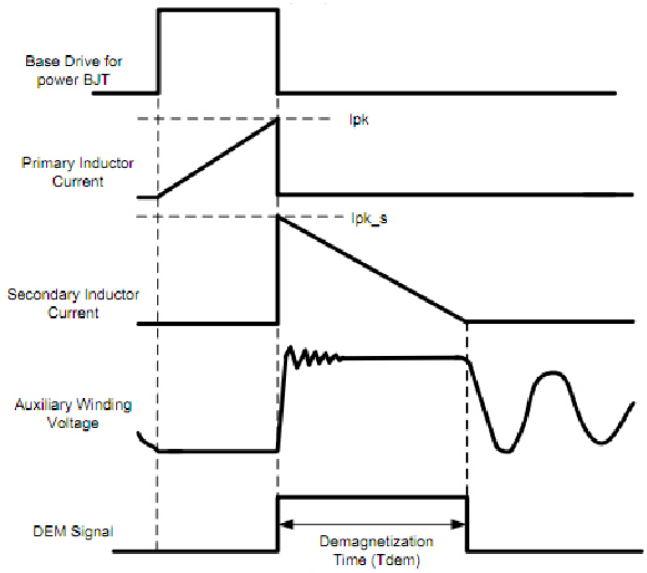


Fig.1

In the figure shown above, the IC generates a demagnetization signal (DEM) in each switching cycle through auxiliary winding. Tdem is demagnetization time for CV/CC control. In DCM mode, Tdem can be expressed as:

$$\frac{V_o}{L_m} \times T_{dem} = \frac{N_s}{N_p} \times I_{pk} \qquad \text{(Eq.2)}$$

In Eq.2, Np and Ns are primary and secondary winding turns respectively.

Combined with Eq.1 and Eq.2, the average output current can be expressed as:

$$I_o = \frac{\eta}{2} \times I_{pk} \times \frac{N_p}{N_s} \times f_s \times T_{dem} \qquad \text{(Eq.3)}$$

CC (Constant Current) Control Scheme

From Eq.3, it can be easily seen that there are two ways to implement CC control: one is PFM (Pulse Frequency Modulation), the control scheme is to keep Ipk to be constant, let the product of Ts and Tdem (fs×Tdem) to be a constant. In this way, Io will be a value independent to the variation of Vo, Lm and line input voltage. Another realization method is PWM duty control, the control scheme is to keep fs to be constant, let the product of Tdem and Ipk (Tdem×Ipk) to be a constant, in another words, by modulating system duty cycle to realize a constant Io independent to the variation of Vo, Lm and line voltages.

ZS292XDM adopts PFM for CC control, the product of Ts and Tdem is given by

$$f_s \times T_{dem} = 0.5 \qquad \text{(Eq.4)}$$

CV (Constant Voltage) Control Scheme

CV control should sample the plateau of auxiliary winding voltage in flyback phase, as shown in Fig.1 The CV control has many implementations, for example, PWM, or PFM, or a combination of both one. In ZS292XDM, the CV control adopts proprietary multi mode control, as mention below.

◆Startup Current / Startup Control / Operating Current

Startup current of ZS292XDM is designed to be very low (Typically 3uA) so that VDD could be charged up above UVLO(ON) threshold level and device starts up quickly. The operating current in ZS292XDM is as small

as 0.5mA (Typical). The small operating current results in higher efficiency and reduces the VDD hold-up capacitance requirement.

◆PSR Controller Description

±4% Precision CV/CC Performance

ZS292XDM can achieve less than ±4% variation of CC/CV precision due to the built-in CV accuracy improvement and CC line and load compensation, as shown in Fig.2.

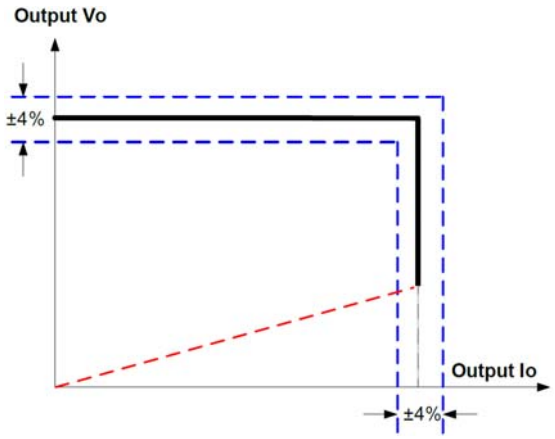


Fig.2.

Cable Drop Compensation

ZS292XDM has a built-in cable voltage drop compensation block which can provide a constant output voltage at the end of the cable over the entire load range in CV mode.

Multi-Mode PSR Control for High Reliability, High Efficiency

Conventional pure PFM controlled PSR system may suffer transformer saturation issue when heavy loading. In ZS292XDM, a multi-mode control is adopted to suppress this issue, Around the full load, the system operates in PWM+PFM mode, which improve the system reliability. Under normal to light load conditions, the

IC operates in PFM mode to achieve excellent regulation and high efficiency.

Soft Start

ZS292XDM features an internal 2mS soft start that slowly increases the threshold of cycle-by-cycle current limiting comparator during startup sequence. Every Startup process is followed by a softstart activation.

Leading Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sensing resistor. To avoid premature termination of the switching pulse, an internal leading edge blanking circuit is built in. During this blanking period (500nS, typical), the cycle-by-cycle current limiting comparator is disabled and cannot switch off the GATE driver.

Minimum and Maximum OFF Time

In ZS292XDM, a minimum OFF time (Typically 2uS) is implemented to suppress ringing when GATE drive is pull off. The maximum OFF time in ZS292XDM is typically 5mS, which provides a large range for frequency reduction. In this way, a low standby power of 70mW can be achieved.

Pin Floating Protection

In ZS292XDM, if pin floating situation occurs, the IC is designed to have no damage to system.

Auto Recovery Mode Protection

As shown in Fig.2, once a fault condition is detected, switching will stop. This will cause VDD to fall because no power is delivered form the auxiliary winding. When VDD falls to UVLO(off) (typical 7.0V), the protection is reset and the operating current reduces to the startup current, which causes VDD to rise, as shown in Fig.3. However, if the fault still exists, the system will experience the above mentioned process. If the fault has gone, the system resumes normal operation. In this manner, the auto restart can alternatively enable

and disable the switching until the fault condition is disappeared.

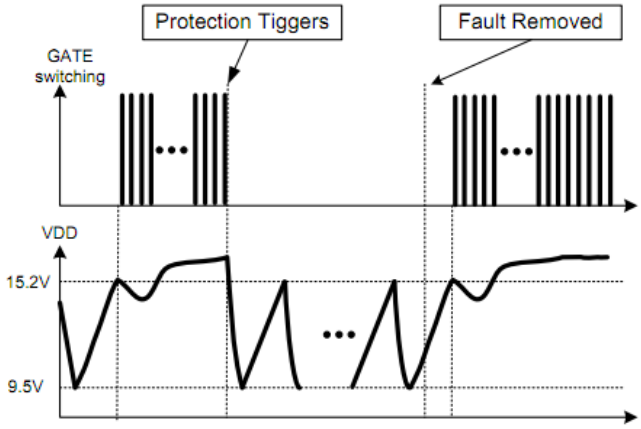


Fig.3

VDD OVP (Over Voltage Protection)

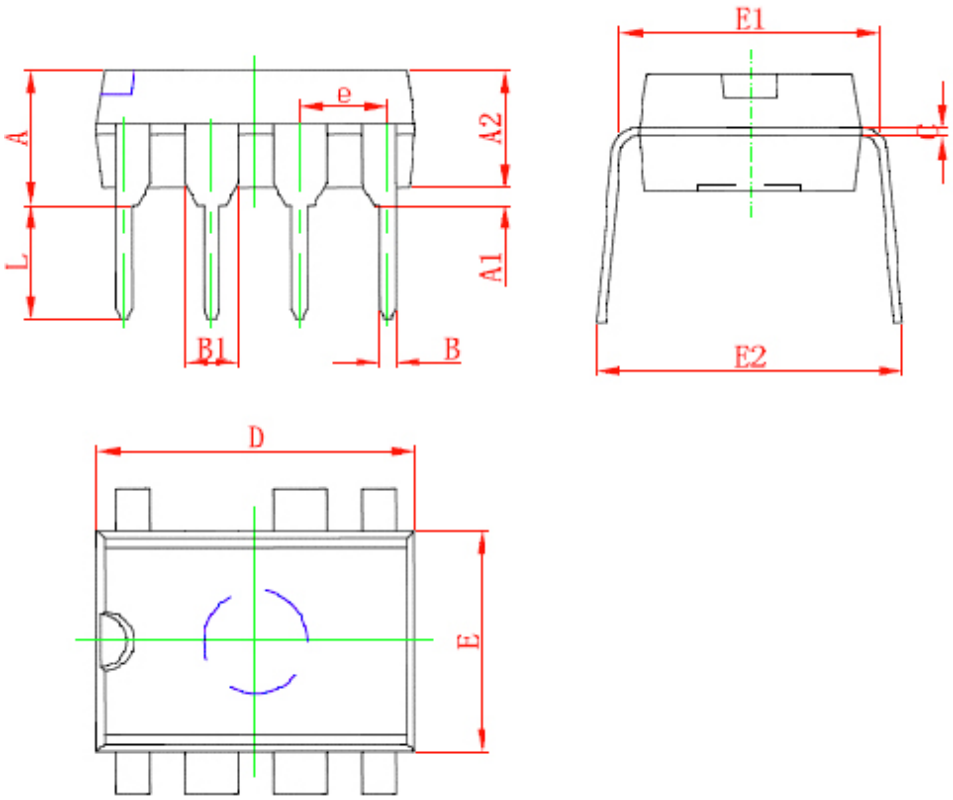
VDD OVP is implemented in ZS292XDM and it is a protection of auto-recovery mode.

VDD OVP (Over Voltage Protection)

ZS292XDM has a soft totem-pole gate driver with optimized EMI performance. An internal 16V clamp is added for MOSFET gate protection at higher than expected VDD input.

Package Information

DIP-7



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.148	0.0170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524(BSC)		0.060(BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.3540	0.370
E	6.200	6.600	0.2440	0.260
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354