



Description

JMT P-channel Enhancement Mode Power MOSFET

Features

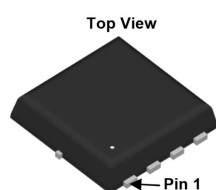
- $V_{DS} = -40V$, $I_D = -8A$
 $R_{DS(ON)} < 43m\Omega$ @ $V_{GS} = -10V$
 $R_{DS(ON)} < 60m\Omega$ @ $V_{GS} = -4.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

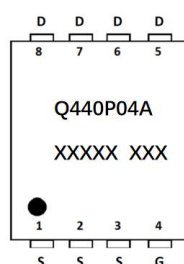
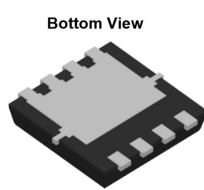
- PWM Applications
- Load Switch
- Power Management



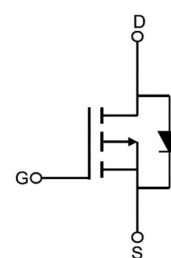
100% UIS TESTED!
100% ΔV_{ds} TESTED!



PDFN3x3-8L



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
Q440P04A	JMTQ440P04A	TAPING	PDFN3x3-8L	13inch	5000	50000

Absolute Maximum Ratings ($T_C = 25^\circ C$ unless otherwise specified)

Symbol	Parameter		Max.	Units
V _{DSS}	Drain-Source Voltage		-40	V
V _{GSS}	Gate-Source Voltage		±20	V
I _D	Continuous Drain Current	T _C = 25°C	-8	A
		T _C = 100°C	-5.2	A
I _{DM}	Pulsed Drain Current ^{note1}		-32	A
E _{AS}	Single Pulsed Avalanche Energy ^{note2}		25	mJ
P _D	Power Dissipation	T _C = 25°C	4.6	W
R _{θJC}	Thermal Resistance, Junction to Case		27	°C/W
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -40V, V _{GS} =0V	-	-	-1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±20V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
R _{DS(on)}	Static Drain-Source on-Resistance note3	V _{GS} = -10V, I _D = -5A	-	33	43	mΩ
		V _{GS} = -4.5V, I _D = -3A	-	44	60	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = -20V, V _{GS} =0V, f=1.0MHz	-	1034	-	pF
C _{oss}	Output Capacitance		-	107	-	pF
C _{rss}	Reverse Transfer Capacitance		-	79.5	-	pF
Q _g	Total Gate Charge	V _{DS} = -20V, I _D = -5A, V _{GS} = -10V	-	20	-	nC
Q _{gs}	Gate-Source Charge		-	3.5	-	nC
Q _{gd}	Gate-Drain(“Miller”) Charge		-	3.3	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DD} = -20V, I _D = -5A, V _{GS} = -10V, R _{GEN} =2.4Ω	-	8.5	-	ns
t _r	Turn-on Rise Time		-	22	-	ns
t _{d(off)}	Turn-off Delay Time		-	27	-	ns
t _f	Turn-off Fall Time		-	35	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	-8	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-32	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -8A	-	-0.8	-1.2	V
trr	Reverse Recovery Time	V _{GS} =0V, I _S = -5A , di/dt=100A/μs	-	13	-	ns
Qrr	Reverse Recovery Charge		-	9	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition: T_J= 25°C, V_{DD}= -20V, V_G= -10V, L=0.5mH, R_G= 25Ω, I_{AS}= -10A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤2%



Typical Performance Characteristics

Figure1: Output Characteristics

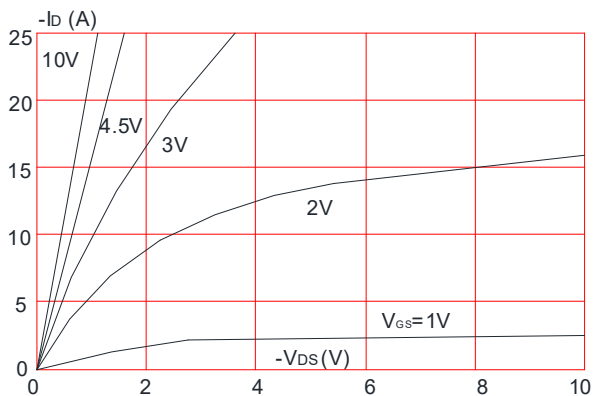


Figure 2: Typical Transfer Characteristics

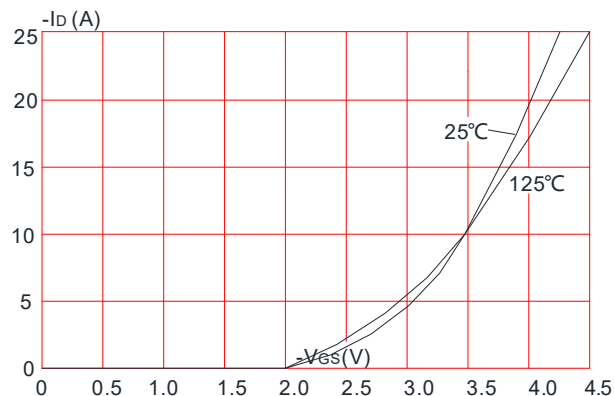


Figure 3: On-resistance vs. Drain Current

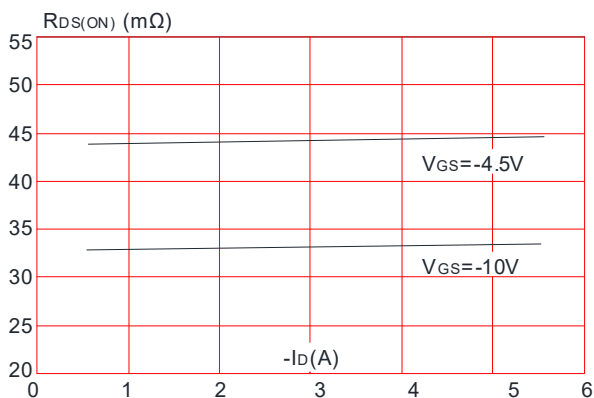


Figure 4: Body Diode Characteristics

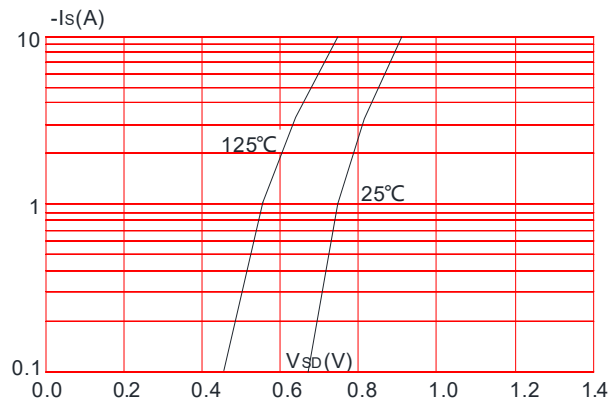


Figure 5: Gate Charge Characteristics

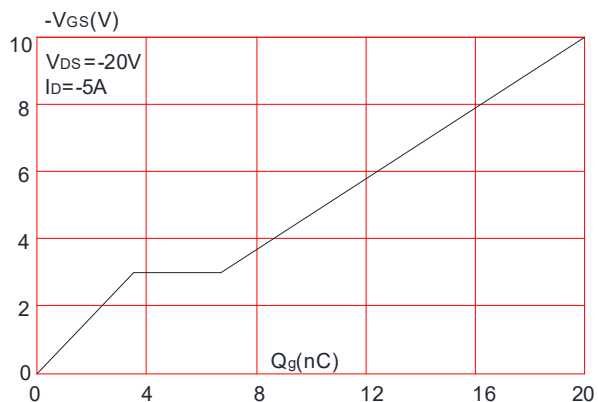


Figure 6: Capacitance Characteristics

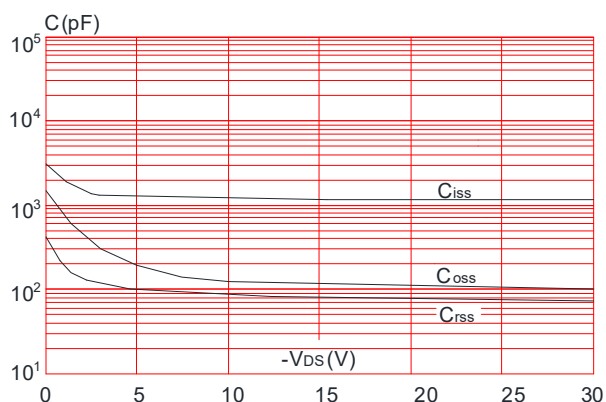


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

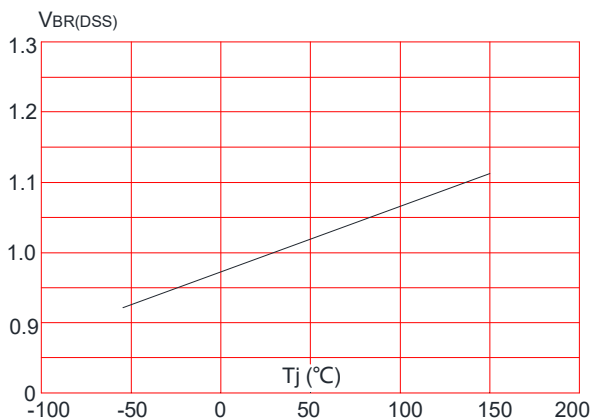


Figure 8: Normalized on Resistance vs. Junction Temperature

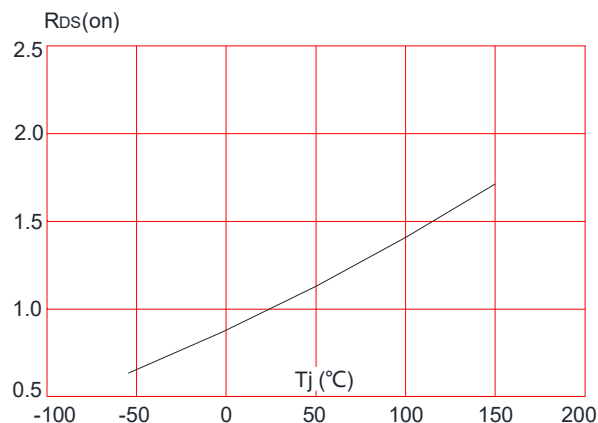


Figure 9: Maximum Safe Operating Area

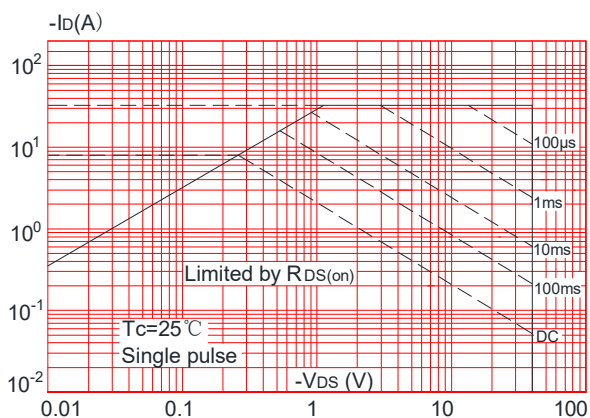


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

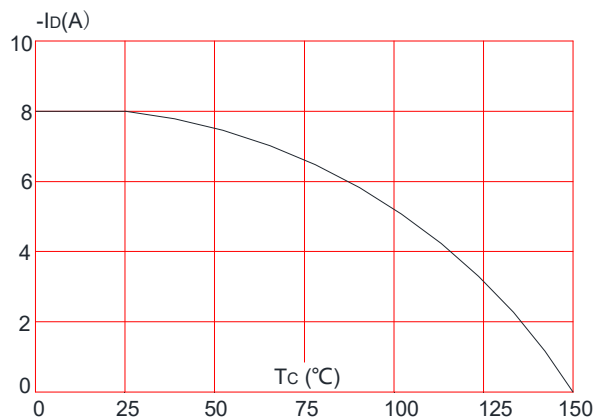
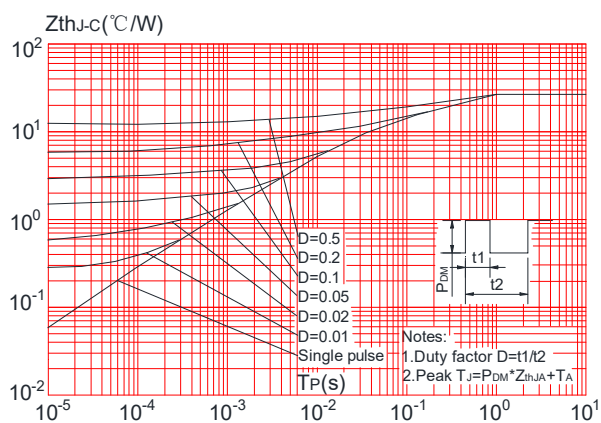
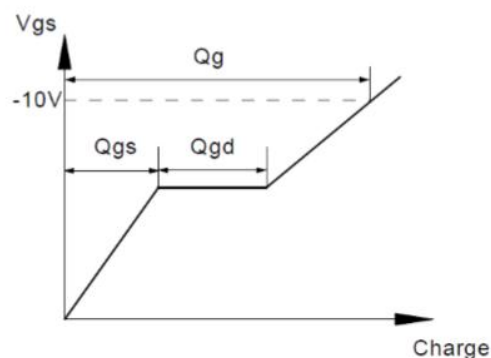
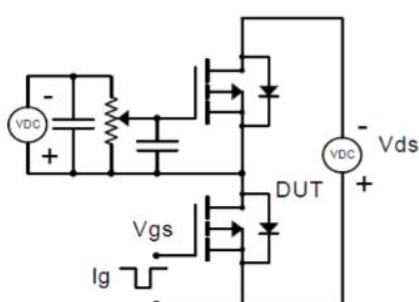


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

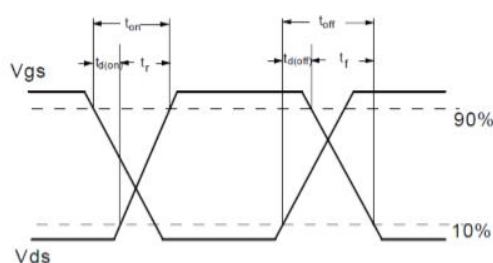
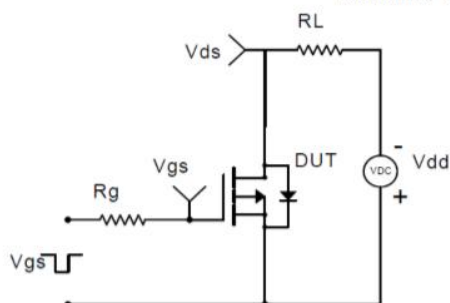


Test Circuit

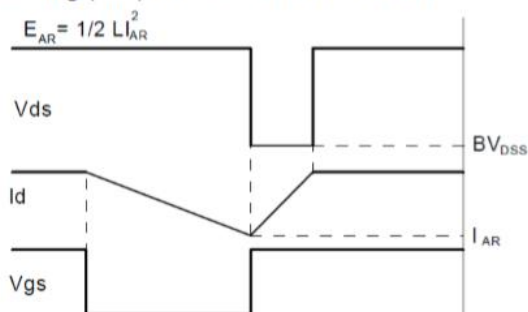
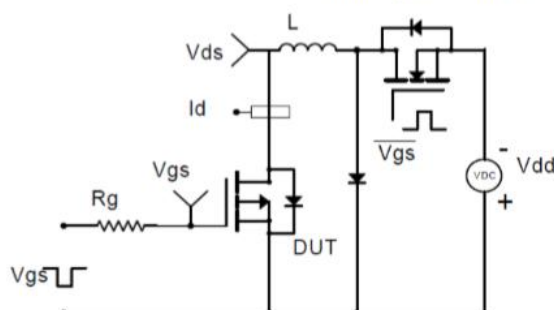
Gate Charge Test Circuit & Waveform



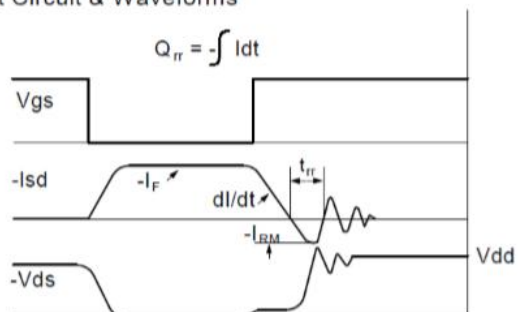
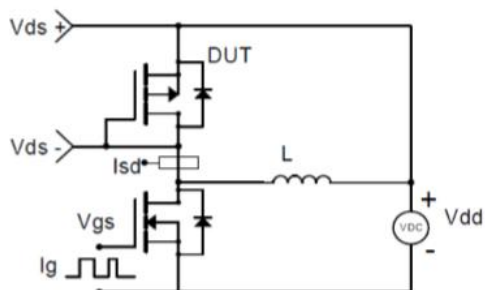
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

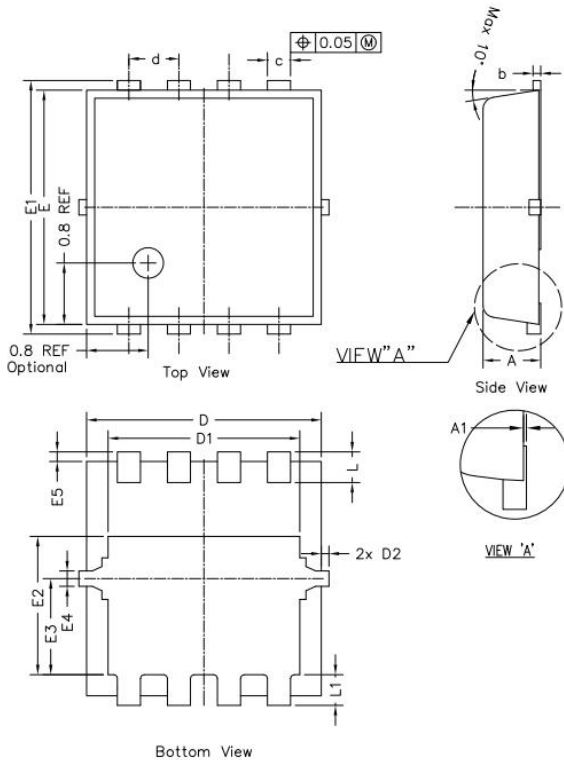


Diode Recovery Test Circuit & Waveforms





Package Mechanical Data-PDFN3x3-8L



SYMBOLS	DIMENSION IN MM			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	---	---	0.050	----	----	0.002
b	0.144	0.152	0.202	0.006	0.006	0.008
c	0.250	0.300	0.350	0.010	0.012	0.014
d	0.65 BSC			0.026 BSC		
D	2.950	3.050	3.150	0.116	0.120	0.124
D1	2.390	2.490	2.590	0.094	0.098	0.102
D2	---	---	0.125	---	---	0.005
E	2.950	3.050	3.150	0.116	0.120	0.124
E1	3.200	3.300	3.400	0.126	0.130	0.134
E2	1.700	1.800	1.900	0.067	0.071	0.075
E3	1.150	1.250	1.350	0.045	0.049	0.053
E4	0.150	0.200	0.250	0.006	0.008	0.010
E5	0.075	0.125	0.175	0.003	0.005	0.007
L	0.300	0.400	0.500	0.01	0.02	0.02
L1	0.300	0.400	0.500	0.01	0.02	0.02

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