Features

- ▲ Power-on Soft Start Reducing MOS Stress
- ▲ Multi-Mode Operation
- ▲ Low VDD startup current (<5uA)
- ▲ Low operation current
- ▲ Extra Low Standby (75mW)
- ▲ Frequency jitter to Minimize EMI
- ▲ Leading edge blanking on current sense
- ▲ Audio Noise Free Operation
- ▲ VDD Under Voltage Lockout with Hysteresis
- ▲ Cycle-by-Cycle over current Protection
- ▲ Over Load Protection (OLP)
- ▲ Internal Over Temperature Protection (OTP)
- ▲ Output Over Voltage Protection (Output OVP)
- ▲ VDD Over Voltage Protection (OVP)
- ▲ Output Short Protection (OSP)

Applications

Offline AC/DC flyback converter for

- ■ AC/DC Adapter
- ■ Set-Top Box Power Supplies
- ■ Auxiliary Power Supply
- ■ Open-frame SMPS

General Description

ZS5362 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

At full loading, the IC operates in fixed frequency mode. When the loading goes low, it operates in Green mode with valley switching for high efficiency. When the load is very small, the IC operates in 'Burst Mode' to minimize the standby power loss. As a result, high conversion efficiency can be achieved in the whole loading range.

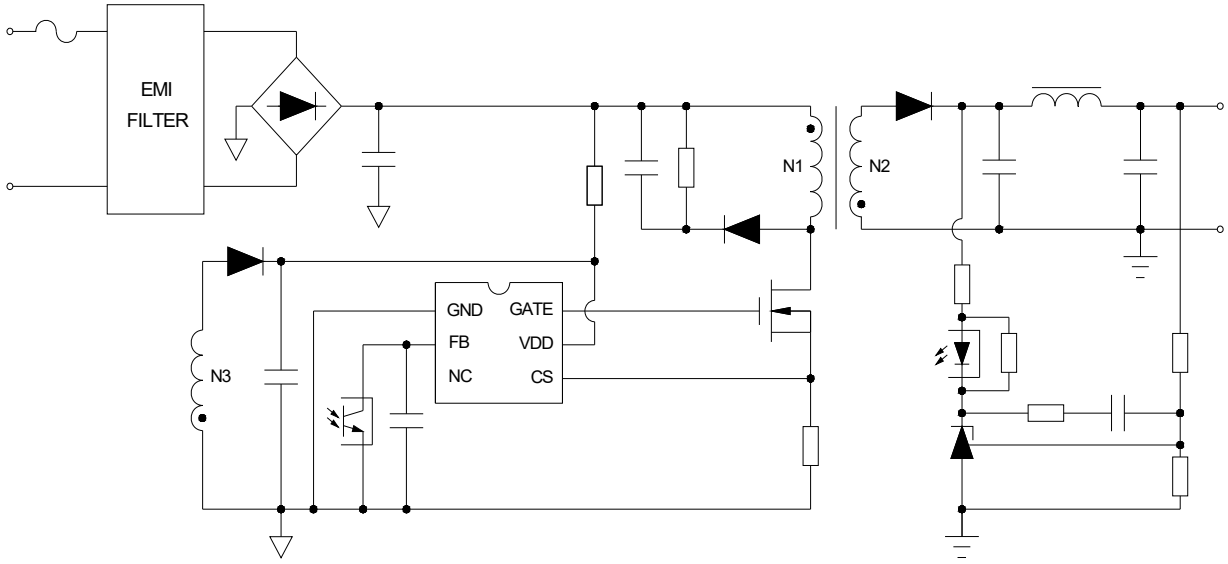
VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with ZS5362.

ZS5362 offer comprehensive protection coverage with auto-recovery including Cycle-by-Cycle current limiting (OCP), VDD under voltage lockout (UVLO), over voltage protection (OVP). Excellent EMI performance is achieved with internal frequency jitter technique.

The tone energy at below 22KHz is minimized in the designed and audio noise is eliminated.

ZS5362 is offered in SOT23-6 package.

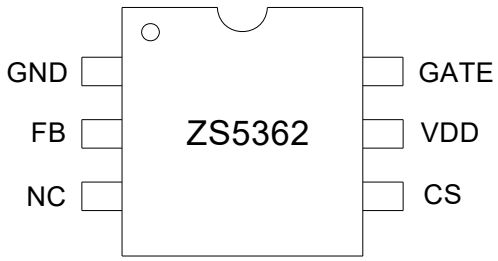
Typical Application Information



General Information

Pin Configuration

TOP VIEW



SOT23-6

Absolute Maximum Ratings

Parameter	Value
VDD DC Supply Voltage	60V
VDD DC Clamp Current	10mA
FB, CS voltage range	-0.3~5V
Package Thermal Resistance	200℃/W
Maximum Junction Temperature	150℃
Operating Temperature Range	-40~85℃
Storage Temperature Range	-55~150℃
Lead Temperature(Soldering, 10sec)	260℃
ESD Capability, HBM	2KV
ESD Capability, MM	200V

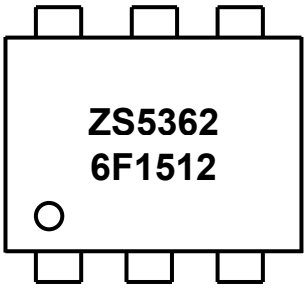
Recommended Operating Conditions

Parameter	Value	Unit
Supply Voltage, VDD	10~26	V
Operating ambient temperature	-40~85	℃
Maximum Switching Frequency	65K	Hz

Pin Description

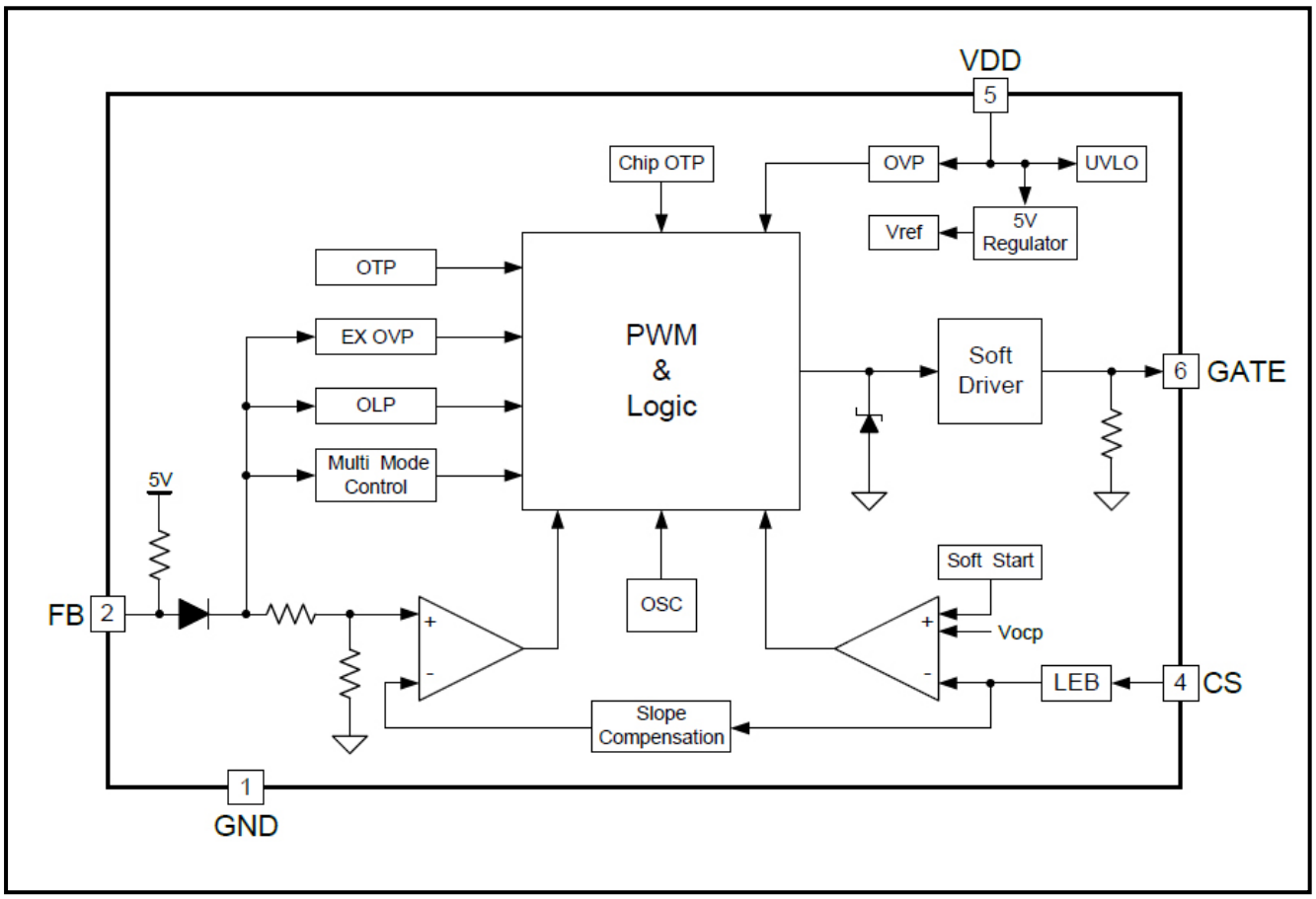
Pin No.	Name	I/O	Function
1	GND	P	Ground reference pin
2	FB	I	System feedback pin
3	NC	--	Not Connection
4	CS	I	Current sense pin, connected to sense resistor the MOSFET current signal
5	VDD	P	Power supply PIN
6	GATE	O	Totem-pole gate drive output for power MOSFET

Ordering and Marking Information



ZS5362：Product name
6F：Internal Code
15：Year Code
12：Week Code

BLOCK DIAGRAM

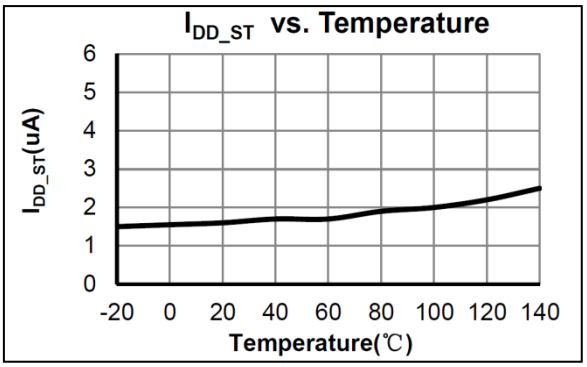


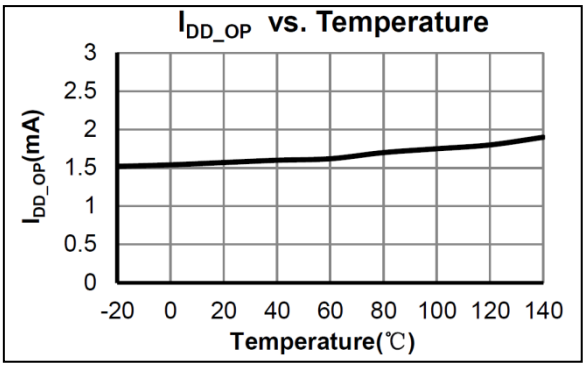
Electrical Characteristics

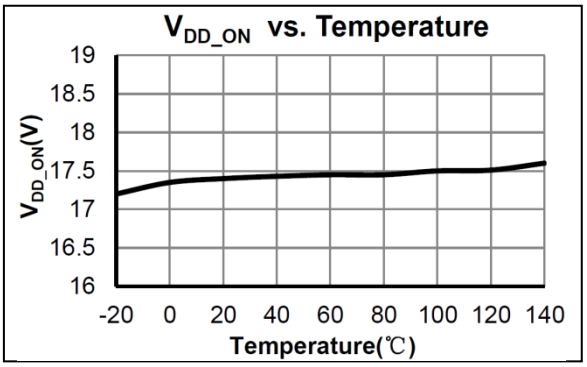
(T_A=25℃, unless otherwise stated, VDD=18.0V)

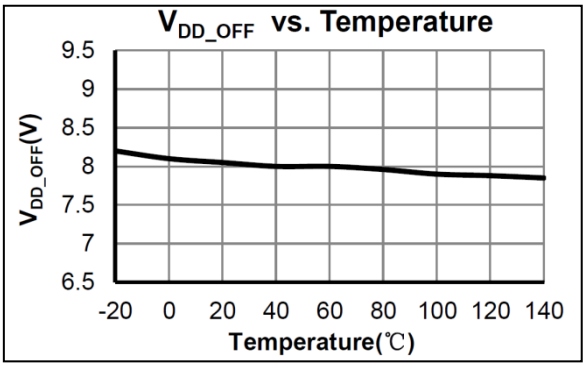
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLY VOLTAGE (VDD PIN)						
I_{DD_ST}	Startup Current	VDD=V_{DD_ON}-1V		3	5	uA
I_{DD_OP}	Operation Current	FB=3V		2	3.0	mA
I_{DD_Burst}	Burst Current	VCS=0V, VFB=0.5V		0.6	0.7	mA
UVLO(ON)	VDD Under Voltage Lockout Exit (Startup)		16.0	17.0	18.0	V
UVLO(OFF)	VDD Under Voltage Lockout Enter		6.0	7.0	8.0	V
V_{DD}_Clamp	VDD Over Voltage Protection trigger	I(V_{DD})=10mA			60	V
Feedback Input Section(FB Pin)						
V_{FB_Open}	FB Open Loop Voltage			4.75		V
A_V	PWM input gain ΔVFB/ΔVCS			1.71		V/V
D_{MAX}	Max duty cycle	VFB=3V, VCS=0.3V	77	80	83	%
V_{Ref_Green}	The threshold enter green mode			2.1		V
$V_{Ref\_Burst\_H}$	The threshold exit Burst mode			1.25		V
$V_{Ref\_Burst\_L}$	The threshold enter Burst mode			1.15		V
I_{FB_Short}	FB pin short circuit current	Short FB pin to GND		0.35		mA
V_{TH_PL}	Power Limiting FB Threshold Voltage			3.7		V
T_{D_PL}	Power limiting Debounce Time			55		mS
Z_{FB_IN}	Input Impedance			20		KΩ
Current Sense Input Section (CS Pin)						
T_{SS}	Soft start time			4		ms
T_{LEB}	Leading edge blanking time			300		ns
T_{D_OC}	Over Current Detection and Control Delay			90		ns
V_{TH_OC}	Current Limiting Threshold Voltage with zero duty cycle			0.75		V
V_{OCP_Clamp}	CS voltage clamper			0.9		V
Oscillator						
FOSC	Normal Oscillation Frequency	VFB=3V,VCS=0V	60	65	70	KHz
FJR	Frequency jitter range			±4		%
FBurst	Burst Mode Switch Frequency			20		KHz

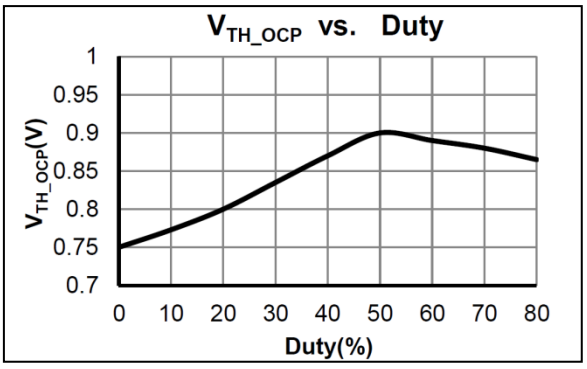
Characterization Plots

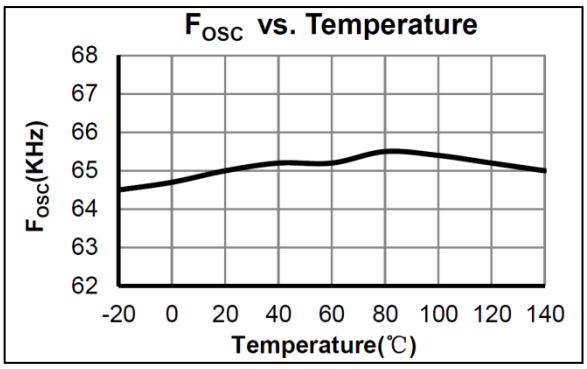


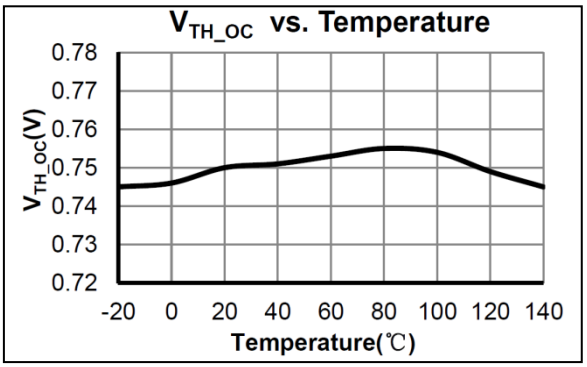












Operation Description

The ZS5362 is a low power off-line SMPS Switcher optimized for off-line flyback converter applications. The Burst Mode control greatly reduces the standby power consumption and helps the designed easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of ZS5362 is designed to be very low so that VDD could be charged up above VD_{D_ON} and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

Operating Current

The Operating current of ZS5362 is low at 2.0mA (typical). Good efficiency is achieved with ZS5362 low operation current together with the Burst Mode control features.

Soft Start

ZS5362 features an internal 4mS (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches V_{DD_ON}, the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

Frequency jitter for EMI improvement

The frequency jitter is implemented in ZS5362. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Oscillator Operation

The switching frequency of ZS5362 is internally fixed at 65KHz. No external frequency setting components are required for PCB design simplification.

Multi-mode Operation for High Efficiency

ZS5362 is a multi-mode controller. The controller changes the mode of operation according to the FB pin voltage. At the normal operating condition, the IC operates in traditional fix frequency (60KHz) PWM mode. As the output load current is decreased, the IC enter into green mode smoothly from the PWM mode. In this mode, the switching frequency will start to linearly decrease from 60KHz to 20KHz. So the switching loss is minimized and the high conversion efficiency can be achieved. At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOS, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light or no load condition to improve the conversion efficiency.

At light load or no load condition, the FB input drops below $V_{Ref\_Burst\_L}$ and device enters Burst Mode control. The Gate drive output switches when FB input rises back to $V_{Ref\_Burst\_H}$. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in ZS5362 current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Driver

The External power MOSFET of ZS5362 is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

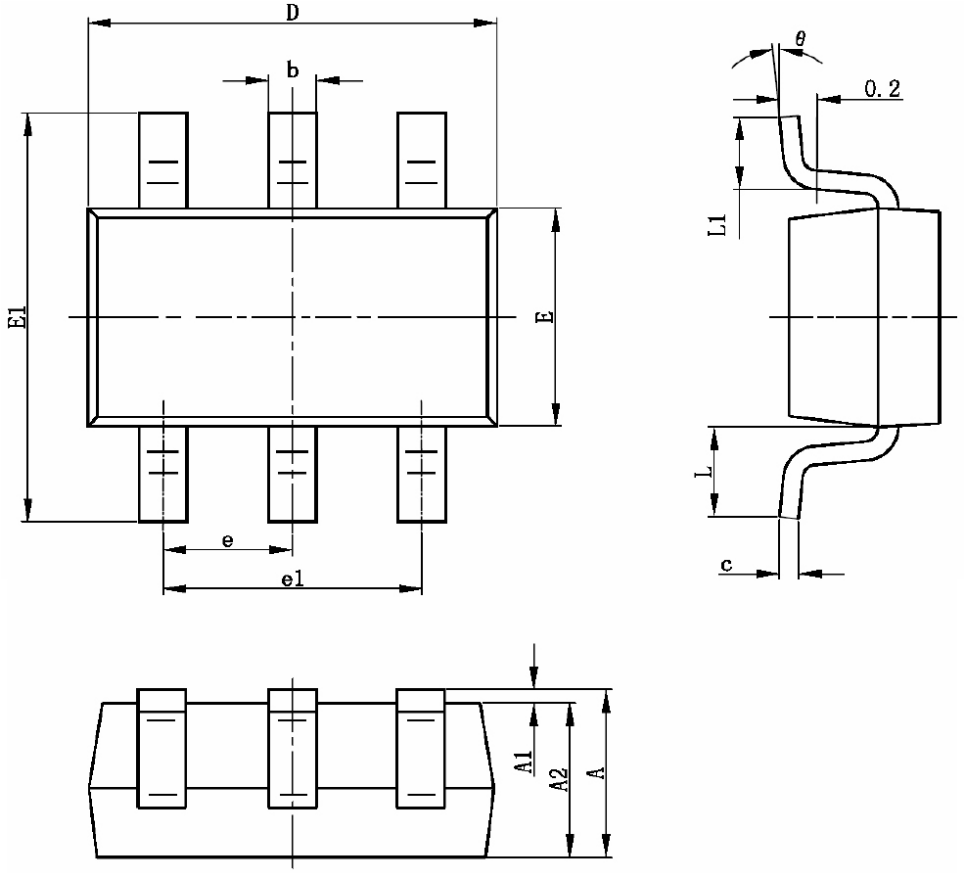
A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VDD Over Voltage Protection (OVP). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than T_{D_PL}, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

Package Information

SOT23-6



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.400	0.012	0.016
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950TYP		0.037TYP	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°