LZC6100

LOZEN TECNOLOGY INC

Critical Conduction Mode PFC Controller

General Description

The LZC6100 is an active power factor correction (PFC) controller with boost topology operates in quasi-resonant mode (QRM). It uses voltage mode PWM control method that compares an internal sawtooth signal with output signal of the error amplifier to generate an external power MOSFET turn-off signal. LZC6100 introduce 500V start-up and novel power supply circuit (patent pending) for VCC without extra axillary winding. LZC6100 sets two levels slope ratio for inner sawtooth signal by input line voltage automatically and builds in vary on time with input line voltage technology to optimize THD greatly.

The LZC6100 provides output over-voltage protection (OVP), CS pin cycle by cycle current limit and the secondary over-current protection (OCP), input line voltage brown in and brown out protection, and under voltage lockout (UVLO). The LZC6100 can be disabled if the VFB pin voltage is lower than 0.45V and the operating current decreases to a very low level. Using a new variable on-time control method, the application can easily get very good total harmonic distortion (THD) result.

Main Features

- Very fewer external components
- Zero-current detection (ZCD) without extra winding
- Internal total harmonic distortion (THD) optimizer
- Low operating current and power supply from HV pin directly without extra auxiliary winding
- Boost quasi-resonant converter controller for adaptors or high brightness LEDs
- Supports high power factor (PF>0.9) and low THD
- High precision constant voltage regulation for universal AC input (85VAC~265VAC)
- Various output voltage by input line voltage
- Maximum switching frequency limitation
- Lower standby power by burst operation
- Building in fast loop to reduce output voltage ripple during load transient
- Disable/Enable function by VFB pin
- Wide VCC operation voltage (8V~26V)
- 10mS CS voltage soft start to avoid inductor current overshot during startup period
- SOP8 package
- Provides complete protection functions
  - Cycle-by-cycle current limit on CS pin
  - The secondary protection on CS pin
  - Input AC under voltage protection
  - Input AC over voltage protection
  - Output over-voltage protection
  - Internal over-temperature protection
  - VCC under-voltage lockout with hysteresis
  - DRV output maximal voltage clamped (17V)

Application

- AC-DC adaptors, chargers, TVs,
- Electronic light ballast
- LED lighting
- All SMPS requiring power factor correction

Typical Application

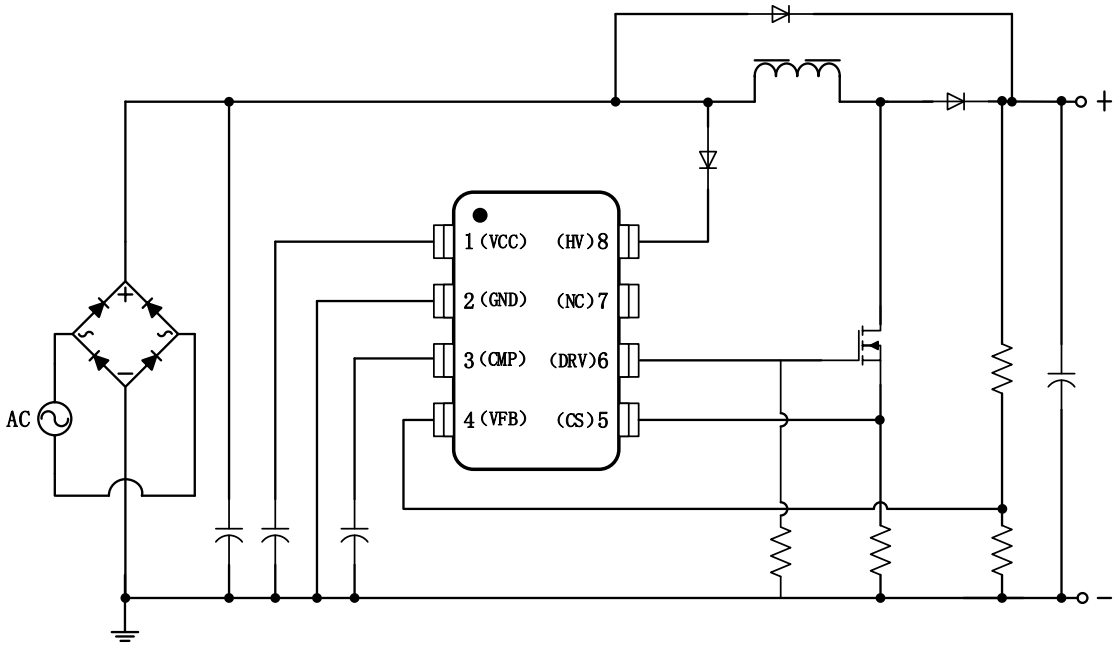


Figure1 LZC6100 typical appliation circuit

Pin Diagram（SOP8）

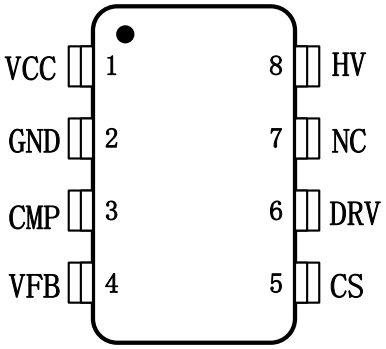


Figure2 Pin assignment

Pin Description

Name	I/O(1)	Pin No.	Description
VCC	Power	1	Power supply.
GND	Power	2	Power ground.
CMP	I	3	Output of the error amplifier. A compensation network is placed between CMP and GND to provide stable loop response.
VFB	I	4	Output voltage detection and controller enable or not.
CS	I	5	Inductor current sense, connect one resistor to GND.
DRV	O	6	Driver external MOSFET output. Various output voltage function enable/disable by a resistor connect form this pin to GND.
NC	/	7	No connection.
HV(2)	I	8	Power supply for VCC and input AC line voltage detection.

Note (1): I=Input, O=Output

Note (2): Pins #8 (HV) are ESD sensitive. Handle with care.

Block Diagram

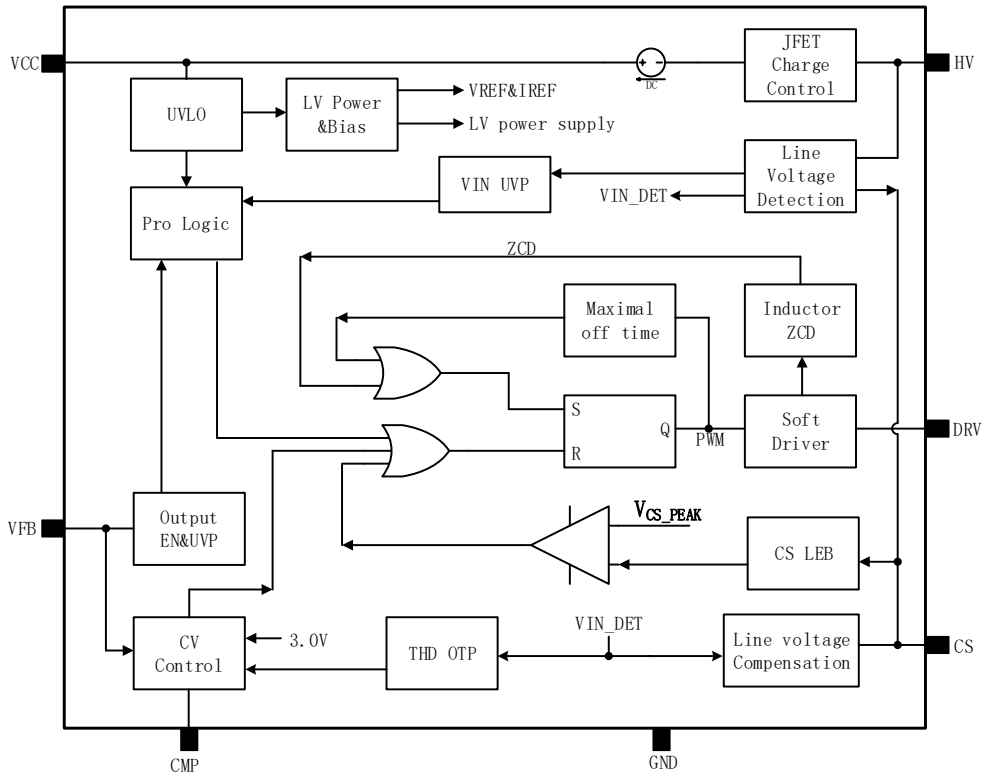


Figure3 Block diagram

Absolute Maximum Ratting (Note 3)

HV ---------- -0.3V~+500V

VCC and DRV ---------- -0.3V~+30V

CMP, VFB, CS ---------- -0.3V to 6.5V

Thermal Impedance, θJA SOP8 ---------- 165℃/W

Junction Temperature ----------160 ℃

Soldering Temperature (10 sec.) ---------- 260℃

Storage Temperature Range ---------- -55℃ to 150℃

ESD Capability (Note4)

HBM ---------- 2.5KV

MM ---------- 200V

Recommended Operating Range (Note5)

Junction Temperature ---------- -40℃ to 150℃

Ambient Temperature ---------- -40℃ to 85℃

VCC Supply Voltage ---------- 10V to 23V

VCC Capacitance Value ---------- 10uF to 22uF

Note 3, the “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed and may cause permanent damage to the LZC6100. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the Electrical Characteristics section of the specification is not implied. The “Electrical Characteristics” table defines the conditions for actual device operation. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note 4, It is sensitive for ESD case， some preventive measures are recommended.

Note 5, Not guaranteed if operated outside recommended operating range.

Electrical Characteristics (Note6, Note7)

（VCC=12.3V, T_A=25℃ unless otherwise noted）

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
VCC Pin (Power supply)						
VCC_{ON}	Turn-on threshold voltage		12.7	13.0	13.6	V
VCC_{OFF}	Turn-off threshold voltage		7.6	7.7	7.9	V
VCC_{OVP}	Turn off PWM driver of DRV pin			27.6		V
VCC_{CLAMP}	VCC clamp voltage	After PWM driver		26		V
VCC_{UV}	Turn on HV sink current to VCC pin	Holding mode		9.0		V
VCC_{UVR}	VCC voltage release VCC_{UV} state	Holding mode		10.2		V
I_{ST1}	VCC startup current	VFB=0.1V (<0.3V) VCC=15V	35.7	55	101.8	uA
I_{SS}	VCC operating current	@DRV=7KHz		TBD		uA
HV Pin (Power supply for VCC and VIN detection)						
I_{HV}	HV pin sink current to VCC pin	HV=50V, VCC=10V		TBD		mA
$IHV_{LEAKAGE}$	Leakage current when turn off sink current from HV pin to VCC pin	HV=50V, VCC=15V			18.9	uA
VIN_{UVP}	Turn off pulse driver once VIN voltage is less than VIN_{UVP}	HV DC voltage		97.5		V
VIN_{UVP_R}	VIN UVP release voltage	HV DC voltage		113		V
T_{VIN_UVP}	Delay time for VIN UVP			35.8		mS
CMP Pin (Loop compensation and THD)						
V_{OTA}	Reference voltage for CV		2.92	3	3.08	V
V_{COMP_H}	High clamp voltage of COMP pin			4.3		V
V_{COMP_L}	Low clamp voltage of COMP pin			1.0		V
I_{COMP_SOURCE}	Maximum source current from COMP pin			15		uA
I_{COMP_SINK}	Maximum sink current from COMP pin			15		uA
GM_{OTA_CV}	Trans-conductance of OTA			50		uA/V

QR_OSC/OSC/Startup timing						
FRE_{MAX}	Maximum frequency			347		KHz
FRE_{MIN}	Minimum frequency			30		KHz
T_{ON_MAX}	Maximum on time			30		uS
T_{ON_MIN}	Minimum on time			400		nS
T_{OFF_MAX}	Maximum off time			288		uS
T_{OFF_MAX}	Minimum off time			1.7		uS
VFB pin (Loop feedback information)						
V_{FBV_EN}	Enable controller			0.6		V
V_{FB_ENN}	Disable controller			0.45		V
V_{FB_MAX}	VFB pin clamped voltage			7.2		V
I_{VFB_MAX}	VFB pin clamped maximal current				1	mA
VFB_{OVP}	VFB over voltage protection			3.32		V
VFB_{OVP_R}	VFB over voltage protection release			3.24		V
CS Pin (Current sense)						
T_{CS_LEB}	Leading-edge blanking time for CS pin			400		nS
V_{PK_CS}	Cycle by cycle protection threshold			1.1		V
V_{OCP}	Over current protection	Note 8		1.8		V
T_{OCP_CV}	OCP delay time			3		PWM
DRV Pin (External driver and ZCD detection)						
V_{MAX_NMOS}	Maximum voltage on DRV for NMOS driver	VCC>15V		12		V
V_{PMOS_EN}	VCC voltage for enable PMOS driver			12		V
V_{PMOS_ENN}	VCC voltage for disable PMOS driver			15		V
$I_{DRVSOURCE}$	Maximum source current for DRV pin	V_{DRV}=11V		1.0		A
$I_{DRVSINK}$	Maximum sink current for DRV pin	V_{DRV}=11V		0.8		A
Temperature Control						
OTP	Over temperature protection	Note 8		151		℃
OTP_R	OTP release temperature	Note 8		130		℃

Note 6: Use of this product outside the limits of the test conditions may experience in a variation of parameters from the published parameters. If additional information is needed, please consult with your Field Application Engineer (FAE) of LOZEN Technology Corp.

Note 7, After minimum off time, switch turn on again until the valley bottom detection is effective, there is a certain deviation between the design value and actual value.

Note 8, these limitation values were got by simulation.

Key Parameter vs. Temperature (Note9)

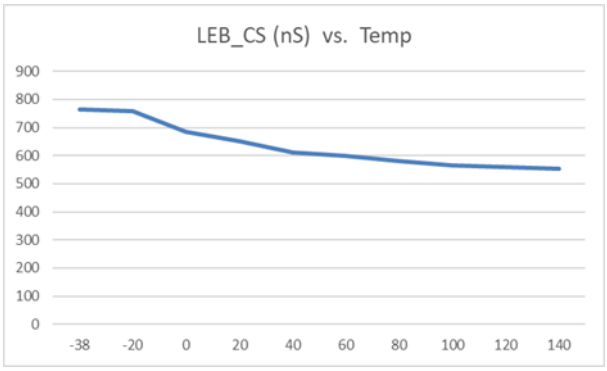


Figure4 LEB_CS vs. temperature

Note9,

Introduction

The LZC6100 is a voltage-mode active power factor correction (PFC) controller with boost topology which operate in quasi-resonant Mode (QRM). LZC6100 adopt a new vary on time method which optimize THD greatly. LZC6100 integrates complete protection functions, including over-voltage protection (OVP), CS pin cycle by cycle current limit and the secondary over-current protection (OCP), input line voltage brown in and brown out protection, VCC under voltage lockout (UVLO) and over temperature protection.

Startup Circuit

When the system is powered on, the DC voltage enters the HV pin and charges the VCC hold capacitance through the internal circuit. As shown in Figure 5, when the voltage of VCC reaches 13.0V, the LZC6100 internal circuit starts to output the driver to turn on the power MOSFET. When the VCC voltage drops below 7.7V, LZC6100 turns off the MOSFET driver and enter in VCC under voltage lockout protection (UVLO). 5.3V VCC hysteresis voltage is implemented to prevent shutdown from a voltage dip during start-up.

IC would turn off gate driver once VCC voltage rises over than 27.6V.

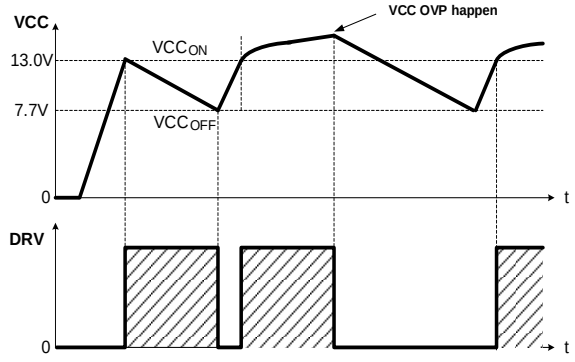


Figure5 VCC working state

Power Factor Correction

The LZC6100 is designed with quasi-resonant mode (QRM) and variation on time T_{on} to achieve high power factor and low THD under normal operation. Compared with the traditional constant on-time PFC, when the input voltage is very low, the input current is also very low, which leads to large current distortion. When the variable on-time is adopted, LZC6100 will increase the ton time with the decrease of input voltage. In this way, input current can be enhanced at low VAC condition，which reducing the current distortion and obtaining a higher PFC and lower THD.

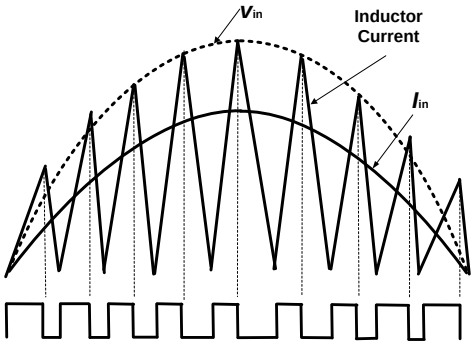


Figure6 The peak inductor current and average input current with PFC

Various output voltage Function

In order to reduce the stress of power device when AC input voltage is low, LZC6100 integrates special various output voltage function. When the maximum DC voltage on HV pin is lower than 135V, the internal reference voltage will drop from 3.0V to 2.3V, then the output voltage will decrease to 76.6% of the standard setting value, when the maximum DC voltage on HV pin exceeds 175V, the reference voltage will return to standard value. The 40V hysteresis design avoids output oscillation. This function is selected by the resistor connect from DRV pin to GND. With 60K resistor, this function is selected, and

with 20K resistor, this function is disabled. This function reduces the stress of the power device at low AC input, especially the smaller size of transformer can be selected.

Enable/Disable Function

The LZC6100 integrates the enable and disable IC operation on VFB pin. The system will be disable operation when the voltage of the VFB input is lower than 0.45V, and it will resume operation until VFB voltage above 0.6V.

Output Voltage Setting

The LZC6100 monitors the output voltage signal by the VFB pin through a resistor divider pair Ra and Rb as shown in Figure7. The input VFB signal compare with the 3.0V internal reference voltage which on the non-inverting input of the transconductance amplifier. The output of the amplifier changes according to the voltage difference of the VFB and the reference voltage. The output voltage of the amplifier is compared with the internal ramp signal to generate the turn-off signal to control the power MOSFET.

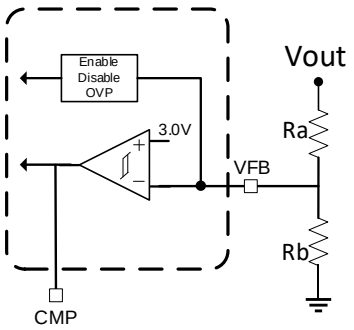


Figure7 Output voltage set circuit

The output voltage is determined by the following relationship:

$$Vout(V) = 3.0 * (1 + \frac{Ra}{Rb})$$

CS Leading-Edge Blanking

When MOSFET turn on, current spike may occur at pin CS due to any parasitic in the application circuit. The LZC6100 controller provides an internal leading-edge blanking (LEB) unit between the CS Pin and the current comparator input to ignore the first 400ns period of each switching cycle at CS signal. During the blanking time, the path, CS Pin to the current comparator input, is blocked. Figure 8 shows the leading-edge blanking of CS pin.

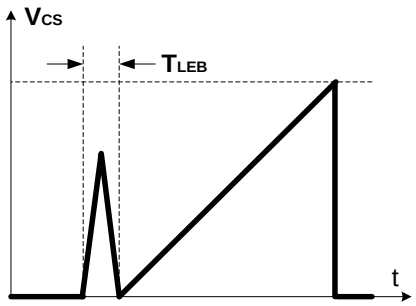


Figure 8 Blanking time for CS

This feature prevents the false-trigger of MOSFET driver, and eliminates the external RC filtering at the CS pin.

Over Voltage Protection

When the load is opened, the load current is charge to the output capacitor. To prevent the over voltage on the output capacitor from the fault condition, LZC6100 is implemented with an OVP function on VFB pin. Whenever the VFB voltage is higher than the OVP threshold voltage 3.32V, the output gate drive circuit will be shutdown simultaneously, the power MOSFET will turn on again until the VFB pin drop to 3.24V.

Over Current Protection

The LZC6100 samples the power MOSFET current from the CS pin, which has cycle-by-

cycle current limit. The maximum voltage threshold of the current sensing pin is set at 1.1V. The MOSFET peak current can be obtained from below equation:

$$Ipeak = \frac{1.1V}{Rcs}$$

The LZC6100 also provides the secondary over-current protection (OCP), when the voltage on CS pin exceeds 1.8V and last for 3 switching cycles, the gate driver will turn off. The circuit will resume until VCC drops to 7.7V followed by rising to above 13.0V.

Over Temperature Protection

When the IC meet a high junction temperature, the over temperature protection will be trigged. The MOSFET driver is turned off once the junction temperature exceeds approximately 151 °C. It resumes normal operation when the junction temperature drops to approximately 130 °C.

Typical Reference Application Circuit (Note 10)

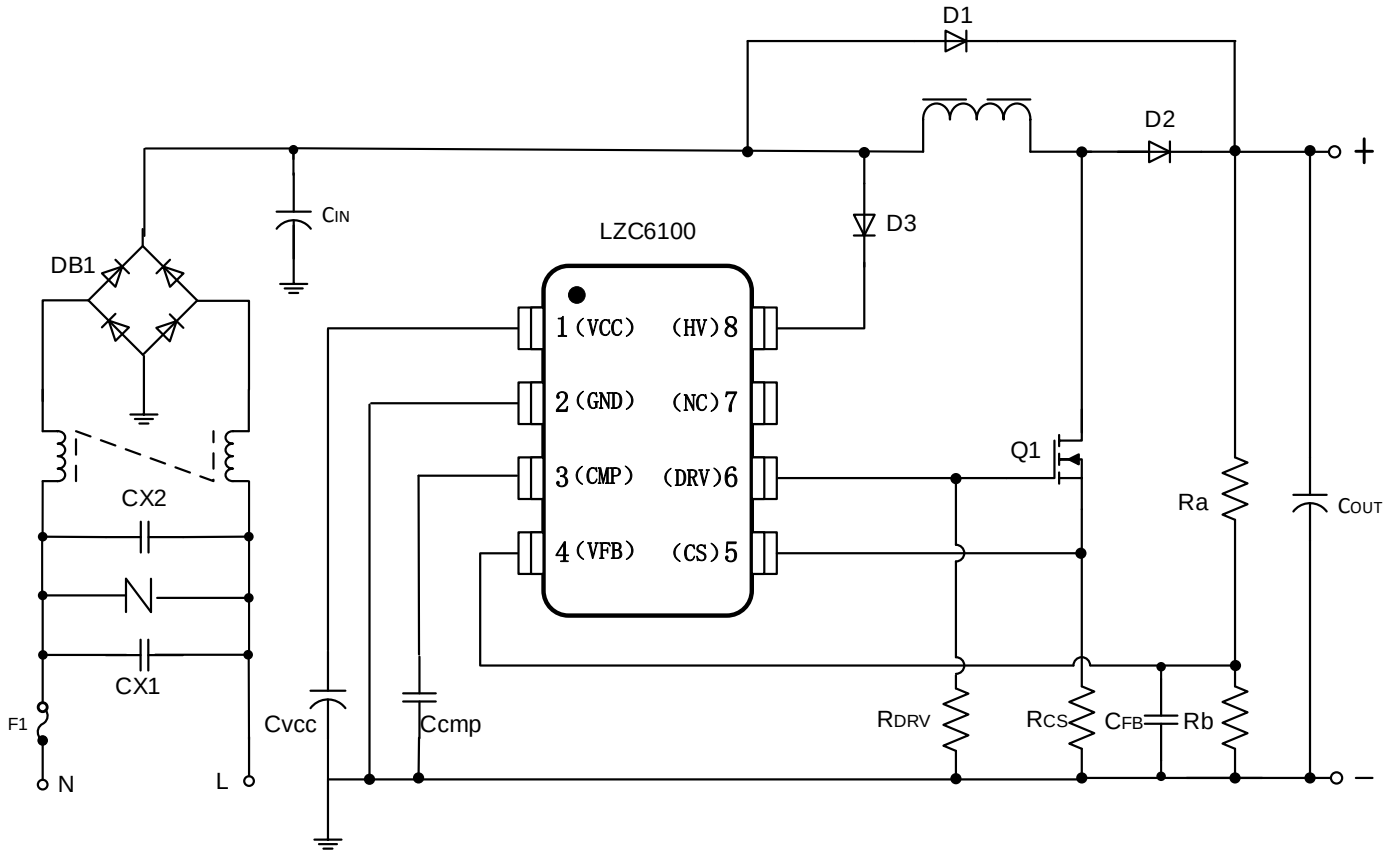
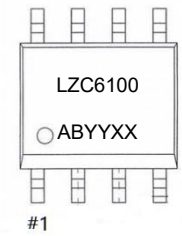


Figure9 LZC6100 application schematic

Note10, it is only reference application circuit, not update to the latest.

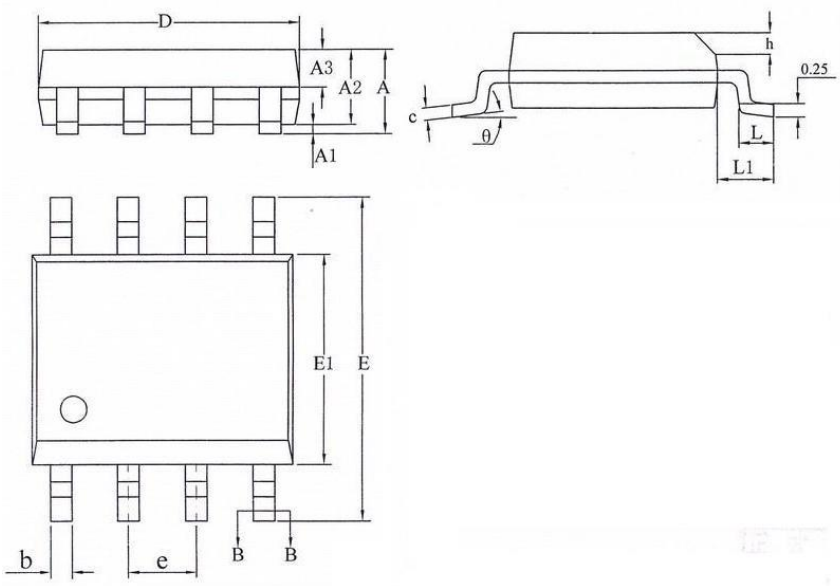
Product Name: LZC6100 SOP8



LZC6100

AB: factor code ; YY: year; XX: week code

Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05BSC		
θ	0	—	8°

Compliant to JEDEC Standard MS12F
Controlling dimensions are in inches; millimeter dimensions are for reference only
This product is RoHS compliant and Halide free.
Soldering Temperature Resistance:
[a] Package is IPC/JEDEC Std 020D Moisture Sensitivity Level 1
[b] Package exceeds JEDEC Std No. 22-A111 for Solder Immersion Resistance; package can withstand 10 s immersion < 270˚C

Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per end. Dimension E1 does not include inter-lead flash or protrusion. Inter-lead flash or protrusion shall not exceed 0.25 mm per side. D and E1 dimensions are determined at datum H. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outer most extremes of the plastic boxy exclusive of mold flash, tie bar burrs, gate burrs and inter-lead flash, but including any mismatch between the top and bottom of the plastic body.