***High Performance Current Mode PWM Controller***

## Features

▲ Extra Low Standby (<75mW)
▲ Power-on Soft Start Reducing MOS Stress
▲ Built-in 650V PowerMOS
▲ Fixed 65KHz Switching Frequency
▲ Low VDD startup and operating current
▲ Frequency Jitter to Minimize EMI
▲ Leading edge blanking on current sense
▲ Audio Noise Free Operation
▲ VDD Under Voltage Lockout with Hysteresis
▲ VDD Voltage Maximum 58V
▲ Cycle-by-Cycle over current Protection
▲ Over Load Protection (OLP)
▲ Over Temperature Protection (OTP)
▲ VDD Over Voltage Protection (OVP)

## Applications

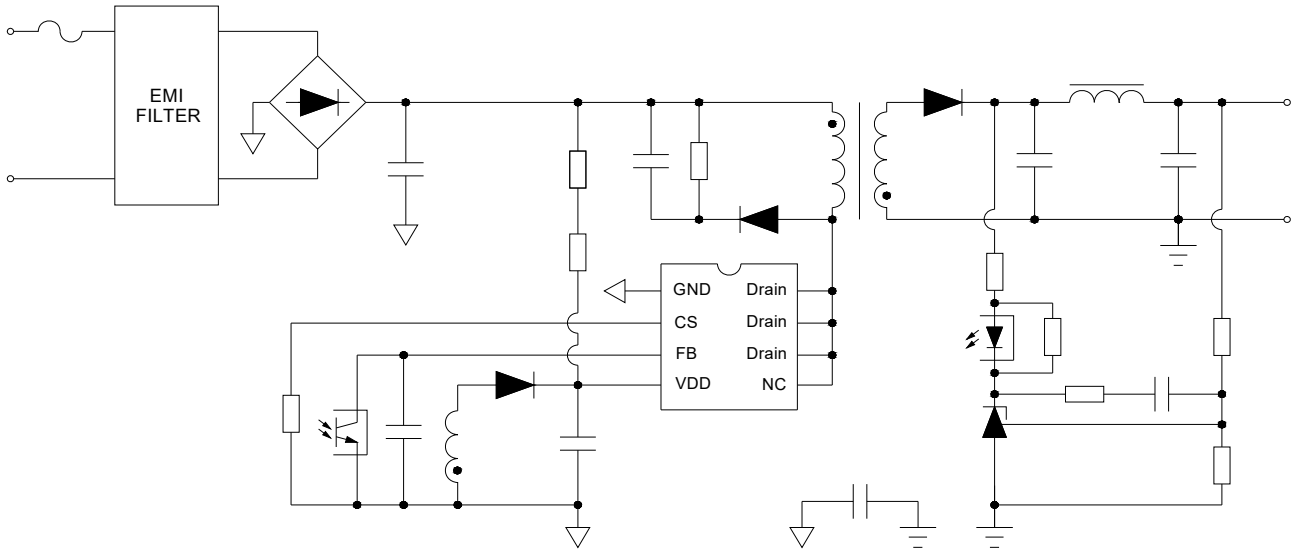
Offline AC/DC flyback converter for
■ AC/DC Adapter
■ Set-Top Box Power Supplies
■ Auxiliary Power Supply
■ Open-frame SMPS

## General Description

ZS6659DM combines a highly integrated current mode PWM controller with a high voltage PowerMOS. It is optimized for high performance, low standby power, and cost effective off line flyback converter application in sub 36W range.
VDD low startup current and low operating current contribute to a reliable power on startup and low standby design with ZS6659DM.
ZS6659DM offers complete protection coverage with automatic self recovery feature including Cycle-by-Cycle current limiting(OCP), Over load protection(OLP), VDD under voltage lockout (UVLO), Over temperature protection(OTP), and over voltage protection(OVP). Excellent EMI performance is achieved with internal frequency jitter technique and soft switching control at the totem pole gate drive output.
The tone energy at below 20KHz is minimized in the design and audio noise is eliminated.
ZS6659DM is offered in DIP-8 package.

ZS6659DM internal 4A650V Power MOS in DIP-8

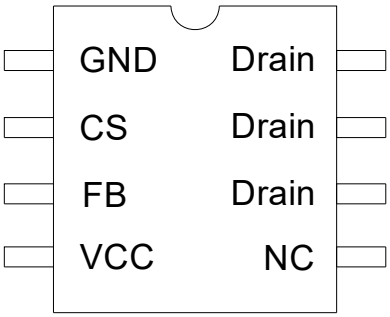
## Typical Application Information



## General Information

### Pin Configuration

TOP VIEW




**DIP-8**

### Absolute Maximum Ratings

| Parameter | Value |
|---|---|
| VDD DC Supply Voltage | 60V |
| VDD DC Clamp Current | 10mA |
| Drain Pin | -0.3~650V |
| FB, CS voltage range | -0.3~5V |
| Maximum Junction Temperature | 150℃ |
| Operating Temperature Range | -40~85℃ |
| Storage Temperature Range | -65~150℃ |
| Lead Temperature(Soldering, 10sec) | 260℃ |
| ESD Capability, HBM | 2KV |
| ESD Capability, MM | 200V |

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress rating only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device’s reliability.

## Recommended Operating Conditions

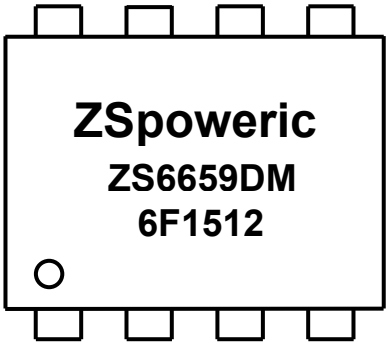
| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| VDD | Supply Voltage | 10 | 60 | V |
| Ta | Operating ambient temperature | -40 | 85 | ℃ |
| Fs | Maximum Switching Frequency | | 65 | KHz |
| $C_{VDD}$ | VDD Capacitor | 4.7 | 10 | uF |
| $P_{OMAX}$ | Output Power | | 36 | W |

Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 45℃ ambient. Higher output power is possible with extra added heat sink or air circulation to reduce thermal resistance.

## Pin Descriptions

| Pin No. | Name | I/O | Function |
|---|---|---|---|
| 1 | GND | P | Ground |
| 2 | CS | I/O | Current sense input and Power MOS Source |
| 3 | FB | I | Feedback input pin |
| 4 | VDD | P | Power Supply |
| 5 | NC | - | Not Connection |
| 6/7/8 | Drain | I | Power MOS Drain |

## Ordering and Marking Information

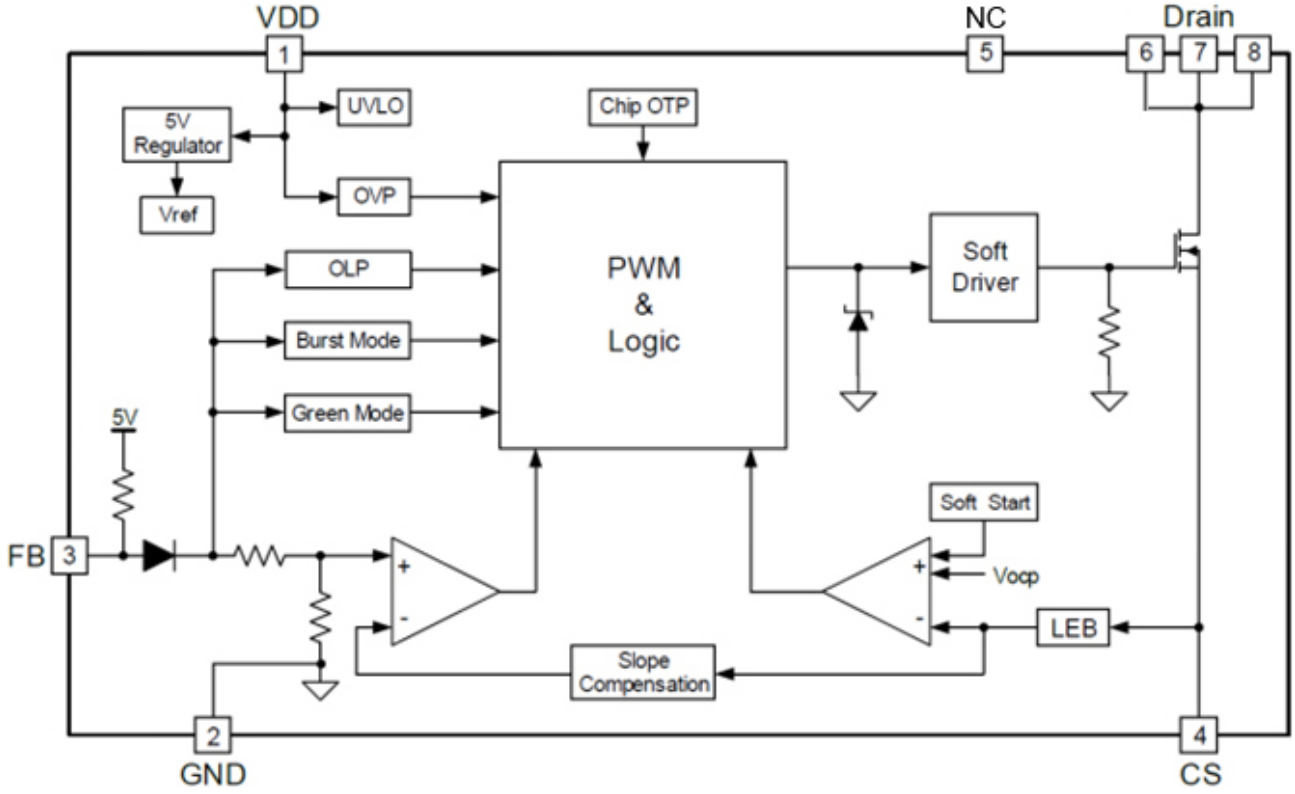



ZSpoweric：Company Logo
ZS6659：Product name
D：DIP Package
6F：Internal Code
15：Year Code
12：Week Code



## BLOCK DIAGRAM

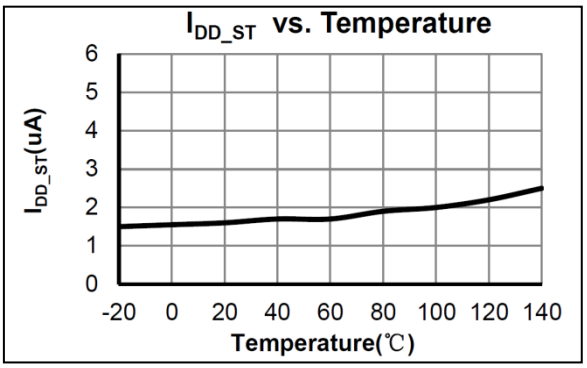


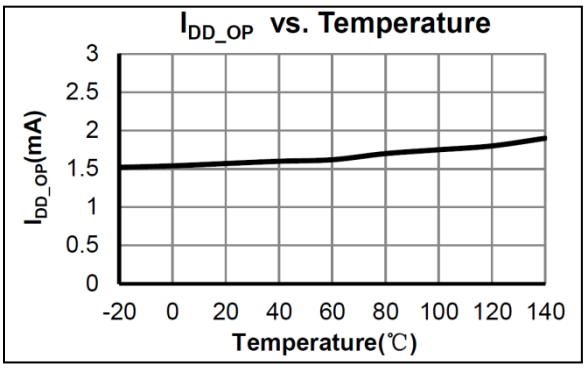
## Electrical Characteristics

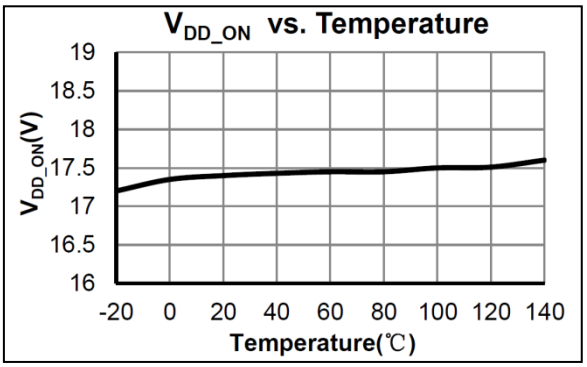
($T_A$=25℃, unless otherwise stated, VDD=18.0V)

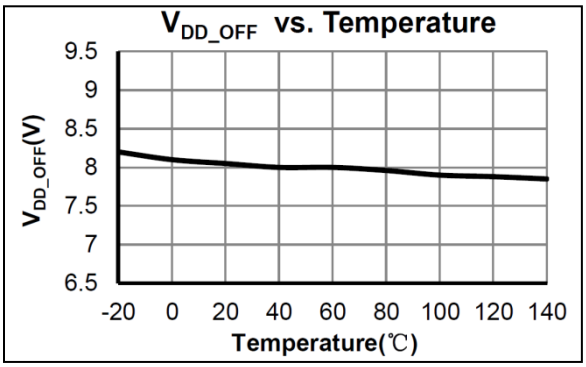
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE (VDD PIN)** | | | | | | |
| $I_{DD\_ST}$ | Startup Current | VDD=$V_{DD\_ON}$-1V | | 3 | 5 | uA |
| $I_{DD\_OP}$ | Operation Current | FB=3V | | 2 | 3.0 | mA |
| $I_{DD\_Burst}$ | Burst Current | VCS=0V,VFB=0.5V | | 0.6 | 0.7 | mA |
| UVLO(ON) | VDD Under Voltage Lockout Exit (Startup) | | 16.0 | 17.0 | 18.0 | V |
| UVLO(OFF) | VDD Under Voltage Lockout Enter | | 6.0 | 7.0 | 8.0 | V |
| $V_{DD}$_Clamp | VDD Over Voltage Protection trigger | I($V_{DD}$)=10mA | | | 60 | V |
| **Feedback Input Section(FB Pin)** | | | | | | |
| $V_{FB\_Open}$ | FB Open Loop Voltage | | | 4.75 | | V |
| $A_V$ | PWM input gain ΔVFB/ΔVCS | | | 1.71 | | V/V |
| $D_{MAX}$ | Max duty cycle | VFB=3V, VCS=0.3V | 77 | 80 | 83 | % |
| $V_{Ref\_Green}$ | The threshold enter green mode | | | 2.1 | | V |
| $V_{Ref\_Burst\_H}$ | The threshold exit Burst mode | | | 1.25 | | V |
| $V_{Ref\_Burst\_L}$ | The threshold enter Burst mode | | | 1.15 | | V |
| $I_{FB\_Short}$ | FB pin short circuit current | Short FB pin to GND | | 0.35 | | mA |
| $V_{TH\_PL}$ | Power Limiting FB Threshold Voltage | | | 3.7 | | V |
| $T_{D\_PL}$ | Power limiting Debounce Time | | | 55 | | mS |
| $Z_{FB\_IN}$ | Input Impedance | | | 20 | | KΩ |
| **Current Sense Input Section (CS Pin)** | | | | | | |
| $T_{SS}$ | Soft start time | | | 4 | | ms |
| $T_{LEB}$ | Leading edge blanking time | | | 300 | | ns |
| $T_{D\_OC}$ | Over Current Detection and Control Delay | | | 90 | | ns |
| $V_{TH\_OC}$ | Current Limiting Threshold Voltage with zero duty cycle | | | 0.75 | | V |
| $V_{OCP\_Clamp}$ | CS voltage clamper | | | 0.9 | | V |
| **Oscillator** | | | | | | |
| $F_{OSC}$ | Normal Oscillation Frequency | VFB=3V,VCS=0V | 60 | 65 | 70 | KHz |
| $F_{JR}$ | Frequency jitter range | | | ±4 | | % |
| $F_{Burst}$ | Burst Mode Switch Frequency | | | 20 | | KHz |
| **Power MOSFET Section** | | | | | | |
| BVdss | Drain-CS Breakdown Voltage | | 600 | 650 | | V |
| $R_{DS(ON)}$ | Drain-CS ON resistance | | | 1.7 | | Ω |
| **In-chip OTP** | | | | | | |
| $T_{OTP\_EN}$ | OTP enter | | | 150 | | ℃ |
| $T_{OTP\_EX}$ | OTP exit | | | 120 | | ℃ |

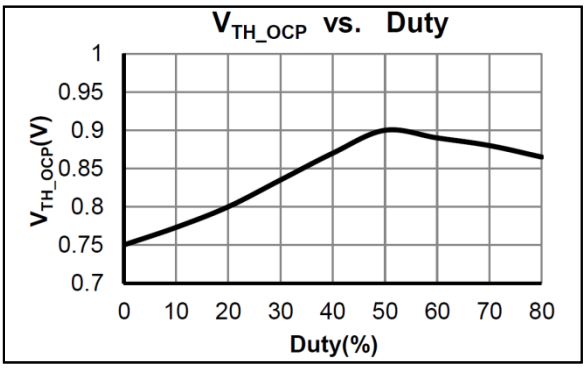
## Characterization Plots

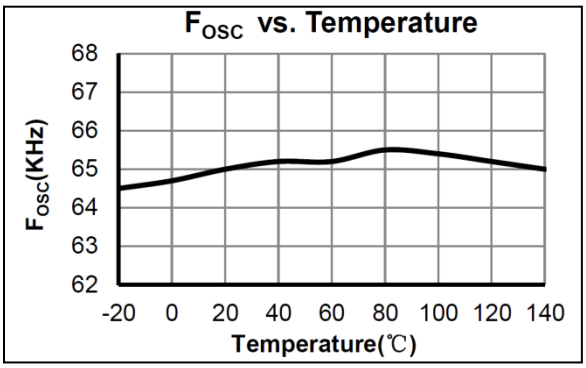


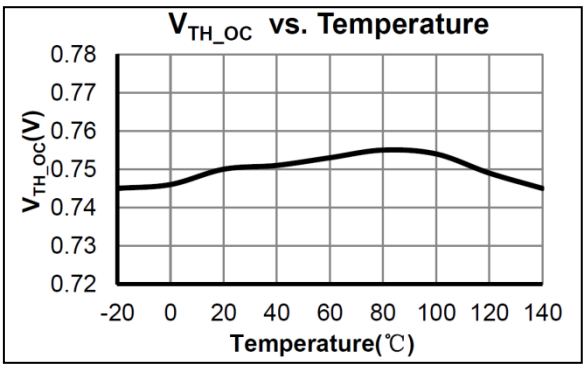



## Function Description

The ZS6659DM is a low power off-line SMPS Switcher optimized for off-line flyback converter applications in sub 36W power range. The Burst Mode control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

### Startup Current and Start up Control

Startup current of ZS6659DM is designed to be very low so that VDD could be charged up above $V_{DD\_ON}$ and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application.

### Operating Current

The Operating current of ZS6659DM is low at 2.0mA (typical). Good efficiency is achieved with ZS6659DM low operation current together with the Burst Mode control features.

### Soft Start

ZS6659DM features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as VDD reaches $V_{DD\_ON}$, the CS peak voltage is gradually increased from 0.05V to the maximum level. Every restart up is followed by a soft start.

### Frequency jitter for EMI improvement

The frequency jitter is implemented in ZS6659DM. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

### Oscillator Operation

The switching frequency of ZS6659DM is internally fixed at 65KHz. No external frequency setting components are required for PCB design simplification.

### Multi-mode Operation for High Efficiency

ZS6659DM is a multi-mode controller. The controller changes the mode of operation according to the FB pin voltage. At the normal operating condition, the IC operates in traditional fix frequency (65KHz) PWM mode. As the output load current is decreased, the IC enter into green mode smoothly from the PWM mode. In this mode, the switching frequency will start to linearly decrease from 65KHz to 20KHz. So the switching loss is minimized and the high conversion efficiency can be achieved. At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOS, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light or no load condition to improve the conversion efficiency.

At light load or no load condition, the FB input drops below $V_{Ref\_Burst\_L}$ and device enters Burst Mode control. The Gate drive output switches when FB input rises back to $V_{Ref\_Burst\_H}$. Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

### Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in ZS6659DM current mode PWM control. The switch current is detected by a sense resistor into the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

### Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp into the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

### Driver

The internal power MOSFET in ZS6659DM is driven by a dedicated gate driver for power switch control. Too weak the gate driver strength results in higher conduction and switch loss of MOSFET while too strong gate driver strength results the compromise of EMI.

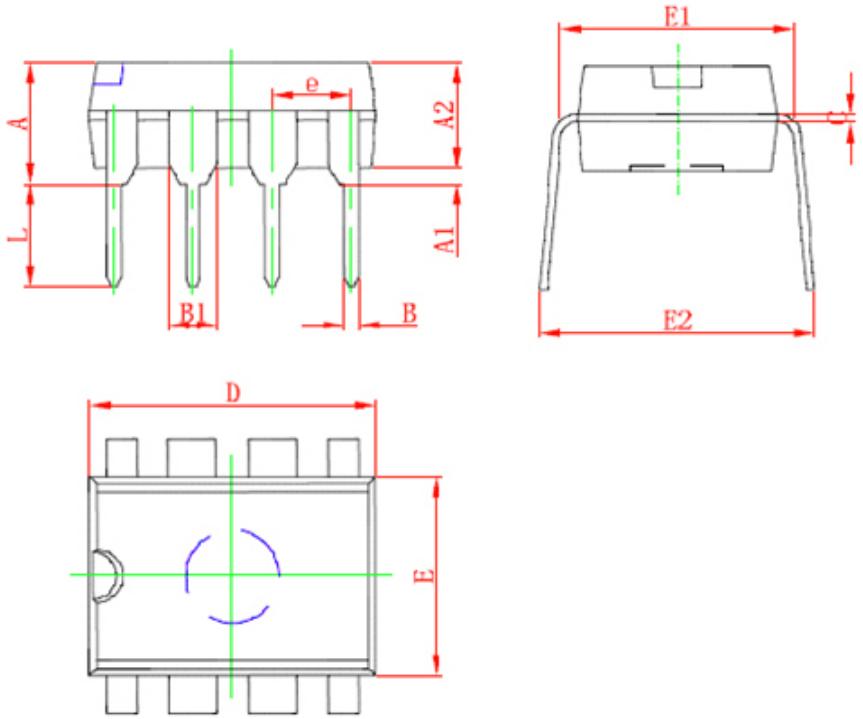
A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme.

### Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on VDD (UVLO), Over Temperature Protection (OTP), VDD Over Voltage Protection (OVP). The OCP is line voltage compensated to achieve constant output power limit over the universal input voltage range. At overload condition when FB input voltage exceeds power limit threshold value for more than $T_{D\_PL}$, control circuit reacts to shut down the converter. It restarts when VDD voltage drops below UVLO limit.

## Package Information

### DIP-8




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 3.710 | 4.310 | 0.148 | 0.0170 |
| A1 | 0.510 | | 0.020 | |
| A2 | 3.200 | 3.600 | 0.126 | 0.142 |
| B | 0.380 | 0.570 | 0.015 | 0.022 |
| B1 | 1.524(BSC) | | 0.060(BSC) | |
| C | 0.204 | 0.360 | 0.008 | 0.014 |
| D | 9.000 | 9.400 | 0.3540 | 0.370 |
| E | 6.200 | 6.600 | 0.2440 | 0.260 |
| E1 | 7.320 | 7.920 | 0.288 | 0.312 |
| e | 2.540(BSC) | | 0.100(BSC) | |
| L | 3.000 | 3.600 | 0.118 | 0.142 |
| E2 | 8.400 | 9.000 | 0.331 | 0.354 |