Features

- Full 16-bit performance
- 2.7 – 5.5 V single-supply operation
- High accuracy: INL 1LSB
- Fast settling speed: 1μs
- 10 nV/ √ Hz output noise density
- Unbuffered voltage output
- SPI compatible interface
- Power-on reset to 0V
- Low glitch: 10 nV-sec
- TPC2160 package: SOP-8
- TPC2161 package: SOP-14

Applications

- Data acquisition systems
- Automatic test equipment
- Industrial process control

Description

The TPC2160, TPC2161 are single channel, 16-bit, voltage output digital-to-analog converters with SPI interface. They accept a wide supply voltage range.

TPC2160 output is 0V to V_{REF}, and TPC2161 can provides bipolar output $\pm V_{REF}$ with external buffer and internal feedback resistor ladder.

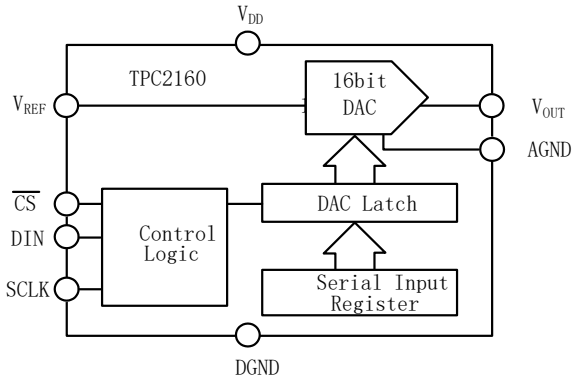
The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0V.

The DACs provides 16bit resolution over the full specified temperature range of −40 °C to 105 °C.

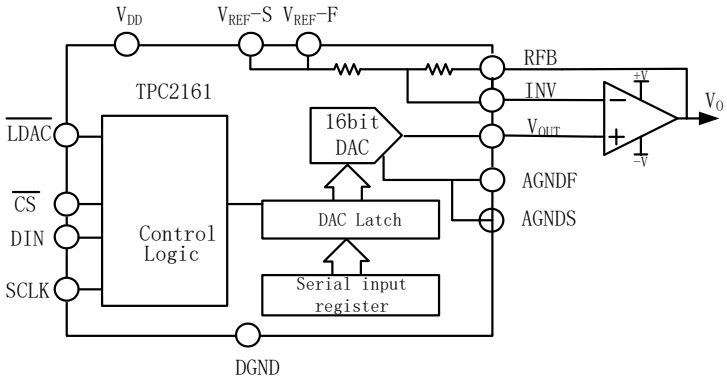
The DACs achieve a 1μs settling time. The outputs are unbuffered, with low power consumption and low offset errors.

Providing a low noise performance of 10 nV/√Hz and low glitch, the DACs are suitable for deployment across multiple end systems.

Functional Block Diagram



TPC2160S1



TPC2161S1

Table of Contents

Revision History

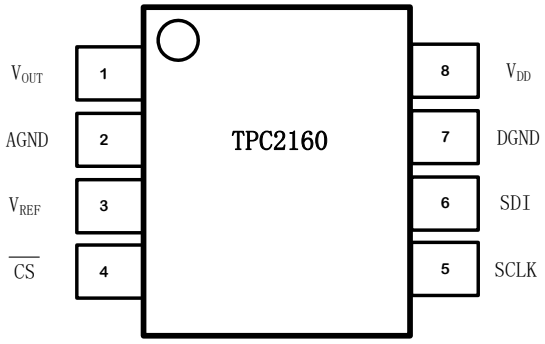
Date	Revision	Notes
2021/6/16	A.01	Initial version
2021/8/24	A.02	Update Absolute Maximum Ratings
2022/1/17	A.03	Update reference input impedance
2022/12/27	A.04	Correct TPC2161 name suffix.

Order Information

Model Name	Order Number	Package	MSL	Transport Media, Quantity	Marking Information
TPC2160S1	TPC2160S1L1A-SO1R-S	SOP-8	1	Tape and Reel, 4,000	2160
TPC2161S1	TPC2161S1L1-SO2R	SOP-14	1	Tape and Reel, 2,500	2161

Pin Configuration and Functions

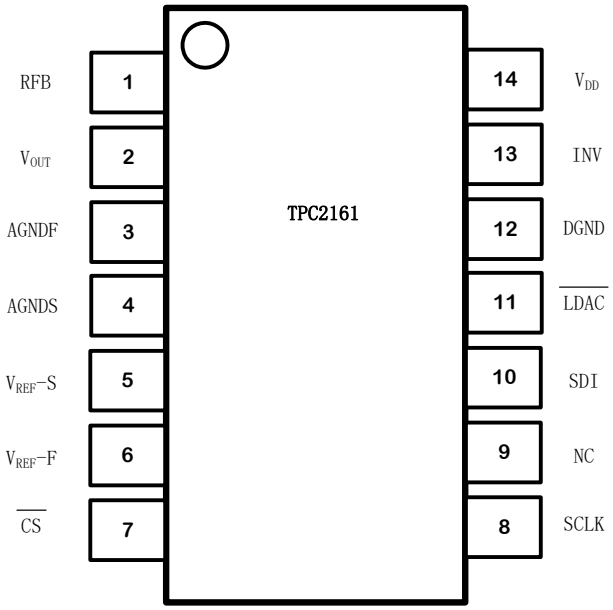
Top view



Pin Functions – TPC2160

Pin		Description
1	V_{OUT}	DAC analog output.
2	AGND	Analog Ground.
3	V_{REF}	Voltage Reference Input for the DAC.
4	$\overline{CS}$	Chip select input (active low)
5	SCLK	Clock Input. Data is clocked into the input register on the rising edge of SCLK.
6	SDI	Serial Data Input.
7	DGND	Digital Ground.
8	V_{DD}	Analog Supply Voltage

Top view



Pin Functions – TPC2161

Pin		Description
1	RFB	Feedback resistor. Connect to the output of external operational amplifier in bipolar mode.
2	V_{OUT}	Analog output of DAC
3	AGNDF	Analog ground (Force)
4	AGNDS	Analog ground (Sense)
5	V_{REF}–S	Voltage reference input (Sense). Connect to external voltage reference
6	V_{REF}–F	Voltage reference input (Force). Connect to external voltage reference
7	$\overline{CS}$	Chip select input (active low). Data are not clocked into SDI unless $\overline{CS}$ is low.
8	SCLK	Serial clock input.
9	NC	No internal connection
10	SDI	Serial data input. Data are latched into input register on the rising edge of SCLK.
11	$\overline{LDAC}$	Load DAC control input. Active low. When $\overline{LDAC}$ is Low, the DAC latch is simultaneously updated with the content of the input register.
12	DGND	Digital ground
13	INV	Junction point of internal scaling resistors. Connect to external operational amplifier inverting input in bipolar mode.
14	V_{DD}	Analog power supply, +3 V to +5 V.

Specifications

Absolute Maximum Ratings[Note1]

Parameter	Min	Typ	Max	Unit
Supply Voltage: $V^+ – V^–$	- 0.3		6	V
Analog input Voltage	- 0.3		V^+ + 0.3	V
Digital input voltage to DGND	-0.3		V^+ + 0.3	V
V_{OUT} to AGND	-0.3		V^+ + 0.3	V
AGND, AGNDF, AGNDS to DGND	- 0.3		+ 0.3	V
Input Current:+ IN, - IN [Note 2]	- 10		+ 10	mA
Output Current: OUT	- 10		+ 10	mA
Operating Temperature Range	- 40		105	°C
Maximum Junction Temperature			150	°C
Storage Temperature Range	- 65		150	°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The inputs are protected by ESD protection diodes to each power supply.

ESD Ratings

Parameter		Condition	Minimum Level	UNIT
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001	5.5	kV
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002	1.5	kV

Thermal Information

PACKAGE	θ_{JA}	θ_{JC}	UNIT
SOP-8	112.4	64.1	℃/W
SOP-14	96.7	46.7	℃/W

Electrical Characteristics

V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ VREF ≤ V_{DD}, AGND = DGND = 0 V. All specifications TA = TMIN to TMAX, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC PERFORMANCE					
Linearity error				±1	LSB
Differential linearity error				±1	LSB
Gain error			±0.5	±7	LSB
Gain drift			±0.1		ppm/℃
Zero Code Error			±0.3	±2	LSB
Zero Code drift			±0.05		ppm/℃
OUTPUT CHARACTERISTICS					
Voltage output		0		V_{DD}	V
Output Impedance			6.25		kΩ
Feedback resistor (TPC2161)	RFB, RINV		28		kΩ
Bipolar resistor matching	RFB / RINV		1		Ω/Ω
	Ratio error		0.01		%
DYNAMIC PERFORMANCE					
Settling time	To 1/2 LSB of FS, CL = 10 pF		1		uS
Slew rate	CL = 10 pF@5V		25		V/μs
Digital-to-analog glitch	1 LSB change around major carry		10		nV-s
Digital feedthrough			0.2		nV-s
Output noise（TPC2160）	DAC code = 0x8400, frequency = 1 kHz TA = +25°C		10		nV/√Hz
Output noise（TPC2161）	DAC code = 0x8400, frequency = 1 kHz TA = +25°C		18		nV/√Hz
Power-supply rejection	V_{DD} varies ±10%		±0.1		LSB
REFERENCE INPUT Note2					
Reference input voltage range		1.25		V_{DD}	V
Reference input impedance Note1 (TPC2160)	Unipolar mode	8.5			kΩ
Reference input impedance Note1 (TPC2161)	Unipolar mode	6.5			kΩ
Reference –3dB bandwidth, BW	Code = FFFFh		1.3		MHz
Reference feedthrough	Code = 0000h, VREF = 1 VPP at 100 kHz		1		mV
Signal-to-noise ratio, SNR			92		dB
Reference input capacitance	Code = 0000h		75		pF
	Code = FFFFh		120		pF

Note 1: Reference input resistance is code-dependent, minimum at 0x8555.

Note 2: Guaranteed by design, not subject to production test.

Electrical Characteristics (continued)

V_{DD} = 2.7 V to 5.5 V, 2.5 V ≤ VREF ≤ V_{DD}, AGND = DGND = 0 V. All specifications TA = TMIN to TMAX, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
VIL Input low voltage				0.2*V_{DD}	V
VIH Input high voltage		0.8*V_{DD}			V
Input current			±0.5	5	μA
Input capacitance Note 2				10	pF
Hysteresis voltage Note 2			0.4		V
POWER SUPPLY					
VDD Power-supply voltage		2.7		5.5	V
IDD Power-supply current	V_{DD}=5			150	μA
Power	V_{DD}=5			825	μW
SPI					
Fclk				25	MHz

Note 1: Reference input resistance is code-dependent, minimum at 0x8555.

Note 2: Guaranteed by design, not subject to production test.

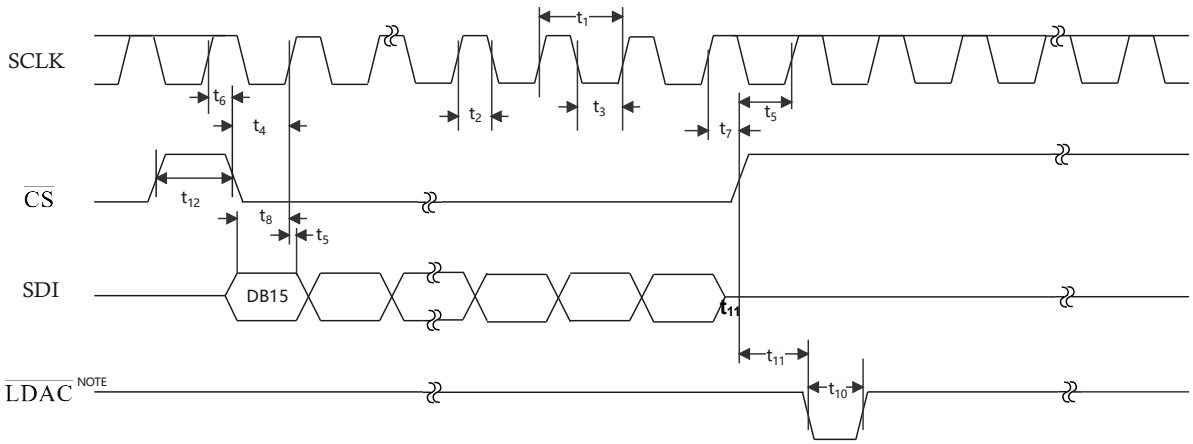
Timing Characteristics

V_{DD} = 2.7 V to 5.5 V ±10%, VREF = 2.5 V, VINH = 3 V and 90% of V_{DD}, VINL = 0 V and 10% of V_{DD}, AGND = DGND = 0 V; TA = TMIN to TMAX, unless otherwise noted.

Parameter[Note1,2]	Limit	Unit	Description
f_{SCLK}	25	MHz max	SCLK cycle frequency
t_1	40	ns min	SCLK cycle time
t_2	20	ns min	SCLK high time
t_3	20	ns min	SCLK low time
t_4	10	ns min	$\overline{CS}$ low to SCLK high setup
t_5	15	ns min	$\overline{CS}$ high to SCLK high setup
t_6	30	ns min	SCLK high to $\overline{CS}$ low hold time
t_7	20	ns min	SCLK high to $\overline{CS}$ high hold time
t_8	15	ns min	Data setup time
t_9	4	ns min	Data hold time (VINH = 90% of VDD, VINL = 10% of VDD)
t_{10}	7.5	ns min	Data hold time (VINH = 3V, VINL = 0 V)
t_{11}	30	ns min	$\overline{LDAC}$ pulse width
t_{12}	30	ns min	$\overline{CS}$ high to $\overline{LDAC}$ low setup

Note 1: Guaranteed by design and characterization. Not production tested

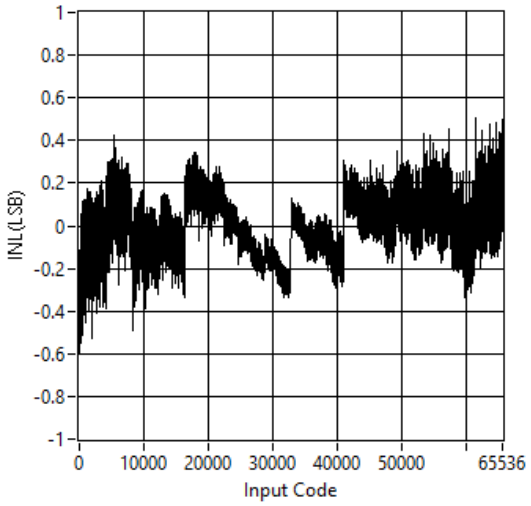
Note 2: All input signals are specified with $t_R = t_F$ = 1 ns/V and timed from a voltage level of $(V_{INL} + V_{INH})/2$.

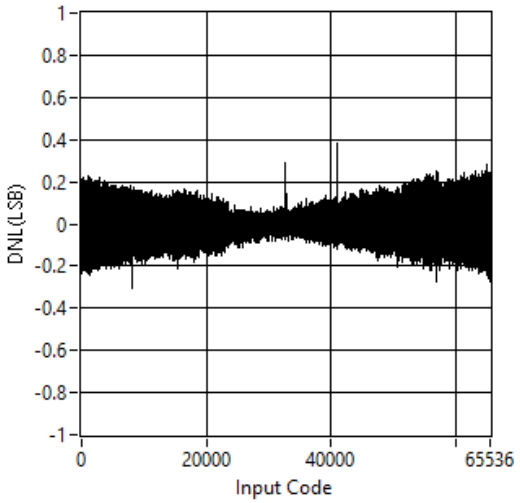


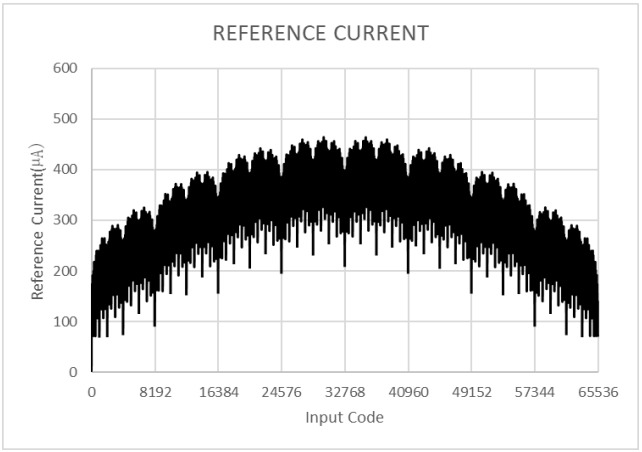
Note: TPC2161 ONLY. CAN BE TIED PERMANENTLY LOW IF REQUIRED

Typical Performance Characteristics

VS = +5V, VCM = 0V, RL = Open, unless otherwise specified.







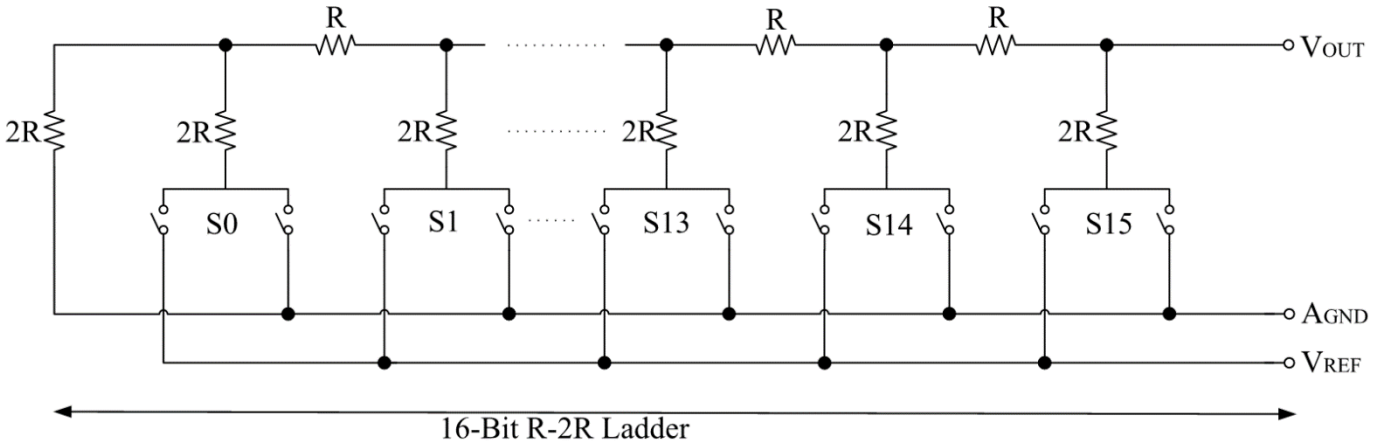
Detailed Description

Overview

The TPC2160 and TPC2161 are single channel 16-bit DACs with R-2R structure. They have an SPI serial interface, with 16-bit word format. The TPC2160 and TPC2161 are reset to zero code.

Digital-To-Analog Sections

A simplified DAC diagram is shown below. The 16 bits of the data word drive switches S0 to S15 of a 16-bit voltage mode R-2R ladder network.



Feature Description

Output Range

The output of the DAC is

$$V_{OUT} = (V_{REF} \times Code)/65536$$

Where *Code* is the decimal data word loaded to the DAC latch.

Power-On Reset

The TPC2160 and TPC2161 have power on reset function, to make sure the output is a known state at power-up, and the DAC Registers are zero until new data are loaded. Therefore, after power-up, the output of V_{OUT} is 0 V.

Serial Interface

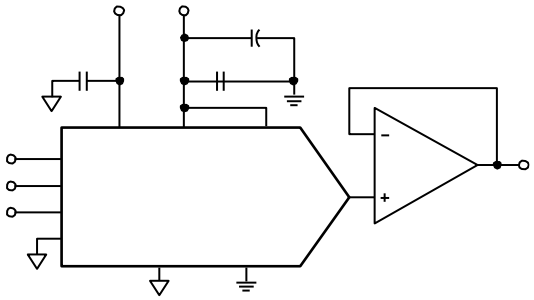
The digital interface is a standard 3-wire serial interface compatible with SPI.

When $\overline{CS}$ turns low, the transmission is started, and the SDI data is shifted in and latched on the edge of SCLK. The data registers are 16-bit, so $\overline{CS}$ must go high after 16 SCLKs to transfer a whole data word.

In the TPC2160, the input register is latched to DAC immediately after the input register is loaded, so the DAC output is updated at the same time.

The TPC2161 has an $\overline{LDAC}$ pin. After $\overline{CS}$ goes high, the DAC register can be updated by bringing $\overline{LDAC}$ low. And $\overline{LDAC}$ can also be tied low permanently, in this case, the DAC register is updated immediately after the input register is loaded, and DAC output is updated at the same time.

TPC2160 Unipolar Output Operation



DAC Latch Contents		
MSB	**LSB**	**Analog Input**
1111 1111 1111 1111		V_{REF} × (65,535 / 65,536)
1000 0000 0000 0000		V_{REF} × (32,768 / 65,536) = ½ V_{REF}
0000 0000 0000 0001		V_{REF} × (1 / 65,536)
0000 0000 0000 0000		0 V

Considering gain error, INL and zero-scale error, the worst-case output voltage may be calculated by following equation:

Unipolar Mode Worst-Case Output

$$V_{OUT\_U} = \frac{D}{2^{16}} \times (V_{REF} + V_{GE}) + V_{ZSE} + INL$$

Where:

V_{OUT_U} = Unipolar mode worst-case output

D = Code loaded to DAC

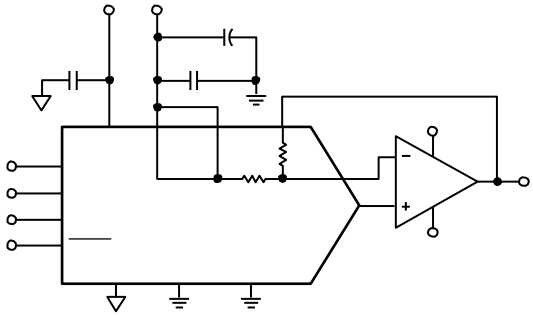
V_{REF} = Reference voltage

V_{GE} = Gain error in volts

V_{ZSE} = Zero-scale error in volts

INL = Integral nonlinearity in volts

TPC2161 Bipolar Output Operation



DAC Latch Contents		
MSB	**LSB**	**Analog Input**
1111 1111 1111 1111		+ V_{REF} × (32,767 / 32,768)
1000 0000 0000 0001		+ V_{REF} × (1 / 32,768)
1000 0000 0000 0000		0 V
0111 1111 1111 1111		− V_{REF}× (1 / 32,768)
0000 0000 0000 0000		− V_{REF} × (32,768 / 32,768) = − V_{REF}

Considering non-idealities of external amplifier, the worst-case output voltage may be calculated from the following equation:

Bipolar Mode Worst-Case Output

$$V_{OUT\_B} = \frac{\left[\left(V_{OUT\_U} + V_{OS}\right)(2 + RE) - V_{REF}(1 + RE)\right]}{1 + \frac{2 + RE}{A}}$$

Where:

V_{OS} = External operational amplifier input offset voltage

RE = RFB and RIN resistor matching error

A = Operational amplifier open-loop gain

Output Amplifier Selection

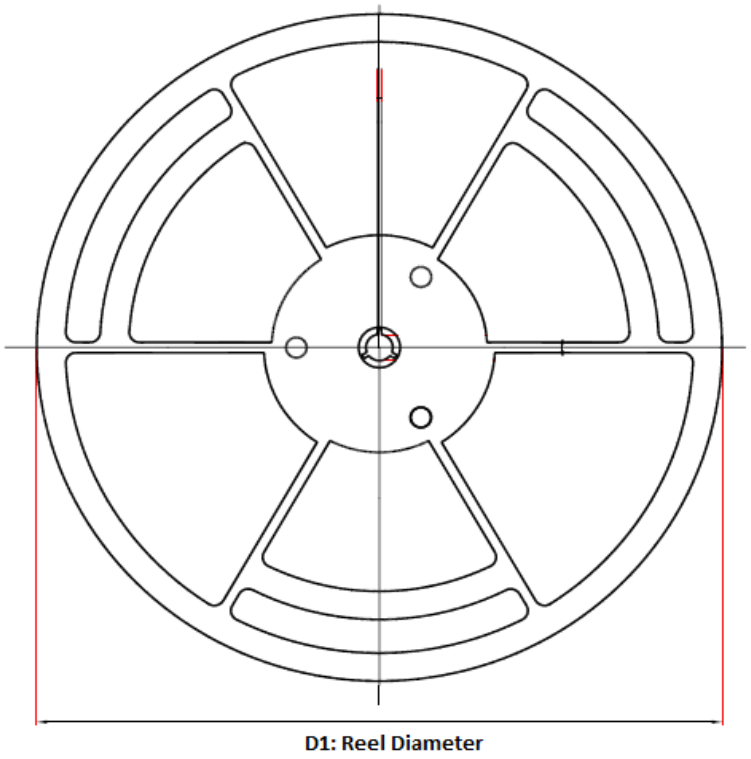
For bipolar mode, to provide the $\pm V_{REF}$ output, a precision amplifier should be used, supplied from a dual power supply.

In a single-supply application, selection of a suitable operational amplifier is also important. Input offset, input bias current, rail-to-rail input and output range, -3dB bandwidth and slew rate, are key features for amplifier selection.

Power Supply and Reference Bypassing

It is recommended that the reference and supply pins are bypassed with a 10 uF tantalum capacitor in parallel with a 0.1 uF ceramic capacitor, for good supply and noise suppression, and then accurate performance,

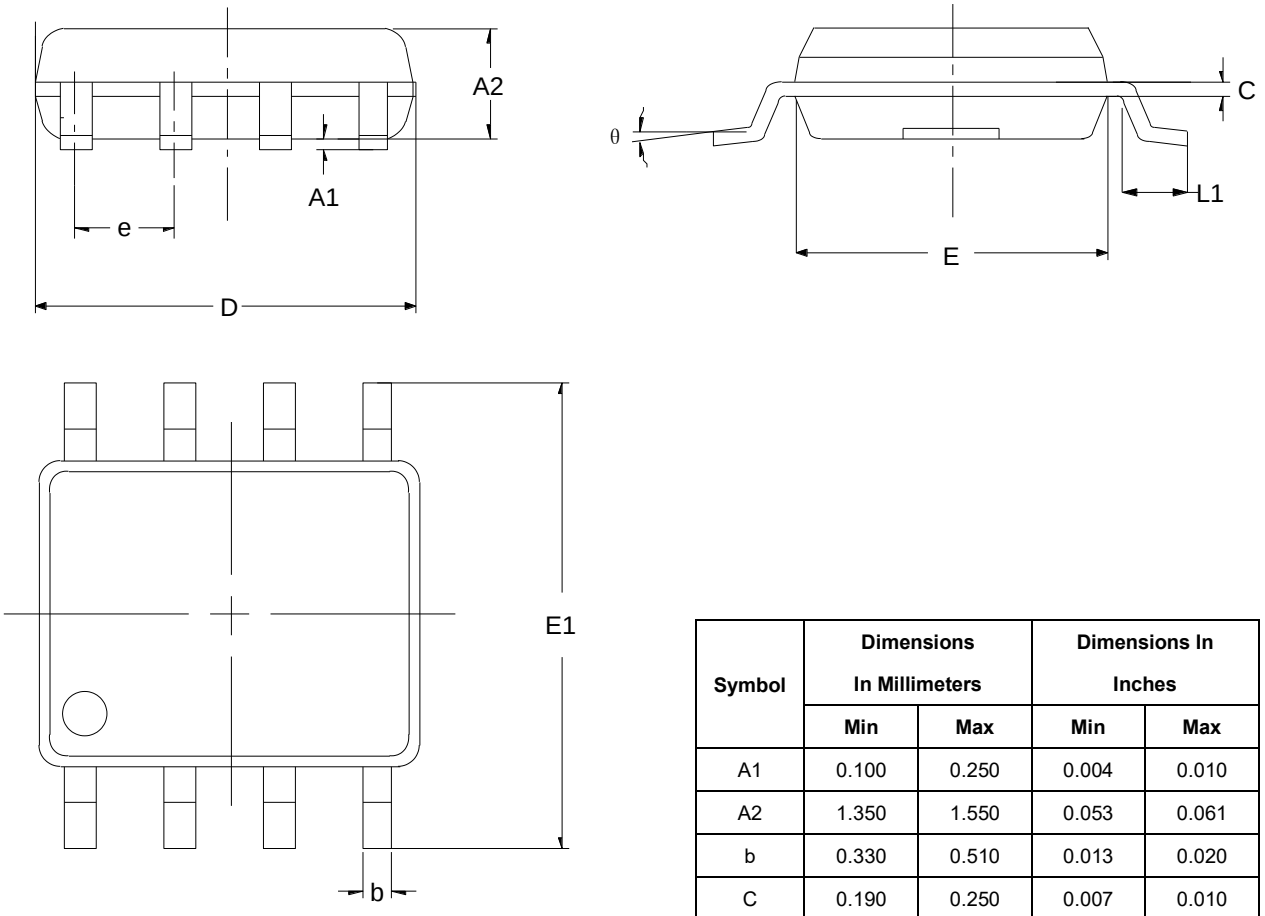
Tape and Reel Information



Order Number	Package	D1	W1	A0	B0	K0	P0	W0	Pin1 Quadrant
TPC2160S1L1A-SO1R-S	SOP-8	330.0	17.6	6.4	5.4	2.1	8.0	12.0	Q1
TPC2161S1L1-SO2R	SOP-14	330.0	21.6	6.5	9.0	2.1	8.0	16.0	Q1

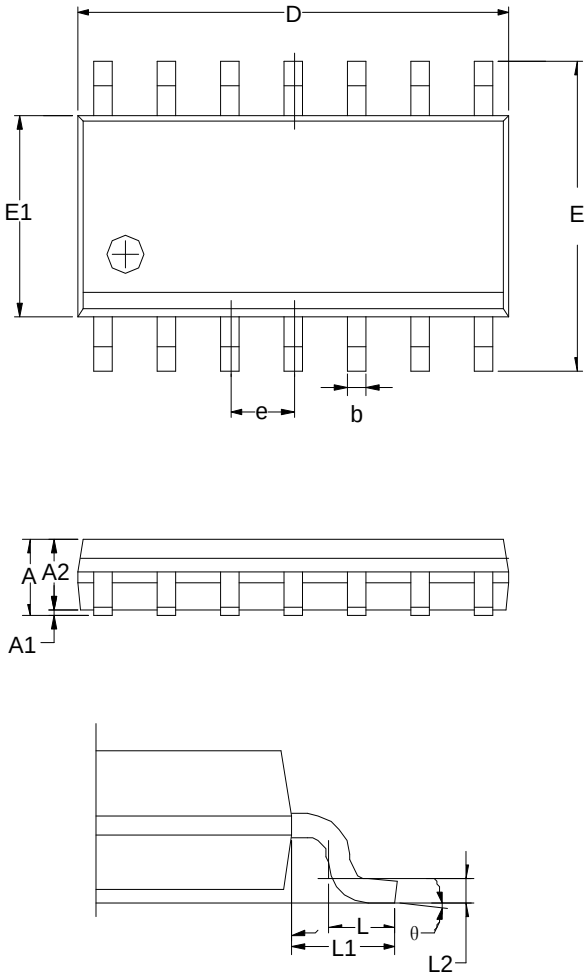
Package Outline Dimensions

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.70	5.100	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270TYP		0.050TYP	
L1	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

SOP-14



Symbol	Dimensions In Millimeters		
	MIN	TYP	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
b	0.36		0.49
D	8.53	8.63	8.73
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.45	0.60	0.80
L1	1.04 REF		
L2	0.25 BSC		
θ	0°		8°