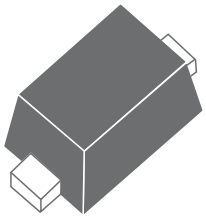
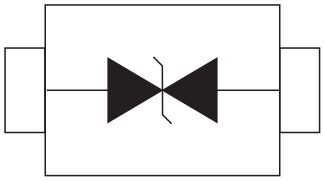
Electro-Static Discharge for Automobile
AESD05EB
Bidirectional TVS Diode

SOD-523



Pin Configuration



Features

- 50 Watts Peak Pulse Power per Line (tp=8/20μs)
- Protects one birectional I/O line
- Low clamping voltage
- Working voltages : 5V
- Low leakage current
- AEC-Q101

IEC Compatibility

- IEC61000-4-2 (ESD) ±20kV (air), ±20kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ηs)

Applications

- Cell Phone Handsets and Accessories
- Microprocessor based equipment
- Personal Digital Assistants(PDA's)
- Notebooks,Desktops,and Servers
- Portable Instrumentation
- Peripherals
- Pagers

Mechanical Characteristics

- SOD-523 Package
- Molding Compound Flammability Rating:L 94V-O
- Quantity Per Reel:5000pcs
- Reel Size:7 inch
- Lead Finish:Lead Free

Maximum Ratings(T_A=25℃ unless otherwise noted)

Maximum Ratings(@25℃ Unless Otherwise Specified)			
Parameter	**Symbol**	**Value**	**Units**
Peak Pulse Power(tp=8/20μs waveform)	P_{PP}	50	Watts
Lead Soldering Temperature	T_L	260(10 sec.)	℃
Operating Temperature Range	T_J	-55~150	℃
Storage Temperature Range	T_{STG}	-55~150	℃

Electrical Characteristics(Ta=25℃ unless otherwise specified)

AESD05EB(Marking: 0)						
Parameter	**Symbol**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Units**
Reverse Stand-off Voltage	V_{RWM}				5	V
Breakdown Voltage	V_{BR}	I_T=1mA	5.8			V
Clamping Voltage	V_C	I_{PP}=5A,tp=8/20μs			10	V
Reverse Leakage Current	I_R	@V_{RWM}			1	μA
Junction Capacitance	$C_{I/O}$	0Vdc,f=1MHz Between I/O Pins and GND		12	15	pF

Ratings and Characteristic Curves

Fig.1 Pulse Waveform

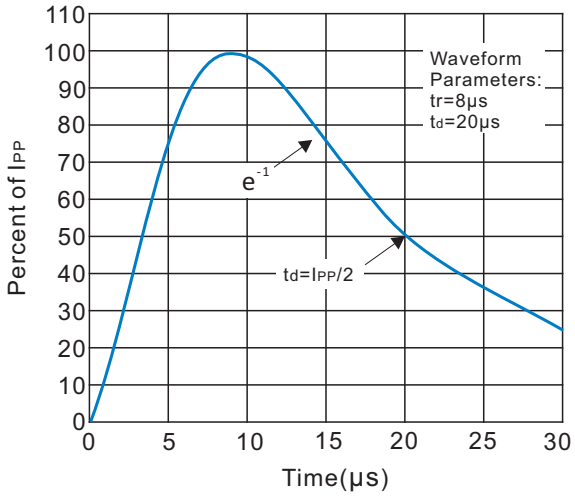
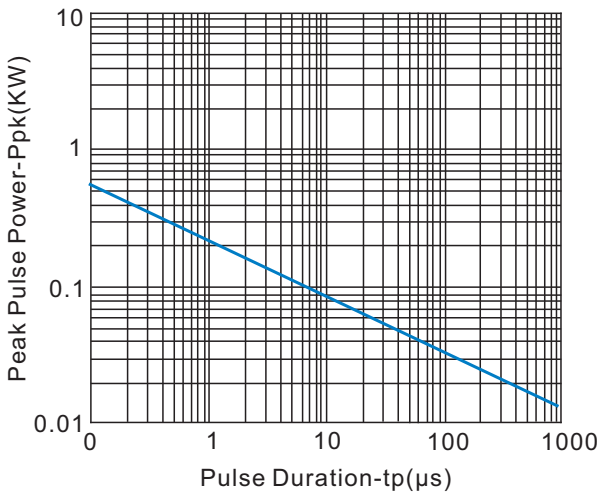
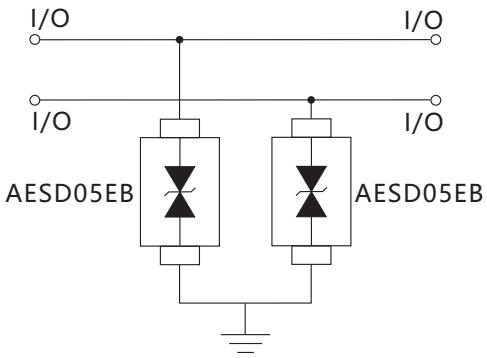


Fig.2 Non-Repetitive Peak Pulse Power vs.Pulse Time



Application Information

I/O Protection



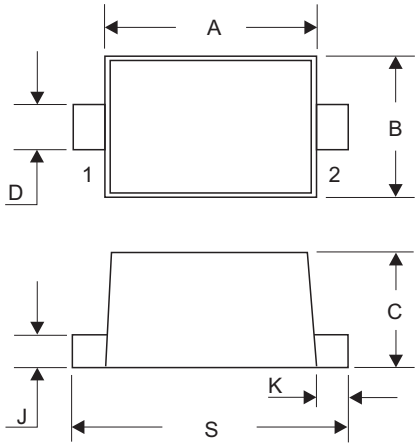
PCB Layout Recommendations

The location and circuit board layout is critical to maximize the effectiveness of the I/O protection circuit. The following guidelines are recommended:

- Locate the protection devices as close as possible to the I/O connector. This allows the protection devices to absorb the energy of the transient voltage before it can be coupled into the adjacent traces on the PCB.
- Minimize the loop area for the high.speed data lines, power and ground lines to reduce the radiated emissions.
- Avoid running protection conductors in parallel with unprotected conductors
- Use ground planes wherever possible to reduce the parasitic capacitance and inductance of the PCB that degrades the effectiveness of a filter device.
- Using shared transient return paths to a common ground point.

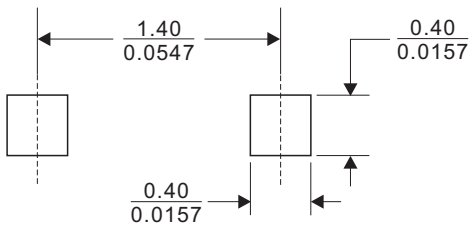
Dimensions(SOD-523)

SOD-523



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	1.10	1.30	0.043	0.051
B	0.70	0.90	0.028	0.035
C	0.50	0.70	0.020	0.028
D	0.25	0.35	0.010	0.014
J	0.07	0.20	0.0028	0.0079
K	0.15	0.25	0.006	0.010
S	1.50	1.70	0.059	0.067

Recommended Mounting Pad Layout



Dimensions in (millimeters / inches)