

TFB0504

Half-Bridge Gate Driver

Features

- Floating high-side driver in bootstrap operation to 100V
- Drives two N-channel MOSFETs or IGBTs in a half bridge configuration
- Integrated bootstrap diode for compact design
- 300mA source/550mA sink output current capability
- Outputs tolerant to negative transients
- Internal dead time of 420ns to protect MOSFETs
- Wide low side gate driver supply voltage: 10V to 20V
- Logic input (IN and SD*) 3.3V capability
- Schmitt triggered logic inputs
- Undervoltage lockout for V_{cc} (logic and low side supply)
- Extended temperature range: -40°C to +125°C
- Space saving TDFN-10 3x3mm package

Description

The TFB0504 is a half-bridge gate driver with integrated bootstrap diode capable of driving N-channel MOSFETs and IGBTs in a half-bridge configuration. TF Semiconductor's advanced process enables the floating high-side driver to operate to 100V in a bootstrap configuration.

The TFB0504 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. TFB0504 has a fixed internal deadtime of 420ns (typical).

To simplify design and decrease the BOM, the TFB0504 has an integrated bootstrap diode. Also the TFB0504 is offered in a space saving TDFN-10 package and operates over an extended -40 °C to +125 °C temperature range.



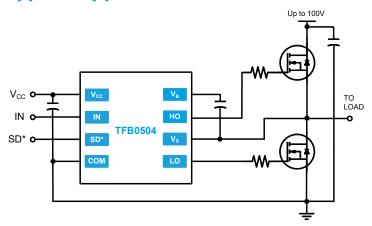
TDFN-10

Year Year Week Week

Applications

- Stepper motor drives
- DC-DC Converters
- Battery powered tools
- BLDC motor drive

Typical Application

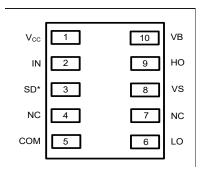


Ordering Information

PART NUMBER	PACKAGE	PACK / Qty	MARK
TFB0504-NHS	TDFN-10	Tube / 120	YYWW
TFB0504-NHP	TDFN-10	T&R / 3,000	TFB0504

www.tfsemi.com Rev 1.0



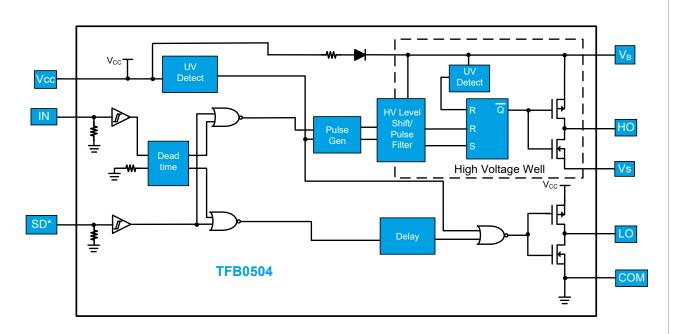


Top View: TDFN-10

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
V _{cc}	1	Logic and low side supply
IN	2	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
SD*	3	Logic input for shutdown, enabled low turns off HO and LO
NC	4, 7	No connect
СОМ	5	Low-side and logic return
LO	6	Low-side gate drive output
V _s	8	High-side floating supply return
НО	9	High-side gate drive output
V _B	10	High-side floating supply

Functional Block Diagram





Absolute Maximum Ratings (NOTE1)

$V_{\scriptscriptstyle B}$ - High side floating supply voltage0.3V to +124V
V_s - High side floating supply offset voltage V_B -24V to V_B +0.3V
V_{HO} -High side floating output voltage V_s -0.3V to V_B +0.3V
dV _s /dt-Offset supply voltage transient50 V/ns
V _{cc} - Low-side fixed supply voltage0.3V to +24V
V_{10} - Low-side output voltage0.3V to V_{cc} +0.3V
V_{IN}^{-} - Logic input voltage (IN and SD*)0.3V to V_{CC}^{-} +0.3V
IN 3 , CC

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

P_D - Package power dissipation at $T_A \le 25$ °C TDFN-10	0.4W
TDFN-10 Thermal Resistance (NOTE2)	
$ heta_{JA}$	64°C/W
θ_{JC}	
T _J - Junction operating temperature	+150 °C
T _L - Lead Temperature (soldering, 10 seconds)	+300°C
T _{stg} - Storage temerature	55 to 150 °C

NOTE2 When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V _B	High side floating supply absolute voltage	V _s + 10	V _s + 20	V
V _s	High side floating supply offset voltage	NOTE3	100	V
V _{HO}	High side floating output voltage	V _s	$V_{\scriptscriptstyle B}$	V
V _{cc}	Low side fixed supply voltage	10	20	V
V _{LO}	Low side output voltage	0	V _{cc}	V
V _{IN}	Logic input voltage (IN and SD*)	0	5	V
T _A	Ambient temperature	-40	125	°C

NOTE3 Logic operational for VS of -5V to +100V.



DC Electrical Characteristics (NOTE4)

 $\rm V_{BIAS} \, (V_{CC}, V_{BS} \,) = 15V, T_A = 25 \, ^{\circ} C$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit	
V _{IH}	Logic "1" (IN) & Logic "0" (SD*) input voltage	V _{CC} = 10V to 20V	2.5				
V _{IL}	Logic "0" (IN) & Logic "1" (SD*) input voltage	NOTE5			0.8	V	
V _{OH}	High level output voltage, V _{BIAS} - V _O	I _o = 2mA		0.05	0.2		
V _{OL}	Low level output voltage, V _o	I _o = 2mA		0.02	0.1		
I _{LK}	Offset supply leakage current	VB = VS = 100V			50		
I _{BSQ}	Quiescent V _{BS} supply current	V _{IN} = 0V or 5V		7	50	μΑ	
I _{ccq}	Quiescent V _{cc} supply current	V _{IN} = 0V or 5V		350	500		
I _{IN+}	Logic "1" input bias current	IN = 5V, SD* = 0V		3	10		
I _{IN-}	Logic "0" input bias current	IN = 0V, SD* = 5V			5		
V_{CCUV+}	V _{cc} supply under-voltage positive going threshold		7.0	8.4	9.8		
V _{CCUV} -	V _{cc} supply under-voltage negative going threshold		6.5	7.8	9.3	V	
V_{BSUV+}	V _{BS} supply under-voltage positive going threshold		3.6	4.5	5.6	V	
V_{BSUV}	V _{BS} supply under-voltage negative going threshold		3.0	3.7	4.6	V	
I _{O+}	Output high short circuit pulsed current	$V_O = 0V$, PW $\leq 10 \mu s$	130	300			
l ₀₋	Output low short circuit pulsed current	$V_0 = 15V, PW \le 10 \ \mu s$	270	550		mA	

NOTE4 The V_{liv} V_{Th} and I_{liv} parameters are applicable to the two logic input pins: IN and SD*. The V_{o} and I_{o} parameters are applicable to the respective output pins: HO and LO.

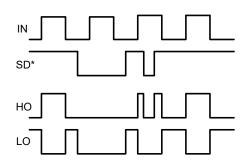
NOTE5 For optimal operation, it is recommended that the input pulse (to IN and SD*) should have an amplitude of 2.5V minimum with a pulse width of 840ns minimum.

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AC Electrical Characteristics $V_{BIAS}(V_{CC}, V_{BS}) = 15V, C_L = 1000 pF, and T_A = 25 \, ^{\circ}C$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t _{on}	Turn-on propagation delay	$V_s = 0V$		560	820	
t _{off}	Turn-off propagation delay	V _s = 600V		150	220	
t _{DM}	Delay matching, HS & LS turn-on/turn-off				70	ns
t _r	Turn-on rise time			80	170	ns
t _f	Turn-off fall time	$V_S = 0V$		35	90	
t _{DT}	Deadtime: t _{DT LO-HO} & t _{DT HO-LO}		300	420	650	



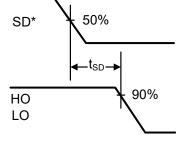


Figure 1. Input / Output Timing Diagram

Figure 2. Shutdown Waveform Definition

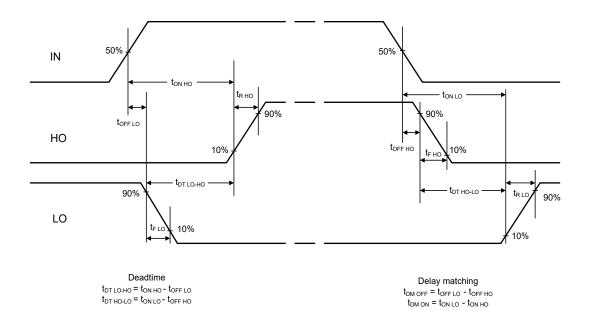
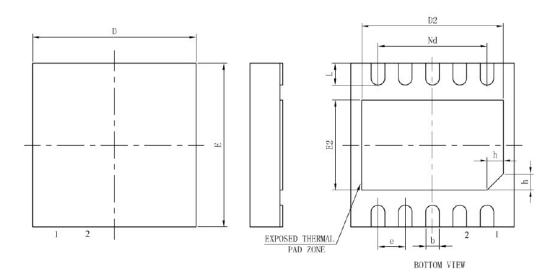


Figure 3. Switching time waveform definitions

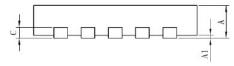


Package Dimensions (TDFN-10)

Please contact support@tfsemi.com for package availability.



SYMBOL	MILLIMETER			
SYMBOL	MIN	NOM	MAX	
A	0.70	0.75	0.80	
A1	-	0.02	0.05	
ь	0.18	0.25	0.30	
с	0.18	0.20	0.25	
D	2.90	3.00	3.10	
D 2	2.40	2.50	2.60	
с	0. 50BSC			
Nd	2. 00BSC			
E	2.90	3.00	3.10	
E2	1. 45	1.55	1. 65	
L	0.30	0.40	0.50	
h	0.20	0. 25	0.30	



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Revision History

Half-Bridge Gate Driver

Rev.	Change	Owner	Date
1.0	First release, AI datasheet	Keith Spaulding	6/7/2023

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