TF Semiconductor Solutions

TF21844M

Half-Bridge Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in a half-bridge configuration**
- **1.4A source / 1.8A sink output current capability**
- **Outputs tolerant to negative transients**
- **Programmable dead time to protect MOSFETs**
- **Wide low-side gate driver supply voltage: 10V to 20V**
- **Wide logic supply voltage offset voltage: -5V to 5V**
- **Logic input (IN and SD*) 3.3V capability**
- **Schmitt triggered logic inouts with internal pull down**
- **Undervoltage lockout for high and low side drivers**
- **Extended temperature range:-40°C to +125°C**

Description

The TF21844M is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductors's high voltage process enables the TF21844M's high side to switch to 600V in a bootstrap operation.

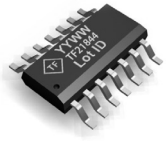
The TF21844M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. Programmable dead time, by an external resistor, provides more system level flexibility.

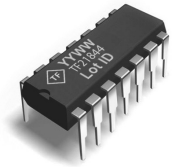
The TF21844M is offered in PDIP-14 and SOIC-14(N) packages. It operates over an extended -40 °C to +125 °C temperature range.

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

SOIC-14(N)





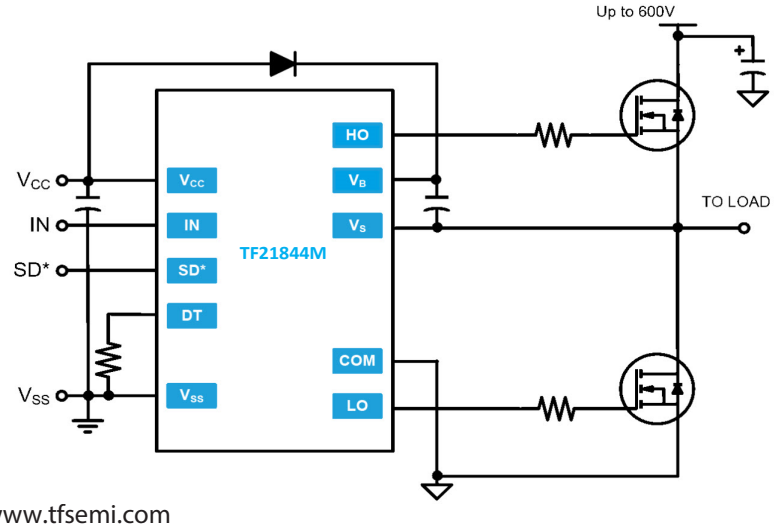
PDIP-14

Ordering Information

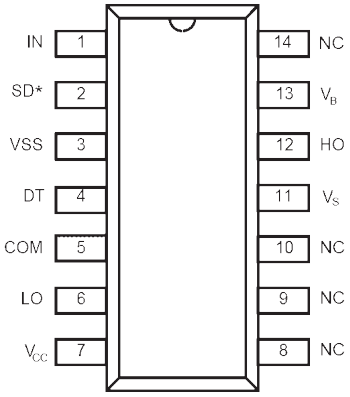
Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF21844M-TUU	SOIC-14(N)	Tube / 50	TF YYWW TF21844M Lot ID
TF21844M-TUH		T&R / 2500	
TF21844M-3BS	PDIP-14	Tube / 25	TF YYWW TF21844M Lot ID

Typical Application



Pin Diagrams



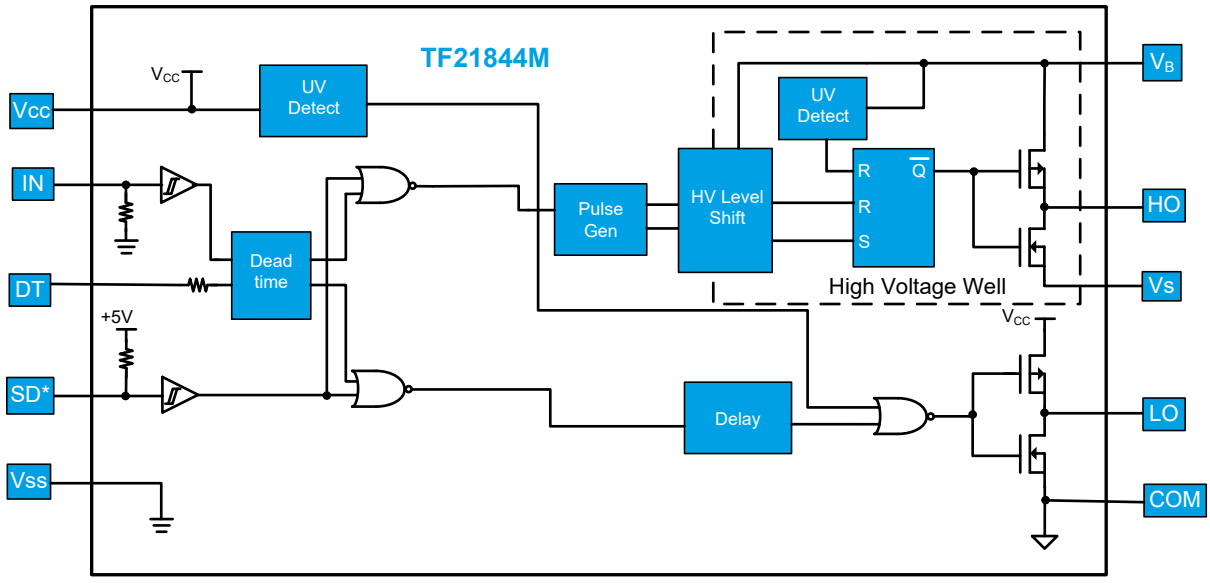
Top View: PDIP-14, SOIC-14

TF21844M

Pin Descriptions

PIN NAME	PIN DESCRIPTION
IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO (referenced to VSS).
SD*	Logic input for shutdown (referenced to VSS), enabled low.
V_{SS}	Logic ground
DT	Programmable deadtime lead, referenced to VSS.
COM	Low-side return
LO	Low-side gate drive output
V_{CC}	Low-side and logic fixed supply
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S/dt - Offset supply voltage transient.....50 V/ns
V_{DT}- Programmable dead time pin voltage....V_{SS}-0.3V to V_{CC}+0.3V

V_{CC} - Logic and Low side fixed supply voltage.....-0.3V to +24V
V_{LO} - Low side output voltage.....-0.3V to V_{CC}+0.3V
V_{SS} - Logic supply offset voltage.....V_{CC}-24V to V_{CC}+0.3V
V_{IN} - Logic input voltage (IN and SD*).....V_{SS}-0.3V to V_{CC}+0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \le 25$ °C
SOIC-14.....1.0W
PDIP-14.....1.6W

SOIC-14 Thermal Resistance ***(NOTE2)***
θ_{JA}.....120 °C/W
PDIP-14 Thermal Resistance ***(NOTE2)***
θ_{JA}.....75 °C/W

T_J - Junction operating temperature .....+150 °C
T_L - Lead temperature (soldering, 10s) ..... +300 °C
T_{stg} - Storage temperature range .....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***	600	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Logic and Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (IN & SD*)	V_{SS}	5	V
V_{DT}	Programmable deadtime pin voltage	V_{SS}	V_{CC}	V
V_{SS}	Logic ground	-5	+5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5V to 600V.*

DC Electrical Characteristics *(NOTE4)*

V_{CC} = V_{BS} = 15V, V_{SS} = COM, and T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage for HO & logic "0" for LO	V_{CC} = 10 V to 20 V ***NOTE5***	2.5			V
V_{IL}	Logic "0" input voltage for HO & logic "1" for LO				0.8	
$V_{SD, TH+}$	SD* input poitive going threshold		2.5			
$V_{SD, TH-}$	SD* input negative going threshold				0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 0A			1.4	
V_{OL}	Low level output voltage, V_O	I_O = 20mA			0.2	
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSO}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V	20	60	150	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V	0.4	1.0	1.8	mA
I_{IN+}	Logic "1" input bias current	IN= 5V, SD* = 0V		25	60	µA
I_{IN-}	Logic "0" input bias current	IN= 0V, SD* = 5V			1.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		8	8.9	9.8	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.4	8.2	9	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8	8.9	9.8	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9.0	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 µs	1.4	1.9		A
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 µs	1.7	2.3		

NOTE4 *The V_{IN}, V_{TH}, I_{IN} parameters are referenced to V_{SS} and are applicable to the two logic input pins: IN and SD*. The V_o and I_o parameters are referenced to COM and are applicable to the respective output pins: HO and LO.*

NOTE5 *For optimal operation, it is highly recommended that the input pulse (to IN and SD*) should have an amplitude of 2.5V minimum with a pulse width of 2 x tdt (deadtime) minimum.*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, V_{SS} = COM, C_L = 1000 pF, and T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	V_S = 0V		680	900	ns
t_{OFF}	Turn-off propagation delay	V_S = 0 V or 600V		270	400	
t_{SD}	Shut-down propagation delay			180	270	
$t_{DM\ ON}$	Delay matching, HS & LS turn-on				90	
$t_{DM\ OFF}$	Delay matching, HS & LS turn-off				40	
t_r	Turn-on rise time	V_S = 0V		40	60	
t_f	Turn-off fall time			20	35	
t_{DT}	Deadtime: $t_{DT\ LO\text{-}HO}$ & $t_{DT\ HO\text{-}LO}$	R_{DT}=0Ω	280	400	520	ns
		R_{DT}= 200kΩ	4	5	6	µs
t_{MDT}	Deadtime matching = $t_{DT\ LO\text{-}HO}$ - $t_{DT\ HO\text{-}LO}$	R_{DT}=0Ω		0	50	ns
		R_{DT}= 200kΩ		0	600	

Timing Waveforms

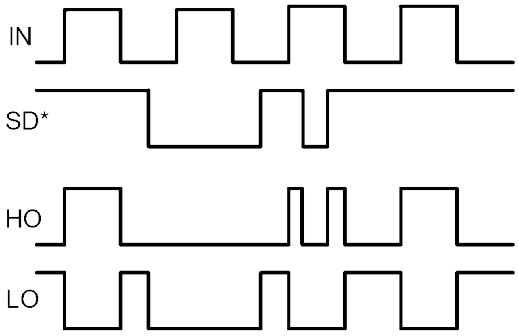


Figure 1. Input / Output Timing Diagram

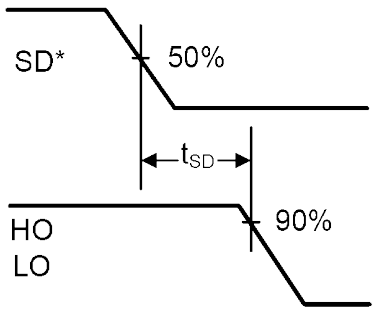
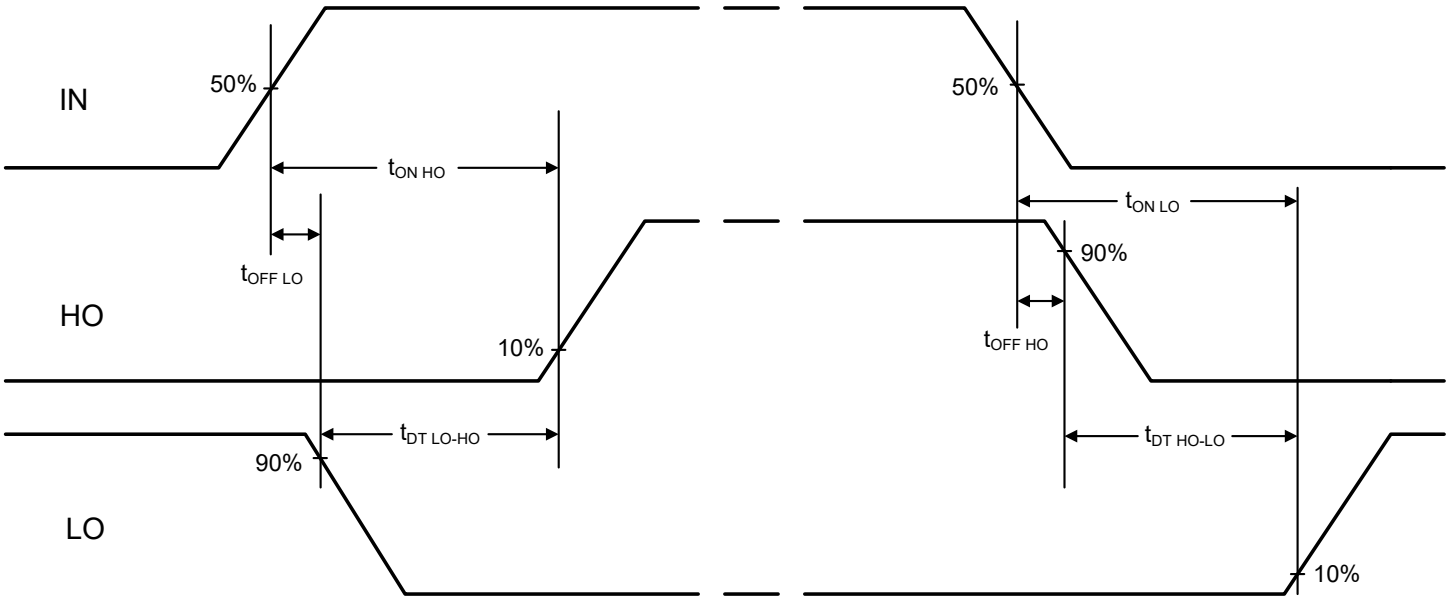


Figure 2. Shutdown Waveform Definitions



Deadtime $t_{DT\ LO-HO} = t_{ON\ HO} - t_{OFF\ LO}$

$t_{DT\ HO-LO} = t_{ON\ LO} - t_{OFF\ HO}$

Deadtime matching

$t_{MDT} = t_{DT\ LO-HO} - t_{DT\ HO-LO}$

Delay matching

$t_{DM\ OFF} = t_{OFF\ LO} - t_{OFF\ HO}$

$t_{DM\ ON} = t_{ON\ LO} - t_{ON\ HO}$

Figure 3. Switching Time Waveform Definitions

Application Information

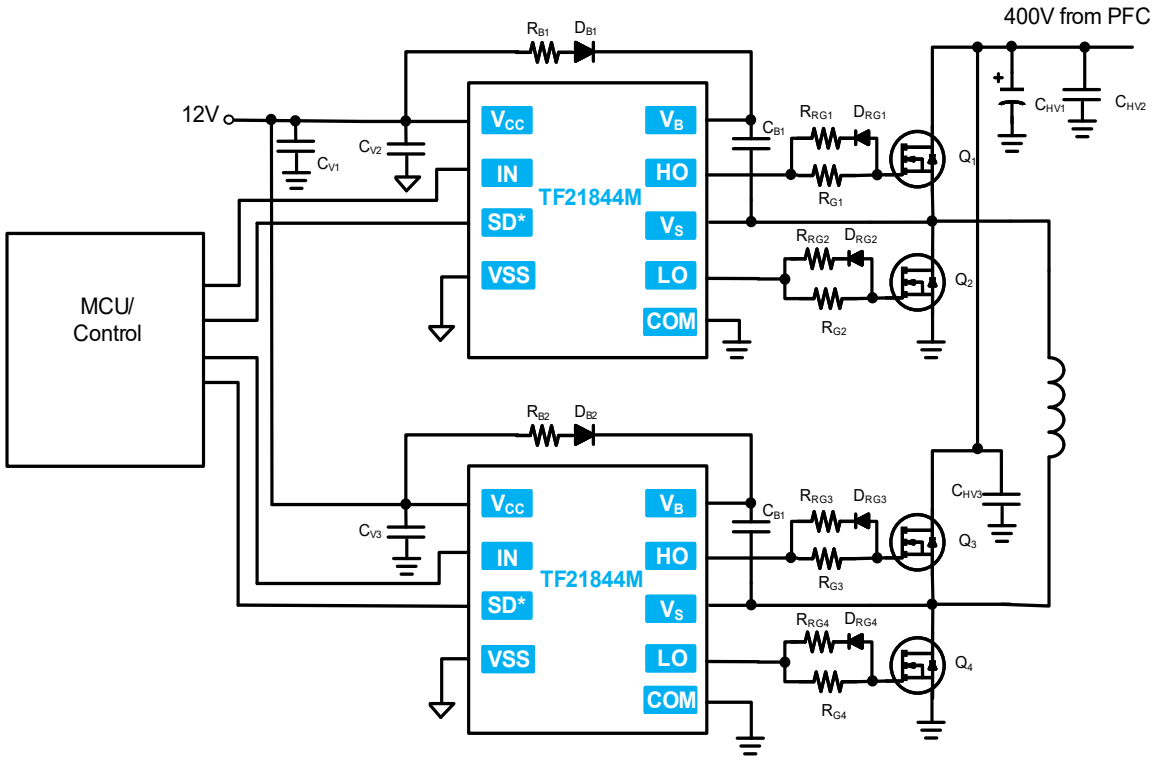


Figure 4. Primary side of Full Bridge converter using TF21844M

- RRG1, RRG2, RRG3, and RRG4 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

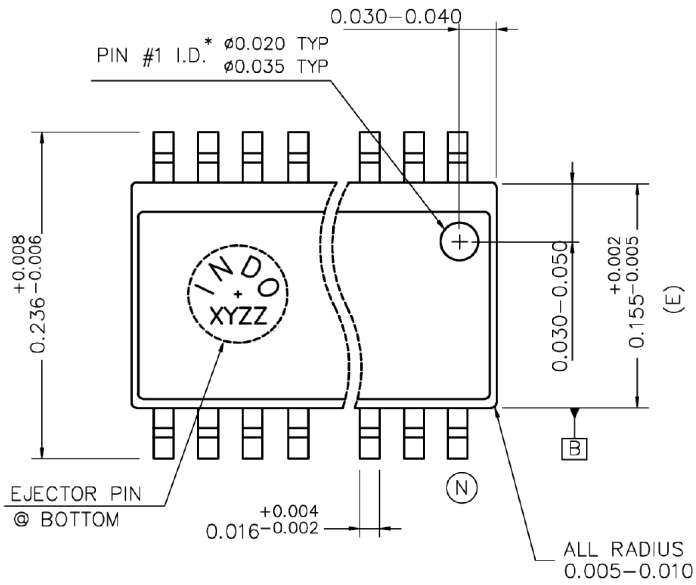
- It is **highly recommended** that the input pulse (to IN and SD*) should have an amplitude of 2.5V minimum (for VDD=15V) with a minimum pulse width of 2 x tdt (deadtime).

- RG1, RG2, RG3, and RG4 values are typically between 10Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RB1 and RB2 value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB1 and DB2 should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

Package Dimensions (SOIC-14)

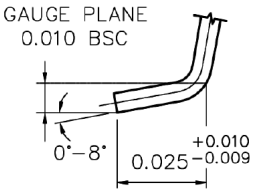
Please contact support@tfsemi.com for package availability.



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

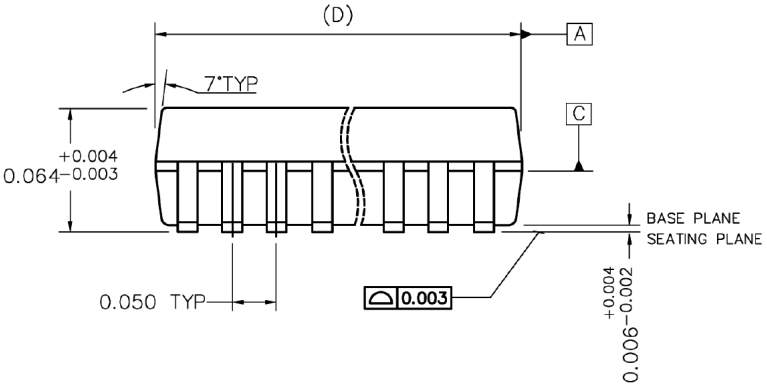
NOTES:

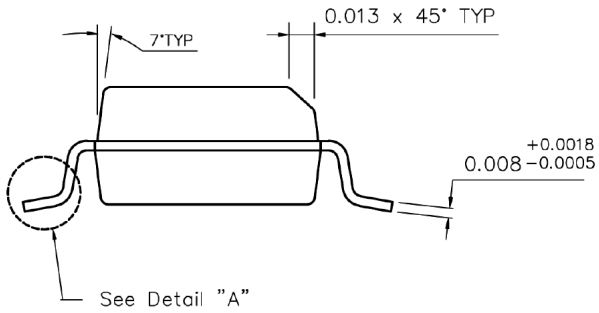
1. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 6 MILS PER SIDE.
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 3 MILS (@ SEATING PLANE) OUTGOING ASSEMBLY & 4 MILS AFTER TEST.
4. THE BOTTOM PACKAGE LEAD SIDE MAY BE BIGGER THAN THE TOP PACKAGE LEAD SIDE BY 4 MILS (2 MILS PER SIDE). BOTTOM PACKAGE DIMENSION SHALL FOLLOW DIMENSION STATED IN THIS DRAWING.
5. THE BOTTOM EJECTOR PIN CONTAINS COUNTRY OF ORIGIN "INDO" AND MOLD ID. (REFER TO TABLE FOR OPTION).
6. THIS DRAWING CONFORMS TO JEDEC REF. MS–012 REV. E



Detail "A"

N	D VARIATION			MGP MOLD			
				STANDARD		MATRIX	
	MIN	NOM	MAX	PIN 1 I.D.	EJECT PIN	PIN 1 I.D.	EJECT PIN
08	0.189	0.193	0.196	N/A		YES	YES
14	0.337	0.339	0.344	YES	NO	YES	YES
⚠ 16	0.386	0.390	0.393	N/A		YES	YES





Package Dimensions (PDIP-14)

Please contact support@tfsemi.com for package availability.

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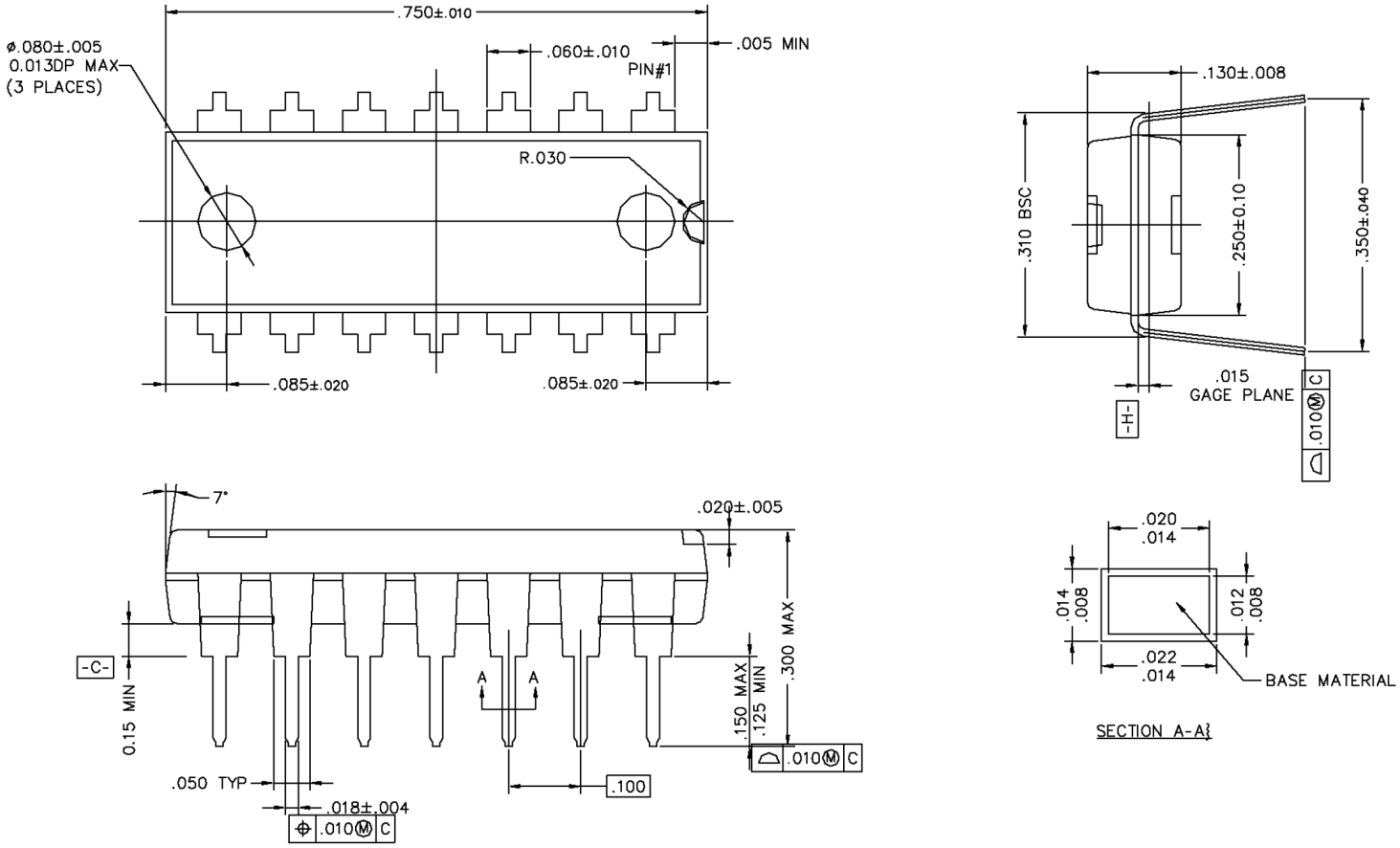

Note: Drawing conforms to jedec ref. MS-001 rev D

Revision History

Rev.	Change	Owner	Date
1.0	First release, final datasheet	Keith Spaulding	9/22/2020
1.1	Application notes update	Raj Selvaraj	06/22/2021

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