



RA MCU 生态工作室

瑞萨RA系列之 keil环境



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1. 瑞萨官网

用户可到瑞萨官网根据需求筛选型号。

(瑞萨官网: <https://www2.renesas.cn/cn/zh>)

2. Keil开发环境:

RA SC(RA Smart Configurator)

(RASA安装包:<https://www2.renesas.cn/cn/en/software-tool/ra-smart-configurator>)

keil : 推荐版本5.34 (尽量5.28或以上)

Jlink: 硬件jlink_V9

(上位机关系不大, 不是太老的版本都可以 推荐: jlink_v698)

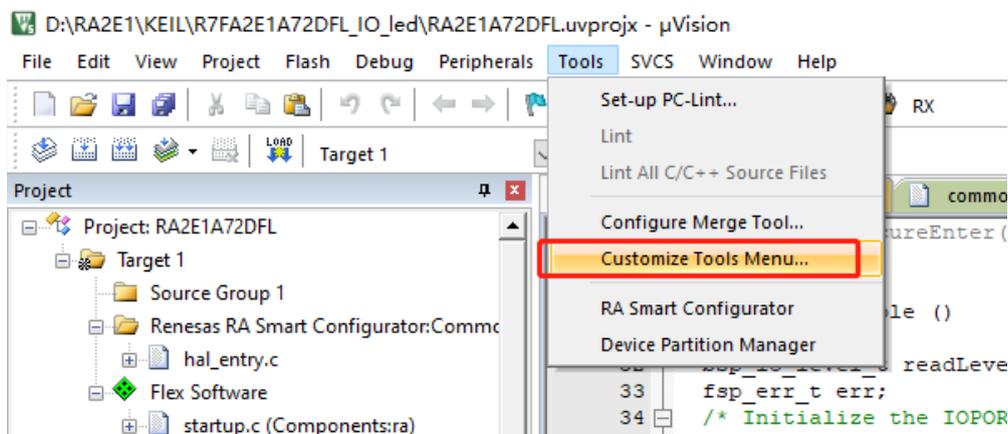
3. 环境安装

参考Flexible Software Package (FSP) User Manual手册第2.6章节的MDK指导, 完成下列步骤

3.1 安装完成RA SC, 安装MDK_Device_Packs (安装尽量使用英文路径, 网盘链接在文末)

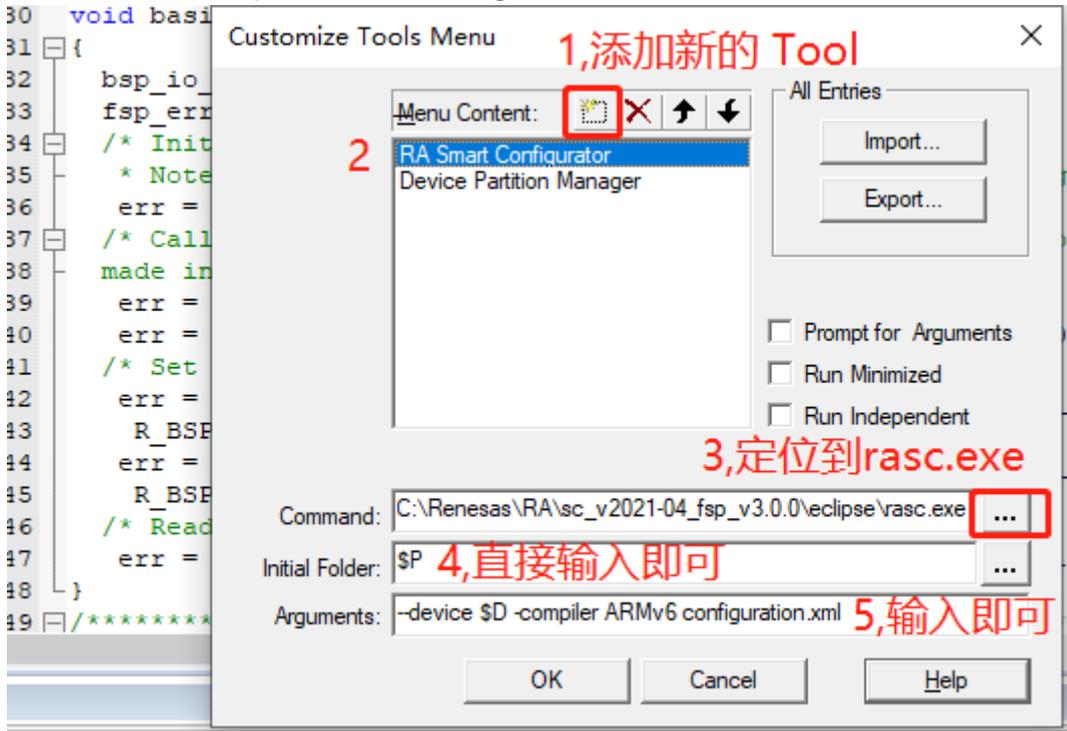
setup_fsp_v2_4_0_rasc_v2021-01.exe	2021/4/25 17:03	应用程序	696,275 KB
Renesas.RA_DFP.3.0.0.pack	2021/4/27 13:47	uVision Software...	2,049 KB

3.2 在keil--tool添加2个配置



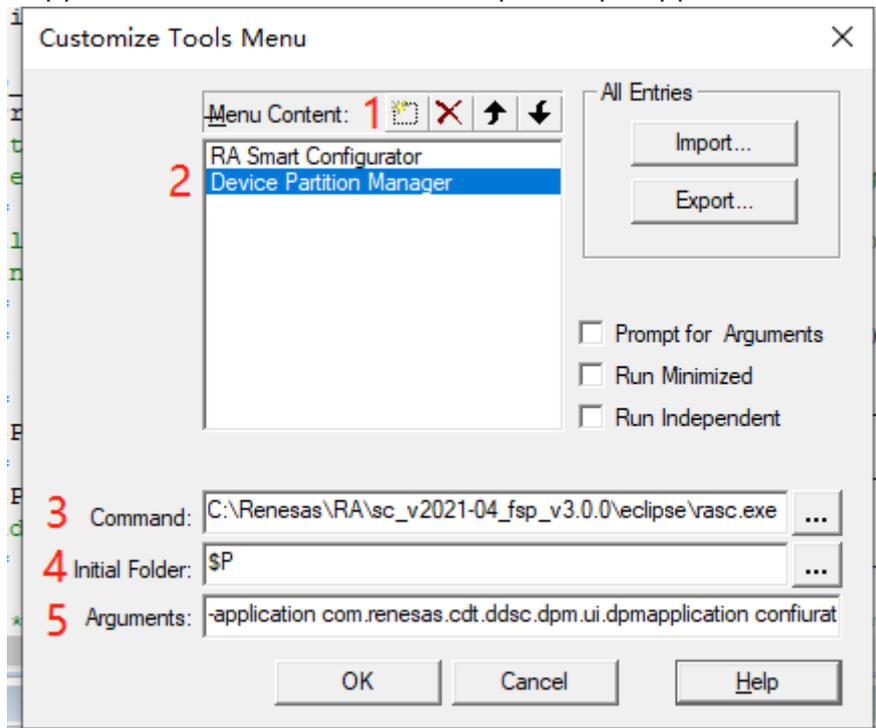
3.2.1 添加 RA Smart Configurator.

(--device \$D -compiler ARMv6 configuration.xml)



3.2.2 参照a添加Device Partition Manager

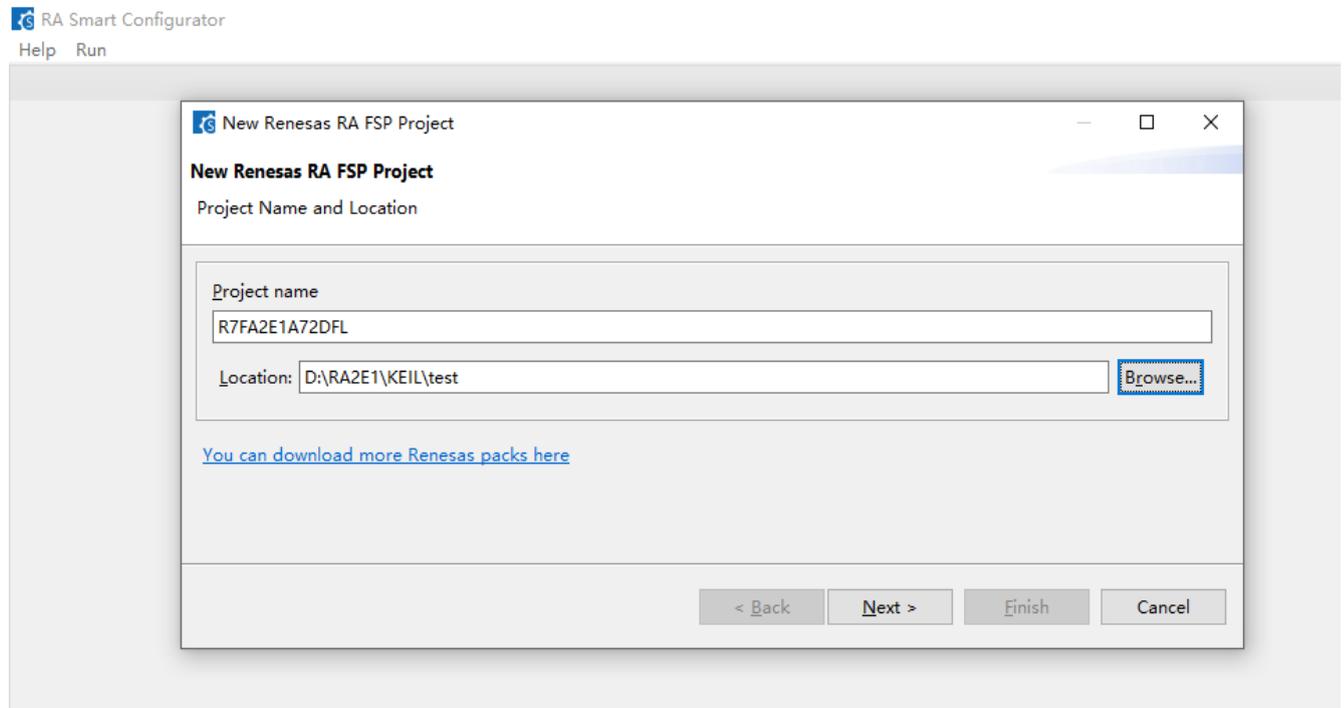
(-application com.renesas.cdt.ddsc.dpm.ui.dpmapplication configuration.xml "SL%L")



4. 创建keil新工程

4.1 打开rasc.exe，输入工程名和工程路径

(rasc.exe默认安装路径是 C:\Renesas\RA\sc_v2021-01_fsp_v2.4.0\eclipse)

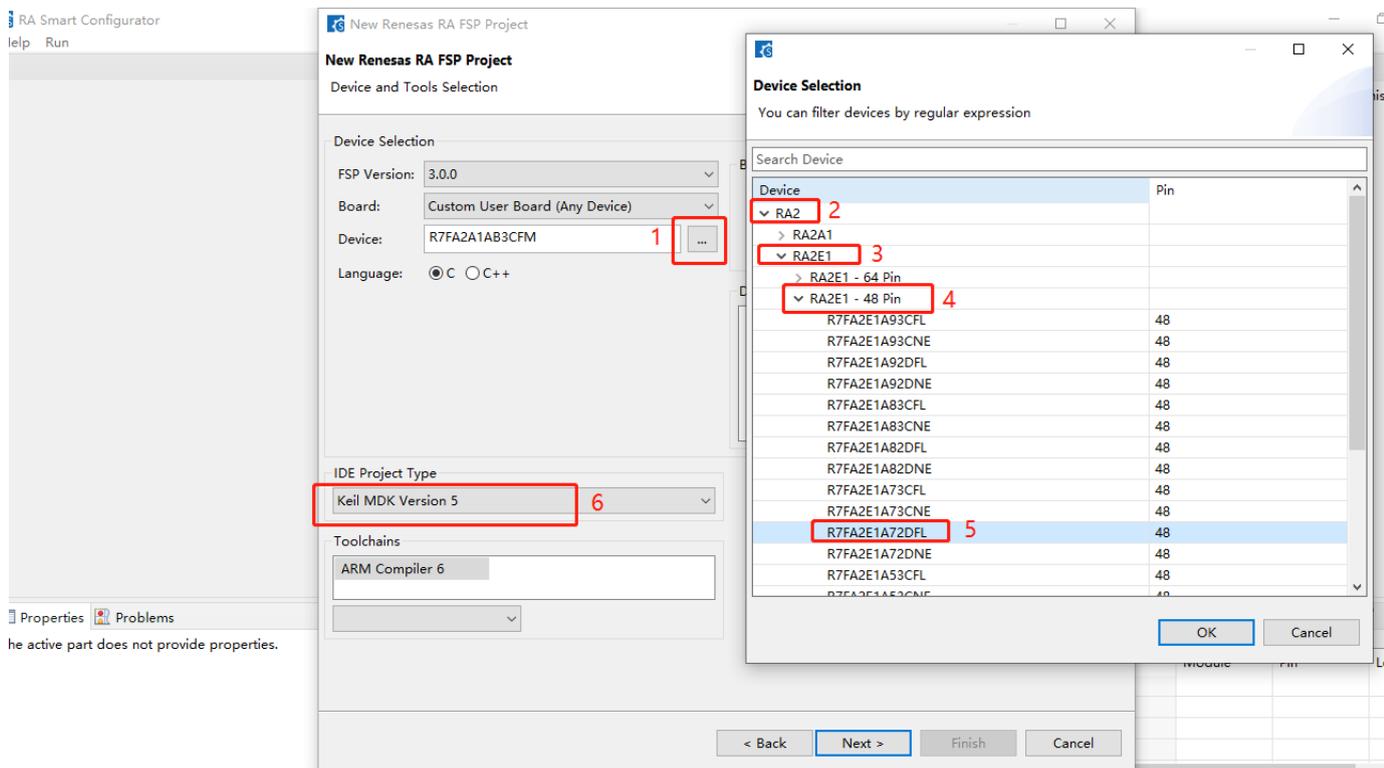


4.2 RA Project配置

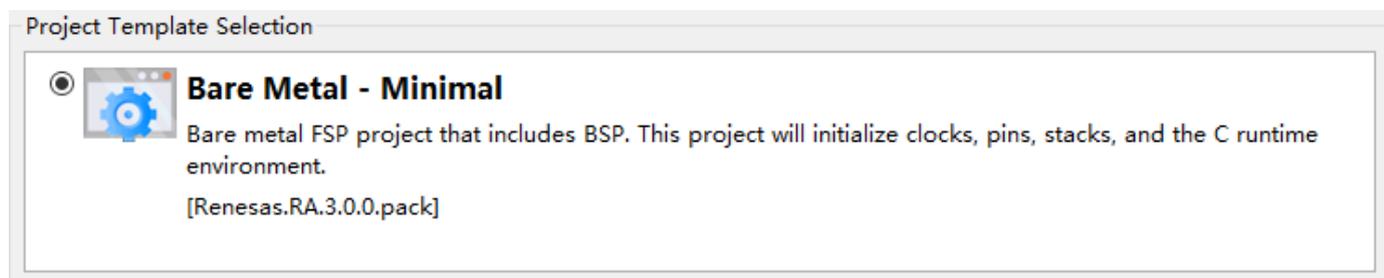
FSP Version是安装的rasc的版本 3.0.0

Device选择MCU具体型号，

IDE选择keil



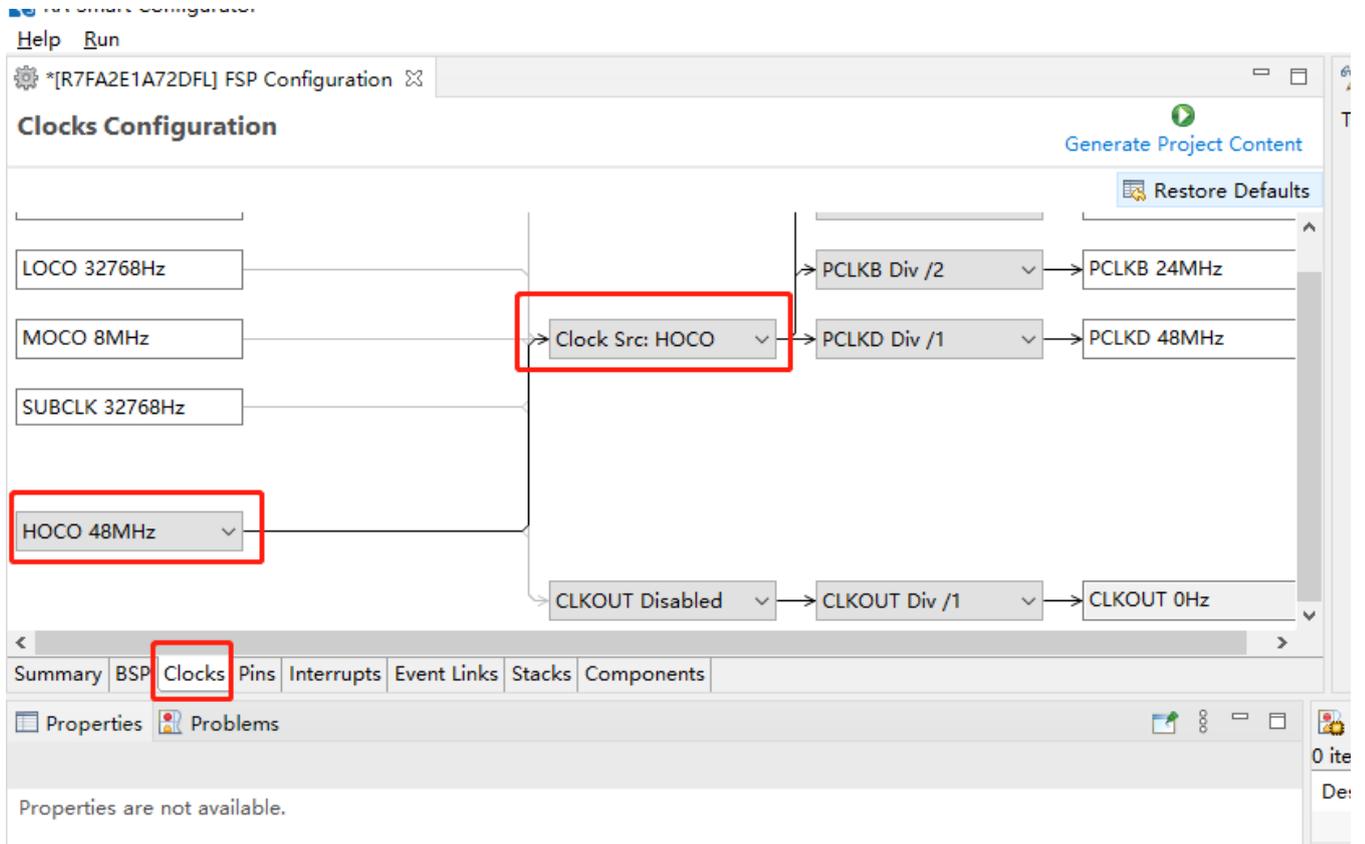
(根据需求选择是否使用RTOS)



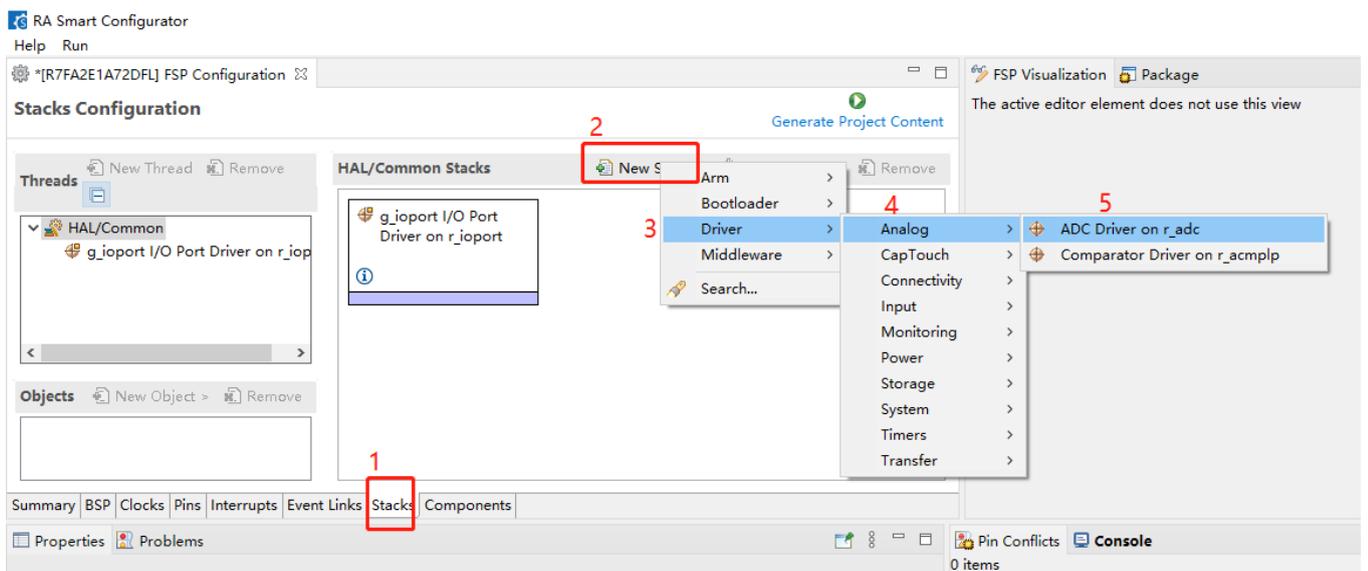
4.3 以配置ADC为例

(具体可参考FSP 4.2章节r_adc部分)

4.3.1 配置主时钟为内部高速48MHz



4.3.2 在stack添加ad模块



4.3.3 在属性栏配置相关参数

RA Smart Configurator

Help Run

*[R7FA2E1A72DFL] FSP Configuration

Stacks Configuration

Generate Pro

Threads New Thread Remove

HAL/Common

Objects New Object Remove

HAL/Common Stacks

New Stack Extend Stack

g_ioport I/O Port Driver on r_ioport

g_adc0 ADC Driver on r_adc

Summary BSP Clocks Pins Interrupts Event Links **Stacks** Components

Properties Problems

g_adc0 ADC Driver on r_adc

Settings	Property	Value
	General	
	Name	1 g_adc0
	Unit	2 0
	Resolution	12-Bit
	Alignment	Right
	Clear after read	On
	Mode	3 Single Scan
	Double-trigger	Disabled
4	> Input	
5	> Interrupts	
	> Extra	
	Pins	
	ADTRG	None
	AN00	6 P000
	AN01	None

- (1) 模块名。
- (2) 配置ad通道。
- (3) 配置扫描模式
- (4) 打开ad通道
- (5) 配置ad中断
- (6) 选择AD通道对应的IO口

4.3.4 点击ad通道 AN00，会出现跳转箭头，可直接跳转到Pins的AD引脚部分进行配置

Stacks Configuration Generate Project Content

Threads: New Thread Remove

HAL/Common Stacks: New Stack > Extend Stack > Remove

g_ioport I/O Port Driver on r_ioport

g_adc0 ADC Driver on r_adc

Objects: New Object > Remove

Summary | BSP | Clocks | Pins | Interrupts | Event Links | **Stacks** | Components

Properties | Problems

g_adc0 ADC Driver on r_adc

Settings	Property	Value
	Module g_adc0 ADC Driver on r_adc	
	> General	
	> Input	
	> Interrupts	
	> Extra	
	> Pins	
	ADTRG	None
	AN00	P000
	AN01	None

RA Smart Configurator

Help Run

*[R7FA2E1A72DFL] FSP Configuration Generate Project Content

Pin Configuration FSP Visualization Package

Select Pin Configuration: R7FA2E1A72DFL.pincfg Export to CSV file Configure Pin Driver Warnings

Generate data: g_bsp_pin_cfg

Pin Selection

Type filter text

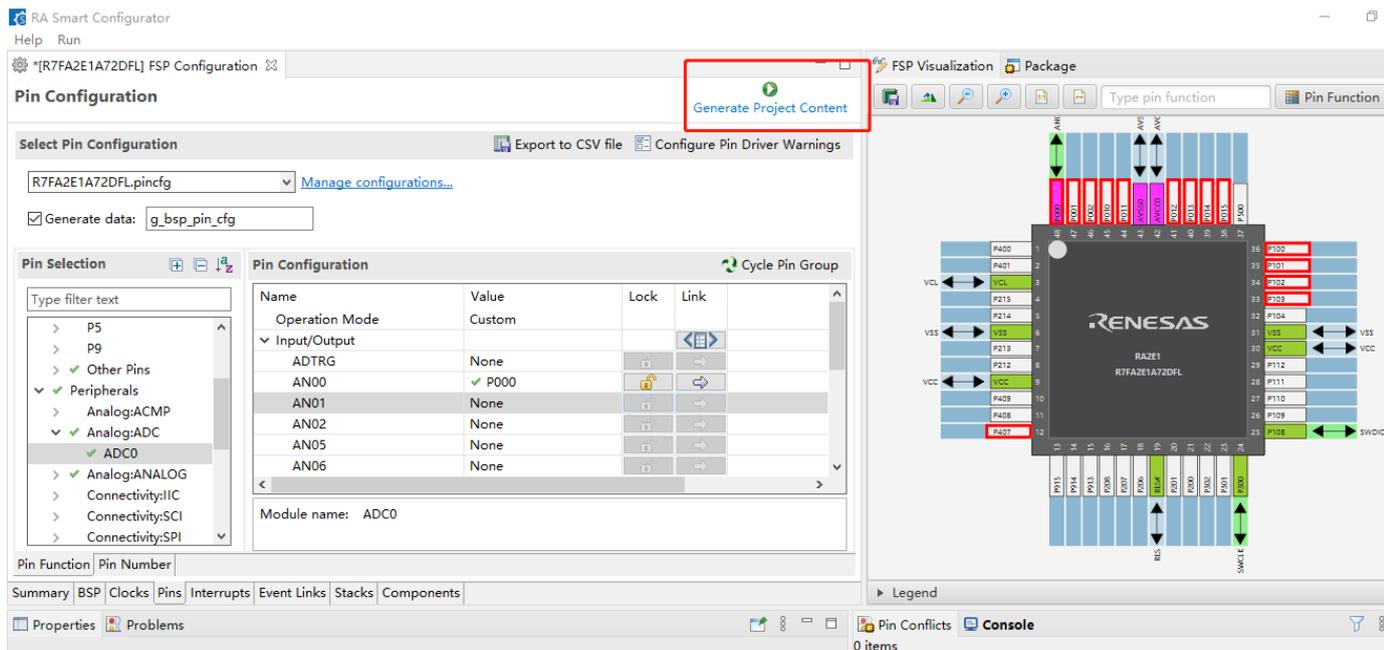
- > P3
- > P4
- > P5
- > P9
- > Other Pins
- > Peripherals
 - > Analog:ACMP
 - > Analog:ADC
 - 1** > ADC0
 - > Analog:ANALOG
 - > Connectivity:IIC
 - > Connectivity:SCI

Pin Configuration Cycle Pin Group

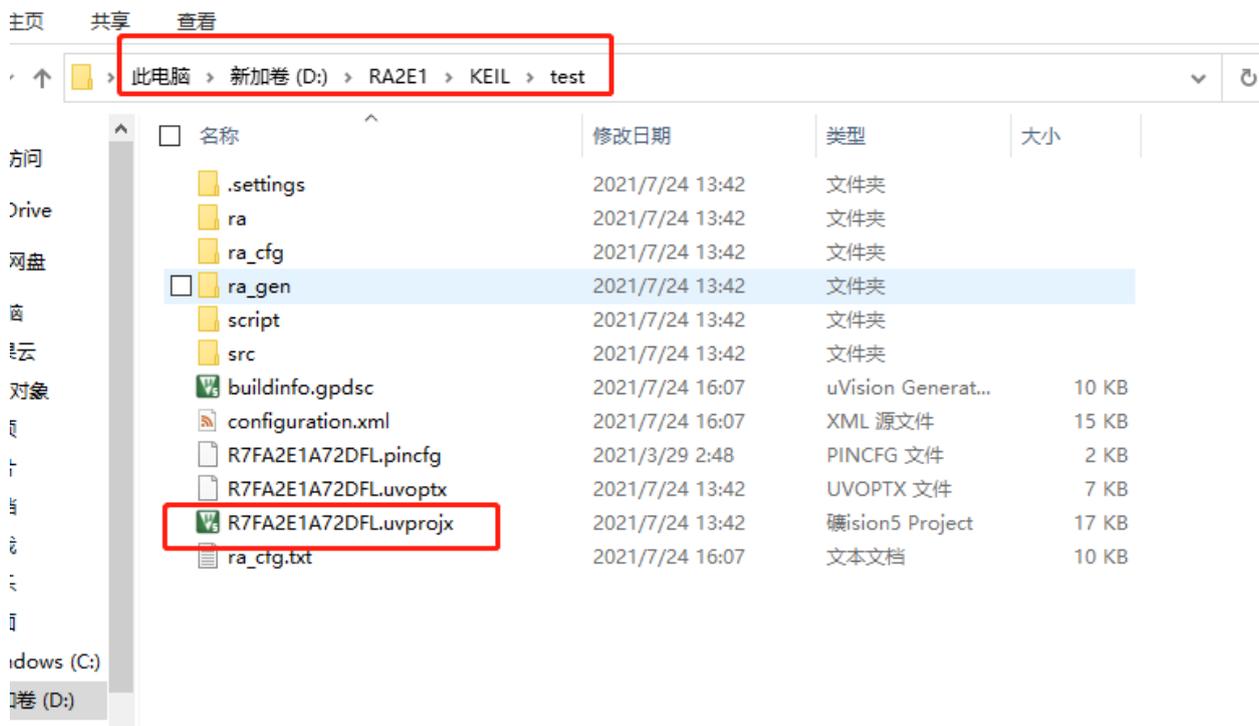
Name	Value	Lock	Link
Operation Mode	2 Custom		
Input/Output			
ADTRG	None		
AN00	3 ✓ P000		
AN01	None		
AN02	None		
AN05	None		
AN06	None		
AN07	None		

Module name: ADC0

FSP Visualization



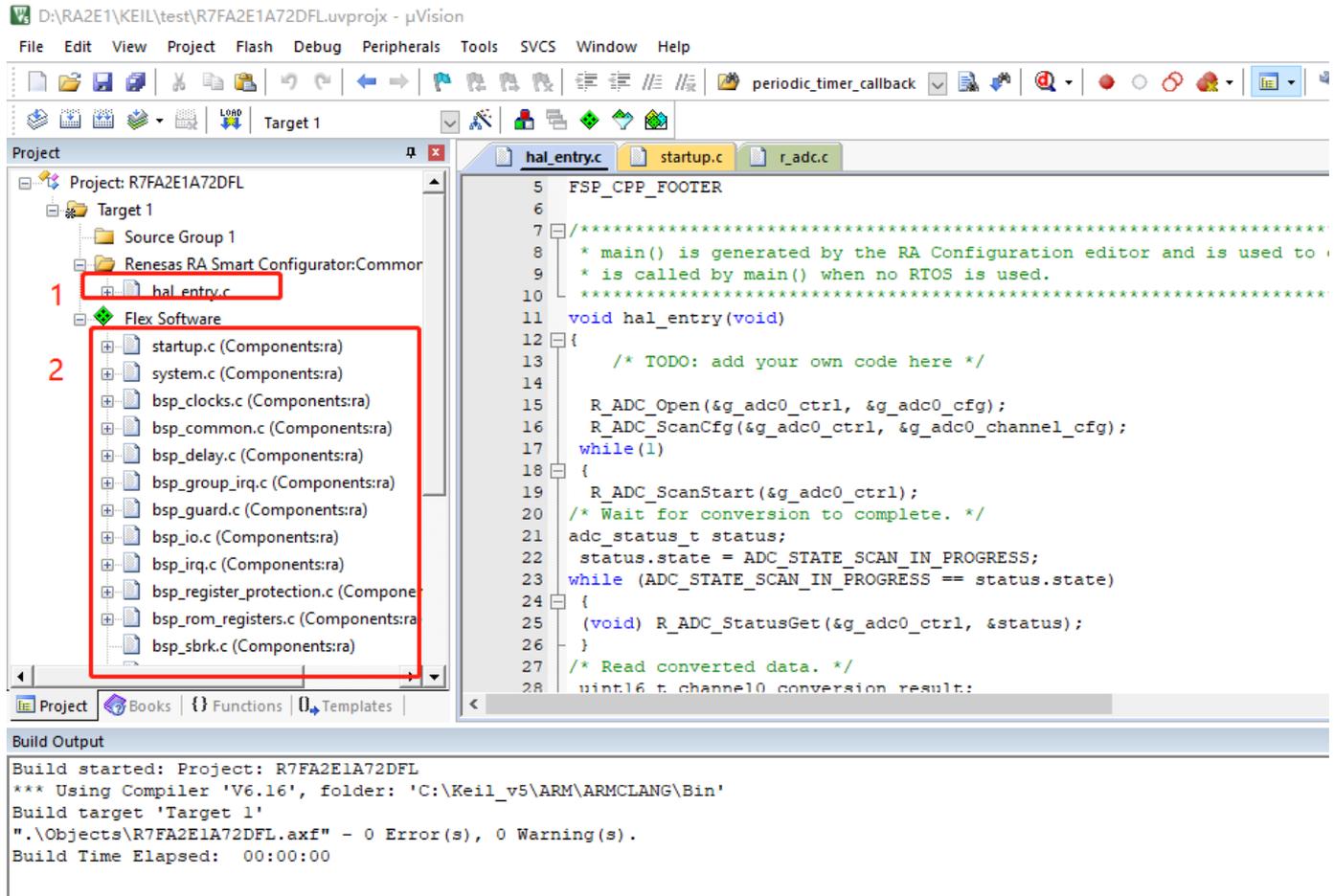
4.3.6 打开生成的工程



4.3.7 生成的工程编译0 Error,0 Warning.

(参考FSP 4.2章节的例程来写代码，或参考官方例程。)

1是用户编写代码的地方，2是RA Smart Configuration配置初始化生成的代码。用户代码尽量写在1 hal_entry.c中，因为当RA Smart Configuration初始化生成代码时会重新覆盖2中的代码。



4.3.8 如果需要再次打开RA Smart Configuration配置参数，

如图下所示，从这里打开RA Smart Configuration就可以与工程关联起来。

D:\RA2E1\KEIL\test\R7FA2E1A72DFL.uvprojx - µVision

File Edit View Project Flash Debug Peripherals Tools SVCS Window Help

Target 1

Project: R7FA2E1A72DFL

Source Group 1

Renesas RA Smart Configurator:Common

hal_entry.c

Flex Software

startup.c (Components:ra)

system.c (Components:ra)

bsp_clocks.c (Components:ra)

bsp_common.c (Components:ra)

bsp_delay.c (Components:ra)

bsp_group_irq.c (Components:ra)

bsp_guard.c (Components:ra)

bsp_io.c (Components:ra)

bsp_irq.c (Components:ra)

bsp_register_protection.c (Componer)

bsp_rom_registers.c (Components:ra)

bsp_sbrk.c (Components:ra)

```

5 FSP_CPP_FOOTER
6
7 /*****
8  * main() is g
9  * is called b
10 *****/
11 void hal_entry
12 {
13     /* TODO: a
14
15     R_ADC_Open(&
16     R_ADC_ScanCf
17     while(1)
18     {
19         R_ADC_ScanSt
20         /* Wait for co
21         adc_status_t s
22         status.state
23         while (ADC_STA
24     {
25         (void) R_ADC_
26     }
27     /* Read conver
28

```

Build Output

```

Build started: Project: R7FA2E1A72DFL
*** Using Compiler 'V6.16', folder: 'C:\Keil_v5\ARM\ARMCLANG\Bin'
Build target 'Target 1'
".\Objects\R7FA2E1A72DFL.axf" - 0 Error(s), 0 Warning(s).
Build Time Elapsed: 00:00:00

```

Manage Run-Time Environment

Software Component	Sel.	Variant	Version	Description
CMSIS	<input checked="" type="checkbox"/>			Cortex Microcontroller
CMSIS Driver	<input checked="" type="checkbox"/>			Unified Device Access
Compiler	<input checked="" type="checkbox"/>	ARM Compiler	1.6.0	Compiler Explorer
Device	<input checked="" type="checkbox"/>			Startup Script
File System	<input checked="" type="checkbox"/>	MDK-Plus	6.13.8	File Access
Flex Software	<input checked="" type="checkbox"/>			Renesas Flex Software
Build Configuration	<input checked="" type="checkbox"/>			
Generated Data	<input checked="" type="checkbox"/>			
Linker Script	<input checked="" type="checkbox"/>			
RA Configuration	<input checked="" type="checkbox"/>		1.0.0	Renesas RA Configuration
Components	<input checked="" type="checkbox"/>			
Graphics	<input checked="" type="checkbox"/>	MDK-Plus	6.10.8	User Interface
Network	<input checked="" type="checkbox"/>	MDK-Plus	7.14.0	IPv4 Network
USB	<input checked="" type="checkbox"/>	MDK-Plus	6.14.1	USB Communication

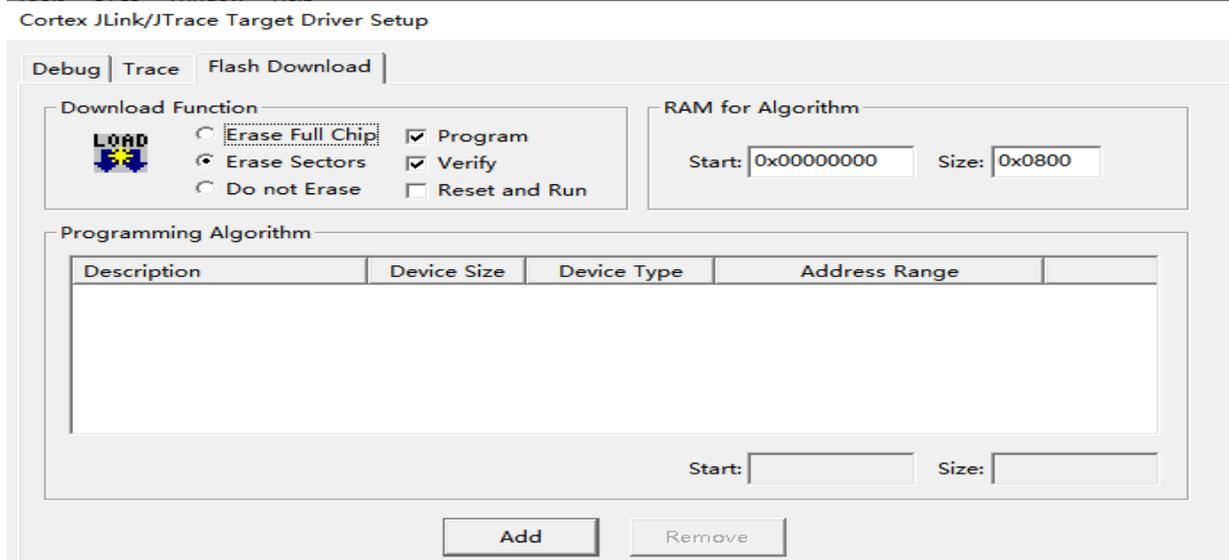
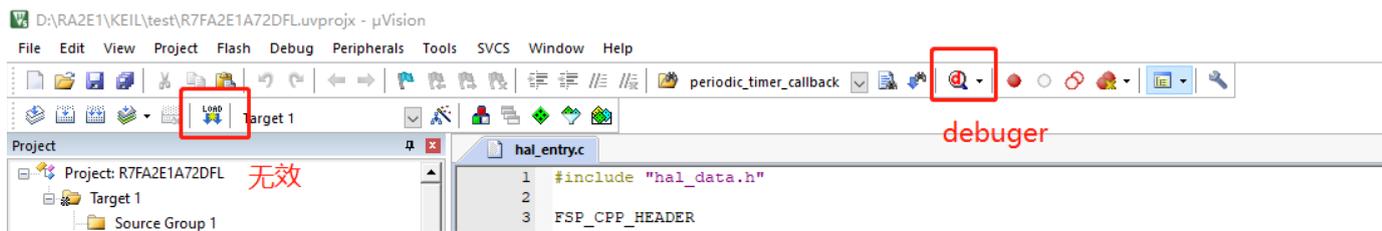
Validation Output

Description

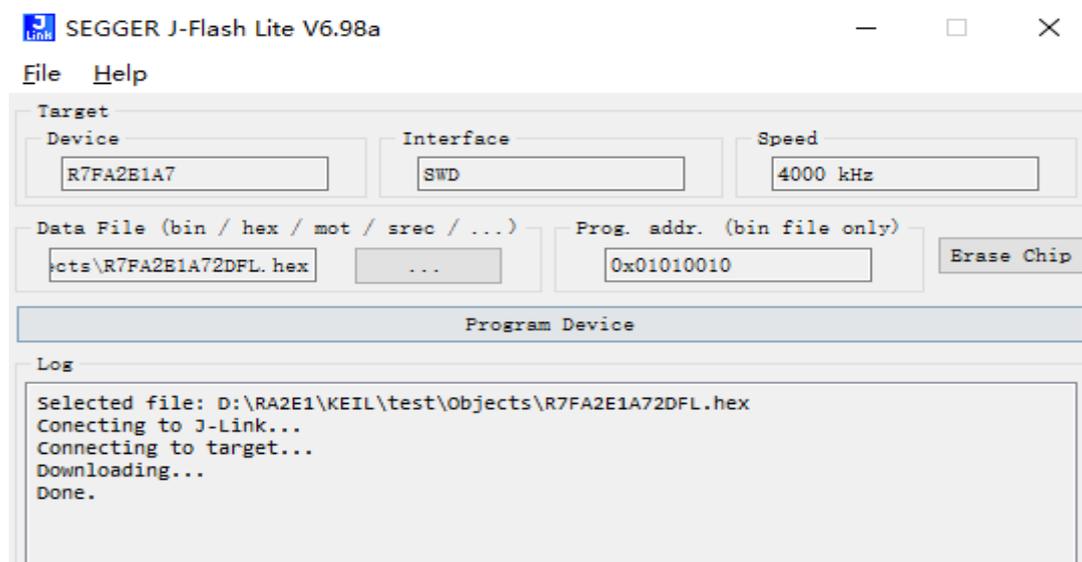
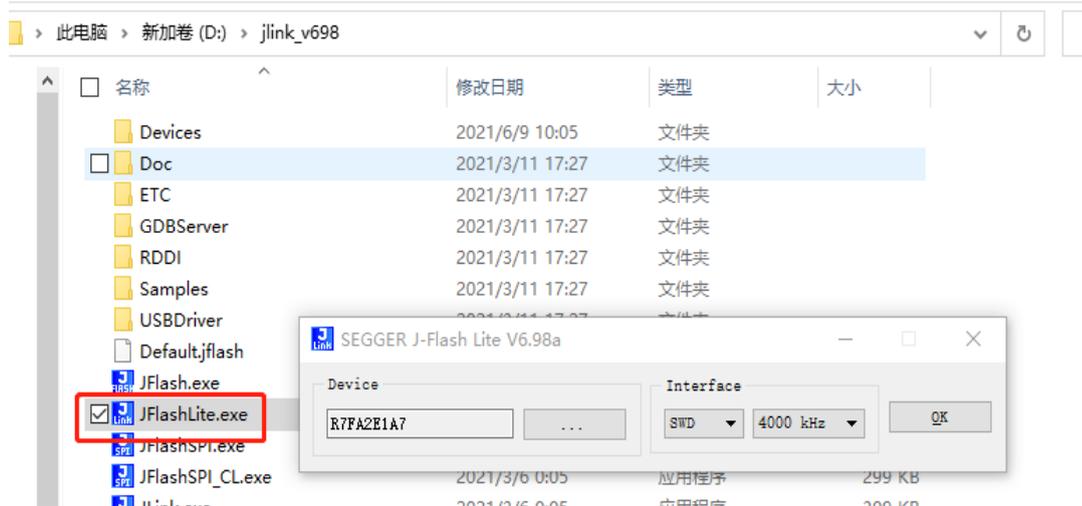
4.3.9 烧录方式

可使用Jlink(硬件V9)在keil中点仿真烧录

(debug-settings-Flash Download中不需要添加)



也可以使用Jlink带的 JFlashLite.exe(注意不是Jflash)。

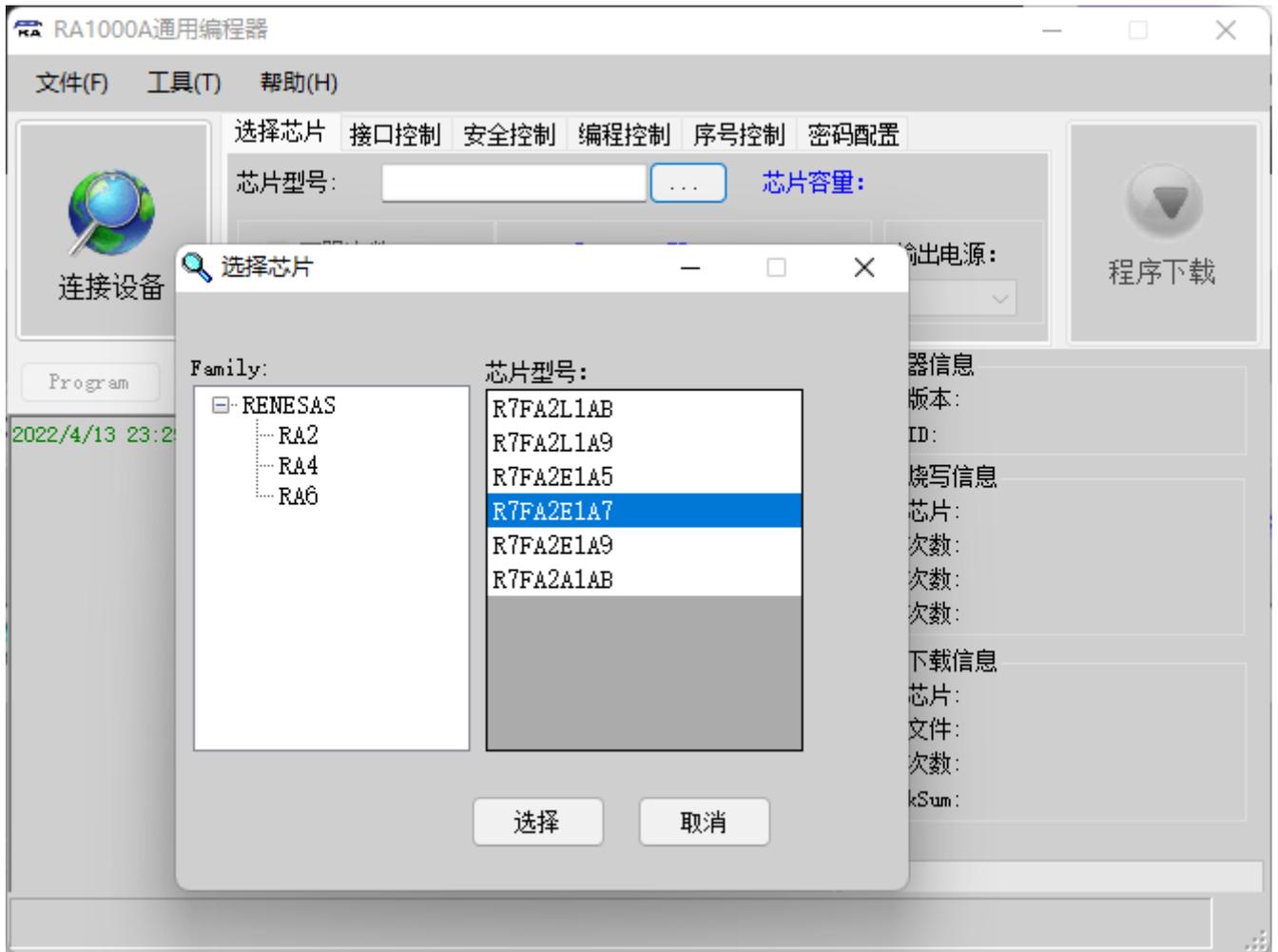


或是使用RA MCU 生态工作室的RA1000A脱机烧录



生态工作室





4.4 功能介绍

在RA Smart Configuration中，可选参数在上半部分，属性在下半部分。

Board Support Package Configuration

Device Selection

FSP version: 3.0.0

Board: Custom User Board (Any Device)

Device: R7FA2E1A72DFL

RTOS: No RTOS

Board Details

Summary **BSP** Clocks Pins Interrupts Event Links Stacks Components

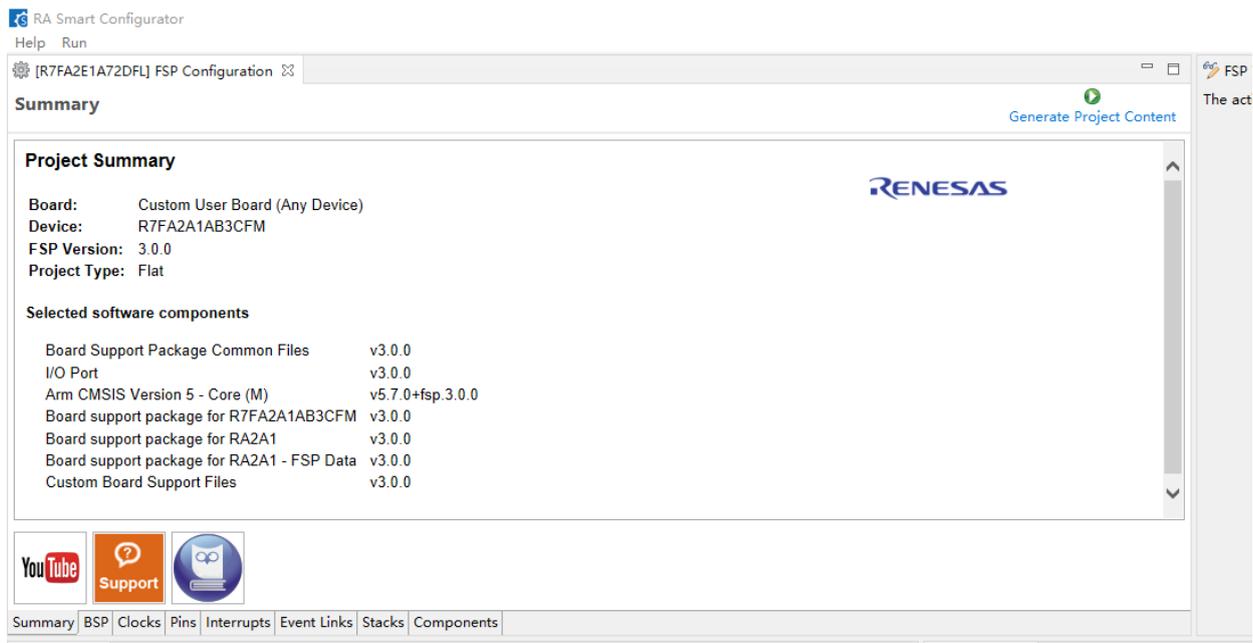
Properties Problems

Custom User Board (Any Device)

Settings	Property	Value
	▼ R7FA2E1A72DFL	
	part_number	R7FA2E1A72DFL
	rom_size_bytes	65536
	ram_size_bytes	16384
	data_flash_size_bytes	4096
	package_style	LQFP
	package_pins	48
	> RA2E1	
	> RA2E1 Family	
	▼ RA Common	
	Main stack size (bytes)	0x400
	Heap size (bytes)	0

4.4.1 Summary 确定了项目的所有关键元素和组件。

显示目标板，设备，工具链和FSP版本。



4.42 BSP 显示当前选择的FSP和device。

Board Support Package Configuration

Device Selection

FSP version: 3.0.0

Board: Custom User Board (Any Device)

Device: R7FA2E1A72DFL

RTOS: No RTOS

Board Details

Summary **BSP** Clocks Pins Interrupts Event Links Stacks Components

Properties Problems

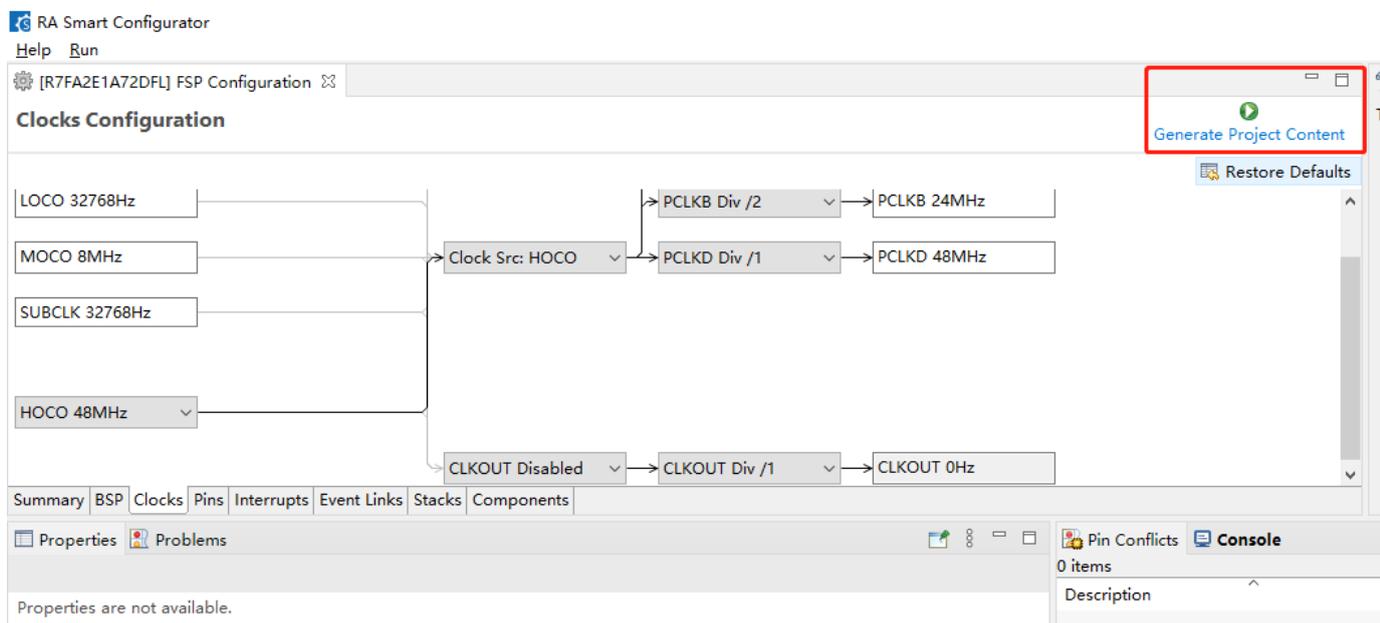
可在BSP属性配置中查看rom size, 也可以配置是否使用副时钟等功能.

Summary		BSP	Clocks	Pins	Interrupts	Event Links	Stacks	Components
Properties		Problems						
Custom User Board (Any Device)								
Settings	Property	Value						
	▼ R7FA2E1A72DFL							
	part_number	R7FA2E1A72DFL						
	rom_size_bytes	65536						
	ram_size_bytes	16384						
	data_flash_size_bytes	4096						
	package_style	LQFP						
	package_pins	48						
	> RA2E1							
	> RA2E1 Family							
	▼ RA Common							
	Main stack size (bytes)	0x400						
	Heap size (bytes)	0						
	MCU Vcc (mV)	3300						
	Parameter checking	Disabled						
	Assert Failures	Return FSP_ERR_ASSERTION						
	Error Log	No Error Log						
	Soft Reset	Disabled						
	Main Oscillator Populated	Populated						
	PFS Protect	Enabled						
	C Runtime Initialization	Enabled						

(When you click the Generate Project Content button, the BSP configuration contents are written to ra_cfg/fsp_cfg/bsp/bsp_cfg.h)

4.43 Clock 显示可配置时钟树

允许修改各种时钟分频器和时钟源，如果时钟设置无效，违规的时钟值将用红色突出显示。仍然可以使用此设置生成代码，但不能保证正确的操作。

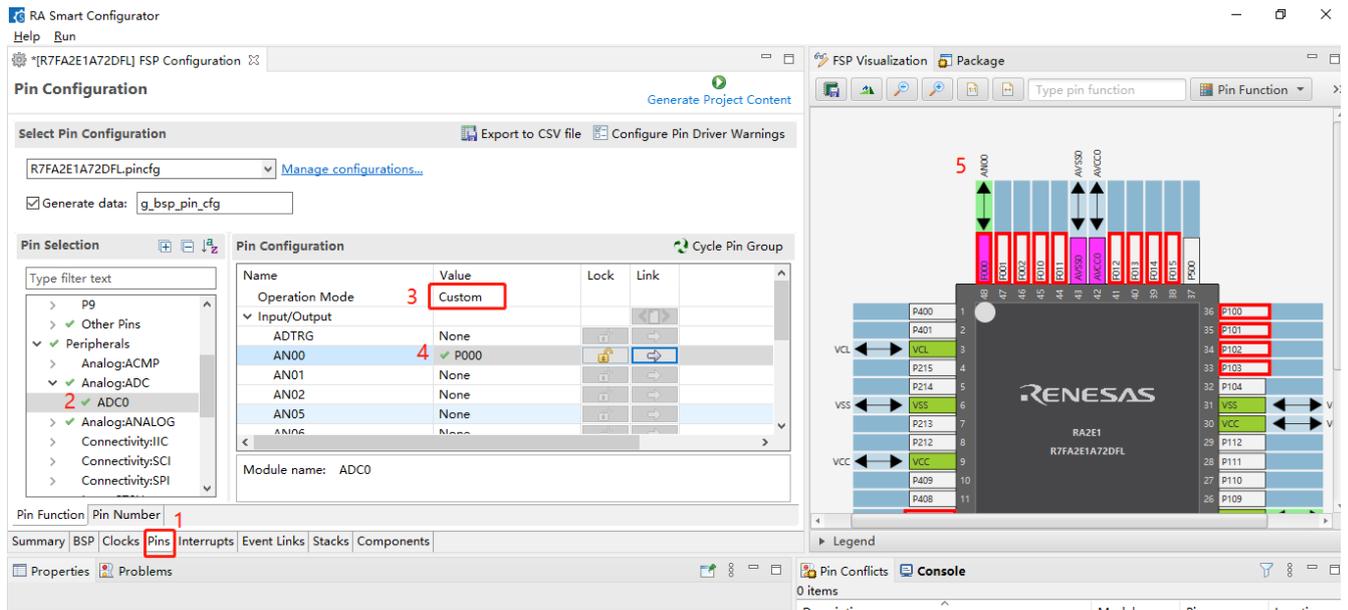


(When you click the Generate Project Content button, the clock configuration contents are written to: ra_gen/bsp_clock_cfg.h)

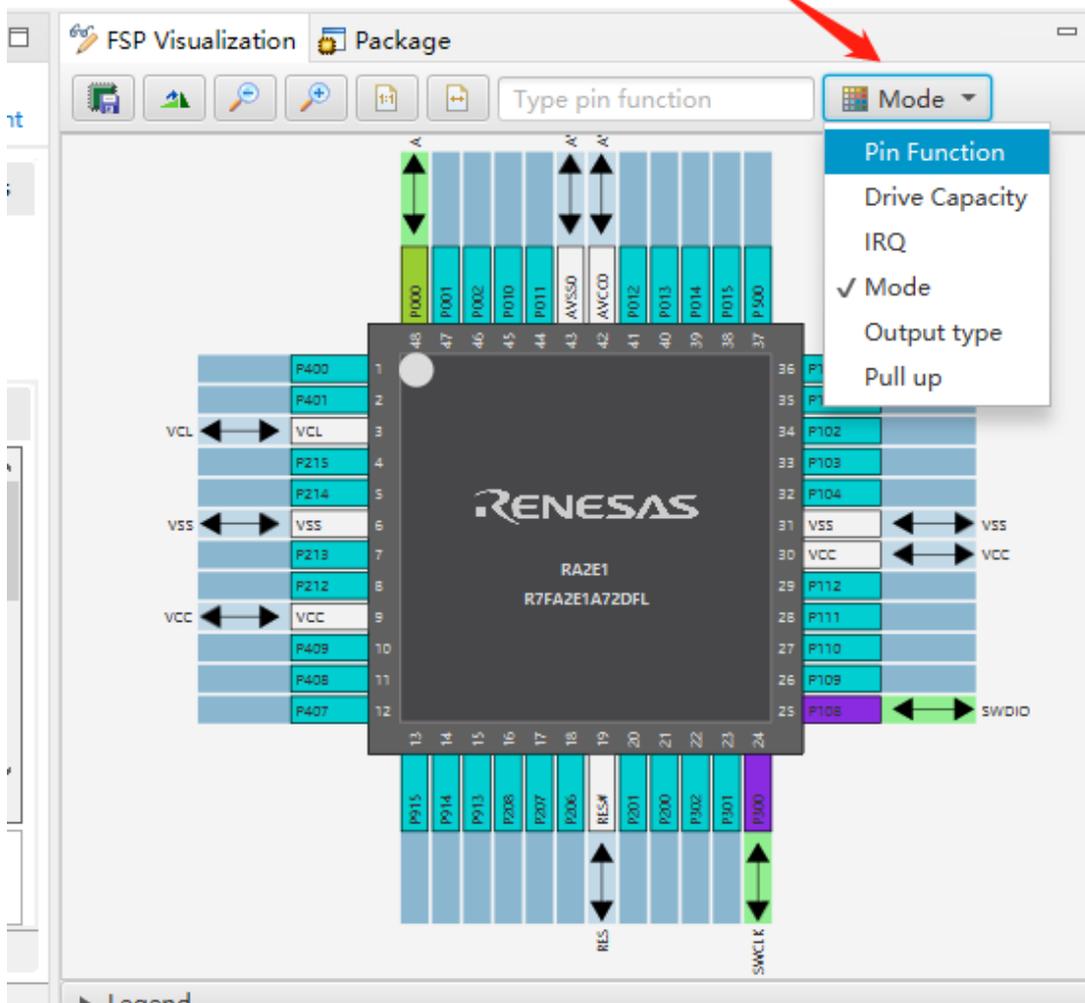
4.44 Pins 配置引脚

提供MCU引脚的灵活配置。由于许多引脚能够提供多种功能，它们可以在外围基础上进行配置，配置相关

功能之后会在右侧Package视图中显示绿色。



可根据每个引脚的选定电气或功能特性显示封装视图。



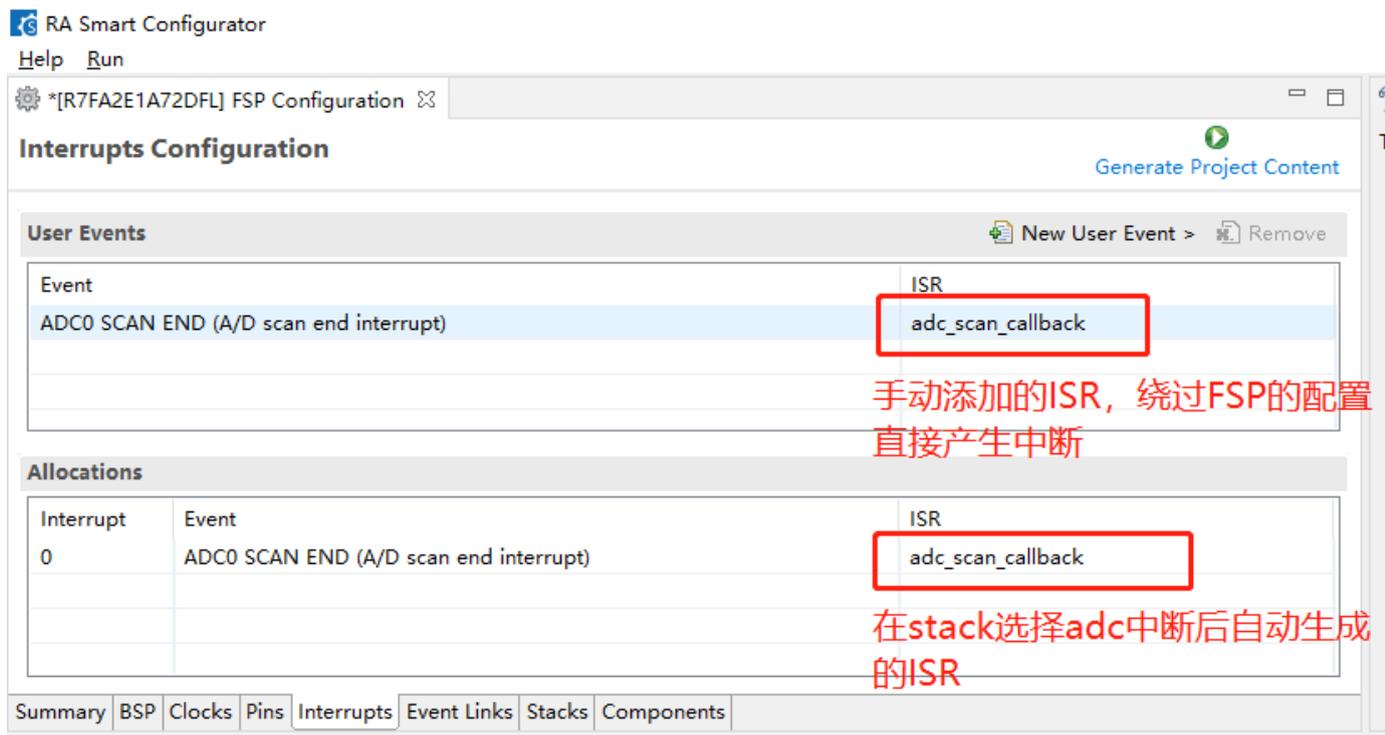
(When you click the Generate Project Content button, the pin configuration contents are
Written to: ra_gen\bsp_pin_cfg.h)

4.45 Interrupts

添加中断的两个方法：

用户可以通过设置自定义ISR来绕过FSP设置的外围中断。这可以通过通过New User event按钮添加一个新事件来实现。

或是使用Stacks选项卡中的Properties视图通过设置中断优先级来启用中断。在Stacks窗格中选择驱动程序以查看和编辑其属性。



4.46 Event Links 可以查看ELC的事件信息。

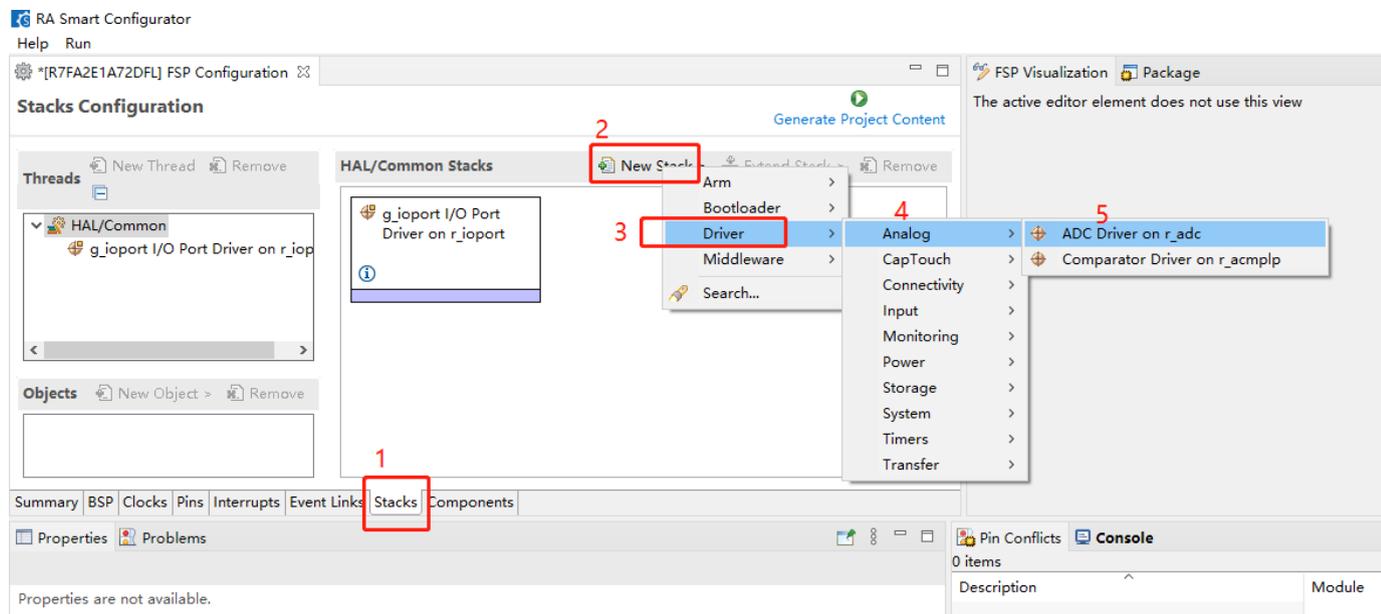
事件按外围设备排序，便于查找和验证。利用各个外设模块产生的事件请求作为源信号，将各个外设模块连接到不同的模块，实现模块之间直接连接，不需要CPU干预，当为模块选择接收一个ELC事件时(或者当手动定义一个事件链接时)，只有项目中配置的模块可用的事件才会显示出来。

4.47 Stack 通过图形界面添加驱动，并在下方的属性中配置参数。

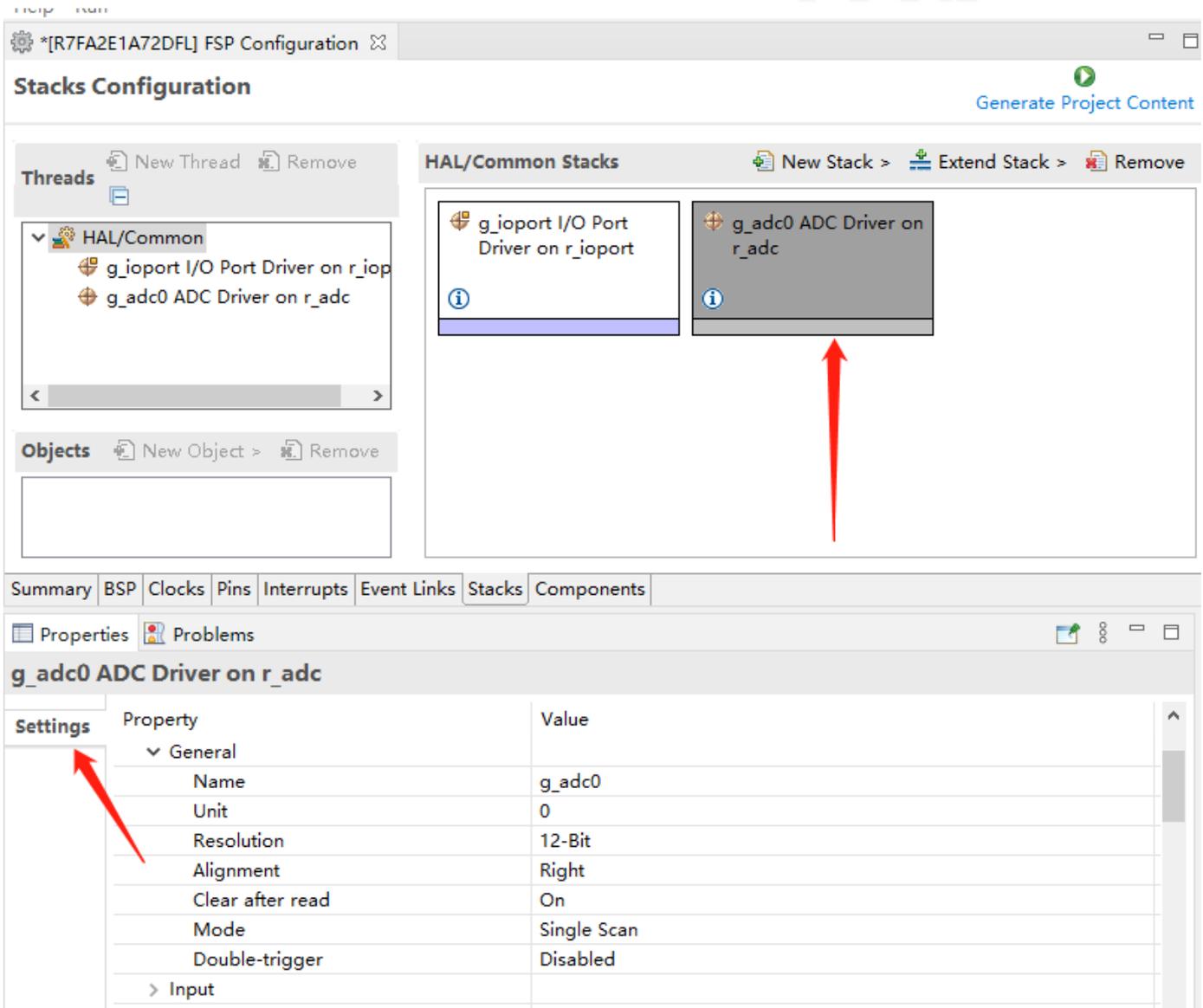
具体如何添加驱动，请参考Flexible Software Package (FSP) User Manual 第2.2.6.1以及2.2.6.2章节。

具体每个属性如何配置，请参考Flexible Software Package (FSP) User Manual 第4.2章节。

下图是添加ADC的过程：



添加ad模块之后点中该模块。可在下方属性中配置具体参数



4.48 Components 允许包含或排除应用程序所需的各个模块。

(链接: https://pan.baidu.com/s/1I38O1_oX4cPG5hpMqfnrxQ
提取码: sfra)

Keil下载失败总结

1. DDSC smart configurator生成完成MDK代码后，MDK打开后其start地址为0x00000000,当我们添加完programming algorithm，由于其初始地址是错误会导致烧录失败。

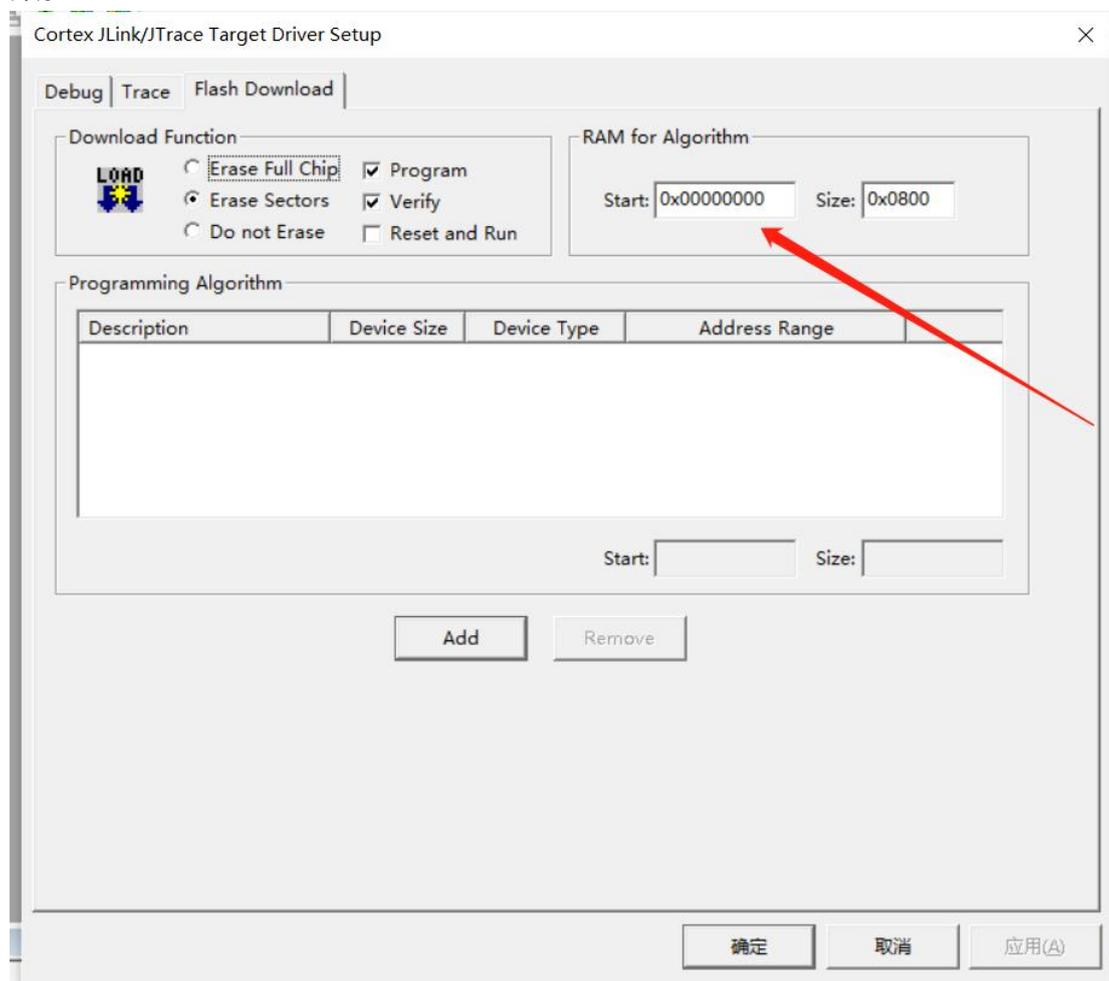


图1 默认状态

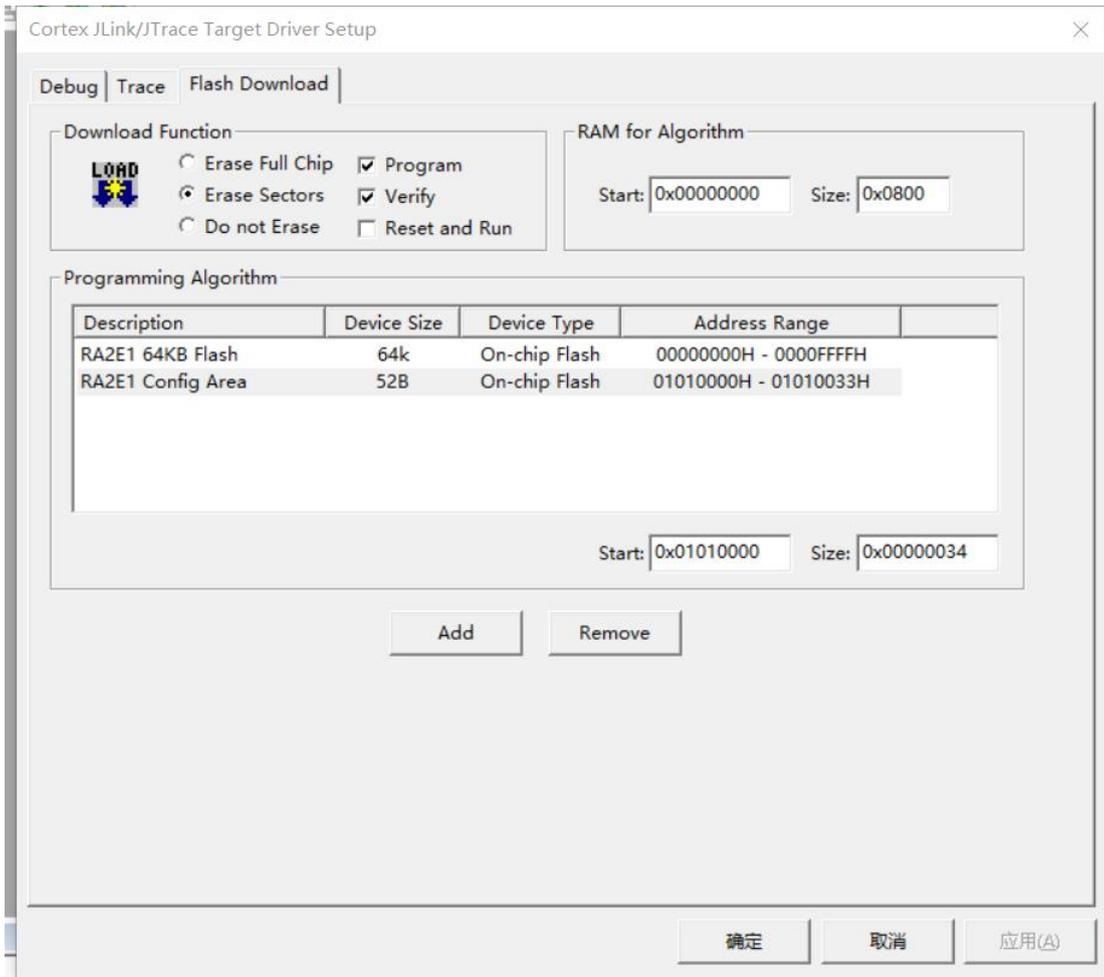


图2 添加完programming algorithm状态

2.失败报错窗口如下

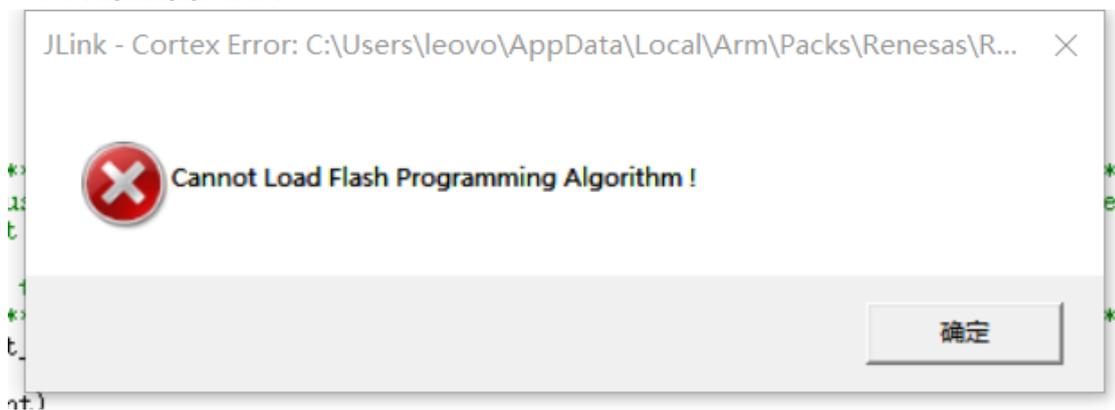


图3 报错1

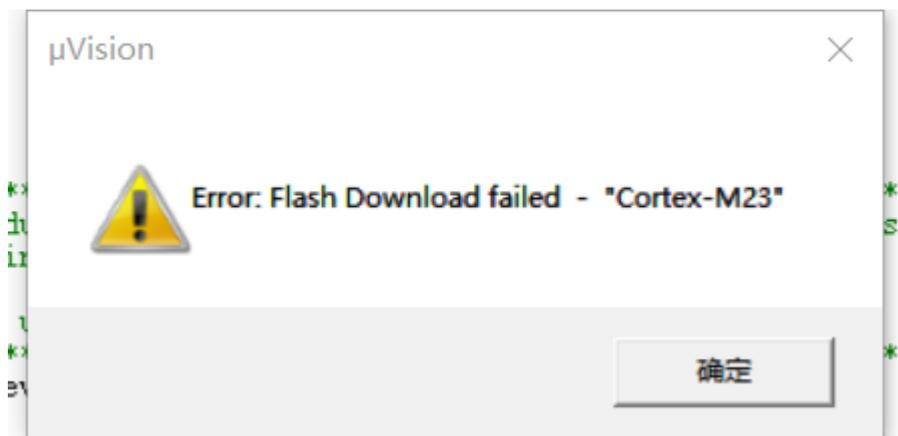


图4 报错2

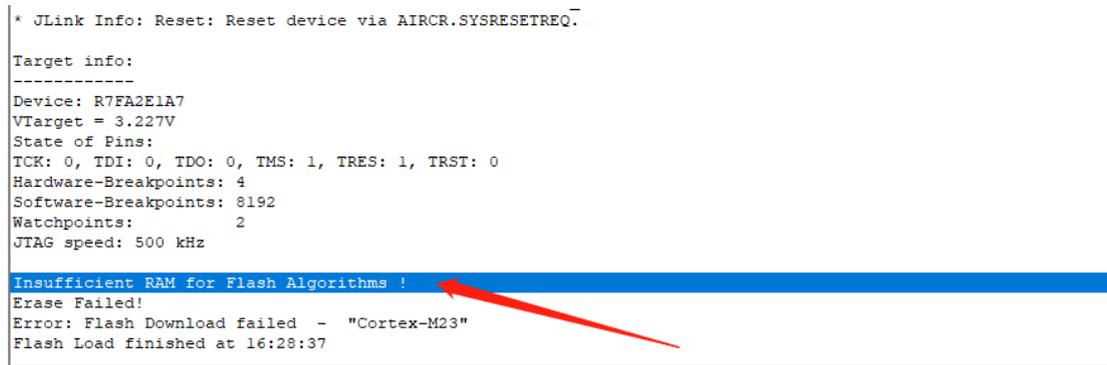


图5 MDK信息栏报错

Cortex JLink/JTrace Target Driver Setup

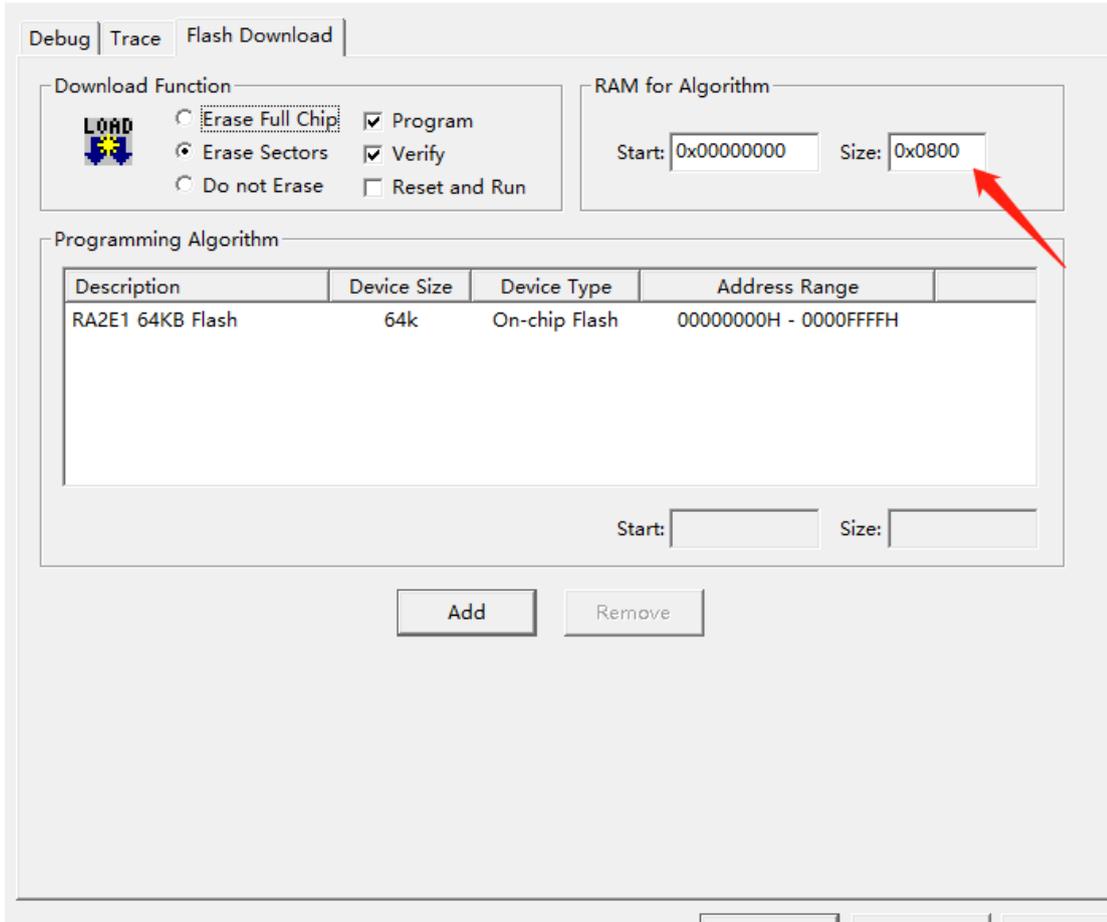


图6 SIZE

3.此时若参考网上的说法"图中箭头所指的地方就是存储烧写算法的RAM空间的大小，这个地方分配过小就会引起上述的错误信息。

将其size改的大一些就可以解决这个问题。"，将size原始0x0800更改为0x1000时，然后下载则会出现如下报错，在第二个报错页面按一下复位时，然后MDK就读不到设备信息了，e2 studio和Renesas Flash Programmer都烧录不进去了

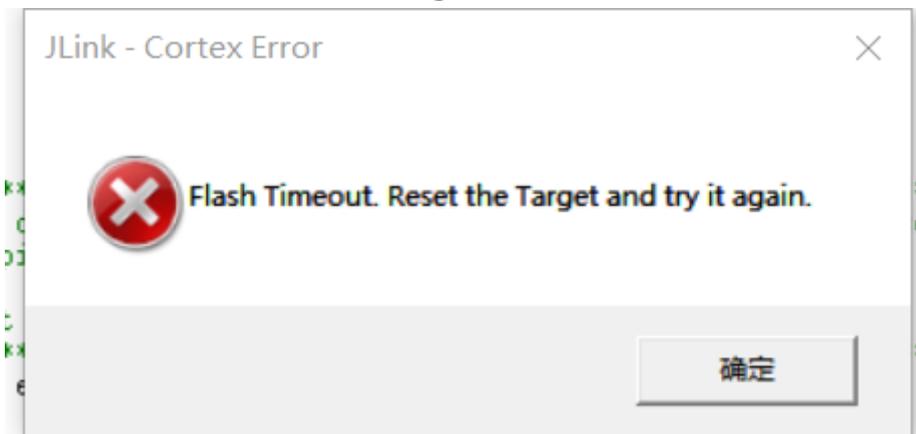


图7 报错1

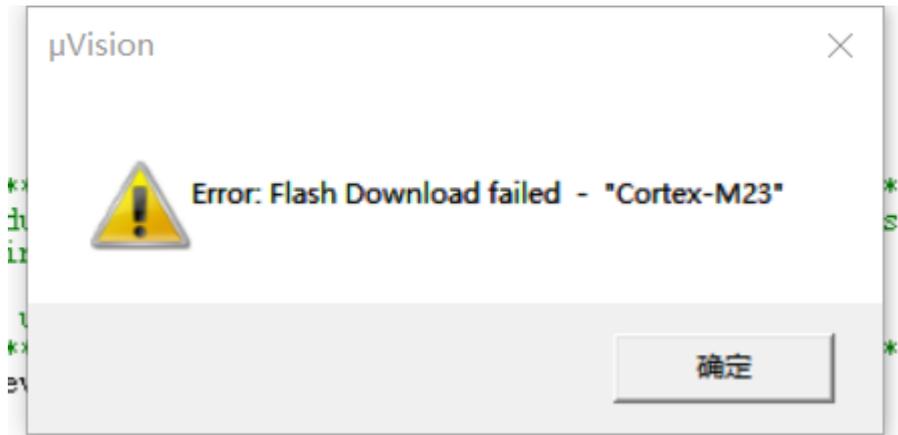


图8 报错2

4.解决方案:

打开JLINK,将供电3.3V改为5V就能读到设备信息,先擦除一下,然后烧录一下,就可换回3.3V供电

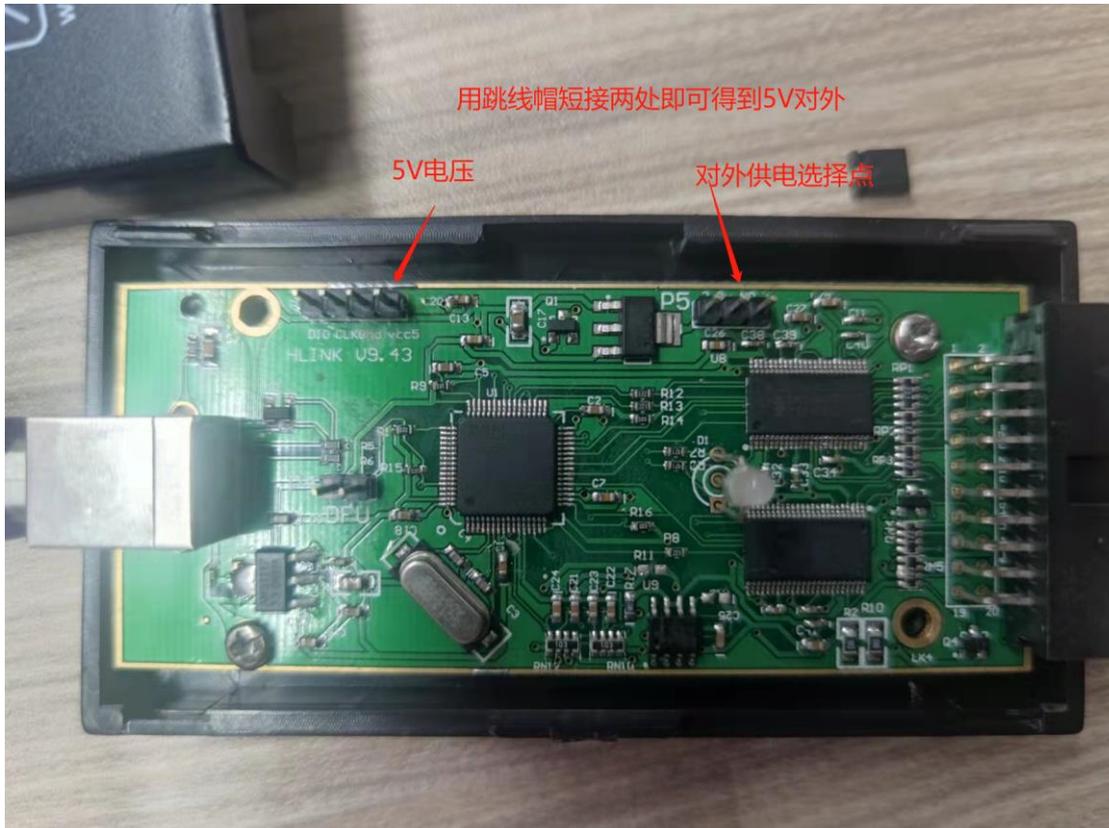


图9 jlink电源选择 (不同版本jlink内部电气不同, 连接仅供参考)

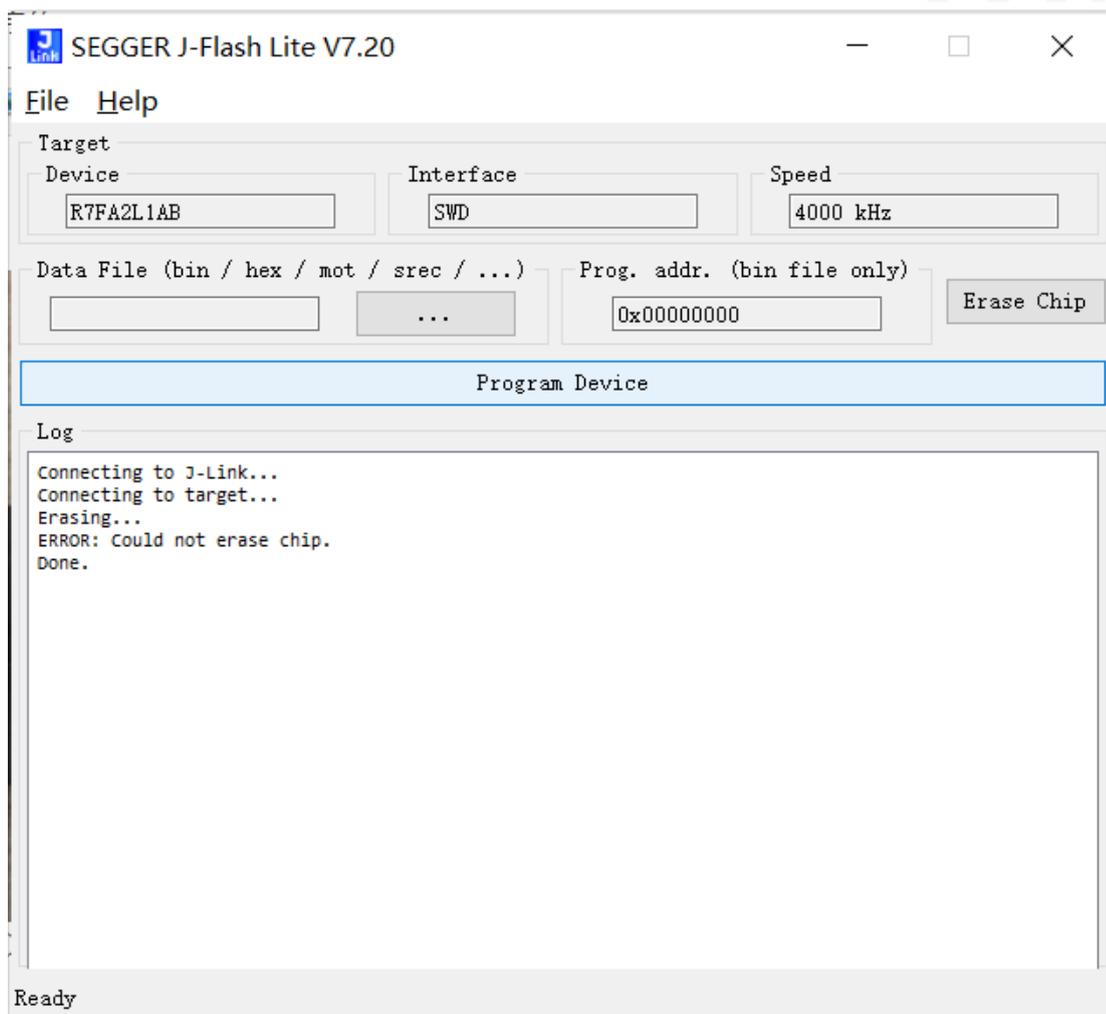


图10 jlink工具擦除成功

5.推出工程并将MDK工程中的.uvoptx文件删除，并重新打开配置jlink,就可得到正确的芯片烧录地址、大小选项，如下图，芯片即可正常烧录仿真了。

Objects	2022/4/1 17:04	文件夹	
ra	2022/4/1 16:05	文件夹	
ra_cfg	2022/4/1 16:05	文件夹	
ra_gen	2022/4/1 16:05	文件夹	
RTE	2022/4/1 16:06	文件夹	
script	2022/4/1 16:05	文件夹	
src	2022/4/1 16:05	文件夹	
.api.xml	2022/4/1 16:06	API_XML 文件	1 KB
.secure_azure	2022/4/1 16:06	SECURE_AZONE 文件	1 KB
.secure.xml	2022/4/1 16:06	SECURE_XML 文件	3 KB
buildinfo.gpdsc	2022/4/1 16:06	GPDSC 文件	9 KB
configuration.xml	2022/4/1 16:06	XML 文档	13 KB
FSP_Project.uvguix.leovo	2022/4/1 17:04	LEOVO 文件	90 KB
FSP_Project.uvoptx	2022/4/1 17:04	UVOPTX 文件	7 KB
FSP_Project.uvprojx	2022/4/1 17:00	vision5 Project	15 KB
JLinkLog.txt	2022/4/1 17:05	文本文档	250 KB
JLinkSettings.ini	2022/4/1 17:03	配置设置	1 KB
memory_regions.scnt	2022/4/1 16:05	SCAT 文件	2 KB
R7FA2E1A72DFL.pincfg	2021/11/18 19:11	PINCFG 文件	2 KB
ra_cfg.txt	2022/4/1 16:06	文本文档	10 KB

Cortex JLink/JTrace Target Driver Setup

Debug | Trace | **Flash Download**

Download Function

Erase Full Chip Program
 Erase Sectors Verify
 Do not Erase Reset and Run

RAM for Algorithm

Start: Size:

Programming Algorithm

Description	Device Size	Device Type	Address Range
RA2E1 64KB Flash	64k	On-chip Flash	00000000H - 0000FFFFH
RA2E1 4KB DataFlash	4k	On-chip Flash	40100000H - 40100FFFH
RA2E1 Config Area	52B	On-chip Flash	01010000H - 01010033H

Start: Size:

Add Remove

确定 取消 应用(A)

Build Output

```
* JLink Info: AP[0]: AHB-AP ROM base: 0x4001A000
* JLink Info: CPUID register: 0x411CD200. Implementer code: 0x41 (ARM)
* JLink Info: Feature set: Baseline
* JLink Info: Found Cortex-M23 r1p0, Little endian.
* JLink Info: FPUnit: 4 code (BP) slots and 0 literal slots
* JLink Info: Security extension: not implemented
* JLink Info: CoreSight components:
* JLink Info: ROMTbl[0] @ 4001A000
* JLink Info: [0][0]: E000E000 CID B105900D PID 000BBD20 DEVARCH 47702A04 DEVTYPE 00 Cortex-M23
* JLink Info: [0][1]: E0001000 CID B105900D PID 000BBD20 DEVARCH 47701A02 DEVTYPE 00 DWT
* JLink Info: [0][2]: E0002000 CID B105900D PID 000BBD20 DEVARCH 47701A03 DEVTYPE 00 FPB
* JLink Info: [0][3]: 40019000 CID B105900D PID 000BBD20 DEVARCH 47710A31 DEVTYPE 31 MTB
ROMTableAddr = 0x4001A000
* JLink Info: Reset: Halt core after reset via DEMCR.VC_CORERESET.
* JLink Info: Reset: Reset device via AIRCR.SYSRESETRQ.

Target info:
-----
Device: R7FA2E1A7
VTarget = 4.933V
State of Pins:
TCK: 0, TDI: 0, TDO: 0, TMS: 1, TRES: 1, TRST: 0
Hardware-Breakpoints: 4
Software-Breakpoints: 8192
Watchpoints: 2
JTAG speed: 4000 kHz

Erase Done.
Programming Done.
Verify OK.
Flash Load finished at 17:05:24
```

6.同样的操作方式若将strat改为0x01010010 (这个地址即是On-chip flash (option-setting memory))size 0x1000, 同上述操作, 在报错二处按下复位键, 则一直提示要输入ID CODE,目前没有方法解决。

