RA MCU 生态工作室

瑞萨RA系列之 keil环境

1. 瑞萨官网

用户可到瑞萨官网根据需求筛选型号。

（瑞萨官网：https://www2.renesas.cn/cn/zh）

2. Keil开发环境：

RA SC(RA Smart Configurator)

（RASA安装包:https://www2.renesas.cn/cn/en/software-tool/ra-smart-configurator）

keil ： 推荐版本5.34 (尽量5.28或以上)

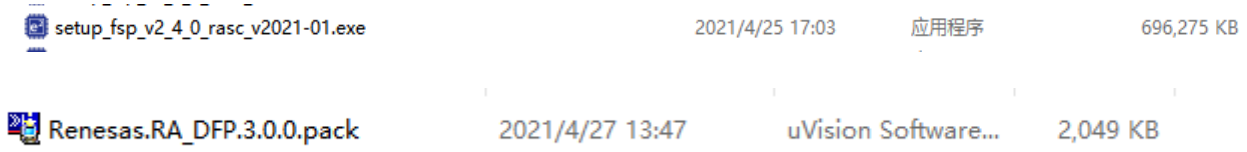
Jlink：硬件jlink_V9

（上位机关系不大，不是太老的版本都可以 推荐：jlink_v698）

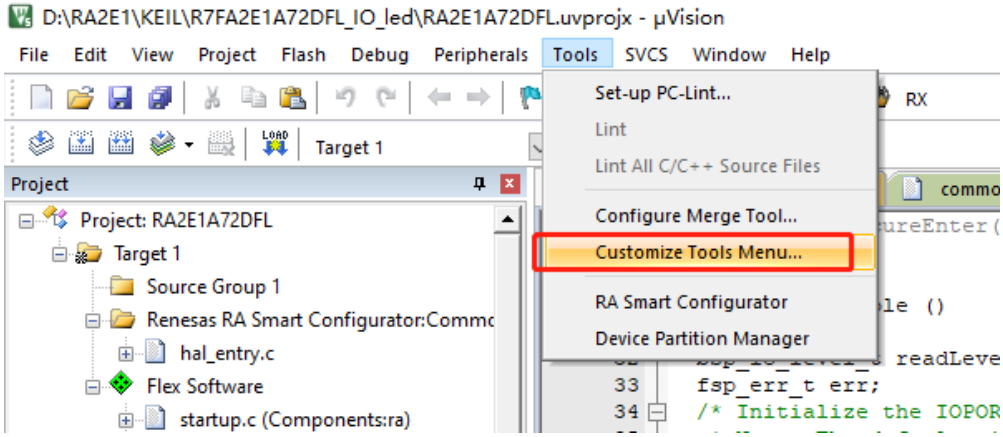
3. 环境安装

参考Flexible Software Package (FSP) User Manual手册第2.6章节的MDK指导，完成下列步骤

3.1 安装完成RA SC，安装MDK_Device_Packs（安装尽量使用英文路径,网盘链接在文末）

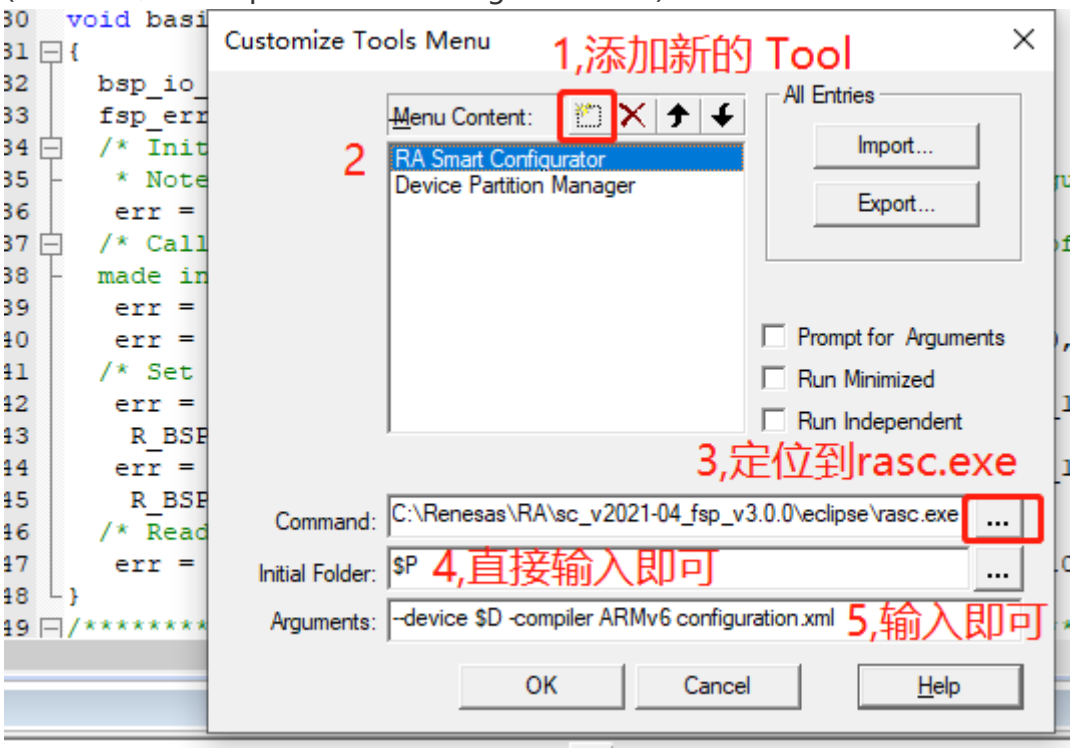


3.2 在keil--tool添加2个配置



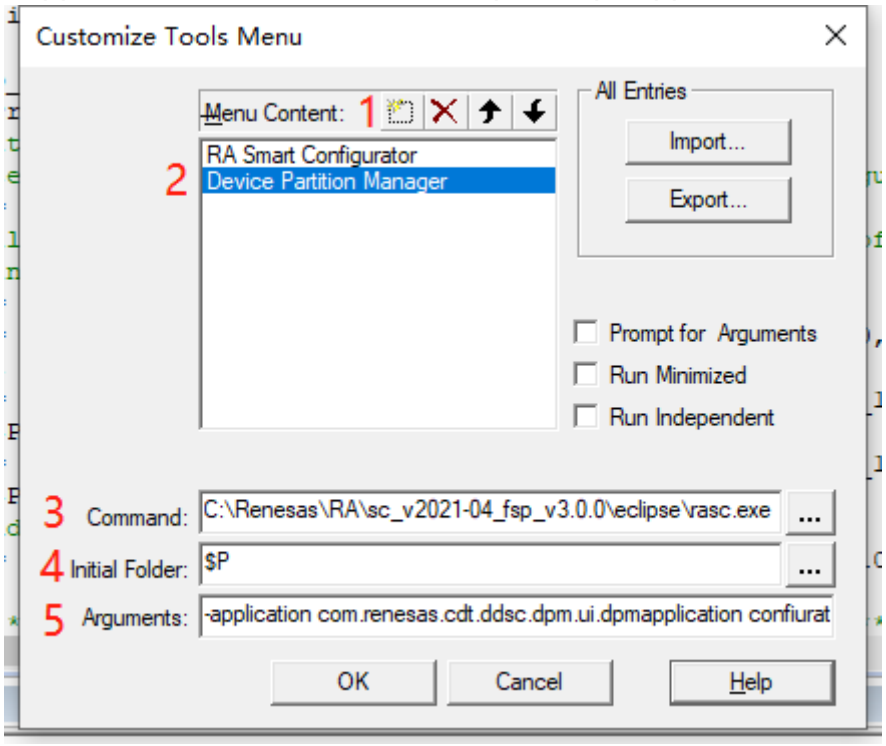
3.2.1 添加 RA Smart Configurator.

(--device $D -compiler ARMv6 configuration.xml)



3.2.2 参照a添加Device Partition Manager

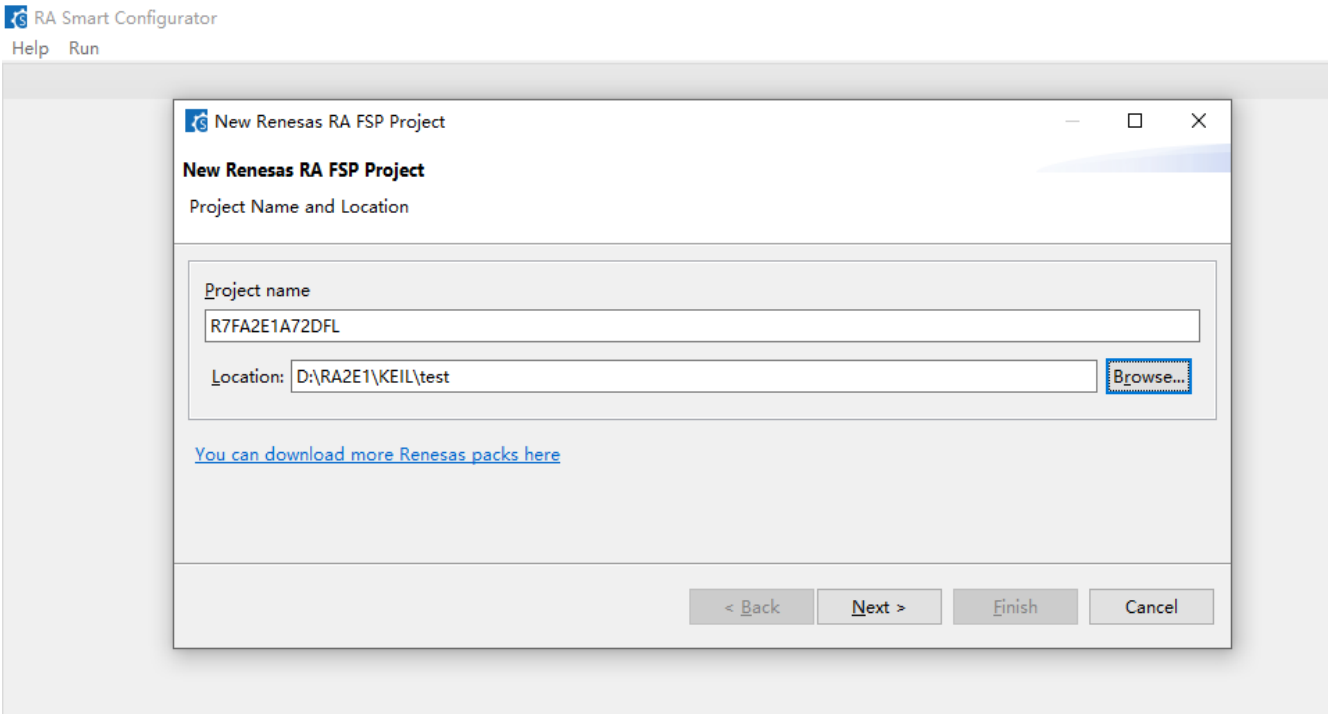
(-application com.renesas.cdt.ddsc.dpm.ui.dpmapplication confiuration.xml "SL%L")



4. 创建keil新工程

4.1 打开rasc.exe， 输入工程名和工程路径

(rasc.exe默认安装路径是 C:\Renesas\RA\sc_v2021-01_fsp_v2.4.0\eclipse)

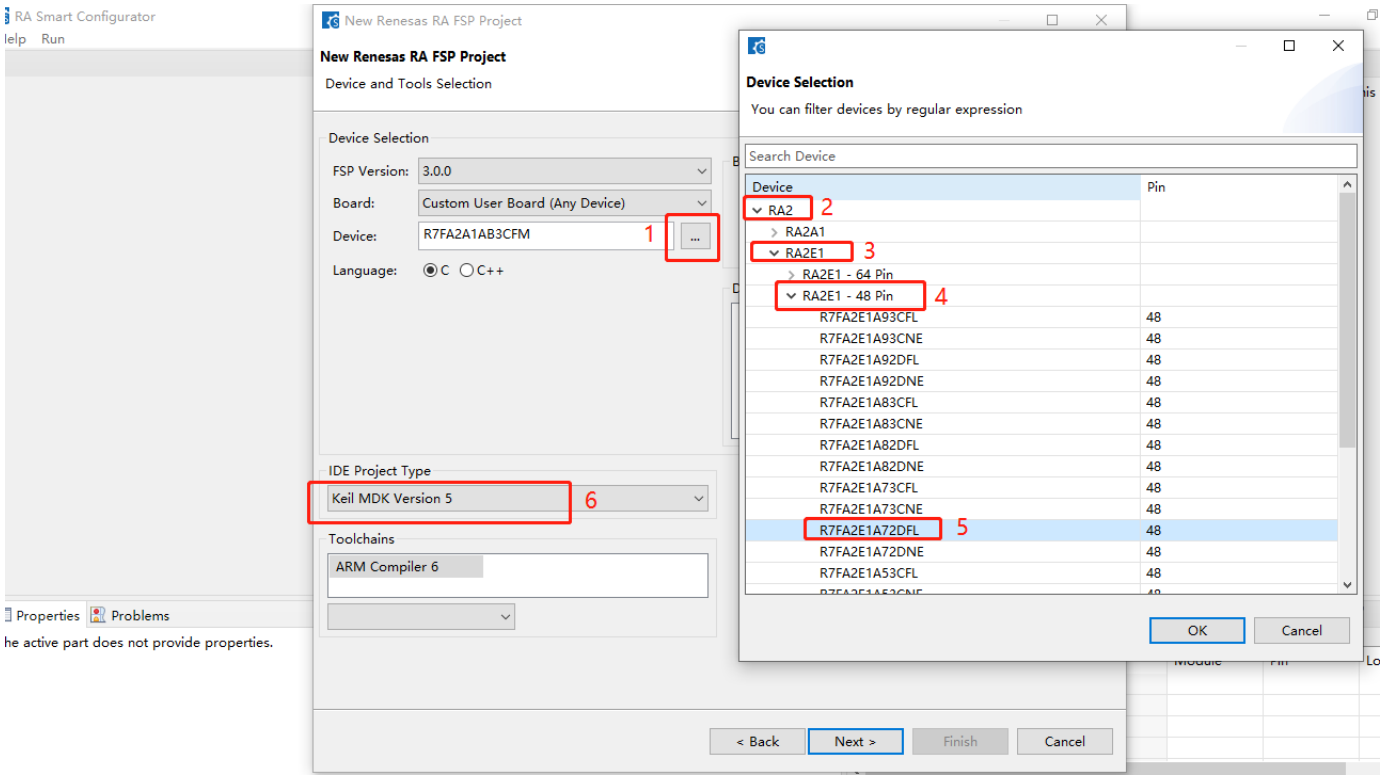


4.2 RA Project配置

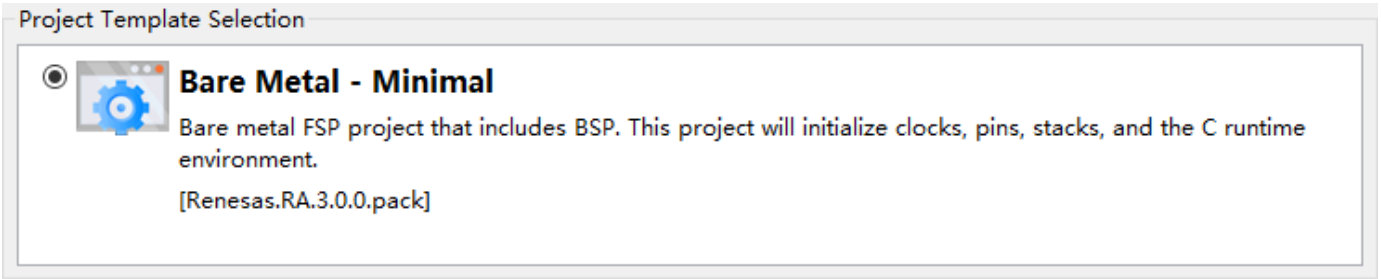
FSP Version是安装的rasc的版本 3.0.0

Device选择MCU具体型号，

IDE选择keil



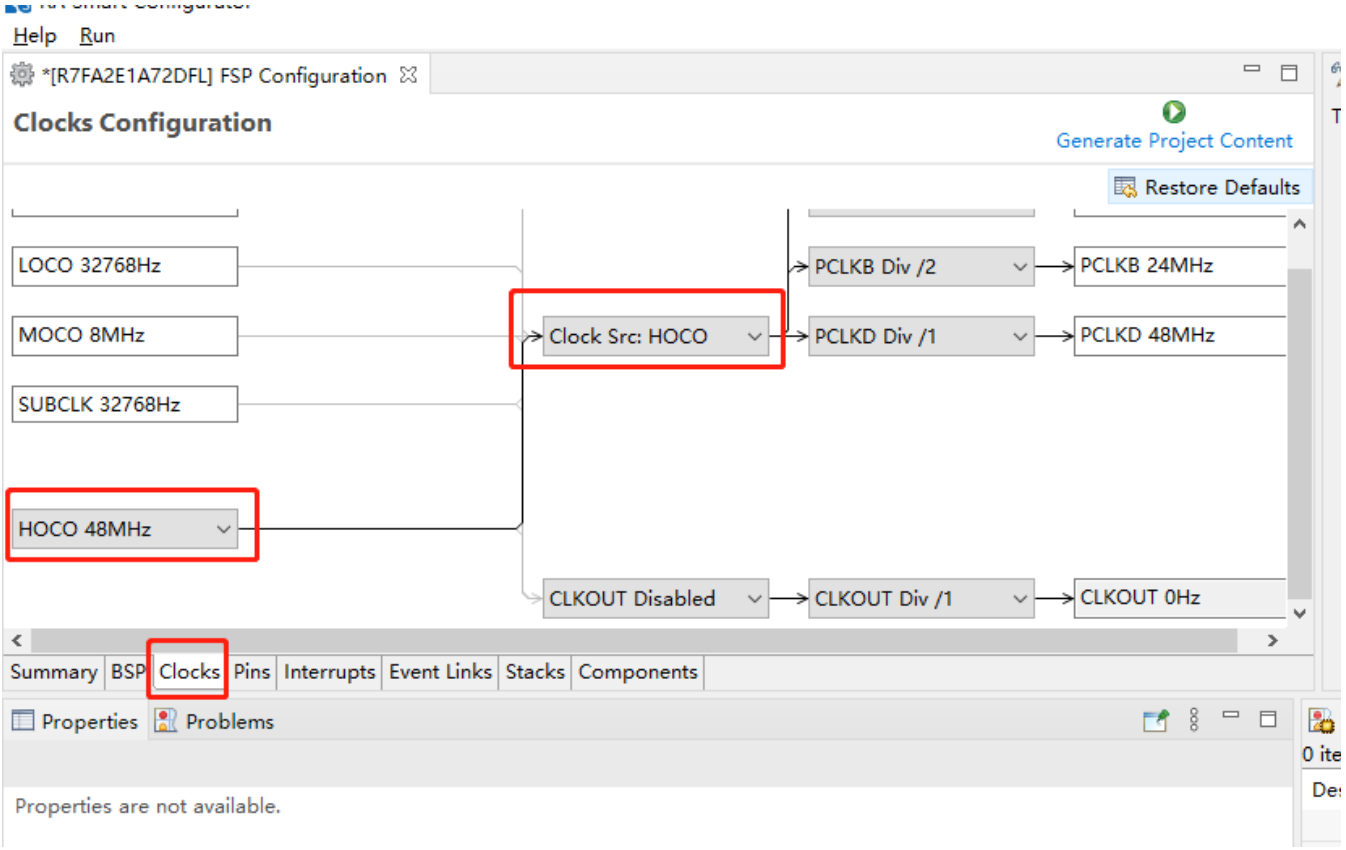
(根据需求选择是否使用RTOS)



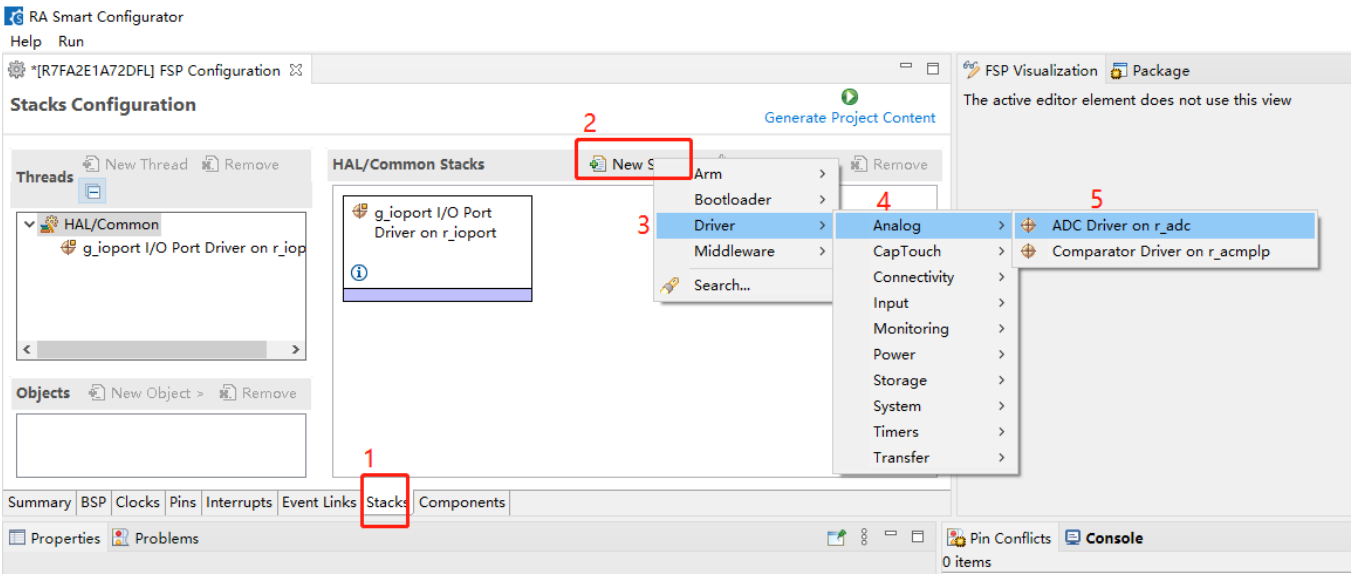
4.3 以配置ADC为例

(具体可参考FSP 4.2章节r_adc部分)

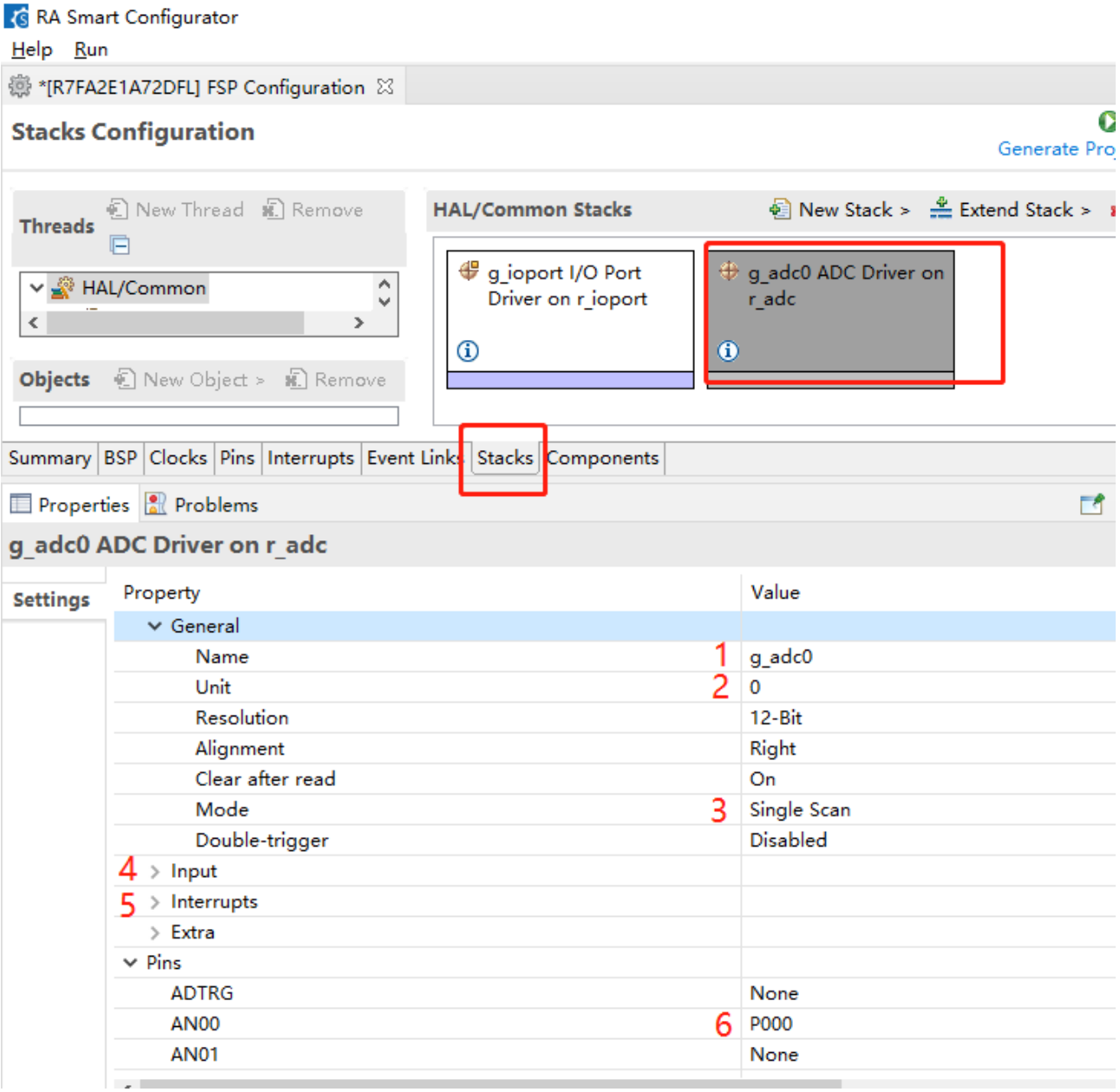
4.3.1 配置主时钟为内部高速48MHz



4.3.2 在stack添加ad模块



4.3.3 在属性栏配置相关参数



(1) 模块名。

(2) 配置ad通道。

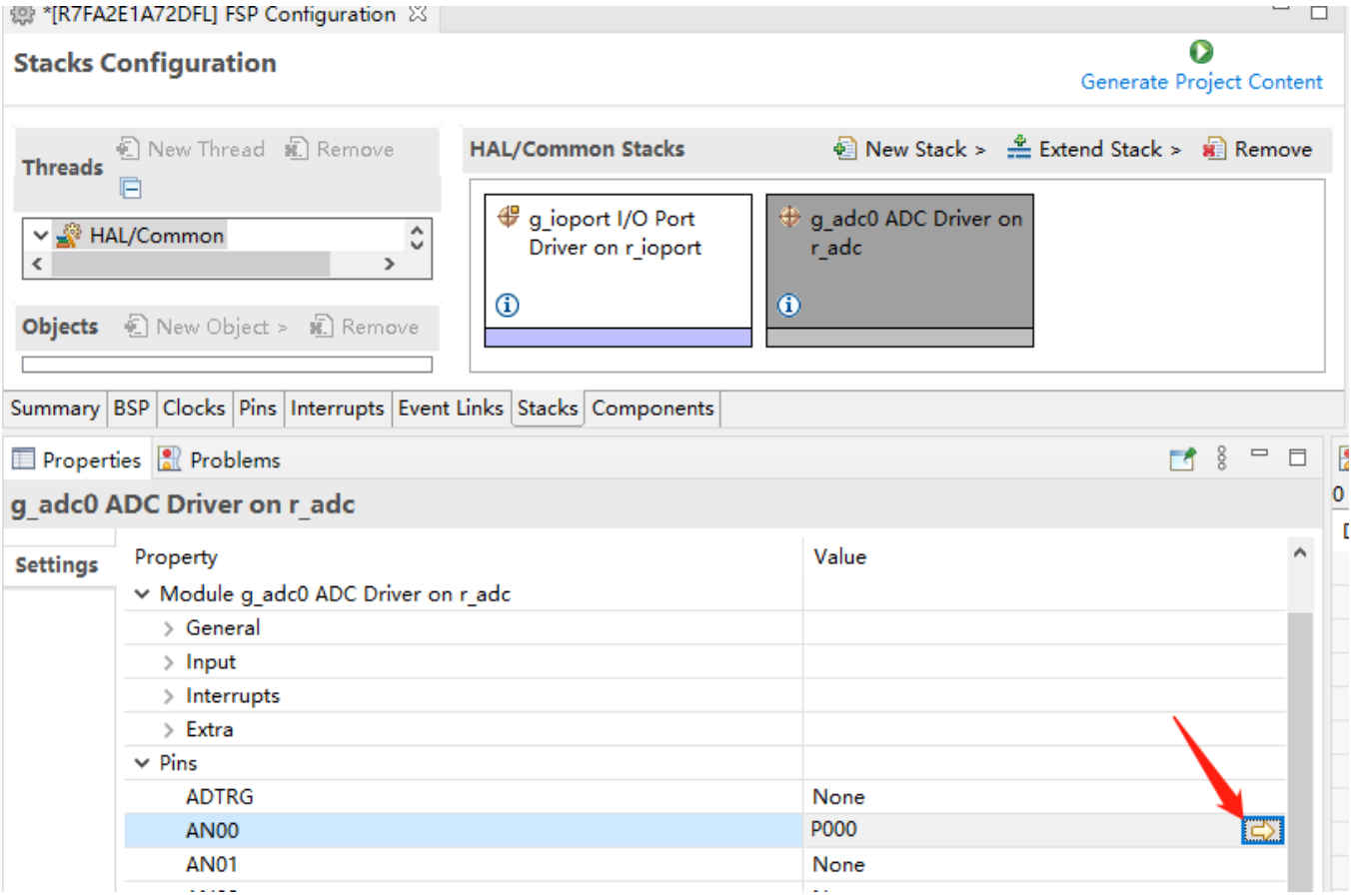
(3) 配置扫描模式

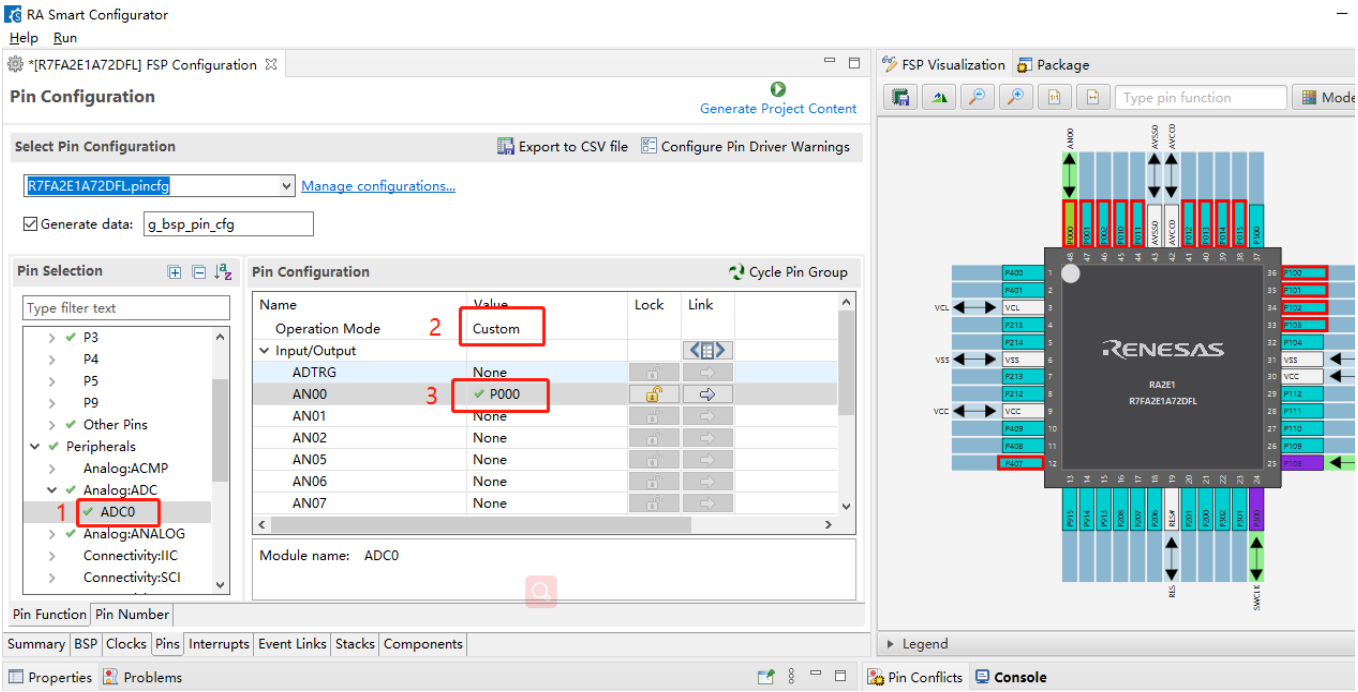
(4) 打开ad通道

(5) 配置ad中断

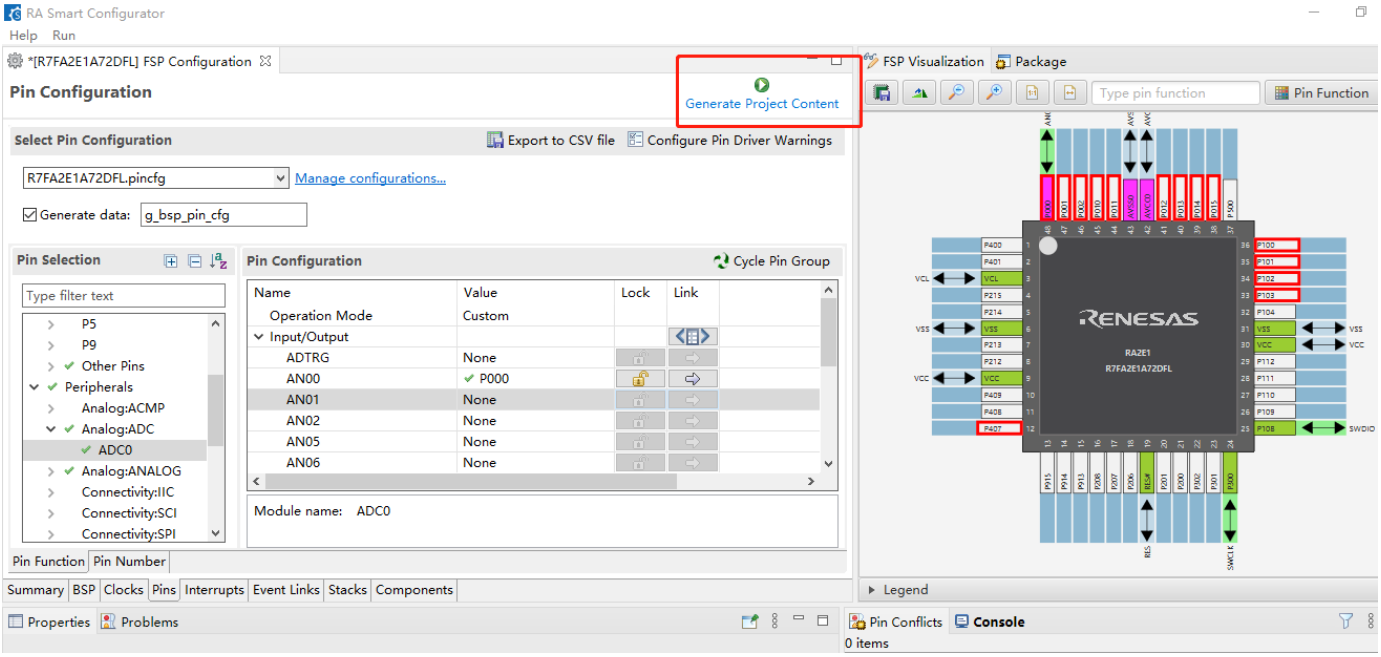
(6) 选择AD通道对应的IO口

4.3.4 点击ad通道 AN00，会出现跳转箭头，可直接跳转到Pins的AD引脚部分进行配置

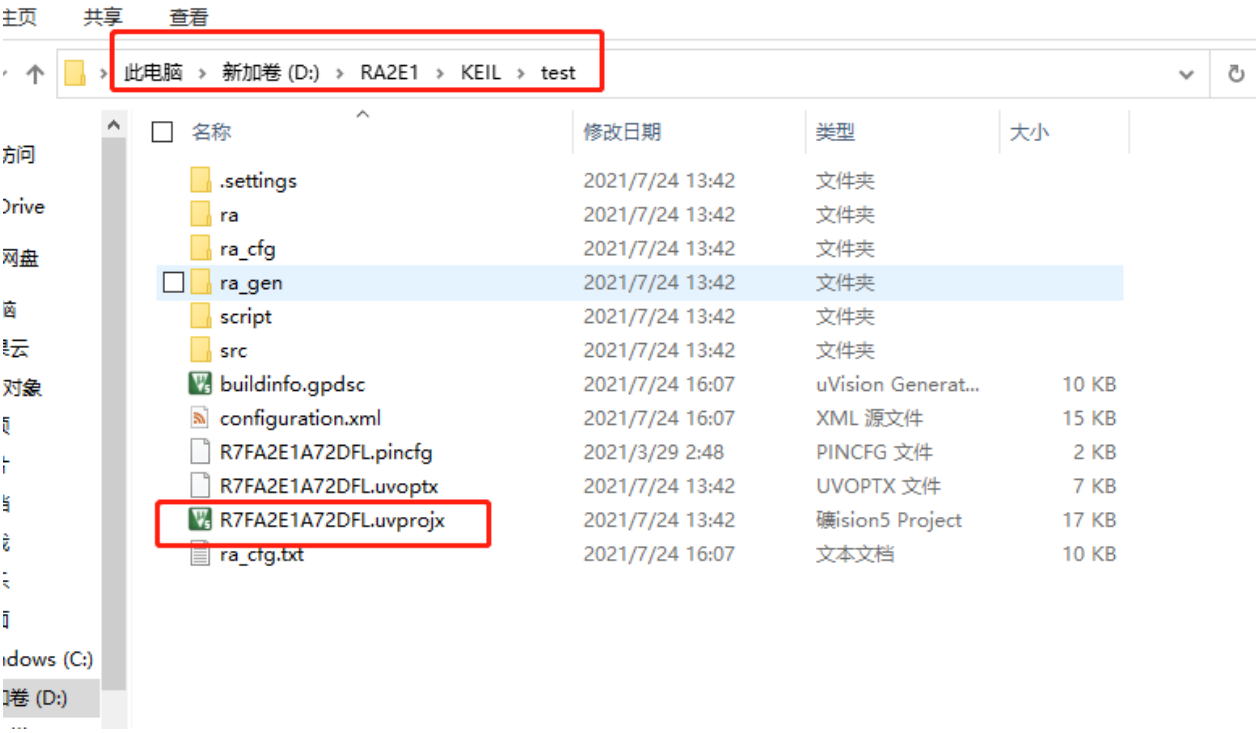




4.3.5 配置完成后点 Generate Project Content生成代码



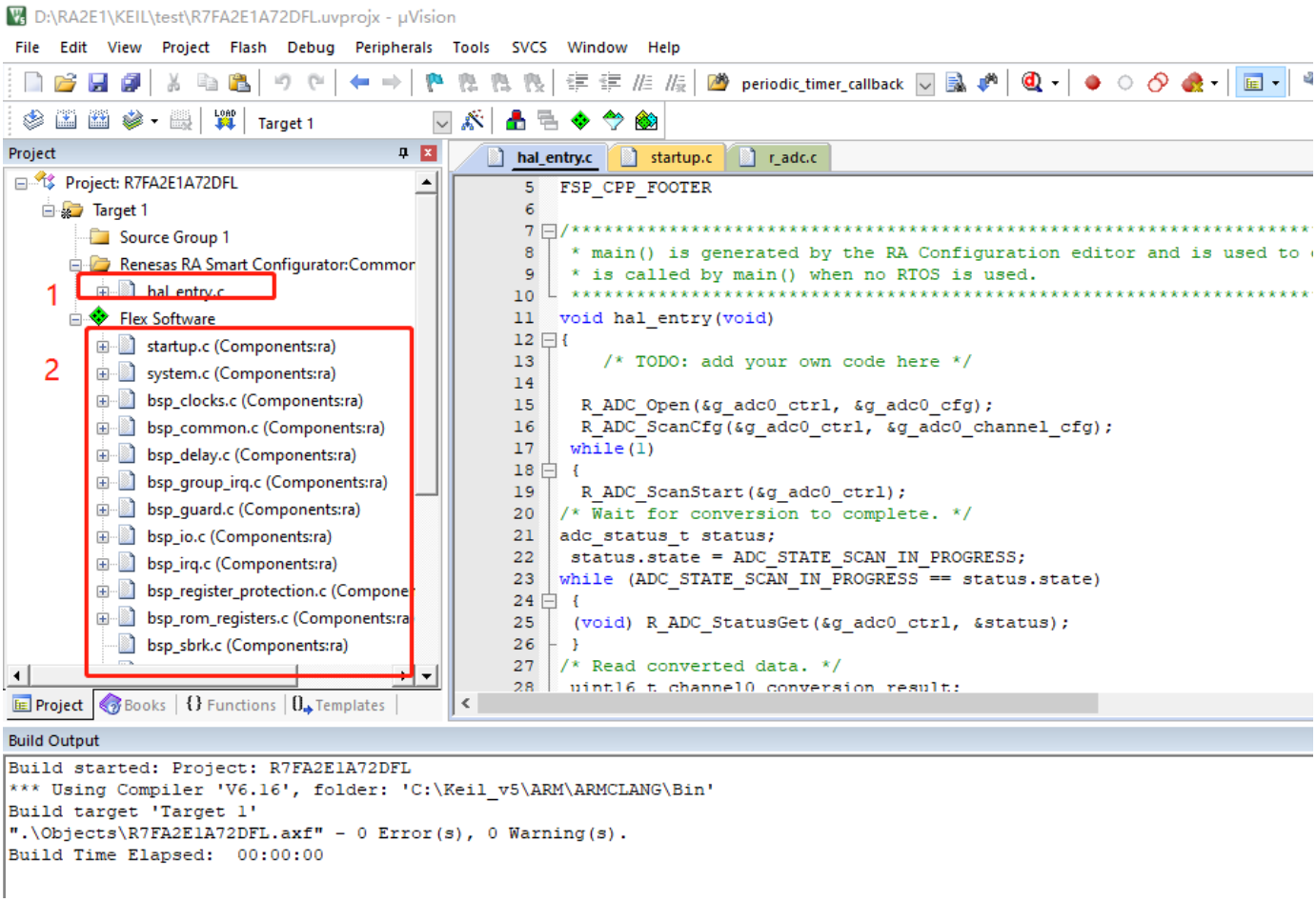
4.3.6 打开生成的工程



4.3.7 生成的工程编译0 Error,0 Warning。

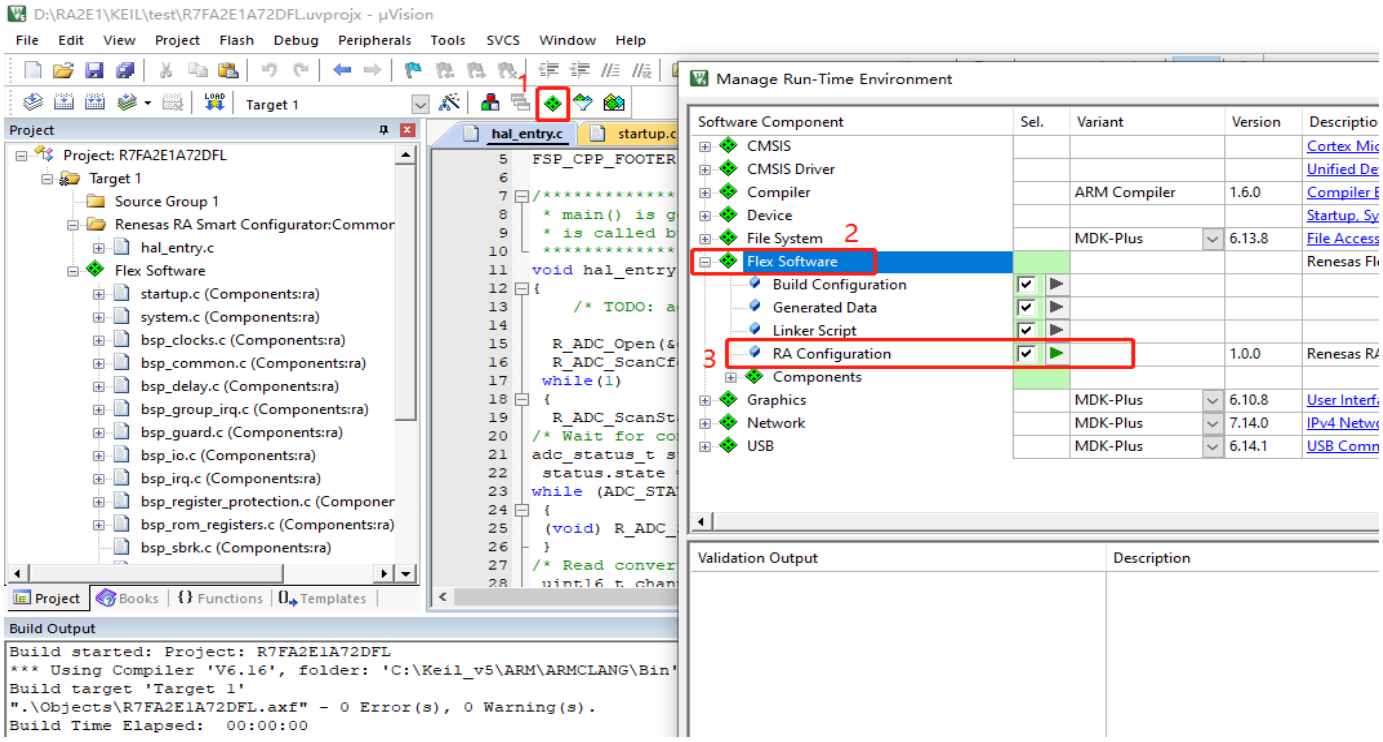
（参考FSP 4.2章节的例程来写代码，或参考官方例程。）

1是用户编写代码的地方，2是RA Smart Configuration配置初始化生成的代码。用户代码尽量写在1 hal_entry.c中，因为当RA Smart Configuration初始化生成代码时会重新覆盖2中的代码。



4.3.8 如果需要再次打开RA Smart Configuration配置参数，

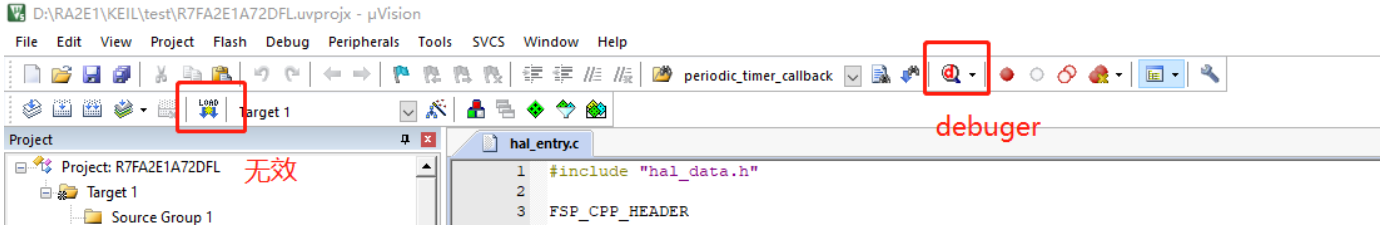
如图下所示，从这里打开RA Smart Configuration就可以与工程关联起来。

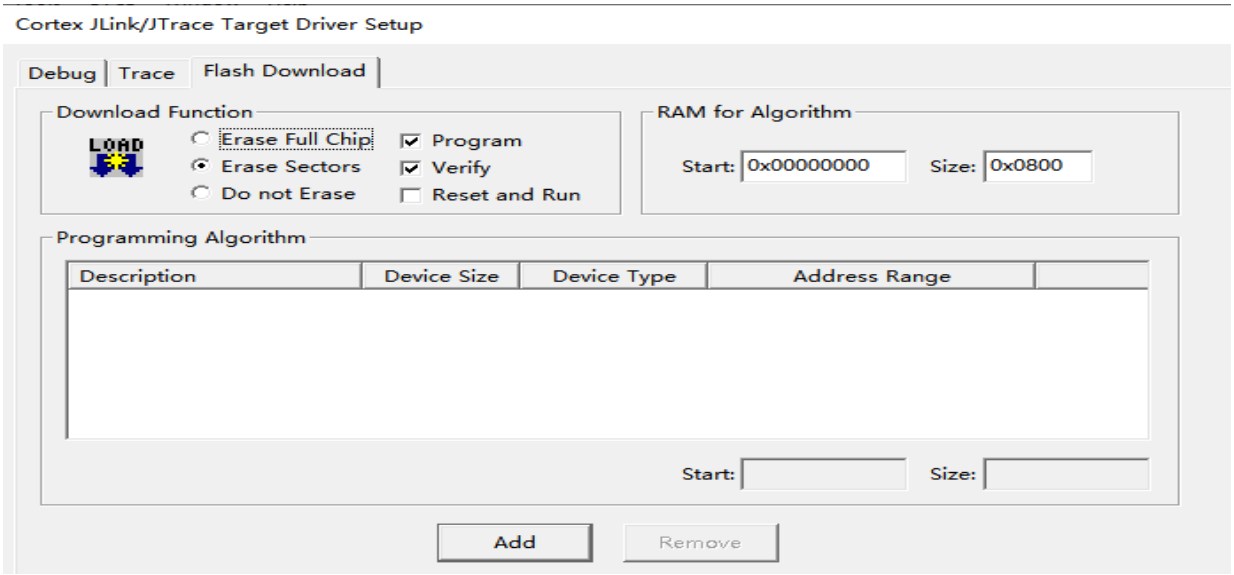


4.3.9 烧录方式

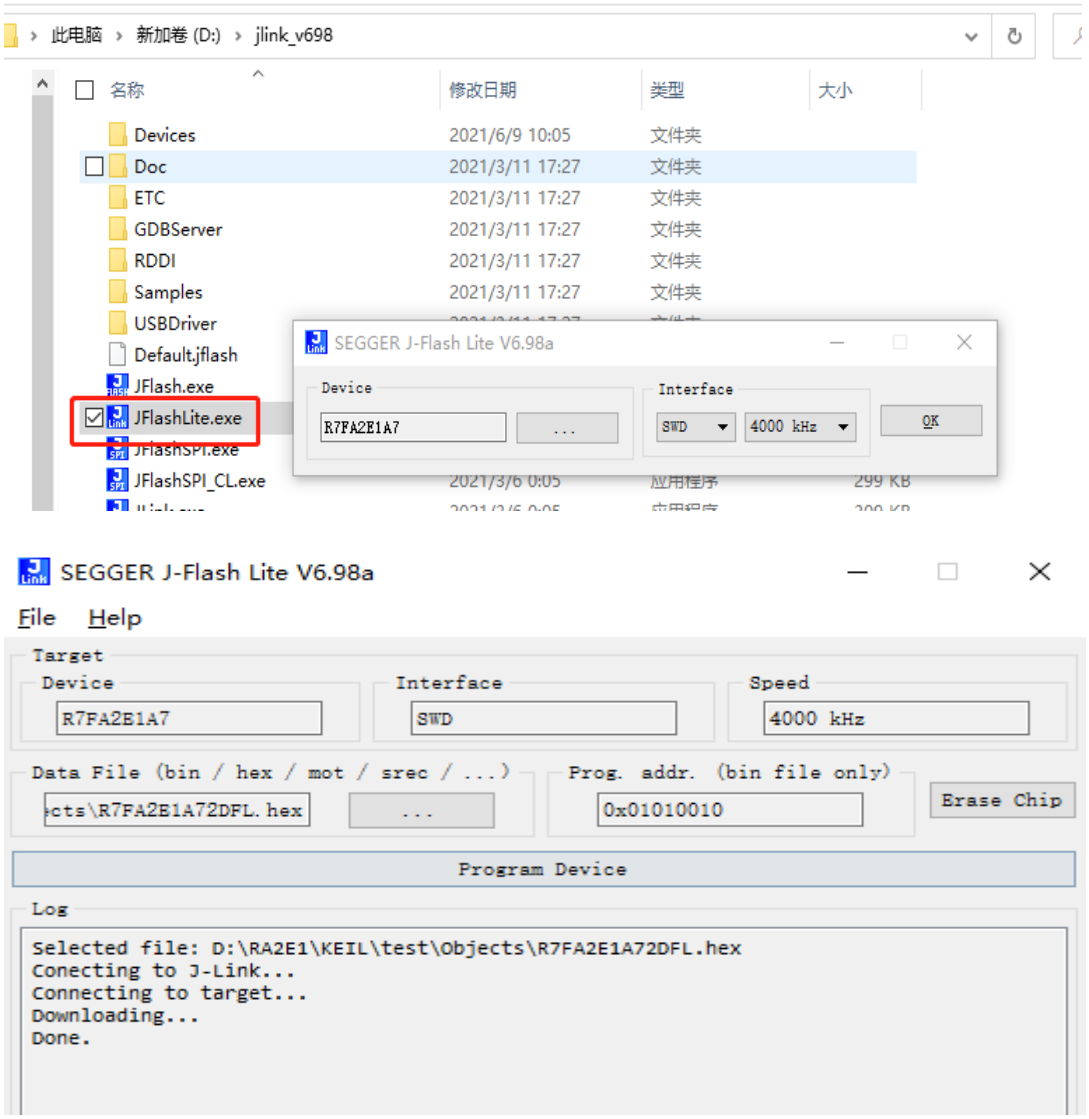
可使用Jlink(硬件V9)在keil中点仿真烧录

(debug-settings-Flash Download中不需要添加)



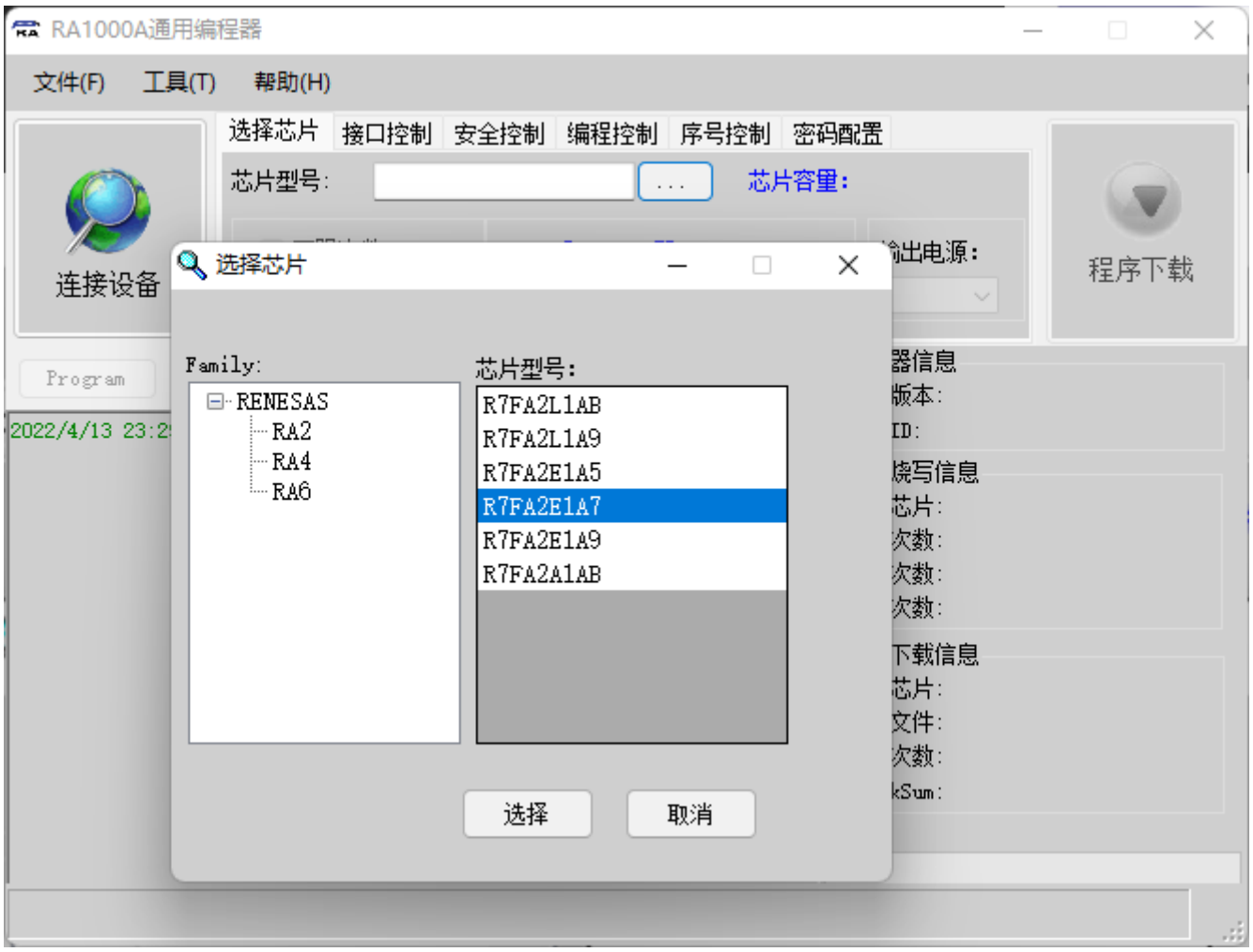


也可以使用Jlink带的 JFlashLite.exe(注意不是Jflash)。



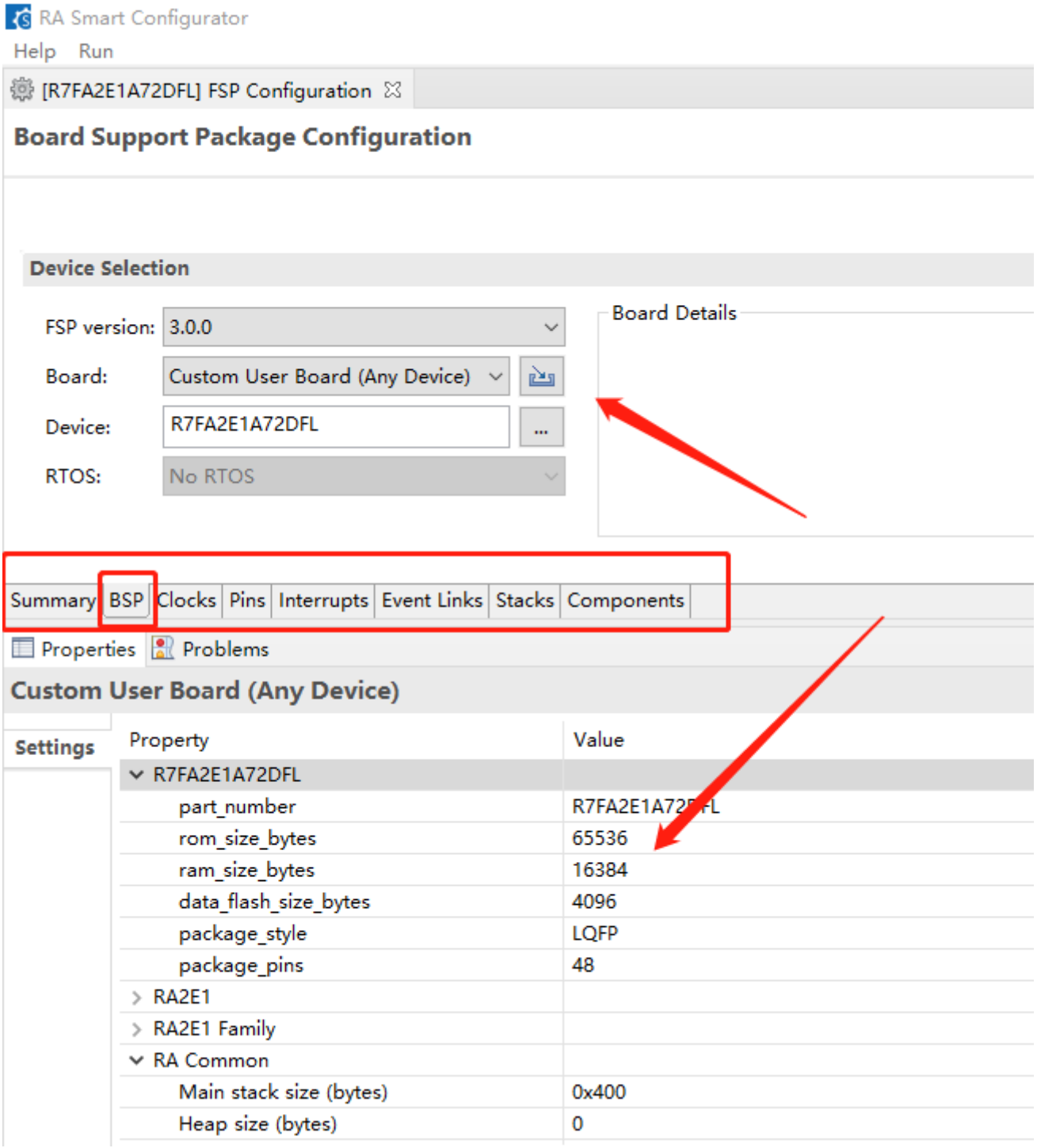
或是使用RA MCU 生态工作室的RA1000A脱机烧录

RENESAS RA
生态工作室



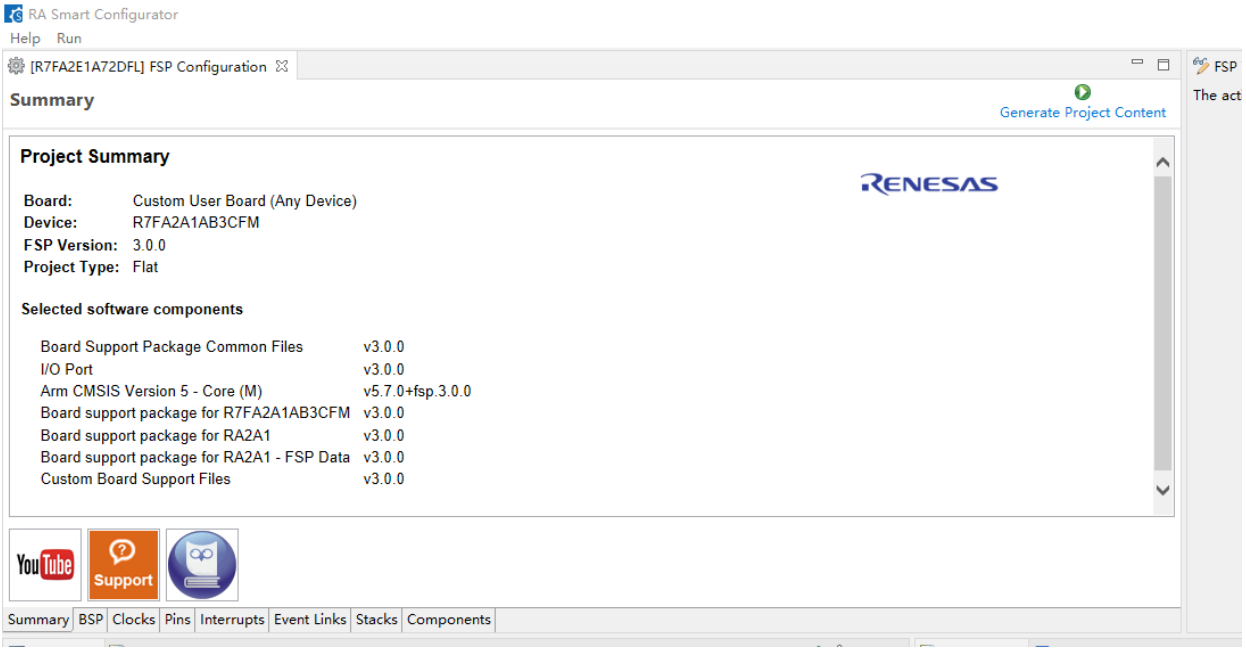
4.4 功能介绍

在RA Smart Configuration中，可选参数在上半部分，属性在下半部分。

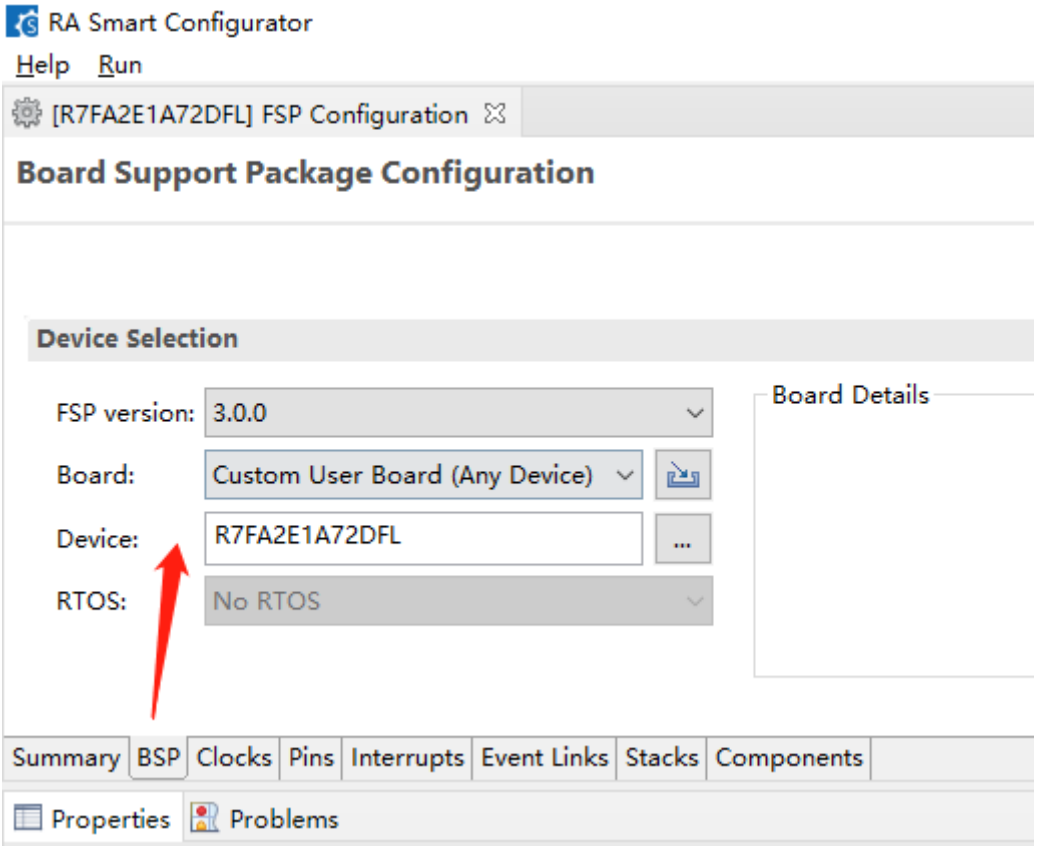


4.4.1 Summary 确定了项目的所有关键元素和组件。

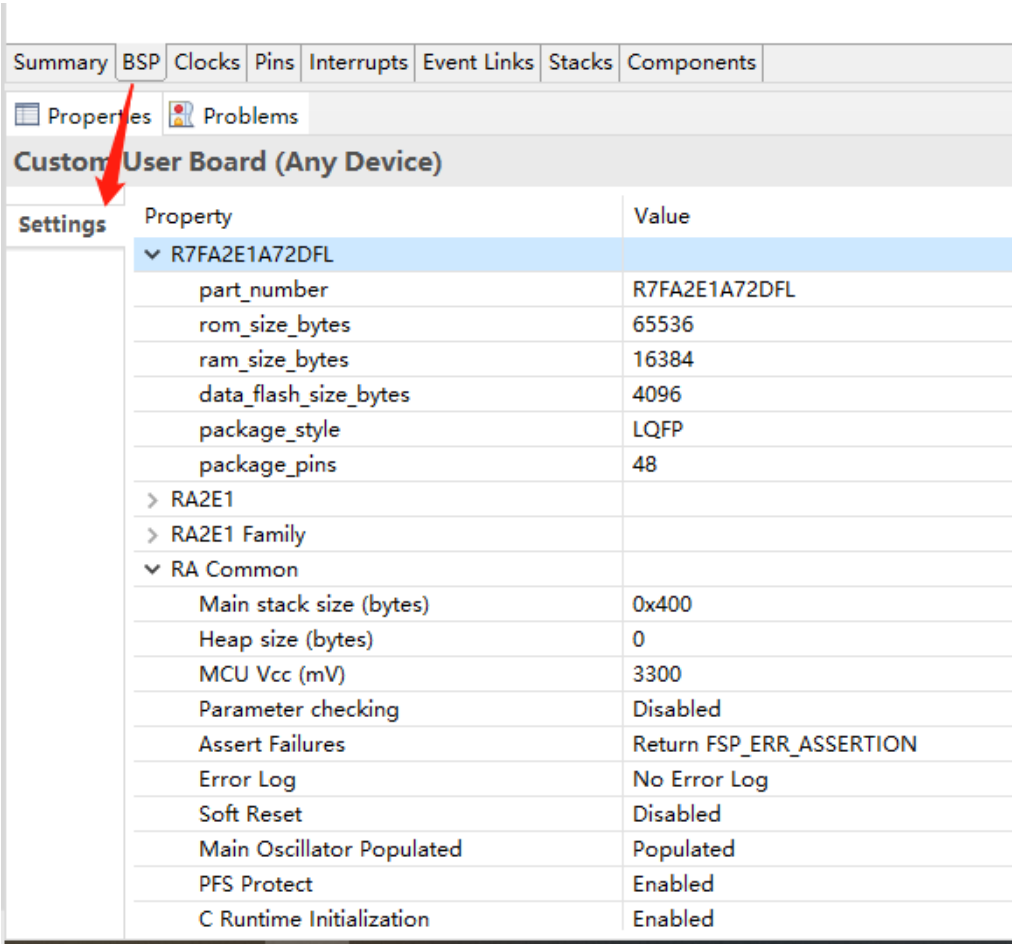
显示目标板，设备，工具链和FSP版本。



4.42 BSP 显示当前选择的FSP和device。



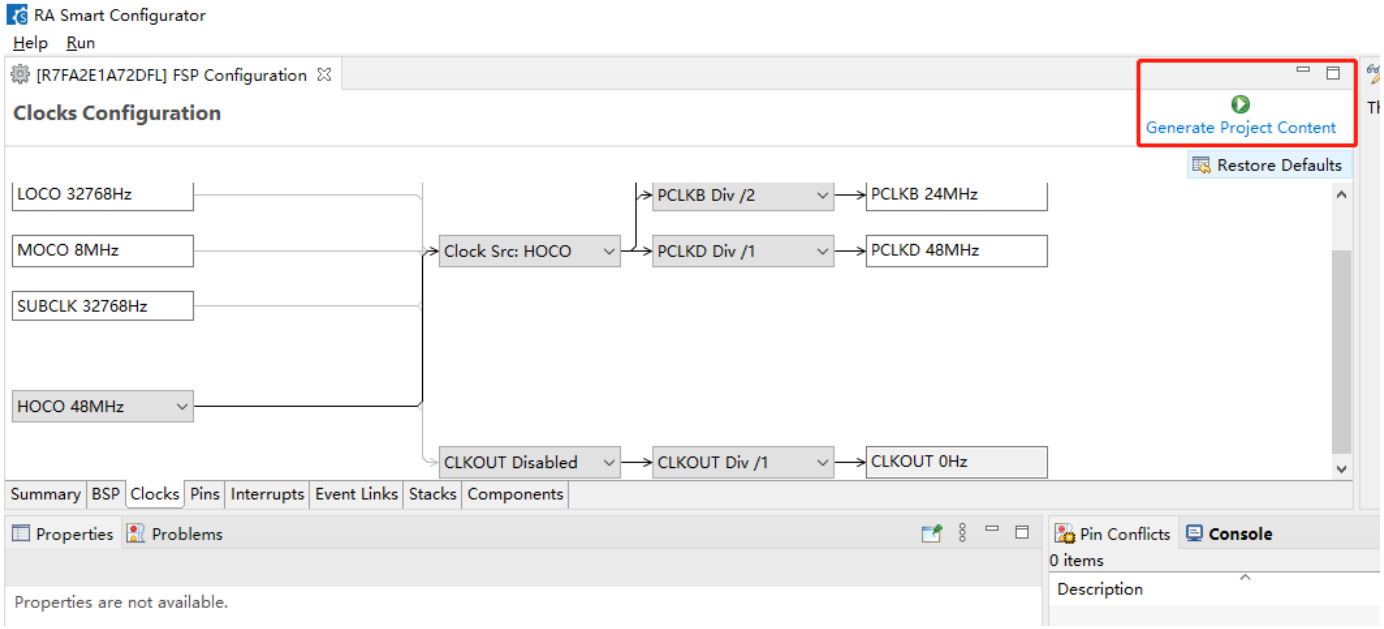
可在BSP属性配置中查看rom size，也可以配置是否使用副时钟等功能.



(When you click the Generate Project Content button, the BSP configuration contents are written to ra_cfg/fsp_cfg/bsp/bsp_cfg.h)

4.43 Clock 显示可配置时钟树

允许修改各种时钟分频器和时钟源，如果时钟设置无效，违规的时钟值将用红色突出显示。仍然可以使用此设置生成代码，但不能保证正确的操作。

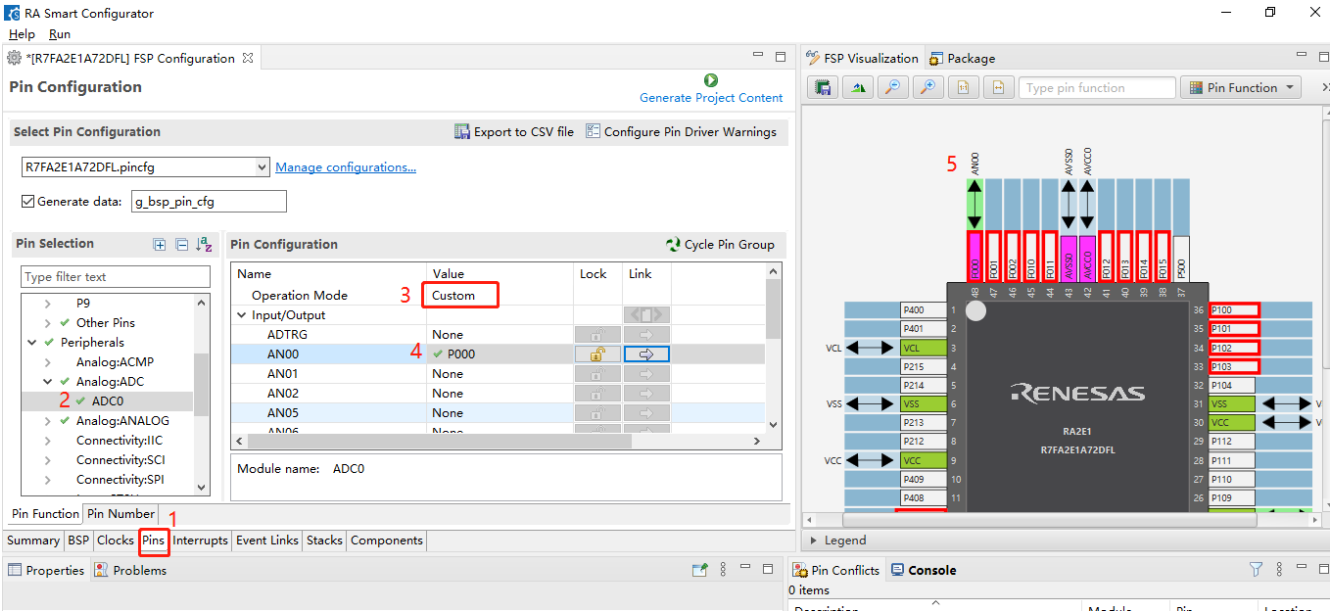


(When you click the Generate Project Content button, the clock configuration contents are written to: ra_gen/bsp_clock_cfg.h)

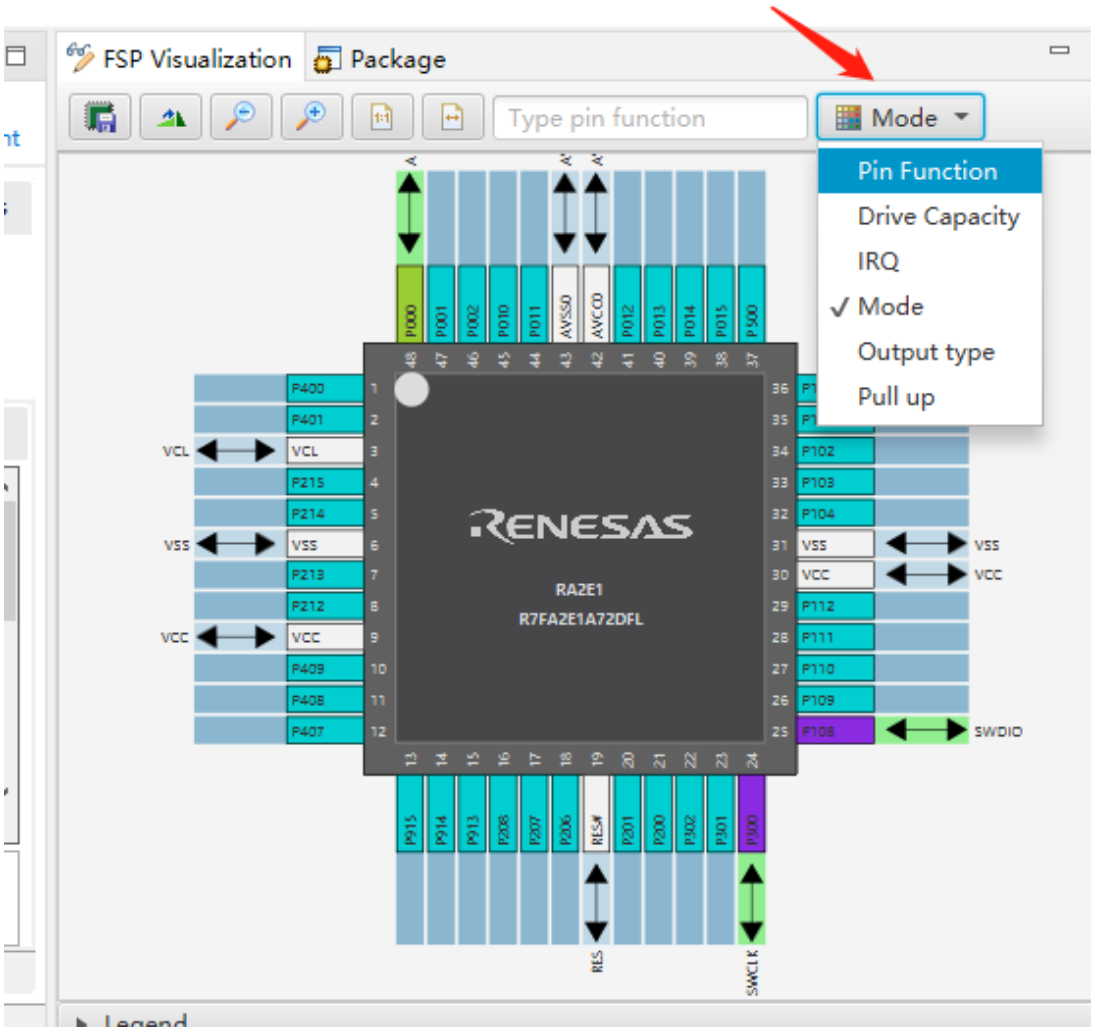
4.44 Pins 配置引脚

提供MCU引脚的灵活配置。由于许多引脚能够提供多种功能，它们可以在外围基础上进行配置，配置相关

功能之后会在右侧Package视图中显示绿色。



可根据每个引脚的选定电气或功能特性显示封装视图。



(When you click the Generate Project Content button, the pin configuration contents are

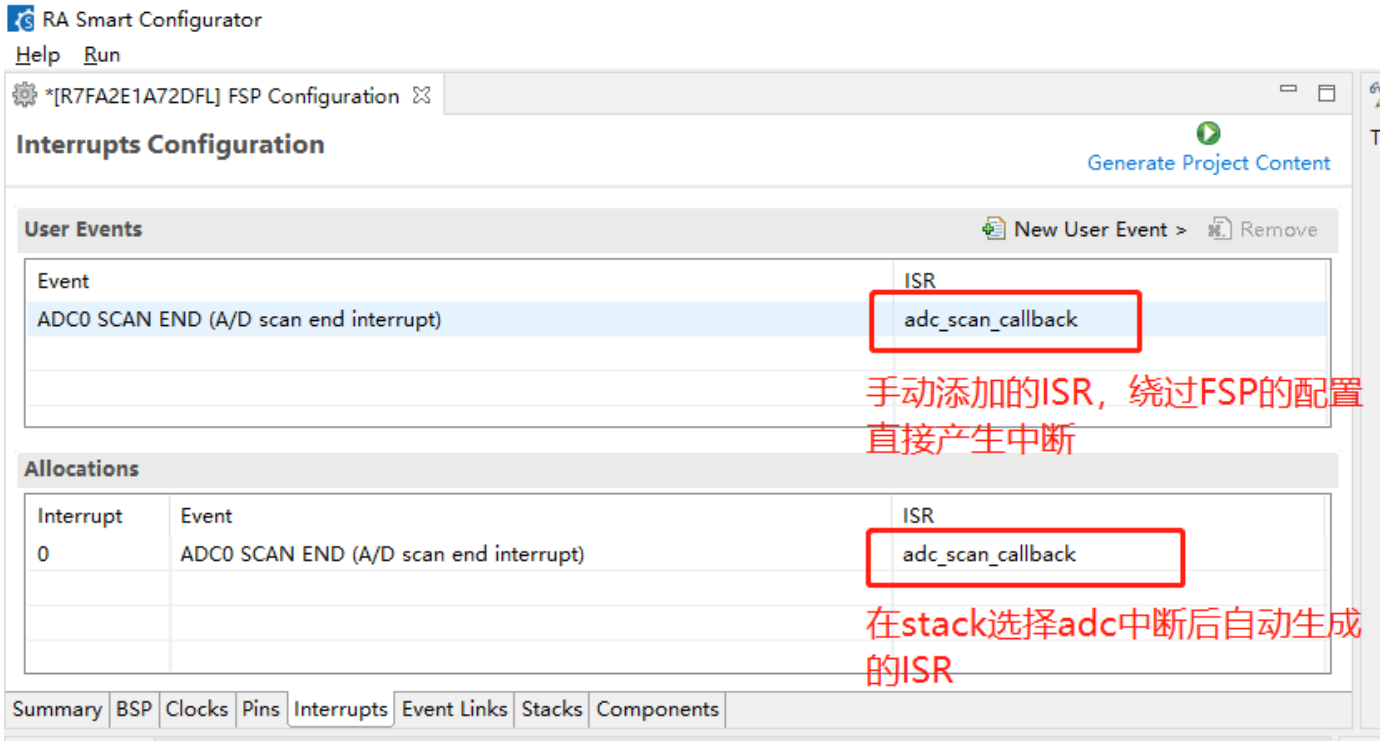
Written to: ra_gen\bsp_pin_cfg.h)

4.45 Interrupts

添加中断的两个方法：

用户可以通过设置自定义ISR来绕过FSP设置的外围中断。这可以通过通过New User event按钮添加一个新事件来实现。

或是使用Stacks选项卡中的Properties视图通过设置中断优先级来启用中断。在Stacks窗格中选择驱动程序以查看和编辑其属性。



4.46 Event Links 可以查看ELC的事件信息。

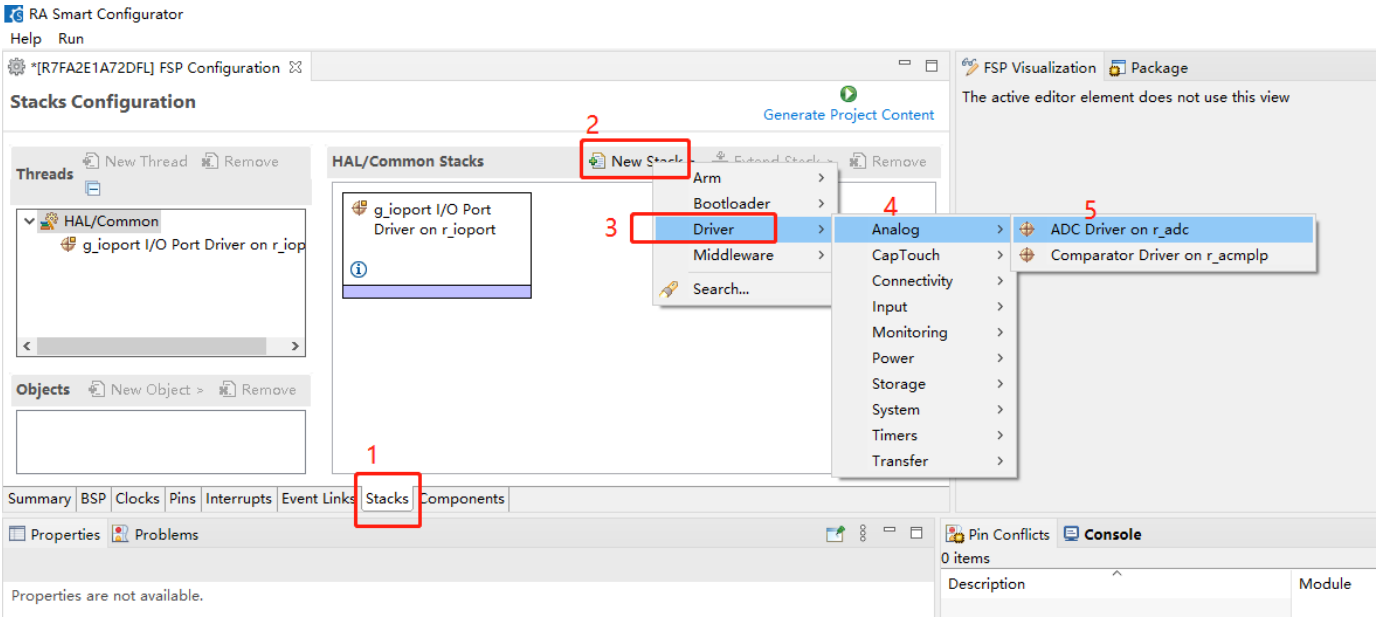
事件按外围设备排序，便于查找和验证。利用各个外设模块产生的事件请求作为源信号，将各个外设模块连接到不同的模块，实现模块之间直接连接，不需要CPU干预，当为模块选择接收一个ELC事件时(或者当手动定义一个事件链接时)，只有项目中配置的模块可用的事件才会显示出来。

4.47 Stack 通过图形界面添加驱动，并在下方的属性中配置参数。

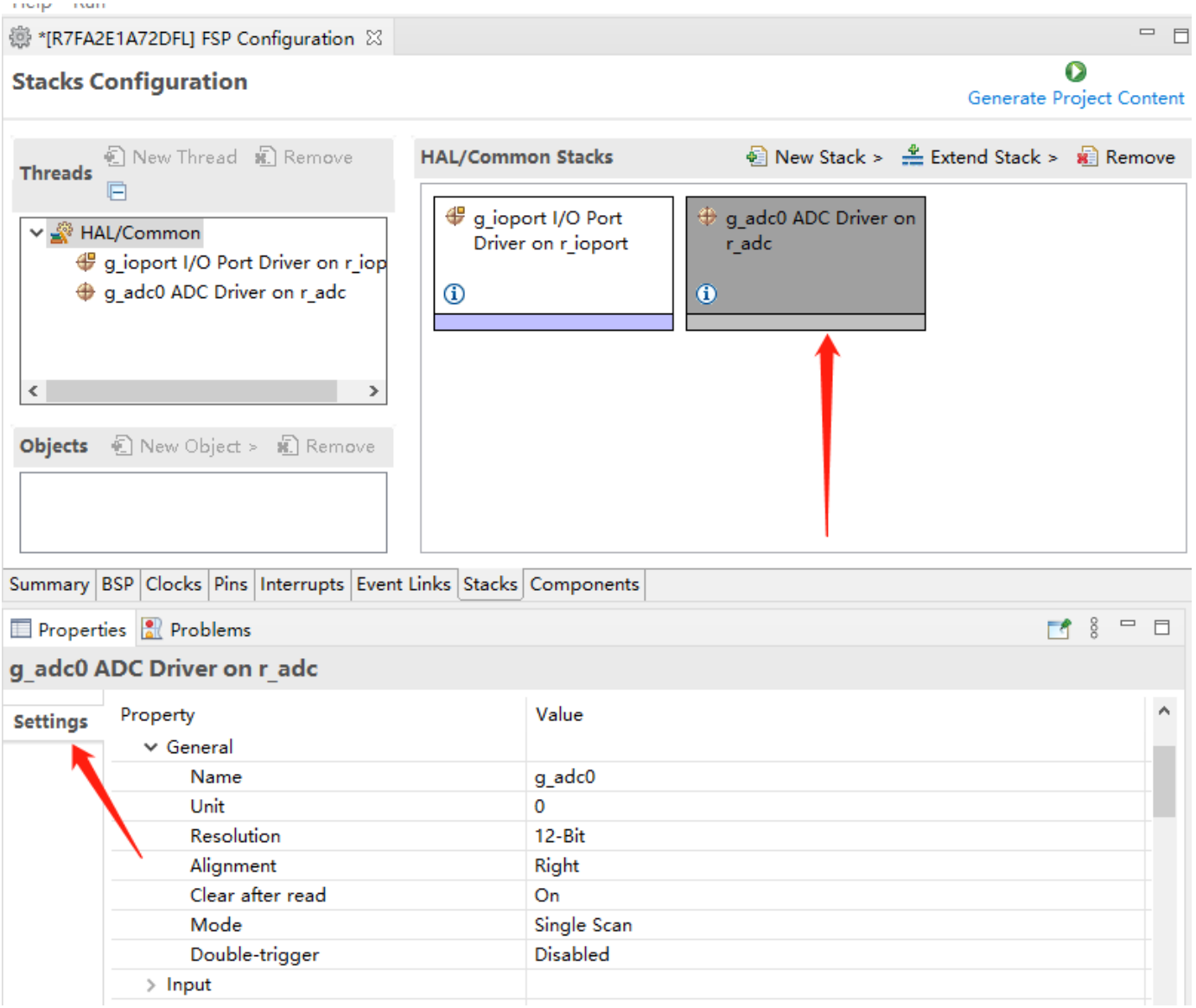
具体如何添加驱动，请参考Flexible Software Package (FSP) User Manual 第2.2.6.1以及2.2.6.2章节。

具体每个属性如何配置，请参考Flexible Software Package (FSP) User Manual 第4.2章节。

下图是添加ADC的过程：



添加ad模块之后点中该模块。可在下方属性中配置具体参数



4.48 Components 允许包含或排除应用程序所需的各个模块。

(链接：https://pan.baidu.com/s/1I38O1_oX4cPG5hpMqfnrxQ
提取码：sfra)

Keil下载失败总结

1.DDSC smart configurator生成完成MDK代码后，MDK打开后其start地址为0x00000000,当我们添加完programming algorithm，由于其初始地址是错误会导致烧录失败。

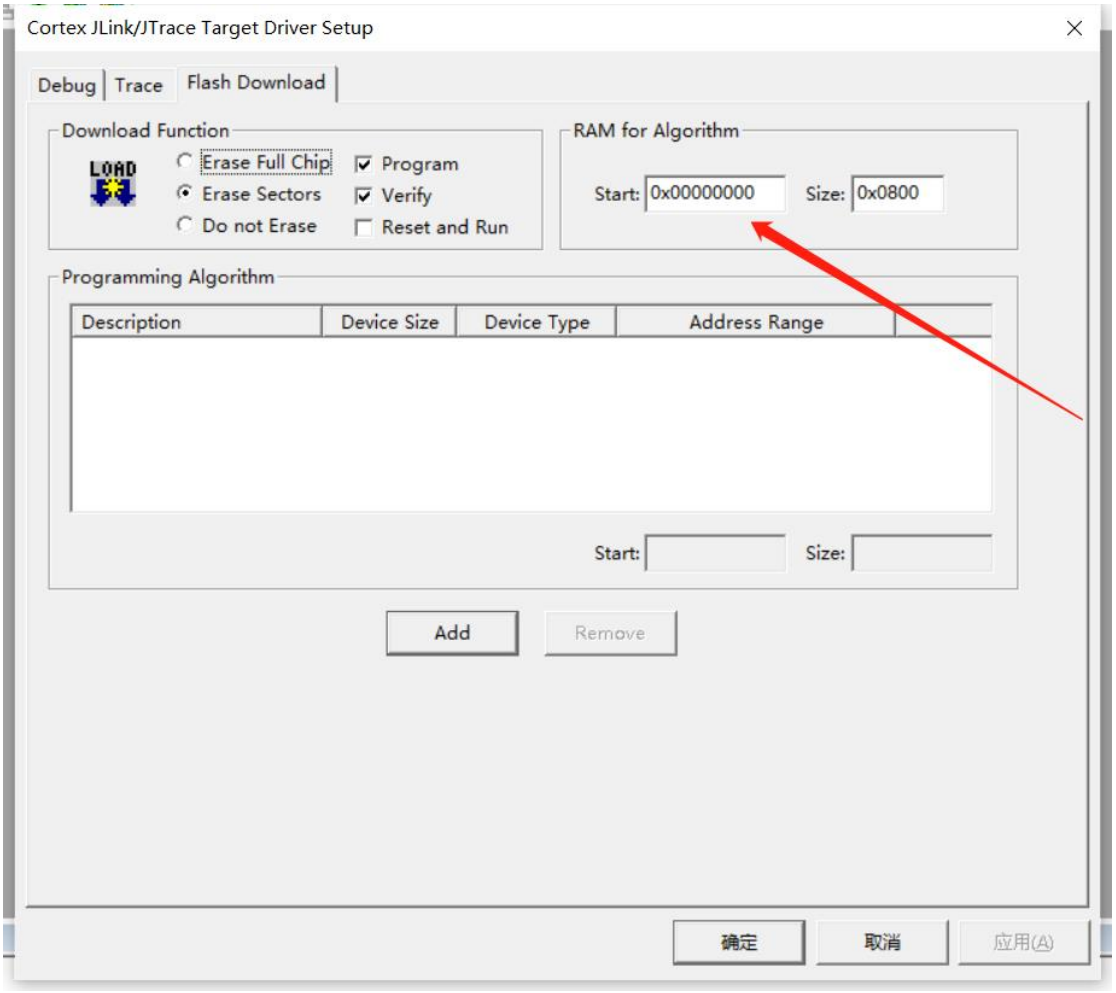


图1 默认状态

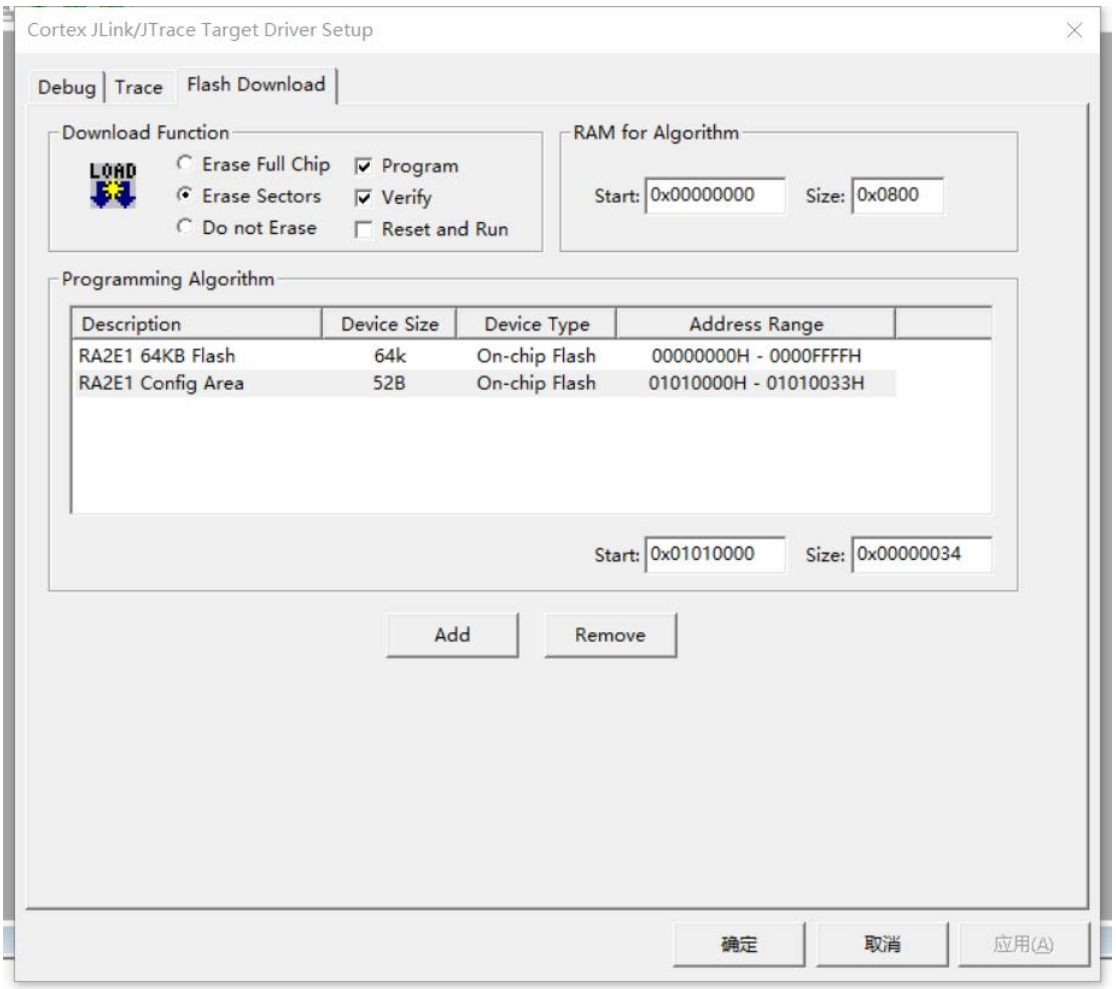


图2 添加完programming algorithm状态

2.失败报错窗口如下

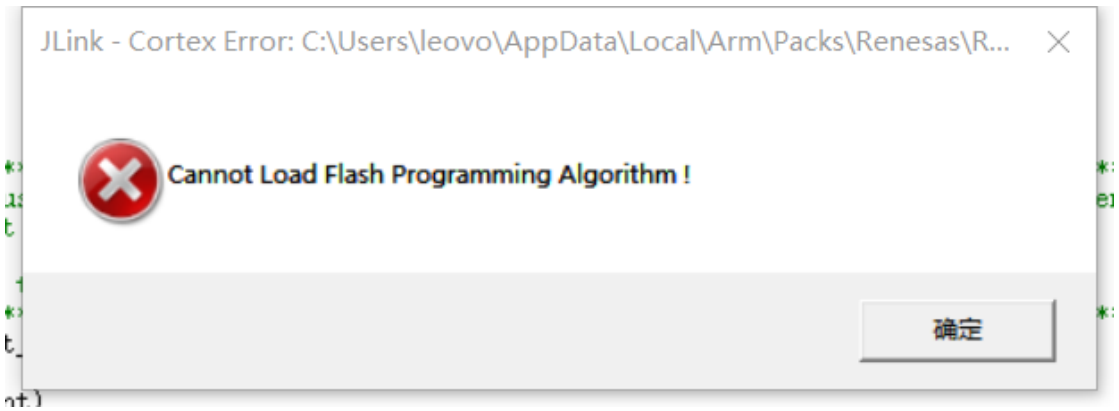


图3 报错1

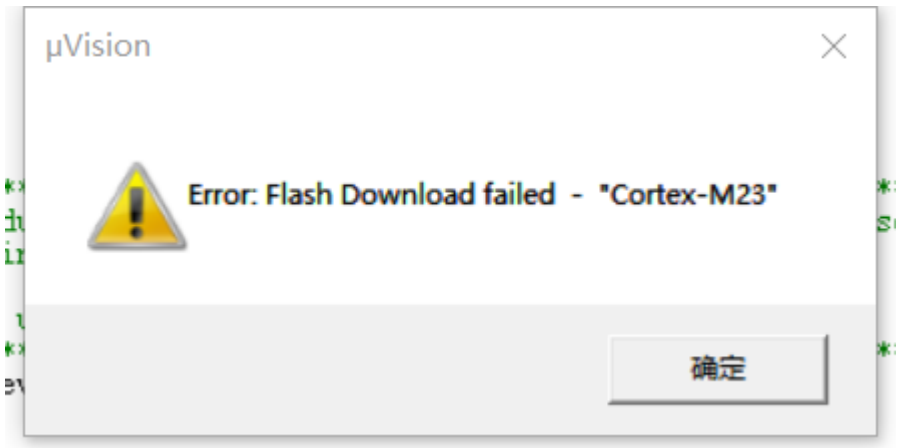


图4 报错2

```
* JLink Info: Reset: Reset device via AIRCR.SYSRESETREQ.

Target info:
------------
Device: R7FA2E1A7
VTarget = 3.227V
State of Pins:
TCK: 0, TDI: 0, TDO: 0, TMS: 1, TRES: 1, TRST: 0
Hardware-Breakpoints: 4
Software-Breakpoints: 8192
Watchpoints:          2
JTAG speed: 500 kHz

Insufficient RAM for Flash Algorithms !
Erase Failed!
Error: Flash Download failed  -  "Cortex-M23"
Flash Load finished at 16:28:37
```

图5 MDK信息栏报错

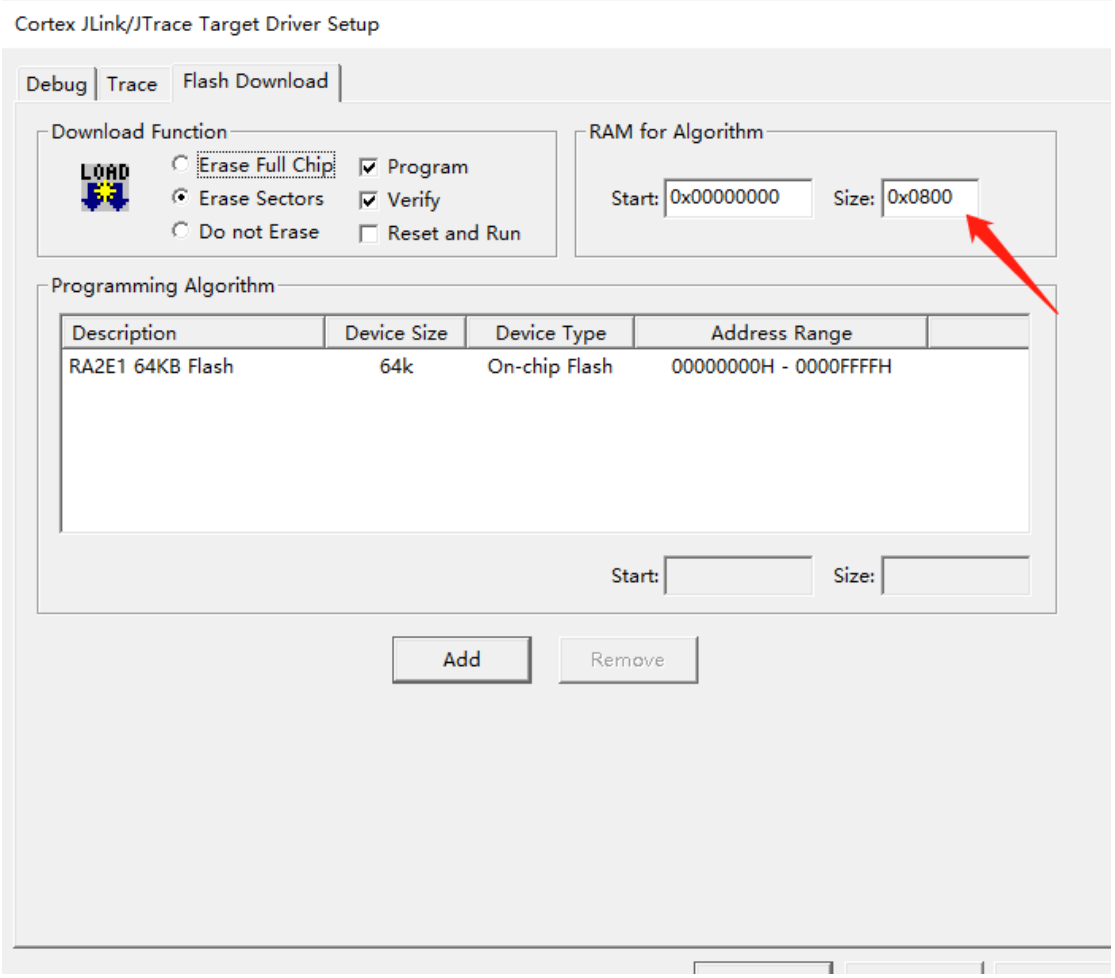


图6 SIZE

3.此时若参考网上的说法"图中箭头所指的地方就是存储烧写算法的RAM空间的大小，这个地方分配过小就会引起上述的错误信息。

将其size改的大一些就可以解决这个问题。"，将size原始0x0800更改为0X1000时，然后下载则会出现如下报错，在第二个报错页面按一下复位时，然后MDK就读不到设备信息了，e2 studio和Renesas Flash Programmer都烧录不进去了

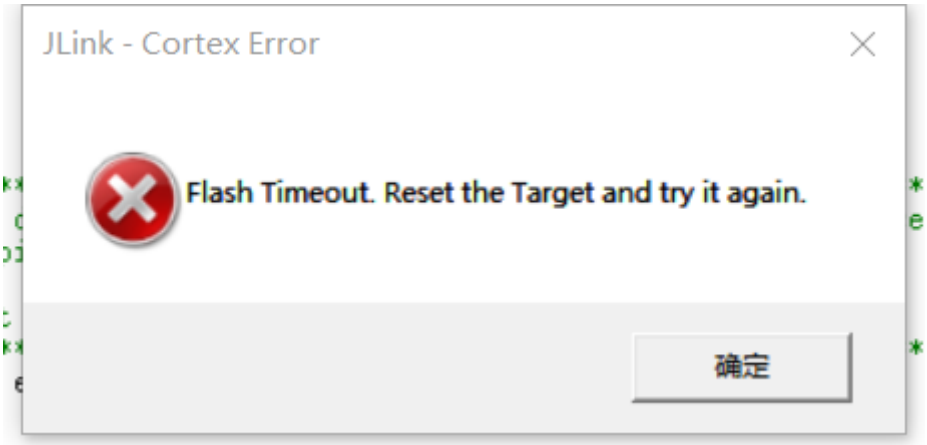


图7 报错1

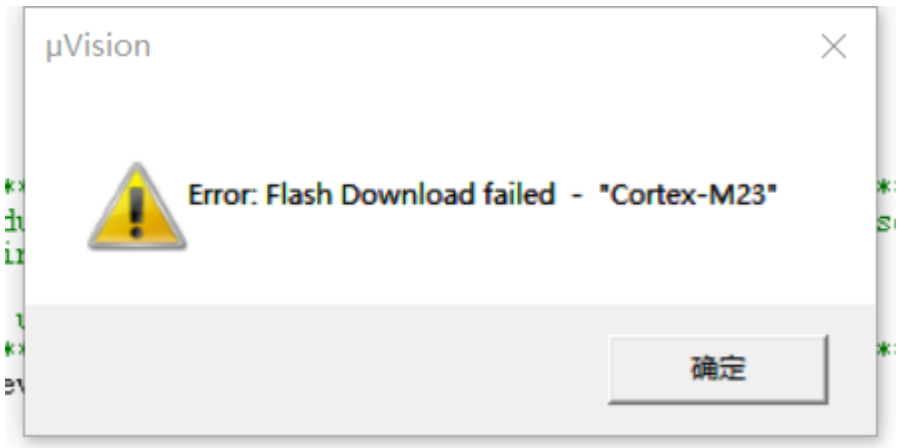


图8 报错2

4.解决方案：

打开JLINK,将供电3.3V改为5V就能读到设备信息，先擦除一下，然后烧录一下，就可换回3.3V供电

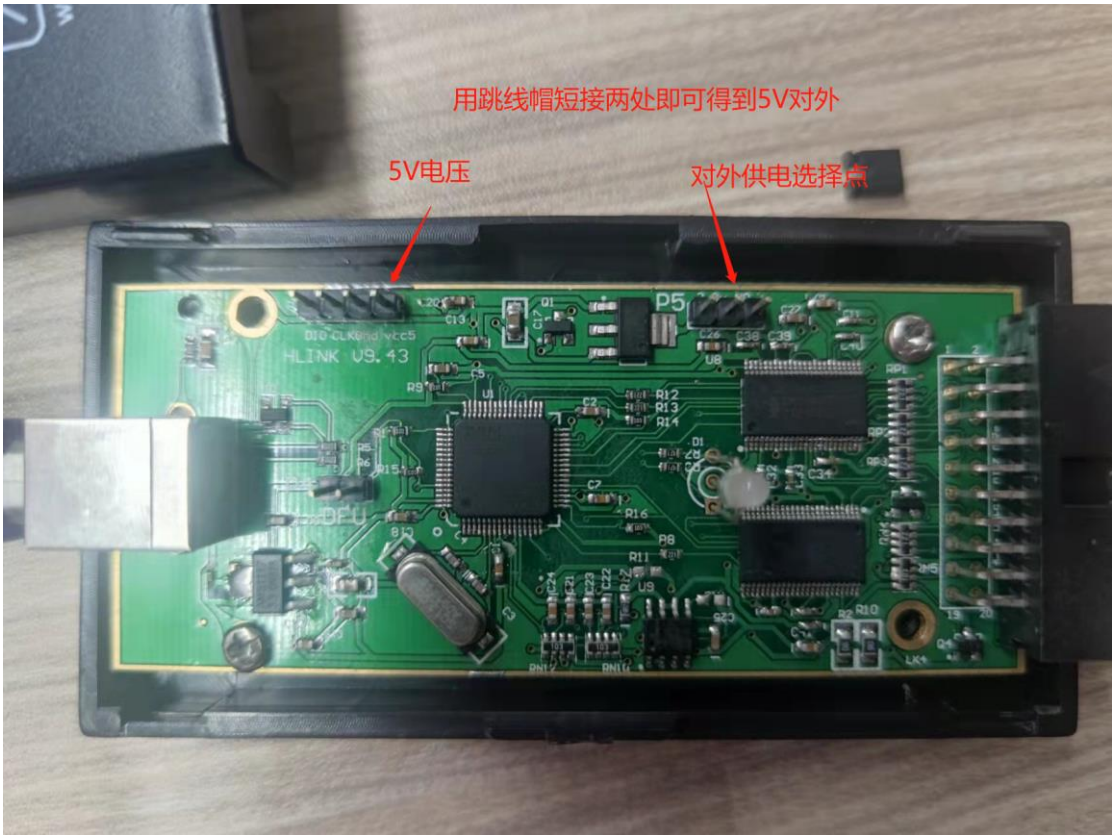


图9 jlink电源选择（不同版本jlink内部电气不同，连接仅供参考）

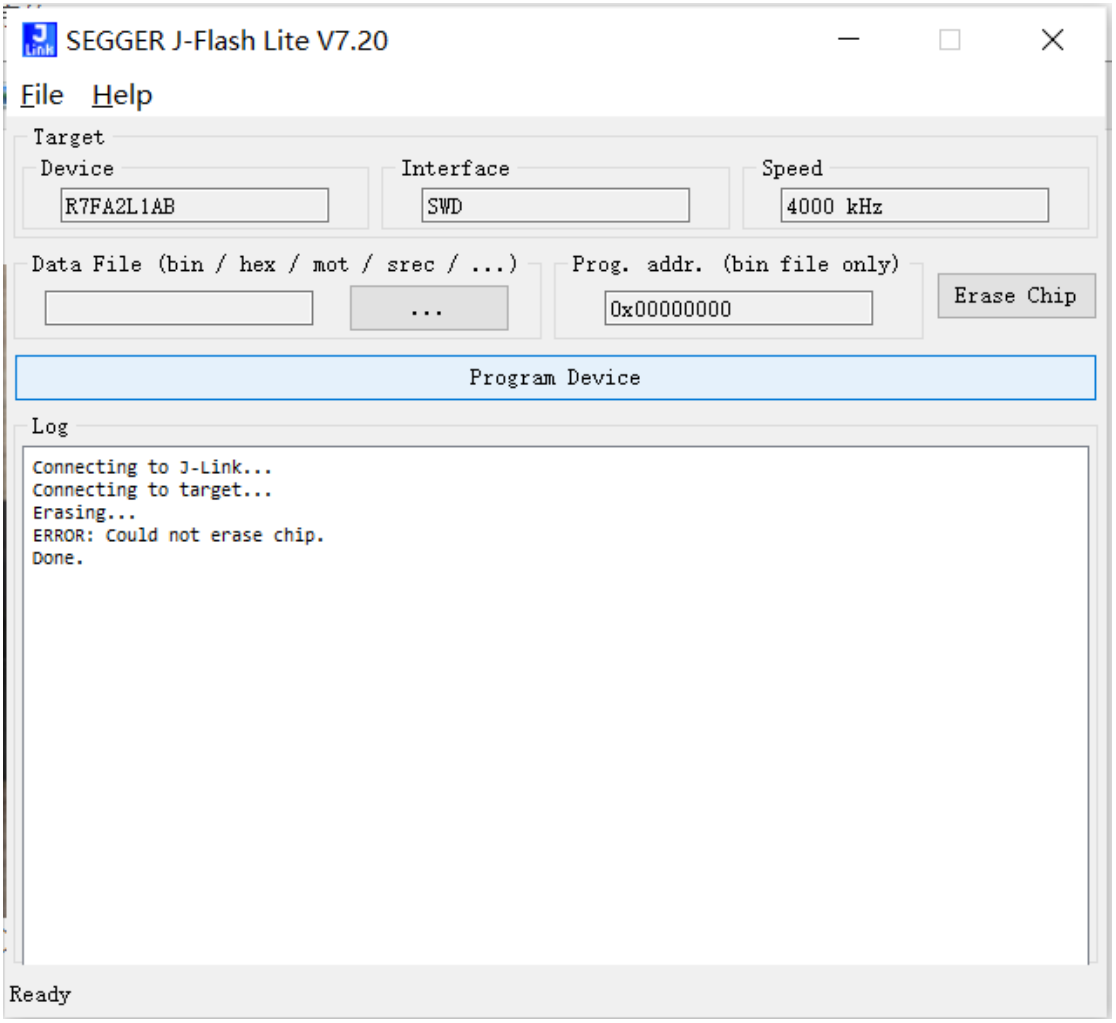
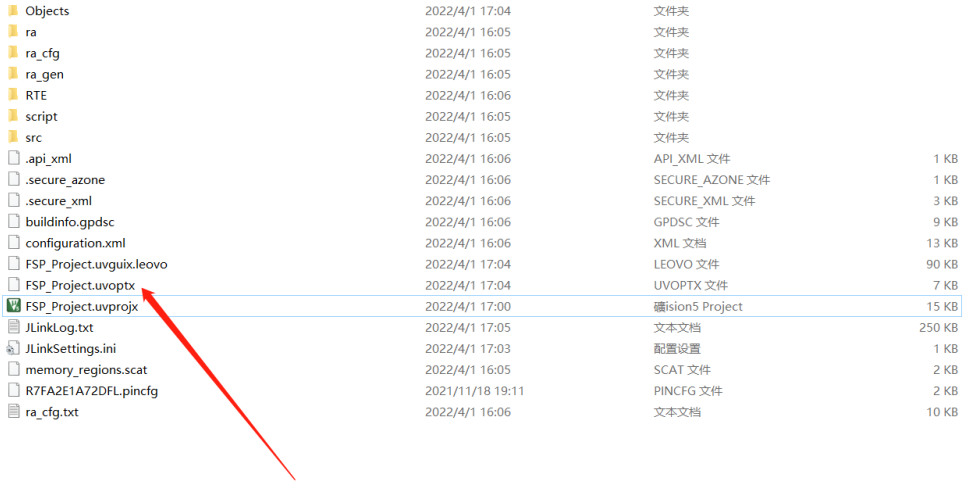
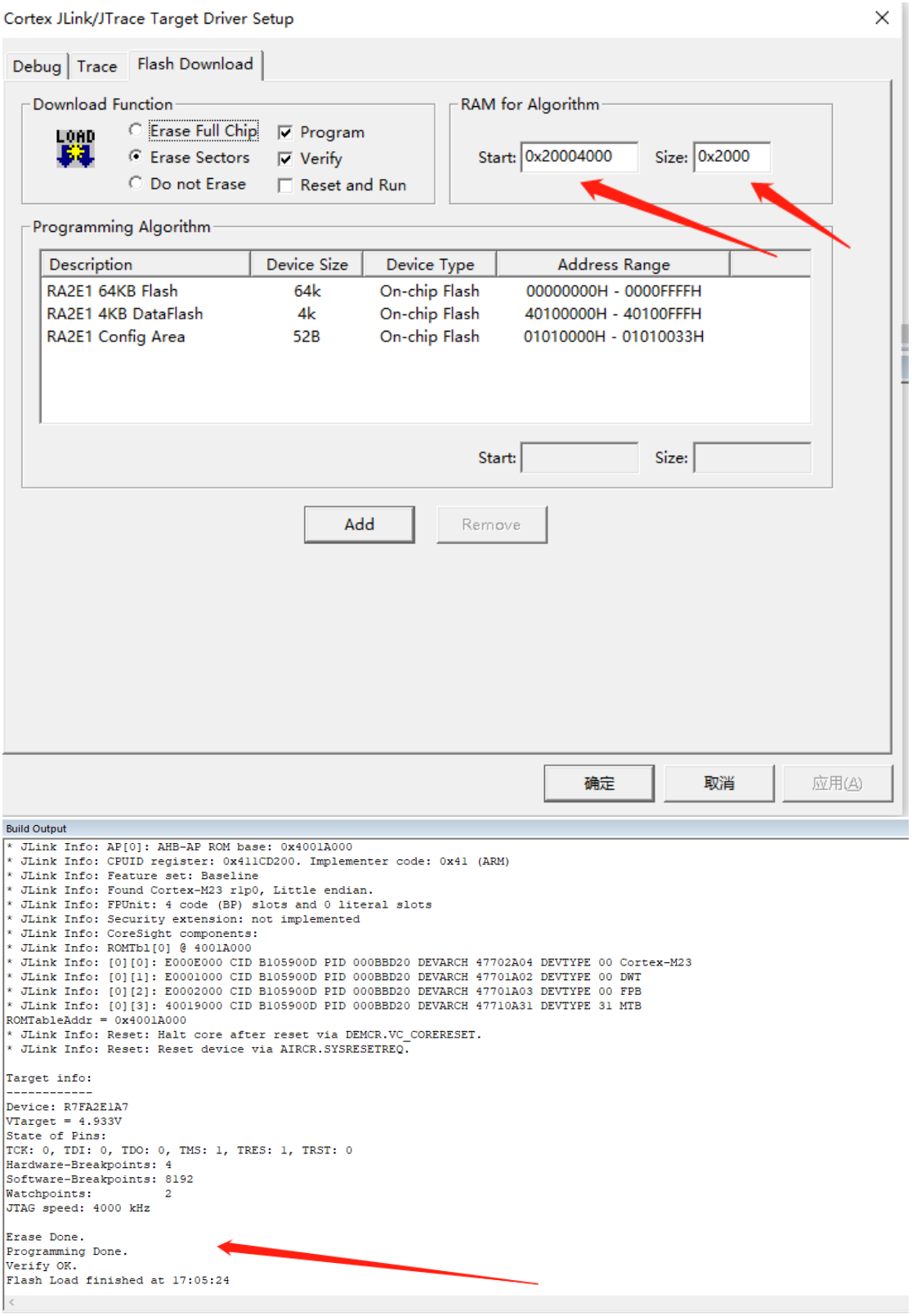


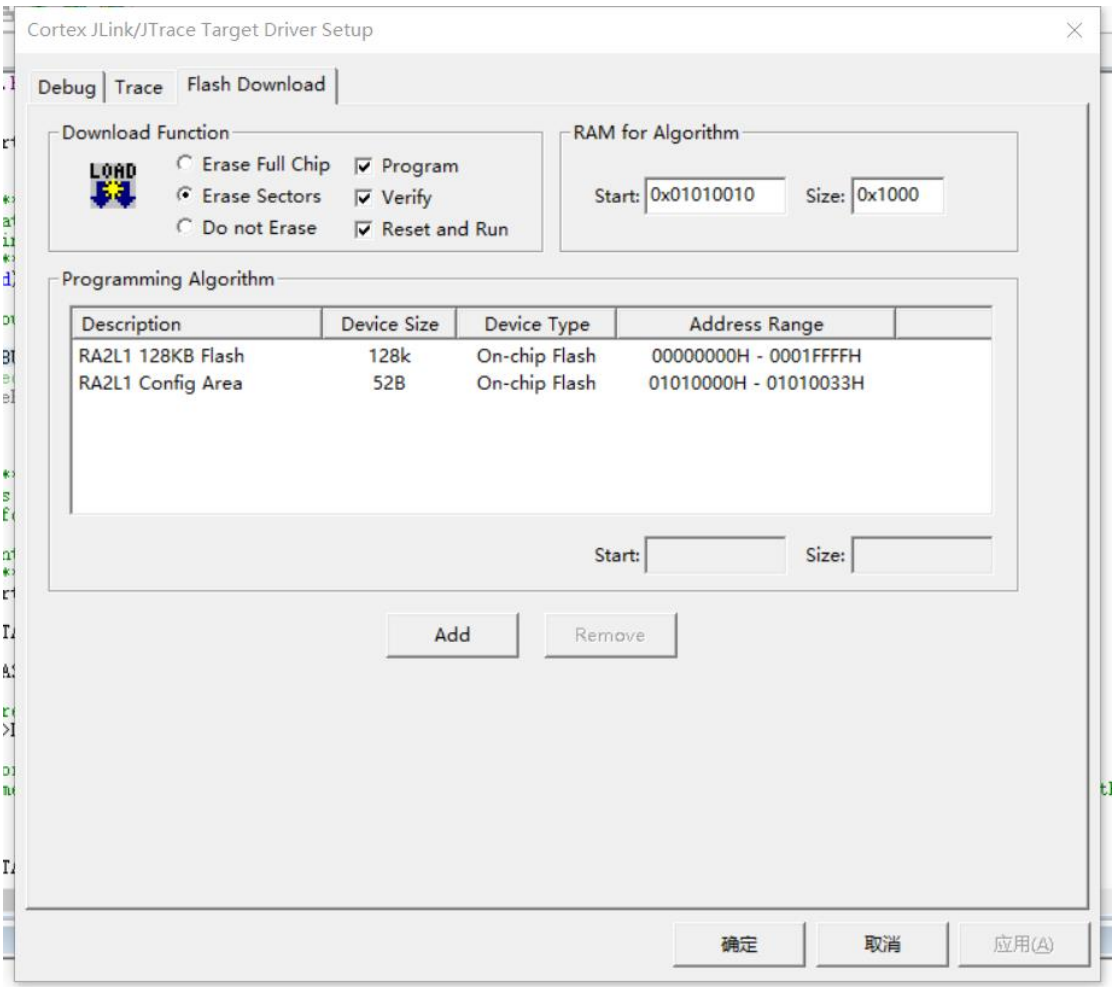
图10 jlink工具擦除成功

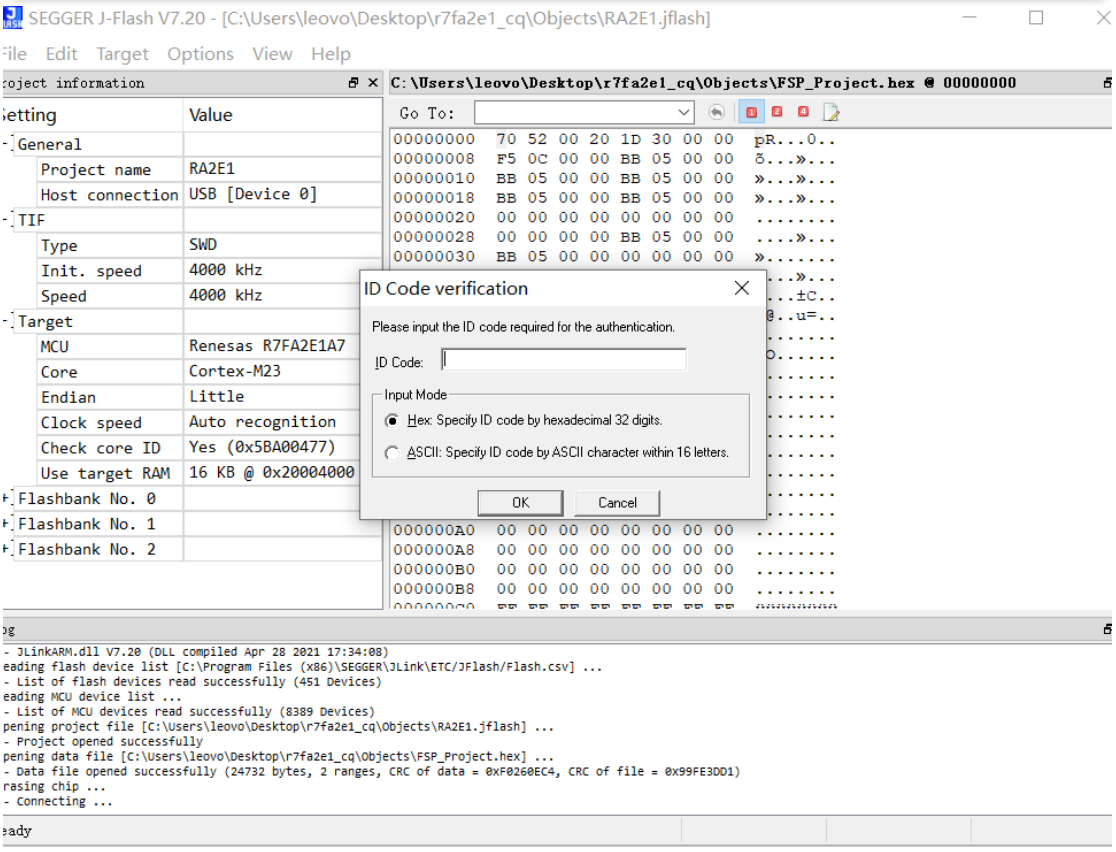
5.推出工程并将MDK工程中的.uvoptx文件删除，并重新打开配置jlink,就可得到正确的芯片烧录地址、大小选项，如下图，芯片即可正常烧录仿真了。





6.同样的操作方式若将strat改为0x01010010 (这个地址即是On-chip flash (option-setting memory))size 0x1000，同上述操作，在报错二处按下复位键，则一直提示要输入ID CODE,目前没有方法解决。


Cortex JLink/JTrace Target Driver Setup
Debug
Trace
Flash Download
Download Function
LOAD
Erase Full Chip
Erase Sectors
Do not Erase
Program
Verify
Reset and Run
RAM for Algorithm
Start: 0x01010010
Size: 0x1000
Programming Algorithm
Description
Device Size
Device Type
Address Range
RA2L1 128KB Flash
128k
On-chip Flash
00000000H - 0001FFFFH
RA2L1 Config Area
52B
On-chip Flash
01010000H - 01010033H
Start:
Size:
Add
Remove
确定
取消
应用(A)


SEGGER J-Flash V7.20 - [C:\Users\leovo\Desktop\r7fa2e1_cq\Objects\RA2E1.jflash]
File Edit Target Options View Help
Project information
Setting
Value
General
Project name
RA2E1
Host connection
USB [Device 0]
TIF
Type
SWD
Init. speed
4000 kHz
Speed
4000 kHz
Target
MCU
Renesas R7FA2E1A7
Core
Cortex-M23
Endian
Little
Clock speed
Auto recognition
Check core ID
Yes (0x5BA00477)
Use target RAM
16 KB @ 0x20004000
Flashbank No. 0
Flashbank No. 1
Flashbank No. 2
C:\Users\leovo\Desktop\r7fa2e1_cq\Objects\FSP_Project.hex @ 00000000
Go To:
00000000 70 52 00 20 1D 30 00 00
00000008 F5 0C 00 00 BB 05 00 00
00000010 BB 05 00 00 BB 05 00 00
00000018 BB 05 00 00 BB 05 00 00
00000020 00 00 00 00 00 00 00 00
00000028 00 00 00 00 BB 05 00 00
00000030 BB 05 00 00 00 00 00 00
000000A0 00 00 00 00 00 00 00 00
000000A8 00 00 00 00 00 00 00 00
000000B0 00 00 00 00 00 00 00 00
000000B8 00 00 00 00 00 00 00 00
ID Code verification
Please input the ID code required for the authentication.
ID Code:
Input Mode
Hex: Specify ID code by hexadecimal 32 digits.
ASCII: Specify ID code by ASCII character within 16 letters.
OK
Cancel
- JLinkARM.dll V7.20 (DLL compiled Apr 28 2021 17:34:08)
eading flash device list [C:\Program Files (x86)\SEGGER\JLink\ETC/JFlash/Flash.csv] ...
- List of flash devices read successfully (451 Devices)
eading MCU device list ...
- List of MCU devices read successfully (8389 Devices)
pening project file [C:\Users\leovo\Desktop\r7fa2e1_cq\Objects\RA2E1.jflash] ...
- Project opened successfully
pening data file [C:\Users\leovo\Desktop\r7fa2e1_cq\Objects\FSP_Project.hex] ...
- Data file opened successfully (24732 bytes, 2 ranges, CRC of data = 0xF0260EC4, CRC of file = 0x99FE3DD1)
rasing chip ...
- Connecting ...
eady