

## 75NF75-VB TO220 Datasheet

### N-Channel 80 V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$	80	V
$R_{DS(on)}$ $V_{GS} = 10$ V	7	$m\Omega$
$R_{DS(on)}$ $V_{GS} = 4.5$ V	9	$m\Omega$
$I_D$	100	A
Configuration	Single	

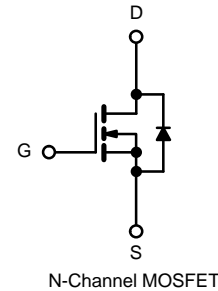
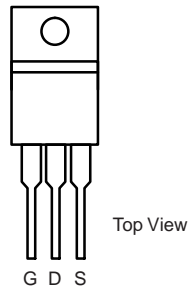
**FEATURES**

- TrenchFET® Power MOSFET
- 100 %  $R_g$  and UIS Tested


**RoHS**  
 COMPLIANT
**APPLICATIONS**

- Primary Side Switching
- Synchronous Rectification
- DC/AC Inverters
- LED Backlighting

TO-220AB



ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	80	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$I_D$	$T_C = 25$ °C	100 <sup>a</sup>
		$T_C = 70$ °C	85 <sup>a</sup>
		$T_A = 25$ °C	28.6 <sup>b, c</sup>
		$T_A = 70$ °C	24.9 <sup>b, c</sup>
Pulsed Drain Current ( $t = 100$ $\mu$ s)	$I_{DM}$	350	A
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25$ °C	
		$T_A = 25$ °C	4.5 <sup>b, c</sup>
Single Pulse Avalanche Current	$I_{AS}$	30	mJ
Single Pulse Avalanche Energy	$E_{AS}$	45	
Maximum Power Dissipation	$P_D$	$T_C = 25$ °C	180
		$T_C = 70$ °C	120
		$T_A = 25$ °C	5 <sup>b, c</sup>
		$T_A = 70$ °C	3.2 <sup>b, c</sup>
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to 150	°C
Soldering Recommendations (Peak Temperature)		260	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{thJA}$	15	18	°C/W
	Steady State		40	50	
Maximum Junction-to-Case		$R_{thJC}$	0.85	1.1	

**Notes**

- Package limited.
- Surface mounted on 1" x 1" FR4 board.
- $t = 10$  s.

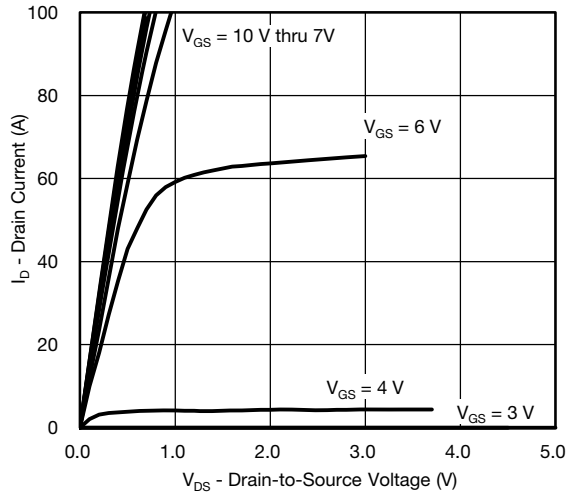
<b>SPECIFICATIONS</b> ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	80			V	
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		37		mV/°C	
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6.1			
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0		3.5	V	
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$	
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10		
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	85			A	
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		7		m $\Omega$	
		$V_{GS} = 6\text{ V}, I_D = 15\text{ A}$		7.5			
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		9			
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$		60		S	
<b>Dynamic<sup>b</sup></b>							
Input Capacitance	$C_{iss}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3855		pF	
Output Capacitance	$C_{oss}$			1120			
Reverse Transfer Capacitance	$C_{rss}$			376			
Total Gate Charge	$Q_g$	$V_{DS} = 40\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		35.5		nC	
		$V_{DS} = 40\text{ V}, V_{GS} = 6\text{ V}, I_D = 10\text{ A}$		22			
		$V_{DS} = 40\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		18			
Gate-Source Charge	$Q_{gs}$		5.3				
Gate-Drain Charge	$Q_{gd}$		7.3				
Output Charge	$Q_{oss}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$		57	86		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$	0.5	1.3	2	$\Omega$	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		12	24	ns	
Rise Time	$t_r$			8	16		
Turn-Off Delay Time	$t_{d(off)}$			32	64		
Fall Time	$t_f$			7	14		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 40\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 6.0\text{ V}, R_g = 1\text{ }\Omega$		14	28		
Rise Time	$t_r$			11	22		
Turn-Off Delay Time	$t_{d(off)}$			30	60		
Fall Time	$t_f$			8	16		
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$			75		A
Pulse Diode Forward Current ( $t = 100\text{ }\mu\text{s}$ )	$I_{SM}$				150		
Body Diode Voltage	$V_{SD}$	$I_S = 5\text{ A}$		0.76	1.1	V	
Body Diode Reverse Recovery Time	$t_{rr}$	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		38	75	ns	
Body Diode Reverse Recovery Charge	$Q_{rr}$			36	70	nC	
Reverse Recovery Fall Time	$t_a$			19		ns	
Reverse Recovery Rise Time	$t_b$			19			

**Notes**

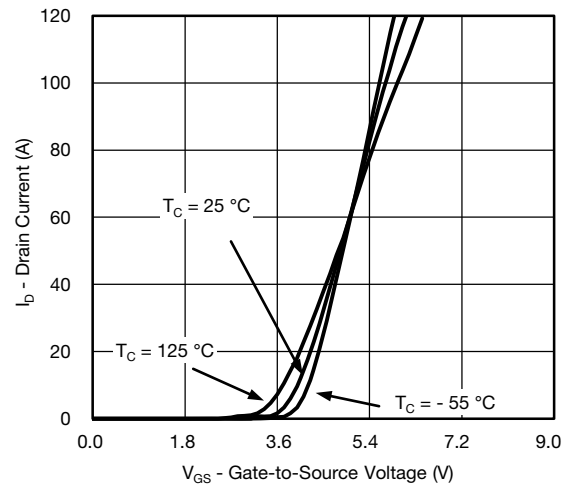
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
 b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

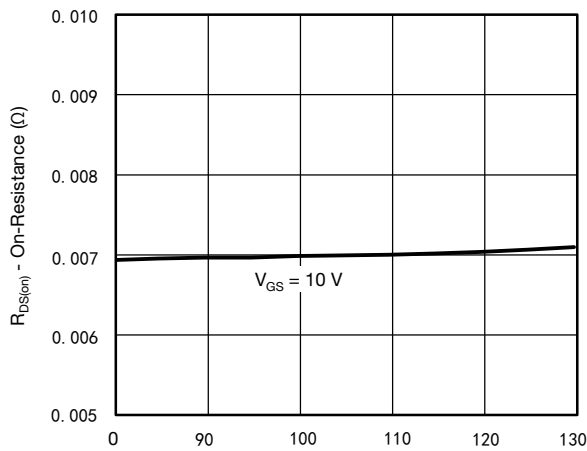
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



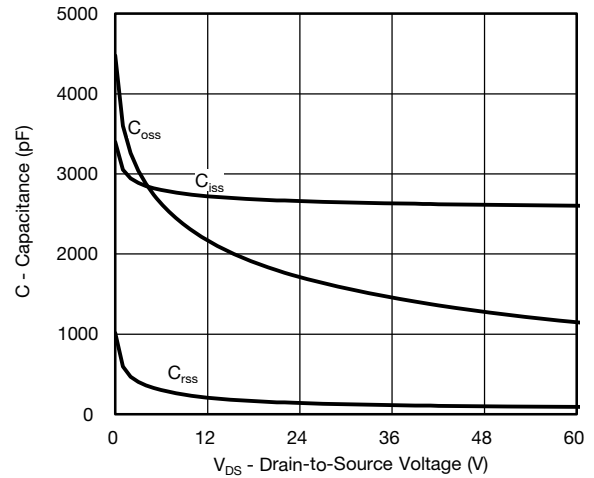
**Output Characteristics**



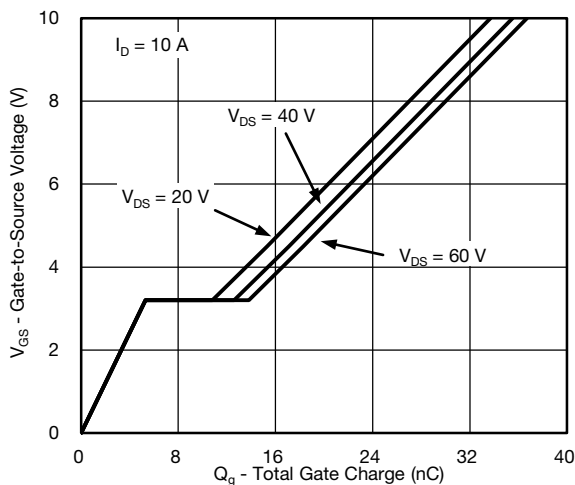
**Transfer Characteristics**



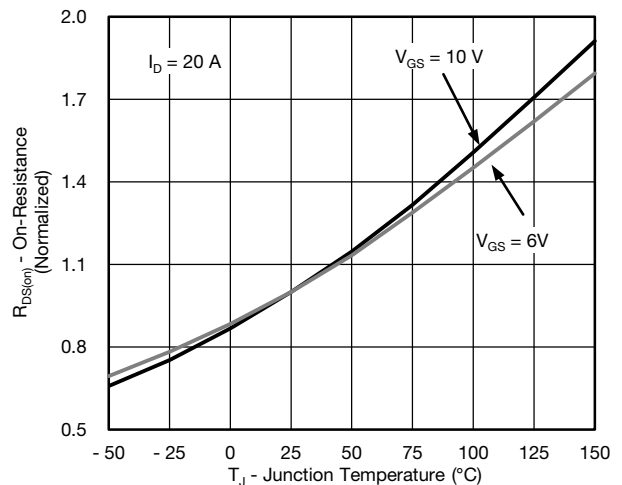
**On-Resistance vs. Drain Current**



**Capacitance**

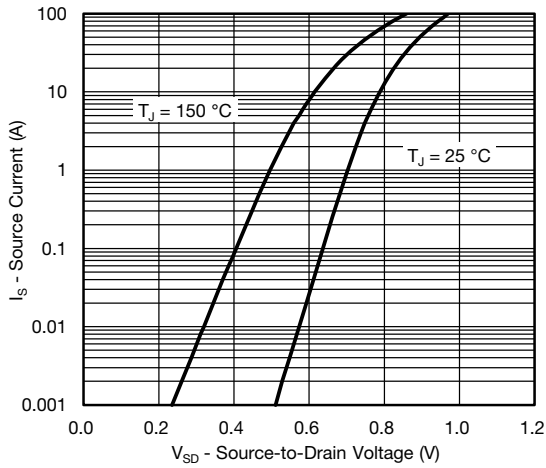


**Gate Charge**

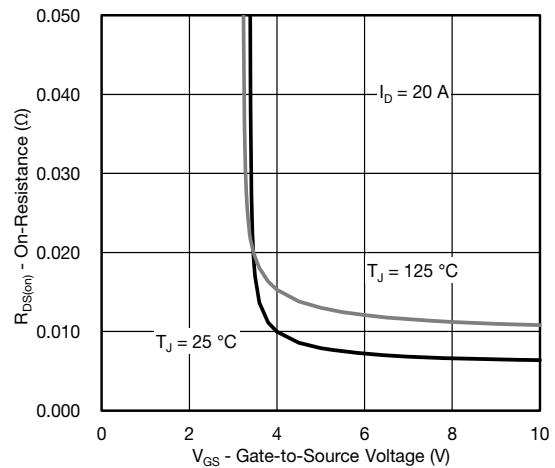


**On-Resistance vs. Junction Temperature**

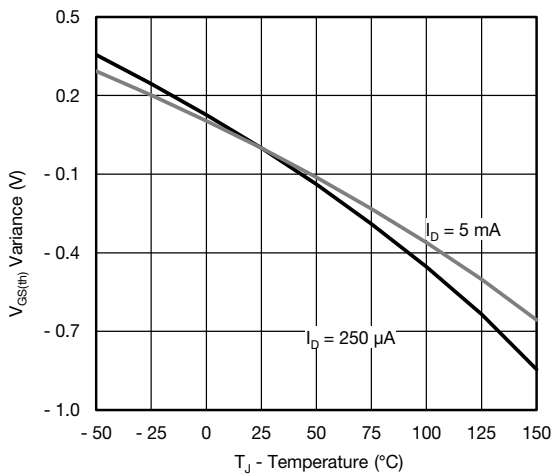
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



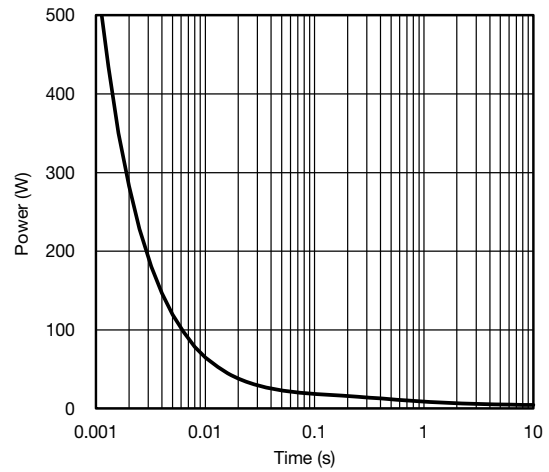
**Source-Drain Diode Forward Voltage**



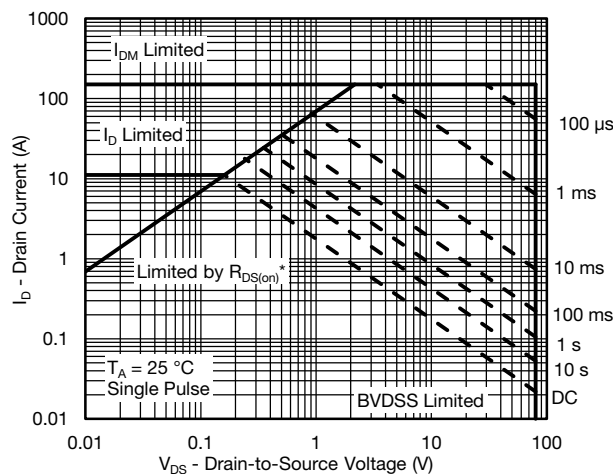
**On-Resistance vs. Gate-to-Source Voltage**



**Threshold Voltage**



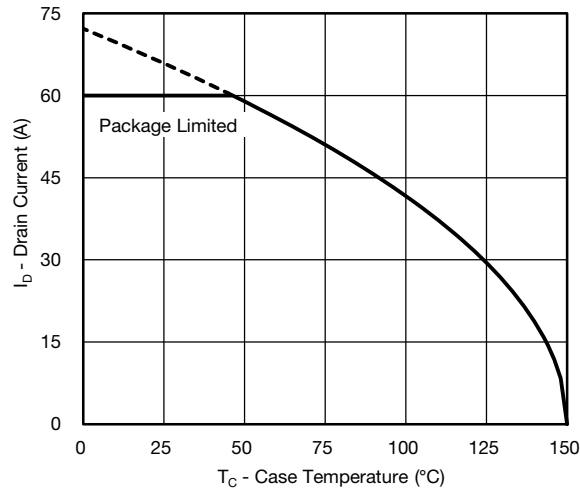
**Single Pulse Power, Junction-to-Ambient**



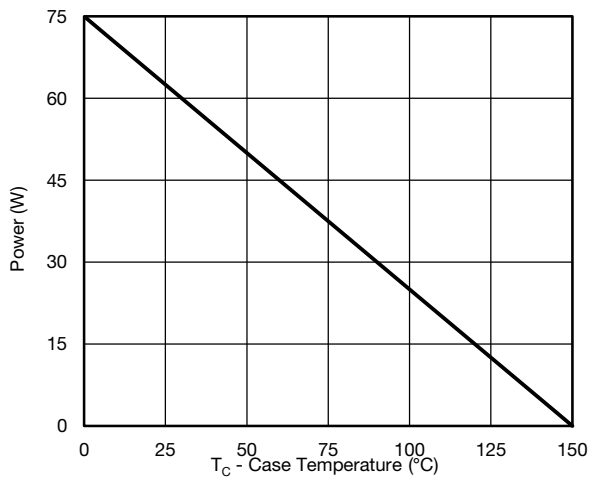
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

**Safe Operating Area, Junction-to-Ambient**

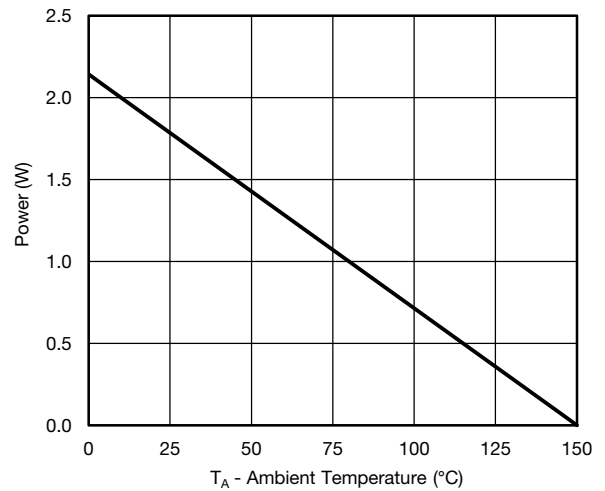
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating\***



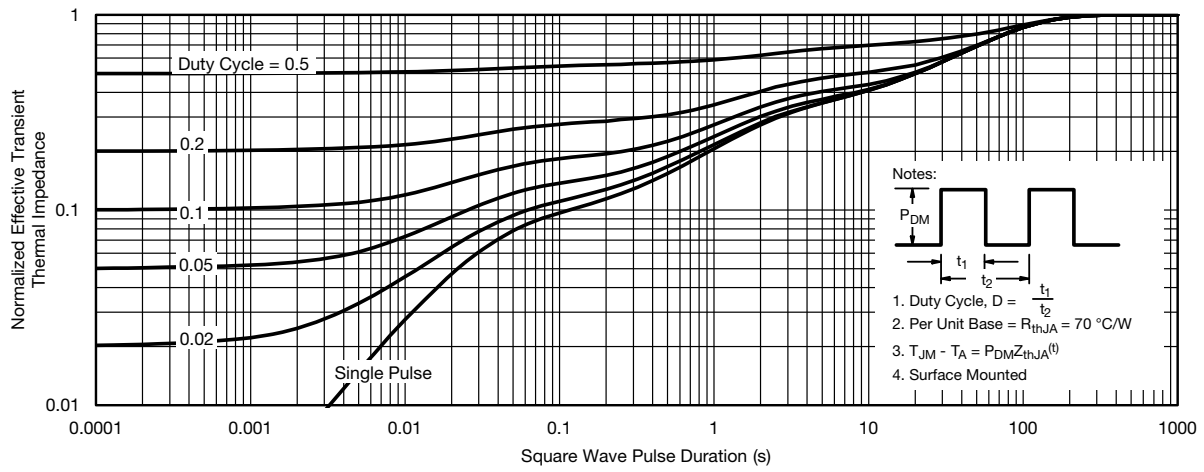
**Power, Junction-to-Case**



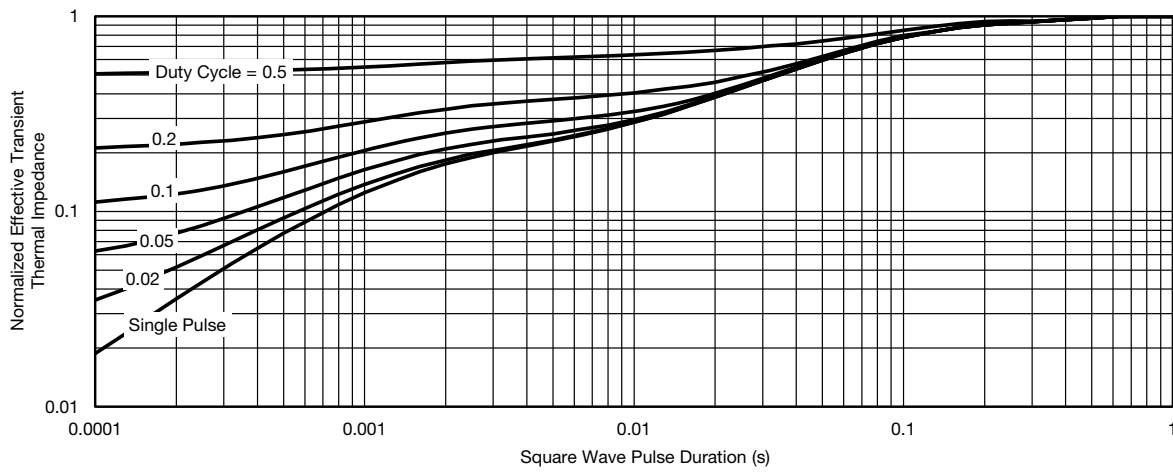
**Power, Junction-to-Ambient**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

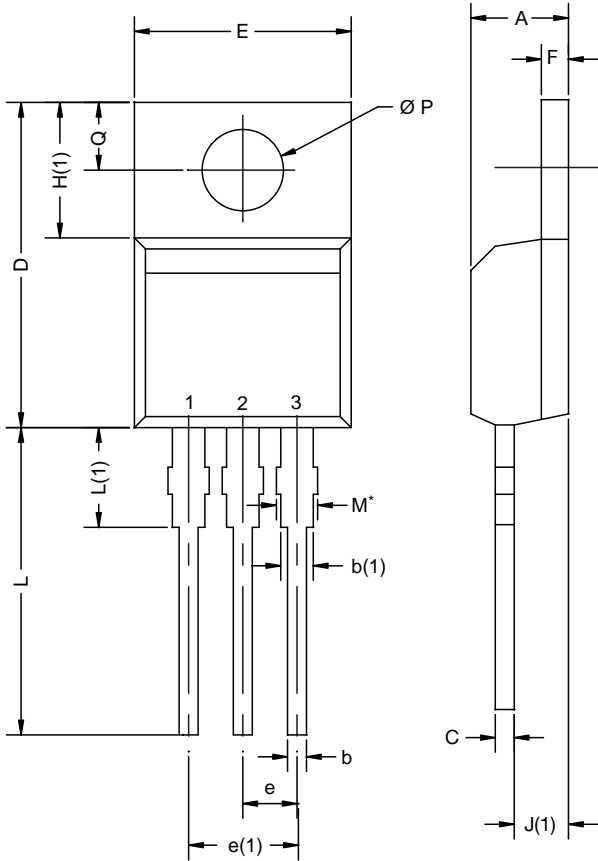


**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

TO-220AB



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
c	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
E	10.04	10.51	0.395	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
Ø P	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118

ECN: X12-0208-Rev. N, 08-Oct-12  
DWG: 5471

Notes

\* M = 1.32 mm to 1.62 mm (dimension including protrusion)  
Heatsink hole for HVM

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