NMOS Motor Full-Bridge Gate Driver

FEATURES

- Wide 5V to 40V Input Voltage Range
- Single Channel H-bridge Gate Driver
  - Drives Four External N-channel MOSFETs
  - Supports 100% Pulse Width Modulation (PWM) Duty Cycle
- OCP Threshold Voltage (V_{DS}) Adjustable：0.12V, 0.24V, 0.48V, 0.96V, Disable
- Peak Source/Sink Current：250mA/500mA
- Supports 1.8V,3.3V and 5V Logical Inputs
- Low-Power Sleep Mode
- Protection Features
  - VM Under-voltage Lockout (UVLO)
  - Charge Pump Undervoltage Lockout (CPUV)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
- Thermally Enhanced Surface Mount Package
  - QFN3x3-16

APPLICATIONS

- DC Brush Motors
- Automotive Actuators
- Automotive brushed DC motors
- Power seat modules
- Door module
- Body control modules
- Power sunroof

GENERAL DESCRIPTION

The TMI8723 is a gate driver IC designed for H- bridge driver applications. It is capable of driving H-bridge consisting of four N- channel power MOSFETs up to 40V.

The TMI8723 integrates a regulated charge pump to generate gate drive power,Peak Sink and Source current can be 500mA and 250mA. At the same time, TMI8723 can set the value of the overcurrent point through the pin VDS.

Internal protection features include programmable short-circuit protection, over-current protection, undervoltage lockout, and thermal shutdown.

The TMI8723 is available in a QFN-16 (3mmx3mm) package with an exposed thermal pad.

TYPICAL APPILCATION

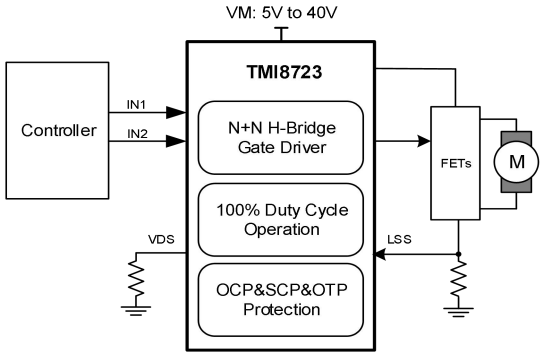


Figure 1. Basic Application Circuit

ABSOLUTE MAXIMUM RATINGS (Note 1)

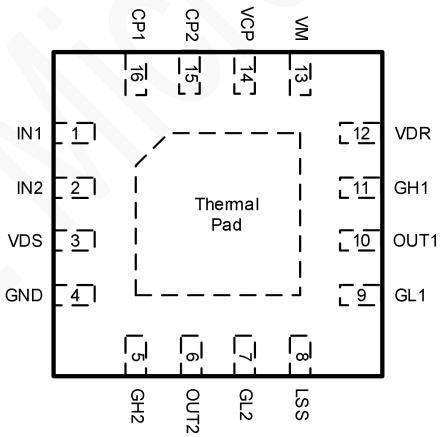
Parameter	Min	Max	Unit
Power supply voltage (VM)	-0.3	45	V
Logic input voltage(IN1, IN2, VDS)	-0.3	6	V
Output pin voltage (OUT1, OUT2)	-0.3	VM + 0.3	V
High-side gate pin voltage (GH1, GH2)	-0.3	VM + 12	V
Low-side gate pin voltage (GL1, GL2)	-0.3	12	V
Current sense input pin voltage (LSS)	-0.3	12	V
Operating ambient temperature, T_a	-40	125	°C
Operating junction temperature, $T_{J\ (Note\ 2)}$	-40	150	°C
Storage temperature	-40	150	°C

ESD RATING

Items	Description	Value	Unit
V_{ESD}	Human body model	±2000	V
	Charged device model (CDM)	±750	V

JEDEC specification JS-001

PACKAGE/ORDER INFORMATION



QFN3x3-16

TMI8723/XXXXX (TMI8723: Device Code, XXXXX: Inside Code) for TMI8723

Part Number	Package	Top mark	Quantity/ Reel
TMI8723	QFN3x3-16	TMI8723 XXXXX	3,000

The TMI8723 device is Pb-free and RoHS compliant.

PIN FUNCTIONS

PIN#	Name	Function
1	IN1	Logic inputs. Controls the output. Internal pulldown.
2	IN2	Logic inputs. Controls the output. Internal pulldown.
3	VDS	VDS monitor setting pin. The resistor value or voltage forced on this pin sets the VDS monitor threshold. For more information see the Table 1.
4	GND	Ground.
5	GH2	High-side gate, connect to the high-side FET gate.
6	OUT2	Connect to high-side FET source and low-side FET drain.
7	GL2	Low-side gate, connect to the low-side FET gate.
8	LSS	Low-side source .
9	GL1	Low-side gate, connect to the low-side FET gate.
10	OUT1	Connect to high-side FET source and low-side FET drain.
11	GH1	High-side gate, connect to the high-side FET gate.
12	VDR	High-side FET drain connection. This pin is common for the two H-bridges.
13	VM	Power supply input. Connect a 0.1μF bypass capacitor to ground, as well as a 10μF(minimum) bulk capacitance for VM.
14	VCP	Charge-pump output. Connect a 1μF ceramic capacitor between this pin and the VM pin.
15	CP2	Charge-pump switching node. Connect a 0.1μF X7R capacitor rated for the supply voltage (VM) between the CP2 and CP1 pins.
16	CP1	
-	GND	Thermal pad. Connect to device power ground.

RECOMMENDED OPERATING CONDITIONS

Items	Description	Min	Max	Unit
VM	Power supply voltage range	5	40	V
V_{IN_X}	Logic input voltage range	-0.3	5	V
f_{IN_X}	Logic input frequency	0	50	kHz
LSS	Low-side Source Connection.	-1	1	V

ELECTRICAL CHARACTERISTICS T_A = 25°C, (unless otherwise noted.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power section (VM)						
Power supply voltage	VM		5		40	V
Quiescent current	I_{VMQ}	VM=13.5V, IN1=IN2=0V, no load			20	μA
	I_{VM}	VM=13.5V, IN1=IN2=5V or IN1=5V & IN2=0V or IN1=0V & IN2=5V, no load	1	1.5	2	mA
	I_{VMPWM}	VM=13.5V, IN1=5V, IN2=50kHz, no load	1	1.8	3	mA
CONTROL LOGIC						
Input logic low threshold	V_{IL}				0.7	V
Input logic high threshold	V_{IH}		1.5		5.5	V
Input logic high current	I_{IH}	VM=13.5V, V_{INx} = 5V		50	70	μA
Input logic low current	I_{IL}	VM=13.5V, V_{INx} = 0V			1	μA
RDS Pulldown resistance	R_{PD}			166		kΩ
RDS Pullup resistance	R_{PU}			93		kΩ
Propagation delay	t_{PD}	IN1, IN2 to GHx or GLx		300		ns
FET GATE DRIVERS (GH1, GH2, GL1, GL2, OUT1, OUT2)						
High-side VGS gate drive (gate-to-source)	V_{GSH}	VM>13.5V(VM=36V)		10.5	11.7	V
		VM=8V	6.2		7.3	V
		VM=5.5V	3.9		4.9	V
Low-side VGS gate drive (gate-to-source)	V_{GSL}	VM>13.5V(VM=36V)		10.5		V
		VM<13.5V		VM		V
High-side Gate Drive current	I_{GHX}	Peak Sink current		500		mA
		Peak Source current		250		mA
Low-side Gate Drive current	I_{GLX}	Peak Sink current		500		mA
		Peak Source current		250		mA
FET gate holdoff resistor	R_{OFF}	Pulldown GHx to OUT		200		kΩ
		Pulldown GLx to GND		200		kΩ
Output dead time	t_{DEAD}			240		ns
Output rise time	t_{RISE}	VM=13.5V, OUTx rising 10% to 90%		150		ns
Output fall time	t_{FALL}	VM=13.5V, OUTx falling 90% to 10%		150		ns
PROTECTION CIRCUITS						
VM undervoltage lockout	V_{UVLO_RISE}	VM rising	4.5	4.7	4.8	V
	V_{UVLO_FALL}	VM falling	4.2	4.4	4.5	V
VCP undervoltage lockout	$V_{CP\_UV\_RISE}$	VCP rising		4.1		V
	$V_{CP\_UV\_FALL}$	VCP falling		3.7		V

ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C, (unless otherwise noted.)

Overcurrent protection trip level, VDS of each external FET High side FETs: VDR – OUTx Low side FETs: OUTx – LSS	V_{DS1}	R(VDS)=2k		0.12		V
	V_{DS2}	R(VDS)=30K		0.24		V
	V_{DS3}	R(VDS)=100K		0.48		V
	V_{DS4}	R(VDS)=FLOATING		0.96		V
	V_{DS5}	VDS>4.5V		Disable		V
V_{Lss} protection trip level	V_{LSS}	V_{Lss} protection trip level	0.8	1	1.2	V
OCP deglitch time	t_{OCP}			4		μs
Overcurrent retry time	t_{RETRY}			2.5		ms
nSLEEP wake-up time	t_{SLEEP}			1		ms
Thermal shutdown	$T_{SD(Note 3)}$			150		°C
Thermal shutdown hysteresis	$T_{HYS (Note 3)}$			25		°C

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\,(MAX)} = (T_{J(MAX)}-T_A)/\theta_{JA}$.

Note 3: Thermal shutdown threshold and hysteresis are guaranteed by design.

OPERATION

Overview

The TMI8723 is single H-bridge drivers, also referred to as gate controllers. The drivers control four external NMOS FETs used to drive a bi-directional brushed-DC motors, with 0.25A source and 0.5A sink current capability. It operates over a wide input voltage range of 5V to 40V, generating a boosted gate drive voltage when the input supply is below 12V. The TMI8723 features a low-power sleep mode, which disables the device and draws a very low supply current.

Both the high-side and low-side FETs are driven with a gate source voltage (VGS) of 10.5 V (nominal) when the VM voltage is more than 13.5 V. At lower VM voltages, the VGS is reduced. The high-side gate drive voltage is generated using a doubler-architecture charge pump that regulates to the VM + 10.5 V.

TMI8723 device also has protection features beyond traditional discrete implementations including: undervoltage lockout (UVLO), overcurrent protection (OCP) and thermal shutdown (TSD).

Sleep Mode (nSLEEP Input)

The IN1 and IN2 pins put the IC into sleep mode and TMI8723 into sleep mode when IN1/IN2 continues to pull down for 1ms. When exiting sleep mode, the part will initiate the power-up sequence described above.

Control Modes

The TMI8723 output consists of four N-channel MOSFETs that are designed to drive high current. These outputs are controlled by the two logic inputs IN1 and IN2 as listed in Table 1.

Table 1: Input Logic Truth Table

IN1	IN2	GH1	GL1	OUT1	GH2	GL2	OUT2	DESCRIPTION
H	L	1	0	H	0	1	L	Forward (Current OUT1 → OUT2)
L	H	0	1	L	1	0	H	Reverse (Current OUT2 → OUT1)
L	L	X	X	Hi-Z	X	X	Hi-Z	Sleep mode H bridge disabled Hi-Z
H	H	0	1	L	0	1	L	Brake low-side slow decay

The inputs can be set to static voltages for 100% duty cycle drive, or they can be pulse-width modulated (PWM) for variable motor speed. When using PWM, switching between driving and braking typically works best. For example, to drive a motor forward with 50% of the maximum RPM, IN1 = 1 and IN2 = 0 during the driving period, and IN1 = 1 and IN2 = 1 during the other period. Alternatively, the coast mode (IN1 = 0, IN2 = 0) for fast current decay is also available. The input pins can be powered before VM is applied.

Overcurrent VDS Monitor

The gate-driver circuit monitors the VDS voltage of each external FET when it is driving current. When the voltage monitored is greater than the OCP threshold voltage (VDS(OCP)) after the OCP

deglitch time has expired, an OCP condition is detected. The TMI8723 device provides VDS(OCP) voltage levels by setting the VDS resistance.

The VDS voltage on the high-side FET is measured across the VDRAIN to OUTx pins. The low-side VDS monitor on half-bridge 1 measures the VDS voltage across the OUTx to LSS pins.

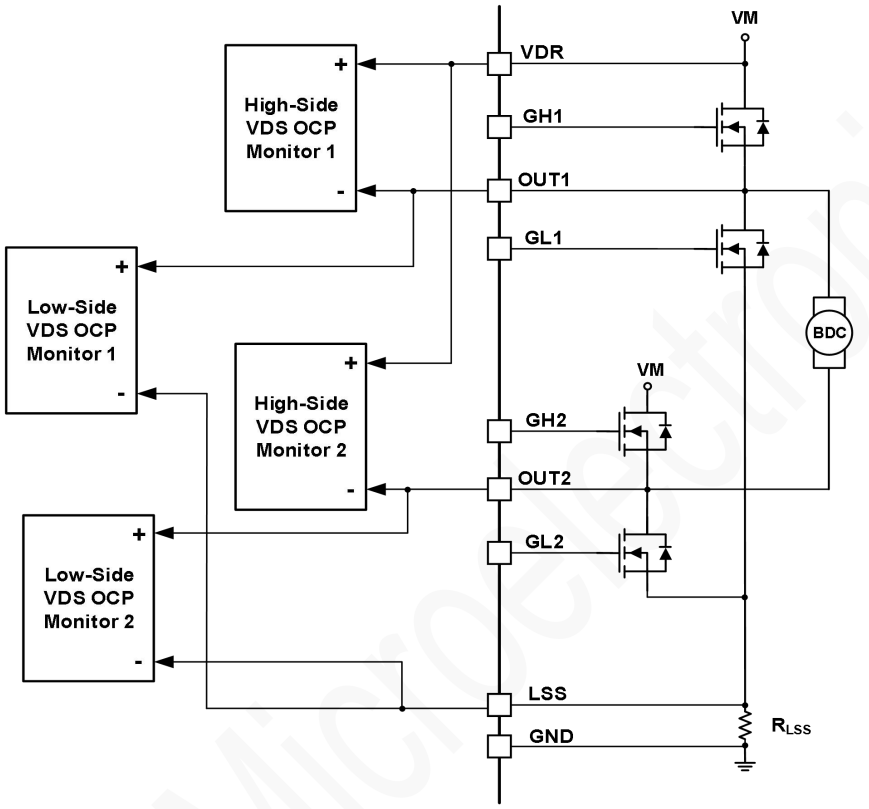


Figure 2. $V_{DS(OCP)}$ Block Diagram

The VDS pin on the TMI8723 device is used to select the VDS threshold voltage for overcurrent detection. For exemple: Tying the VDS pin 2kΩ to ground selects the lowest setting of 0.12V. For a detailed list of VDS configurations, see Table 2.

Table 2. VDS Pin Resistor Setting

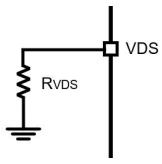
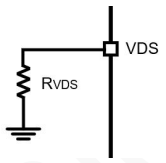
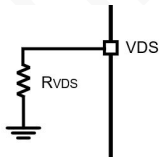
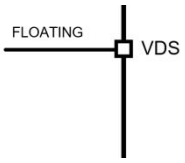
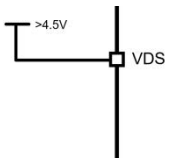
VDS RESISTANCE	VDS VOLTAGE	OVERCURRENT TRIP LEVEL (VDS(OCP))	CIRCUIT
R(VDS)=2kΩ to GND	0.5V	0.12V	

Table 2. VDS Pin Resistor Setting(Continued)

VDS RESISTANCE	VDS VOLTAGE	OVERCURRENT TRIP LEVEL (VDS(OCP))	CIRCUIT
R(VDS)=30kΩ to GND	1.2V	0.24V	
R(VDS)=100kΩ to GND	2.0V	0.48V	
R(VDS)=FLOATING	3.5V	0.96V	
VDS>4.5V	5V	Disable	

UVLO Protection

If at any time the voltage on the VM pin falls below the undervoltage-lockout threshold voltage, all FETs in the device will be disabled. Operation resumes when VM rises above the UVLO threshold.

Overcurrent Protection (OCP)

If the output current exceeds the OCP threshold, IOCP, for longer than t_{OCP}, all FETs in the device are disabled. After a duration of t_{RETRY}, the MOSFET is re-enabled according to the state of the INx pins. If the overcurrent fault is still present, the cycle repeats; otherwise normal device operation resumes.

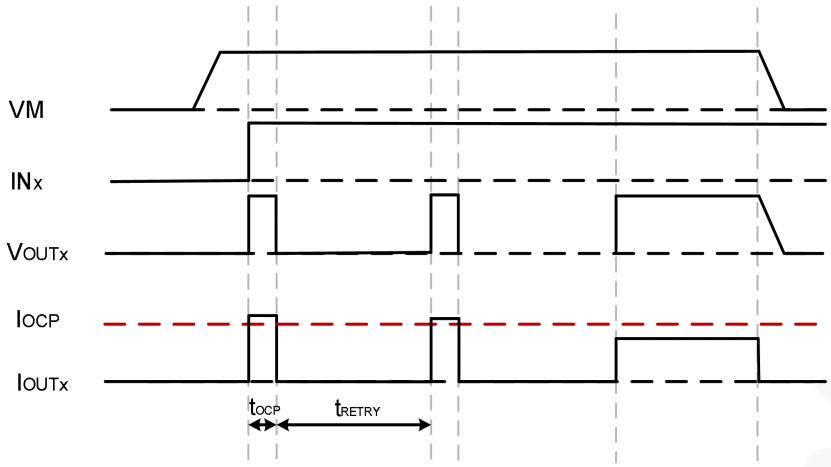


Figure 3. Over current protection Time Periods

LSS Protection

When the LSS pin voltage exceeds 1.0V, TMI8723 triggers LSS overcurrent protection; GHSx and LHx on the high and low sides enter the automatic restart phase, and the automatic restart time tretry is 2.5ms. When the LSS pin voltage is below 1.0V, GHSx and GLHx return to normal.

Thermal Shutdown

If the die temperature exceeds safe limits, all FETs in the the H-bridge are disabled. After the die temperature has fallen to a safe level, operation automatically resumes.

APPLICATION INFORMATION

Application information

The TMI8723 device is typically used to drive one brushed DC motor as below。

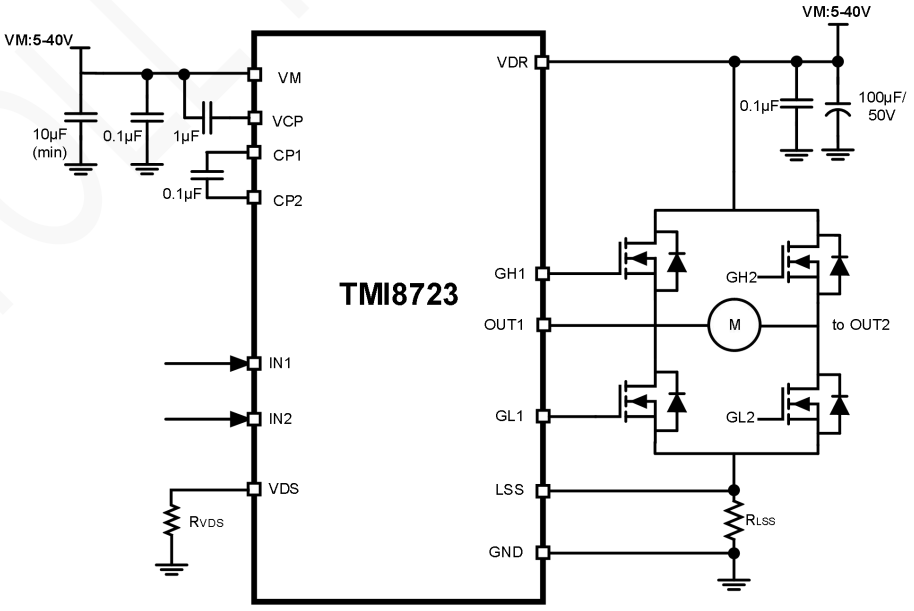


Figure 4.TMI8723 Typical Application

Block Diagram

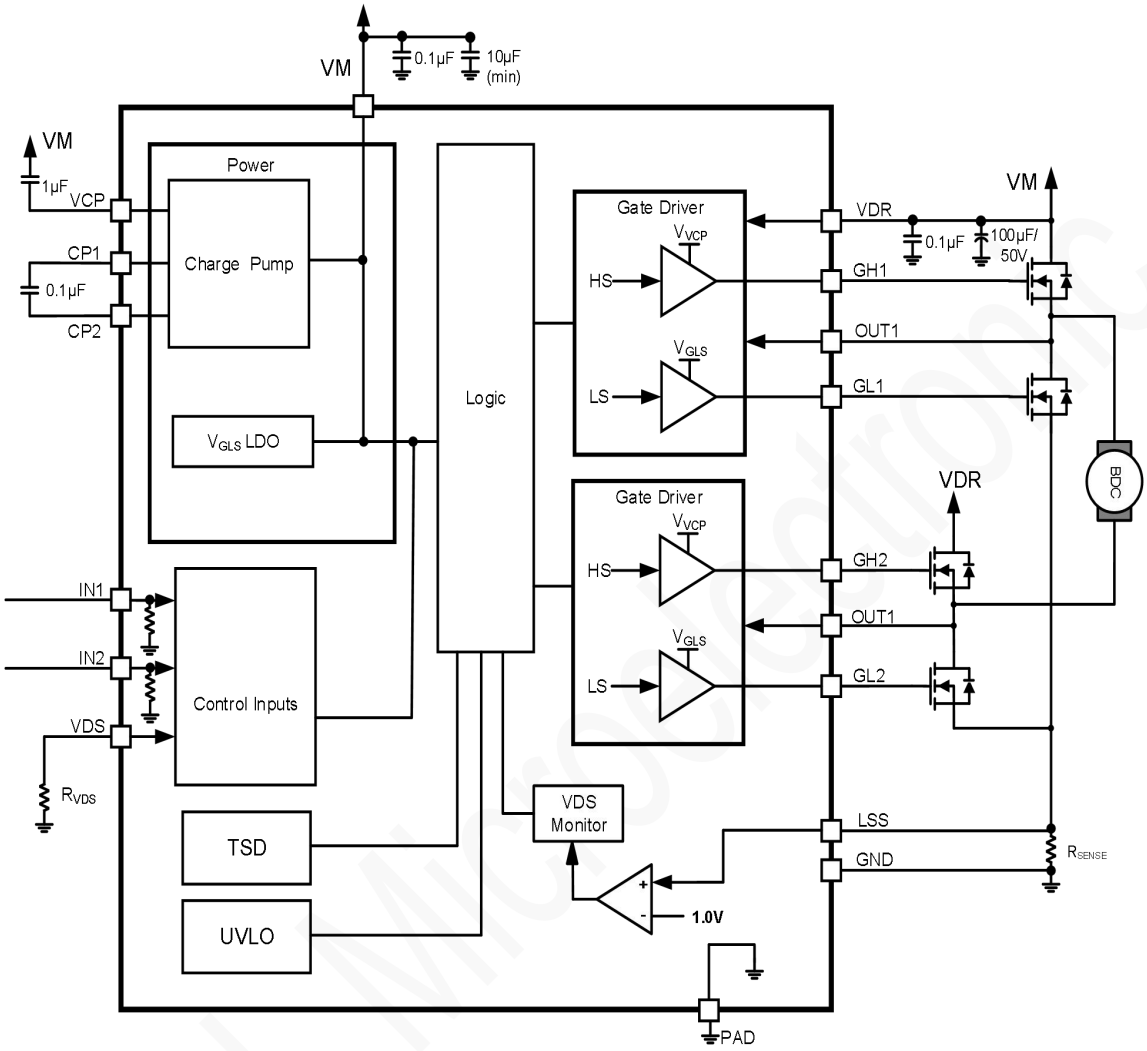
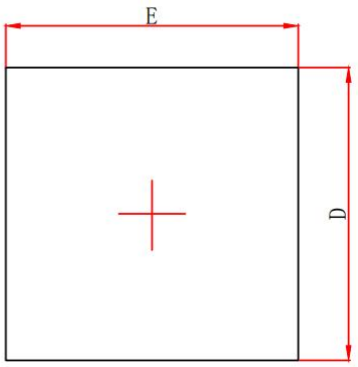


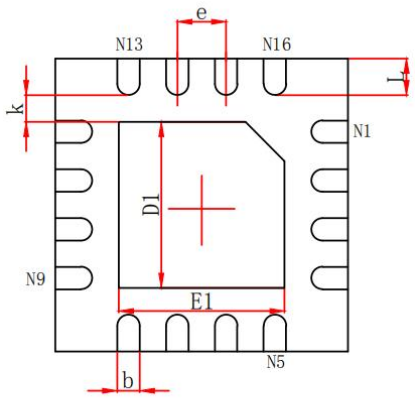
Figure 5. TMI8723 Block Diagram

PACKAGE INFORMATION

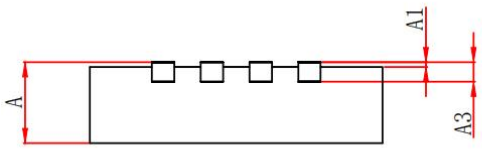
QFN3x3-16



Top View



Bottom View



Side View

Unit: mm

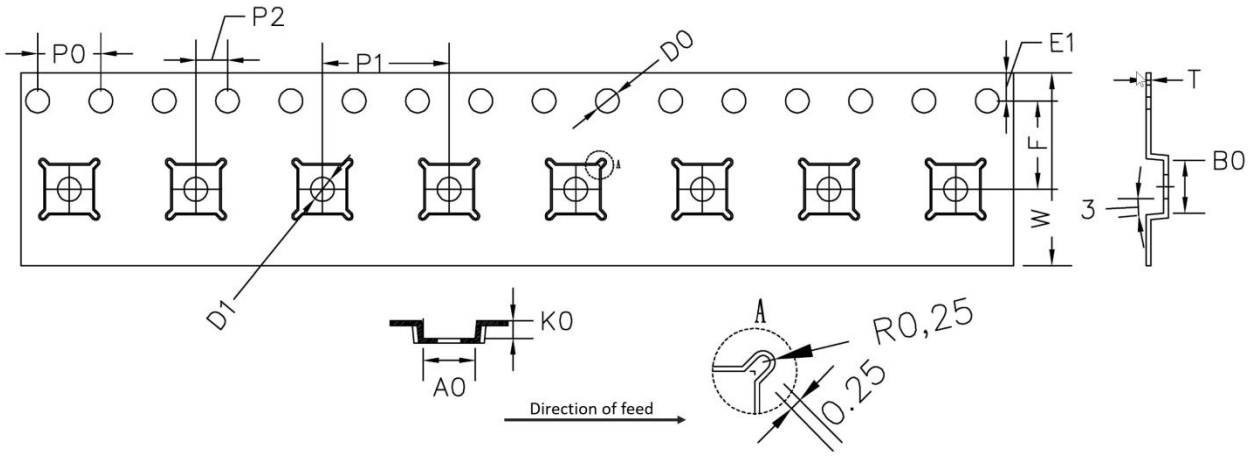
Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	0.70	0.80	E1	1.60	1.80
A1	-	0.05	k	0.2MIN	
A3	0.203REF		e	0.50 TYP	
D	2.90	3.10	b	0.18	0.30
E	2.90	3.10	L	0.30	0.50
D1	1.60	1.80			

Note:

1) All dimensions are in millimeters.
2) Package length does not include mold flash, protrusion or gate burr.
3) Package width does not include inter lead flash or protrusion.
4) Lead popularity (bottom of leads after forming) shall be 0.10 millimeters max.
5) Pin 1 is lower left pin when reading top mark from left to right.

TAPE AND REEL INFORMATION

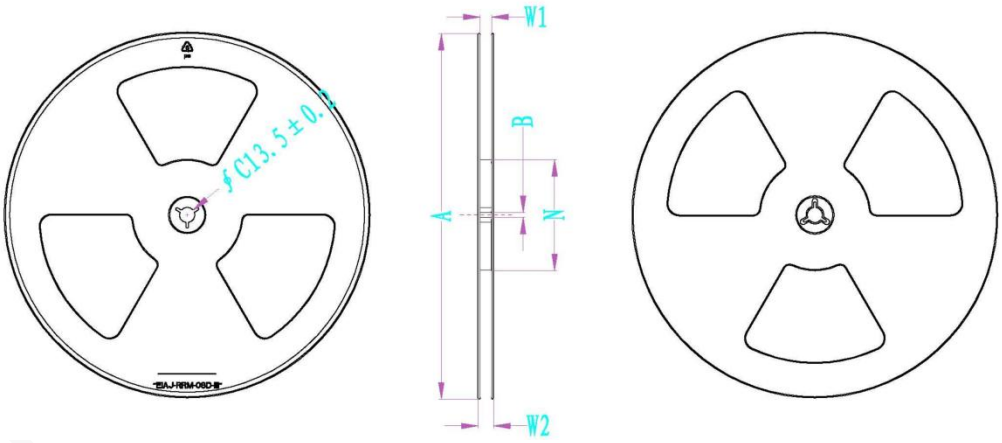
TAPE DIMENSIONS: QFN3x3-16



Unit: mm

Symbol	Dimensions	Symbol	Dimensions	Symbol	Dimensions	Symbol	Dimensions
A0	3.30±0.10	P0	4.00±0.10	E1	1.75±0.10	D1	1.55±0.05
B0	3.30±0.10	P1	8.00±0.10	F	5.50±0.10	T	0.30±0.05
K0	1.10±0.10	P2	2.00±0.10	D0	1.55±0.05	W	12.00±0.30

REEL DIMENSIONS: QFN3x3-16



Unit: mm

Ø A	B	Ø C	Ø N	W1	W2
330±1.0	4.7±0.5	13.5±0.2	100±0.5	13.4±0.5	17.4±0.5

Note:

1) All Dimensions are in Millimeter
2) Quantity of Units per Reel is 3000
3) MSL level is level 3.

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