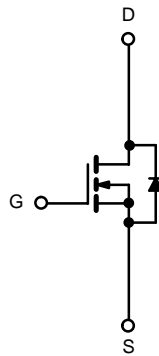
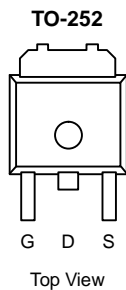


## 3N10L34-VB Datasheet N-Channel 100-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
100	0.030 at $V_{GS} = 10$ V	40
	0.035 at $V_{GS} = 4.5$ V	37

### FEATURES

- TrenchFET<sup>®</sup> Power MOSFETS
- 175 °C Junction Temperature
- Low Thermal Resistance Package



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	100	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175$ °C)	$T_C = 25$ °C	$I_D$	40	A
	$T_C = 125$ °C		23	
Pulsed Drain Current		$I_{DM}$	120	
Avalanche Current		$I_{AR}$	35	
Repetitive Avalanche Energy <sup>a</sup>	$L = 0.1$ mH	$E_{AR}$	61	mJ
Maximum Power Dissipation <sup>a</sup>	$T_C = 25$ °C	$P_D$	107 <sup>b</sup>	W
	$T_A = 25$ °C <sup>c</sup>		3.75	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	(PCB Mount) <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)		$R_{thJC}$	1.4	

Notes:

- Duty cycle  $\leq 1$  %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).

\* Pb containing terminations are not RoHS compliant, exemptions may apply.

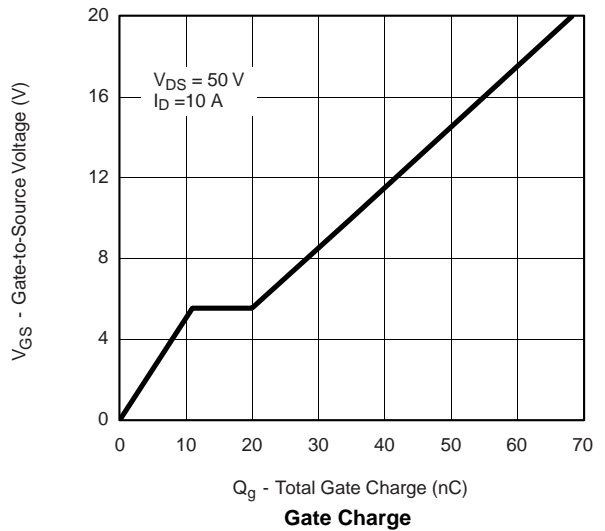
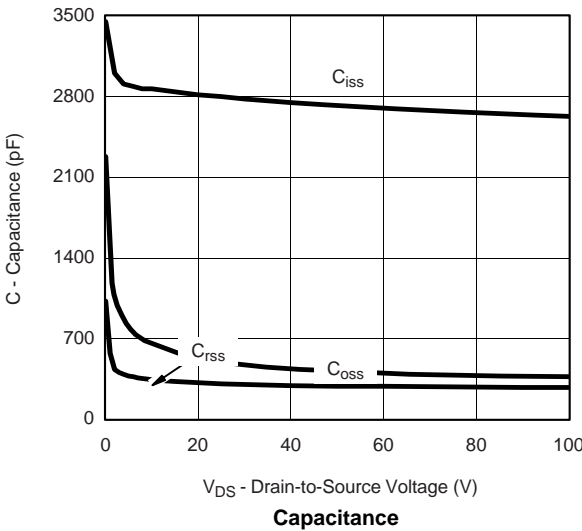
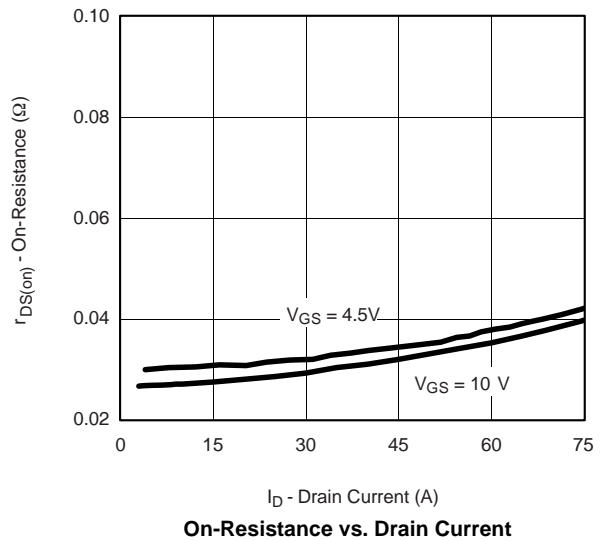
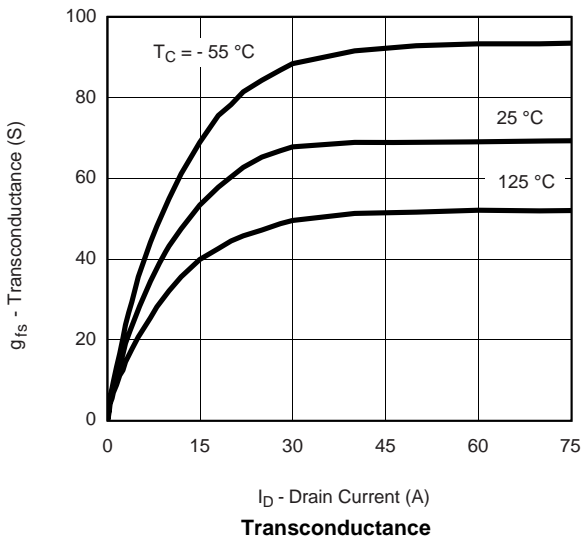
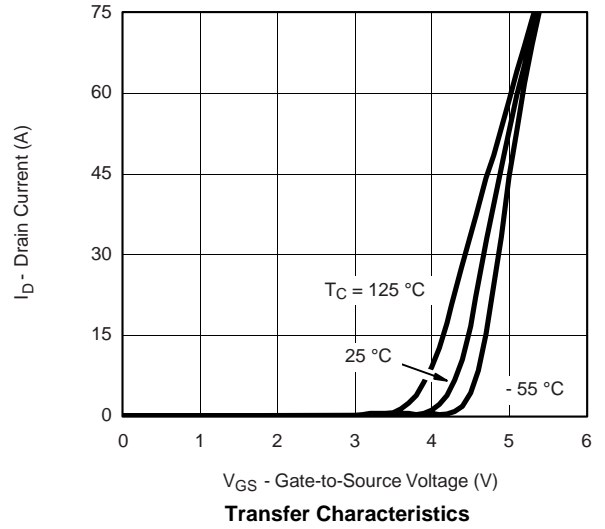
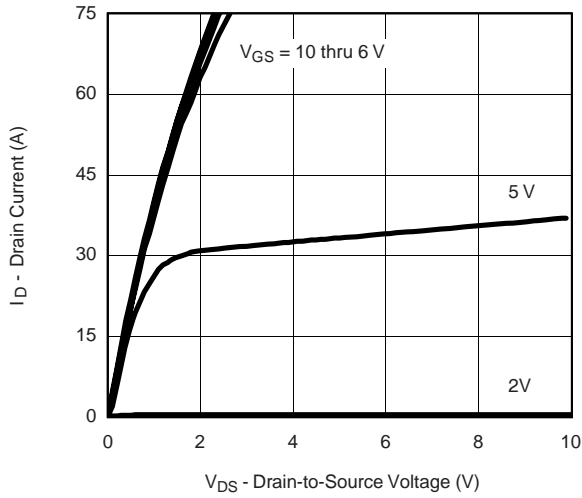
<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{SS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1		3	V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}, T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	75			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		0.030		$\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 3\text{ A}$		0.035		
		$V_{GS} = 10\text{ V}, I_D = 5\text{ A}, T_J = 125\text{ }^\circ\text{C}$		0.053		
		$V_{GS} = 10\text{ V}, I_D = 3\text{ A}, T_J = 175\text{ }^\circ\text{C}$		0.067		
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$	10			S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		2600		$\mu\text{F}$
Output Capacitance	$C_{oss}$			290		
Reverse Transfer Capacitance	$C_{rss}$			120		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		35	60	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			11		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			9		
Gate Resistance	$R_G$			1.7		$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 50\text{ V}, R_L = 1.25\text{ }\Omega$ $I_D \cong 40\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\text{ }\Omega$		11	20	ns
Rise Time <sup>c</sup>	$t_r$			12	20	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			30	45	
Fall Time <sup>c</sup>	$t_f$			12	20	
<b>Source-Drain Diode Ratings and Characteristics</b> $T_C = 25\text{ }^\circ\text{C}^b$						
Continuous Current	$I_S$				40	A
Pulsed Current	$I_{SM}$				120	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 30\text{ A}, V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 30\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		60	100	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			5	8	A
Reverse Recovery Charge	$Q_{rr}$			0.15	0.4	$\mu\text{C}$

Notes:

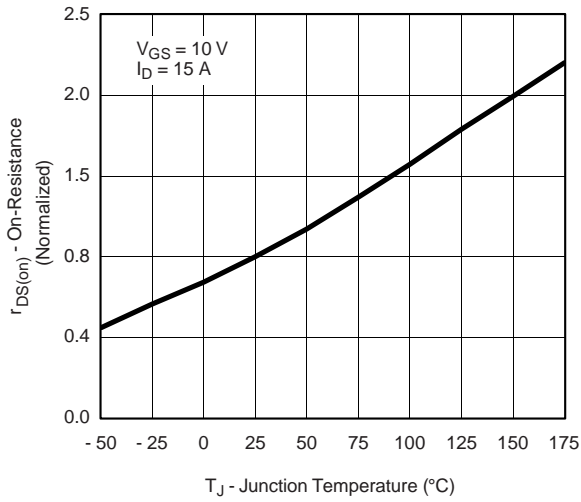
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



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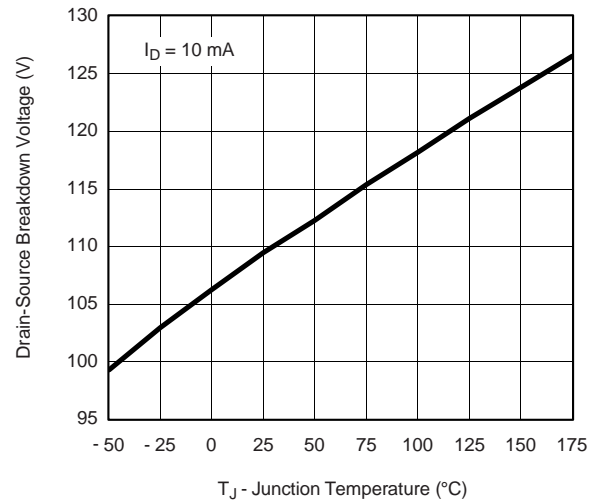
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**

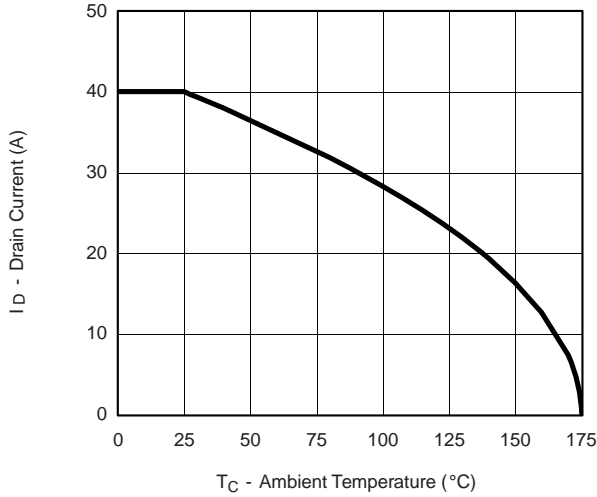


**Avalanche Current vs. Time**

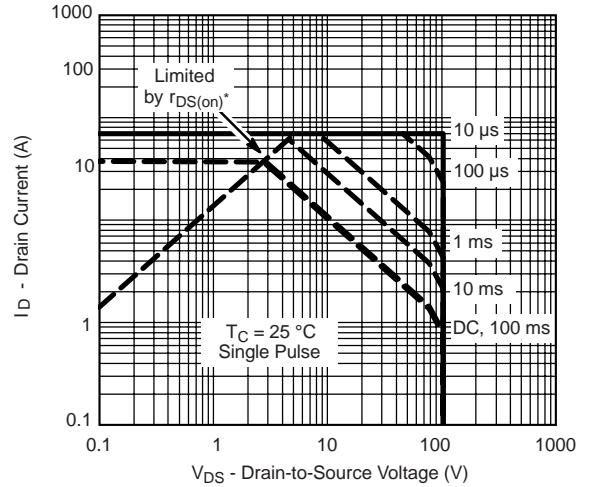


**Drain-Source Breakdown Voltage vs. Junction Temperature**

**THERMAL RATINGS**

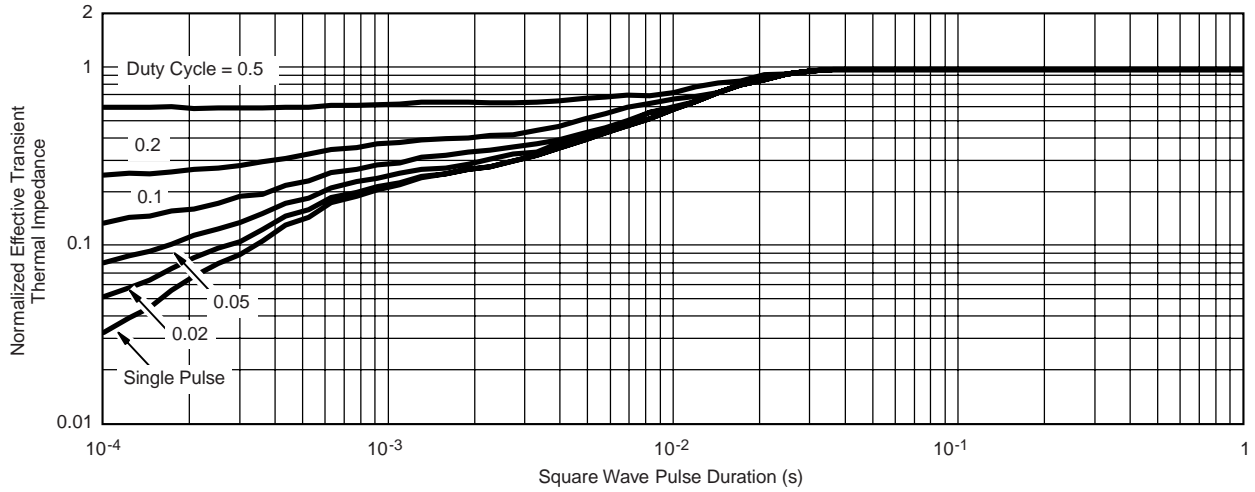


**Maximum Avalanche and Drain Current vs. Case Temperature**



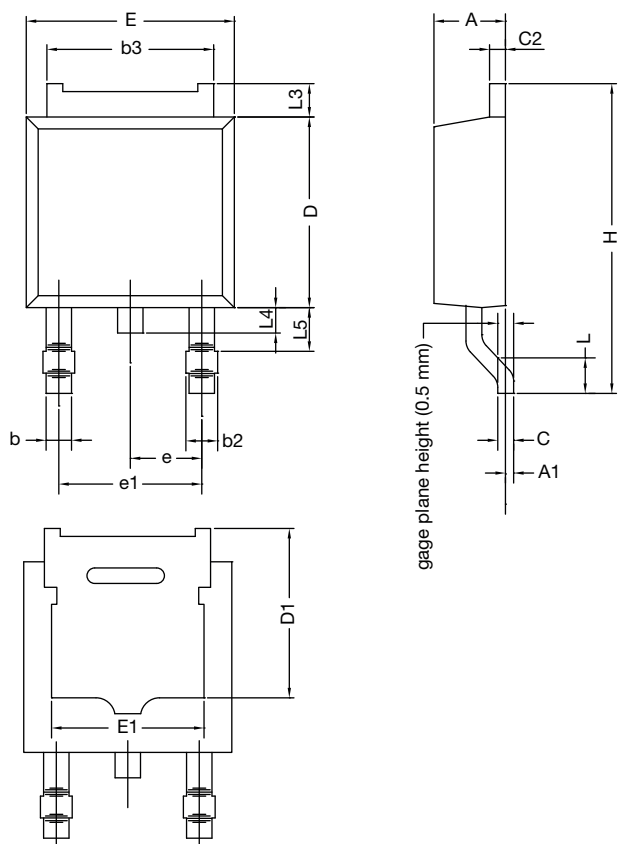
\*  $V_{GS} >$  minimum  $V_{GS}$  at which  $r_{DS(on)}$  is specified

**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Case**

## TO-252AA CASE OUTLINE

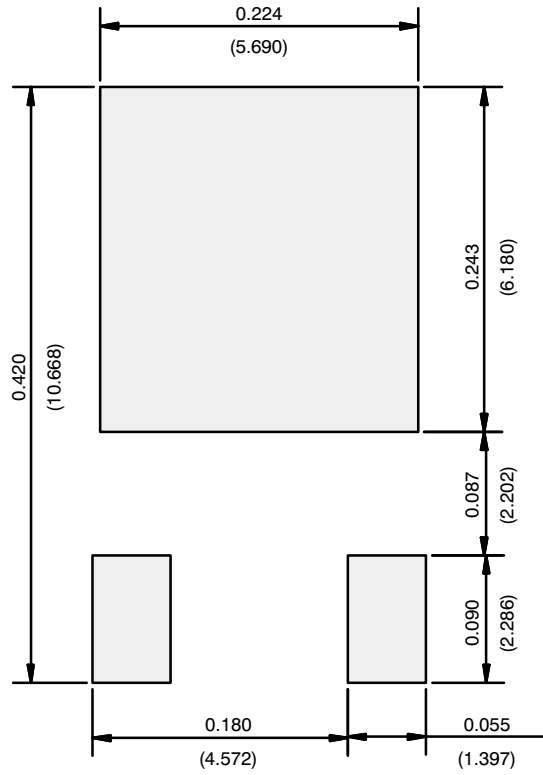


DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

**Note**

- Dimension L3 is for reference only.

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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