TF Semiconductor Solutions

TF21814M

High-Side and Low-Side Gate Driver

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in a half bridge configuration**
- **1.9A source / 2.3A sink output current capability**
- **Outputs tolerant to negative transients**
- **Wide low side gate driver supply voltage: 10V to 20V**
- **Logic input (HIN and LIN) 3.3V capability**
- **Schmitt triggered logic inputs with internal pull down**
- **Undervoltage lockout for high and low side drivers**
- **Extended temperature range: -40°C to +125°C**

Applications

- Motor Drivers
- Motor Controls
- DC-DC Converters
- Class D Power Amplifiers

Description

The TF21814M is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductor's high voltage process enables the TF21814M's high side to switch to 600V in a bootstrap operation.

The TF21814M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The TF21814M is offered in PDIP-14 and SOIC-14(N) packages and operate over an extended -40 °C to +125 °C temperature range.

SOIC-14(N)

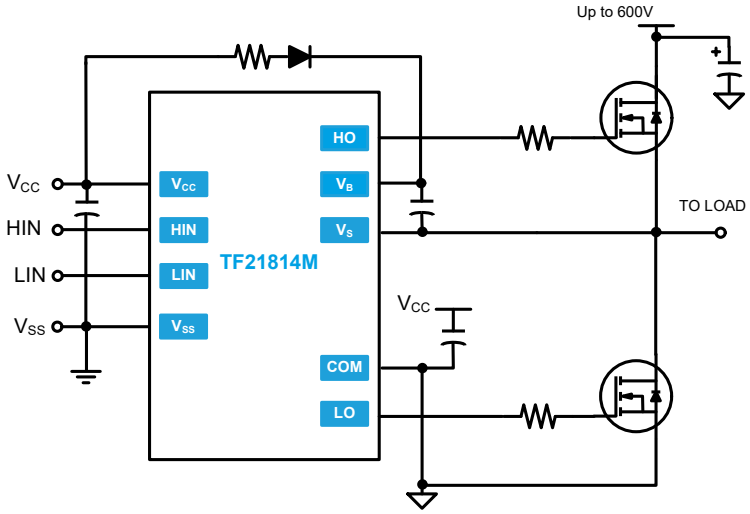
PDIP-14

Ordering Information

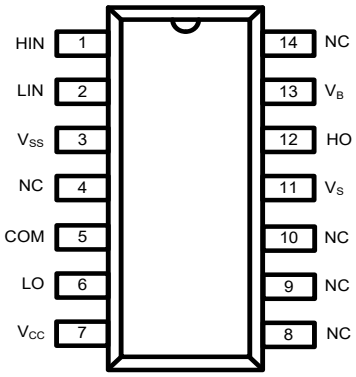
Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF21814M-3BS	PDIP-14	Tube / 25	YYWW TF21814M Lot ID
TF21814M-TUU	SOIC-14(N)	Tube / 50	YYWW TF21814M Lot ID
TF21814M-TUH	SOIC-14(N)	T&R / 2500	

Typical Application



Pin Diagrams

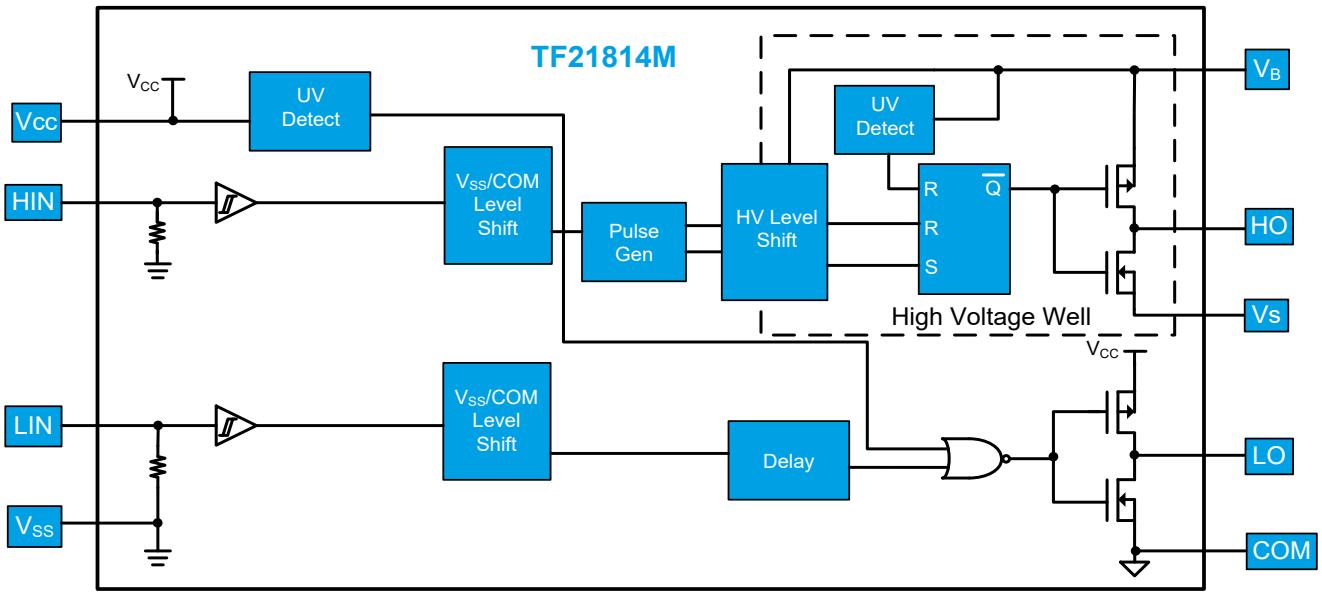


Top View: PDIP-14, SOIC-14

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
HIN	1	Logic input for high-side gate driver output, in phase with HO.
LIN	2	Logic input for low-side gate driver output, in phase with LO.
V_{SS}	3	Logic return
NC	4, 8, 9, 10, 14	No Connect
COM	5	Low-side return
LO	6	Low-side gate drive output
V_{CC}	7	Low-side and logic fixed supply
V_S	11	High-side floating supply return
HO	12	High-side gate drive output
V_B	13	High-side floating supply

Functional Block Diagram



Absolute Maximum Ratings *(NOTE1)*

V_B - High side floating supply voltage.....-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage.....V_S-0.3V to V_B+0.3V
dV_S/dt - Offset supply voltage transient.....50 V/ns
V_{CC} - Low-side fixed supply voltage.....-0.3V to +24V
V_{SS} - Logic supply offset voltage.....V_{CC}-24V to V_{CC}+0.3V
V_{LO} - Low-side output voltage.....-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN).....-0.3V to V_{CC} +0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \leq 25$ °C
SOIC-14.....1.0W
PDIP-14.....1.6W

SOIC-14(N) Thermal Resistance ***(NOTE2)***
θ_{JA}.....120°C/W
PDIP-14 Thermal Resistance ***(NOTE2)***
θ_{JA}.....75°C/W

T_J - Junction operating temperature.....+150 °C
T_L - Lead Temperature (soldering, 10 seconds).....+300 °C
T_{stg} - Storage temerature .....-55 to 150 °C

NOTE2 *Thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.*

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10	V_S + 20	V
V_S	High side floating supply offset voltage	***NOTE3***	600	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	COM	V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN)	V_{SS}	5	V
V_{SS}	Logic Ground	-5	+5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 *Logic operational for VS of -5V to +600V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V *NOTE5*	2.5			V
V_{IL}	Logic "0" input voltage				0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 0A			1.4	
V_{OL}	Low level output voltage, V_O	I_O = 20mA			0.2	
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	µA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V	20	60	150	
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V	50	120	240	µA
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		25	60	µA
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			5.0	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		8.0	8.9	9.8	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.4	8.2	9.0	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8.0	8.9	9.8	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9.0	
I_{O+}	Output high short circuit pulsed current	V_O = 0V, PW ≤ 10 µs	1.4	1.9		A
I_{O-}	Output low short circuit pulsed current	V_O = 15V, PW ≤ 10 µs	1.8	2.3		

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are applicable to the two logic input pins: LIN and HIN. The V_0 and I_0 parameters are applicable to the respective output pins: HO and LO.*

NOTE5 *For optimal operation, it is recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum with a pulse width of 440ns minimum.*

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, C_L = 1000pF, and T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propogation delay	V_S = 0V		180	270	ns
t_{off}	Turn-off propogation delay	V_S = 0V or 600V		220	330	
t_{DM}	Delay matching, HS & LS turn-on/off				35	
t_r	Turn-on rise time	V_S = 0V		40	60	
t_f	Turn-off fall time			20	35	

Timing Waveforms

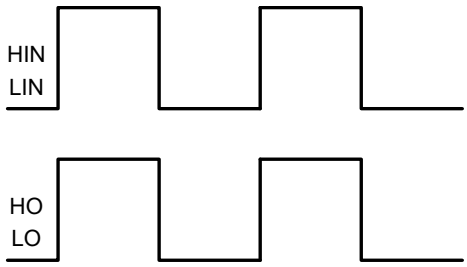


Figure 1. Input / Output Timing Diagram

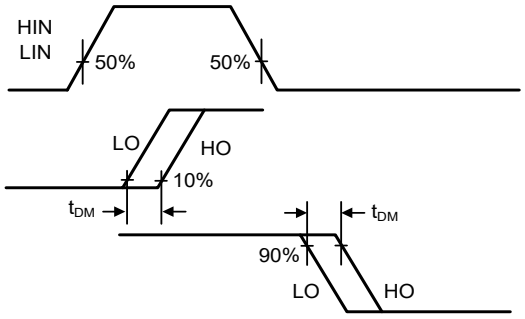


Figure 2. Delay Matching Waveform Definitions

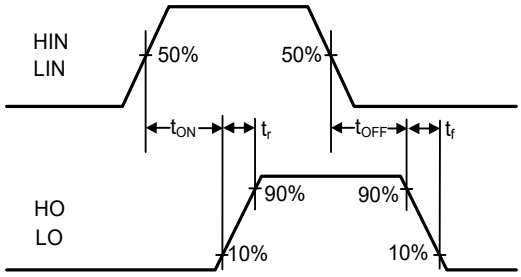


Figure 3. Switching Time Waveform Definitions

Application Information

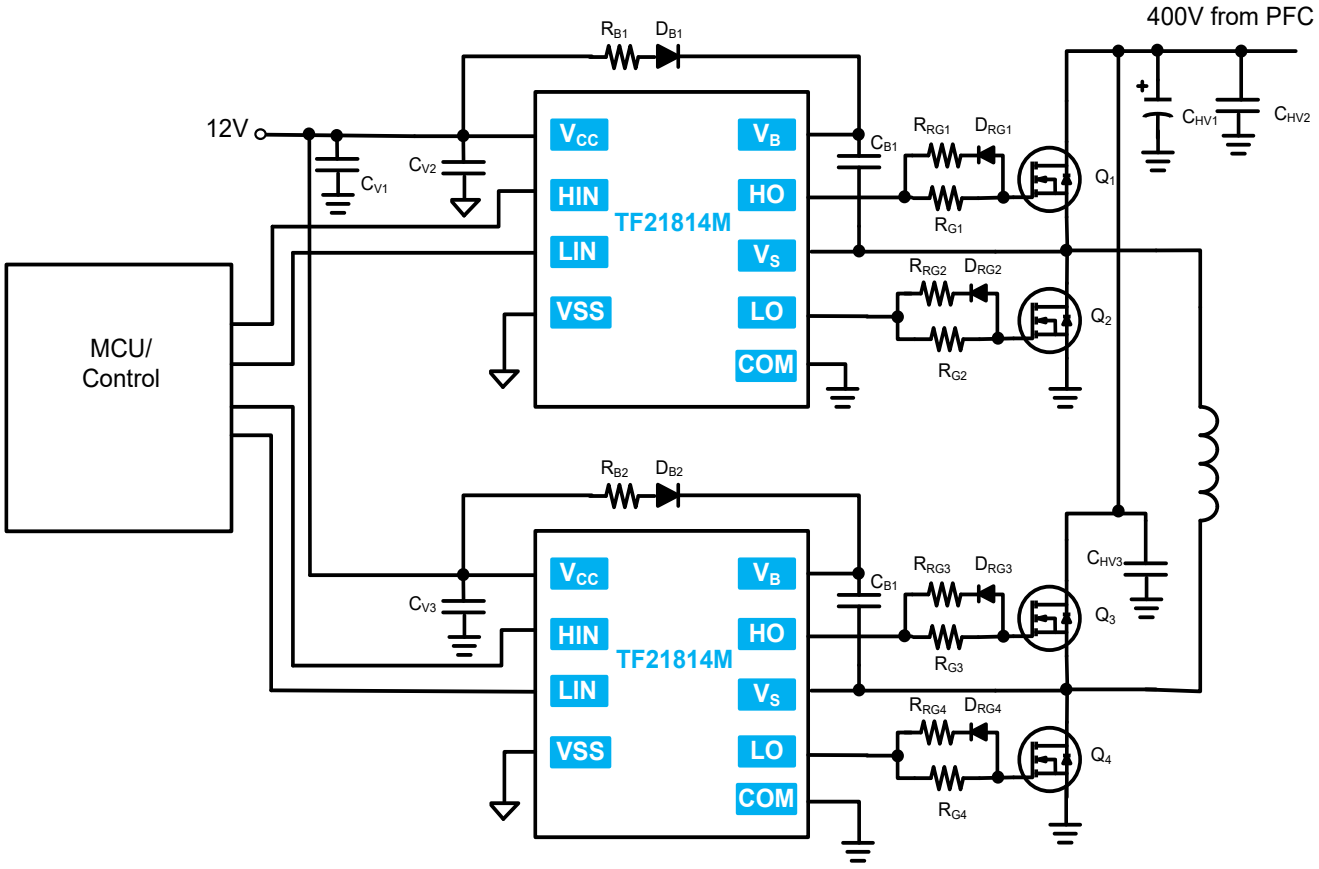


Figure 4. Primary side of Full Bridge converter using TF21814M

- RRG1, RRG2, RRG3, and RRG4 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

- It is **highly recommended** that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum (for VDD=15V) with a minimum pulse width of 440ns.

- RG1, RG2, RG3, and RG4 values are typically between 20Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

- RB1 and RB2 value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB1 and DB2 should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

Typical Performance Graphs V_{CC} = 15V, T_A = 25 °C , unless otherwise specified.

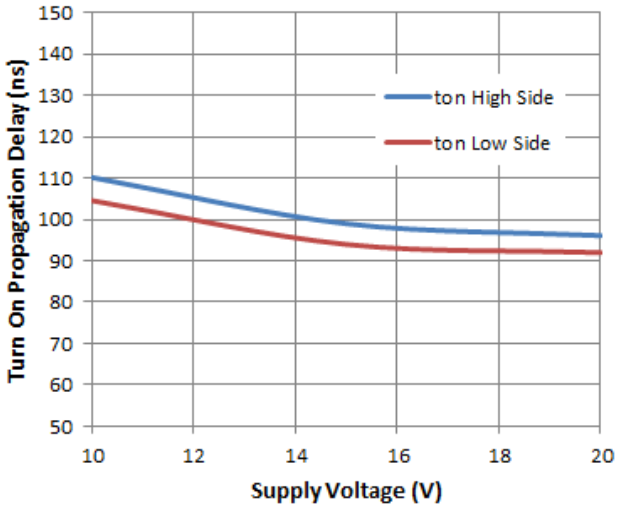


Figure 5. Turn on propagation delay vs. supply voltage

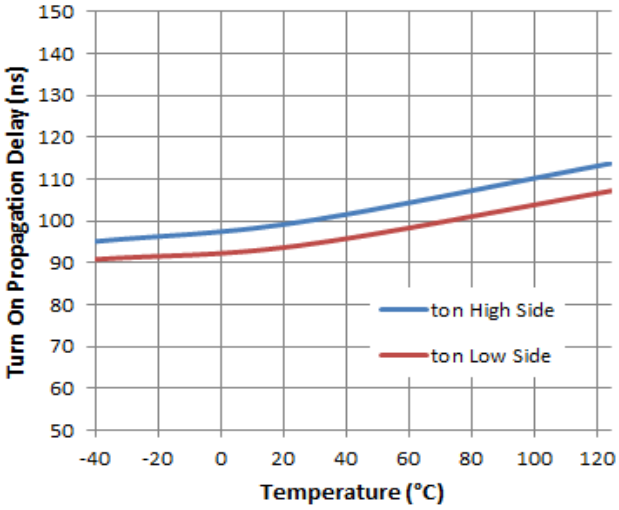


Figure 6. Turn on propagation delay vs. tempearture

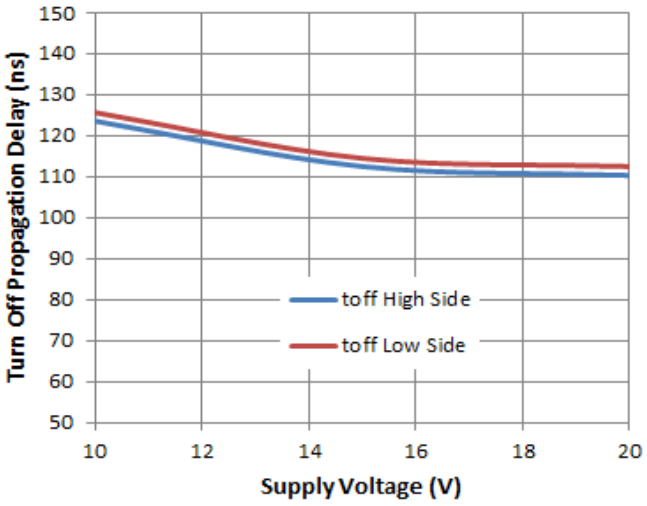


Figure 7. Turn off propagation delay vs. supply voltage

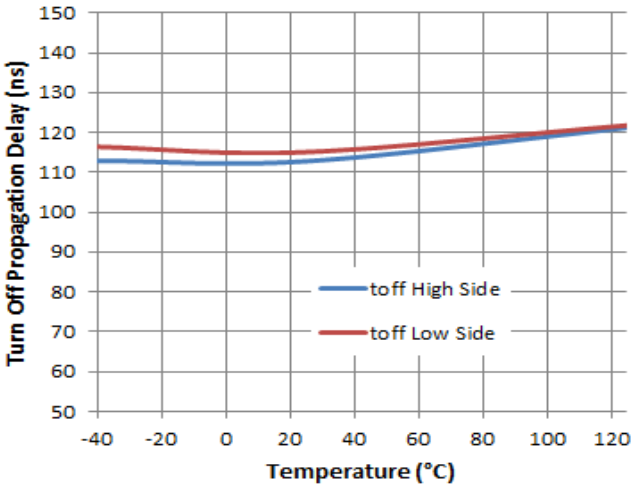


Figure 8. Turn off propagation delay vs. temperature

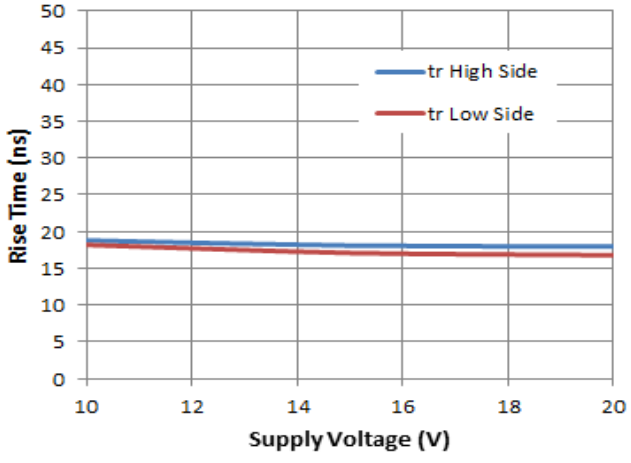


Figure 9. Rise time delay vs. supply voltage

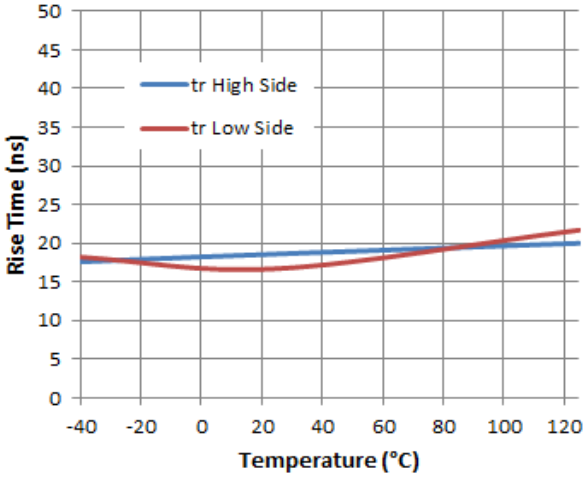


Figure 10. Rise time vs. temperature

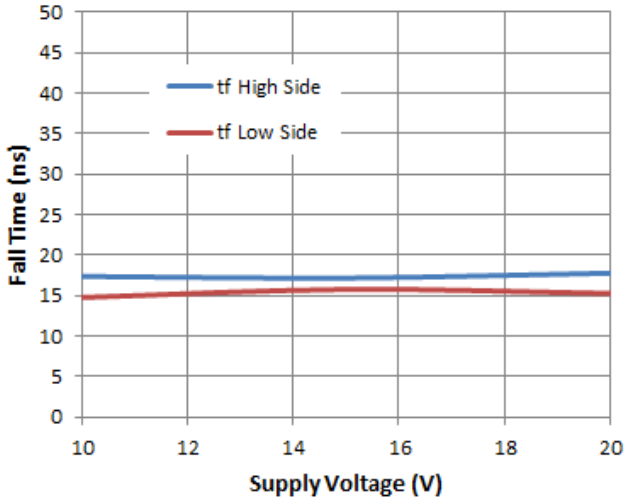


Figure 11. Fall time vs. supply voltage

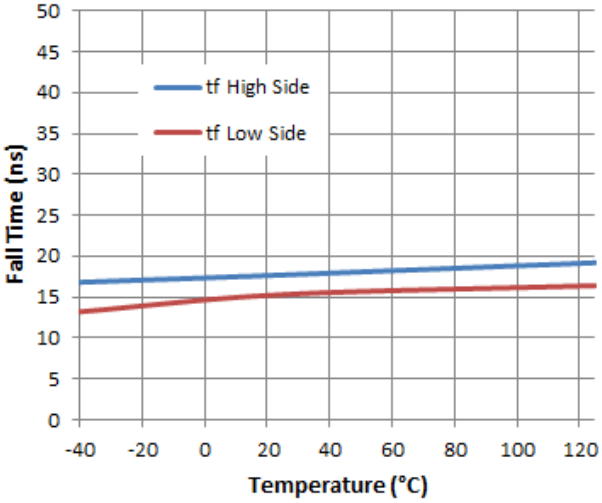


Figure 12. Fall time vs. temperature

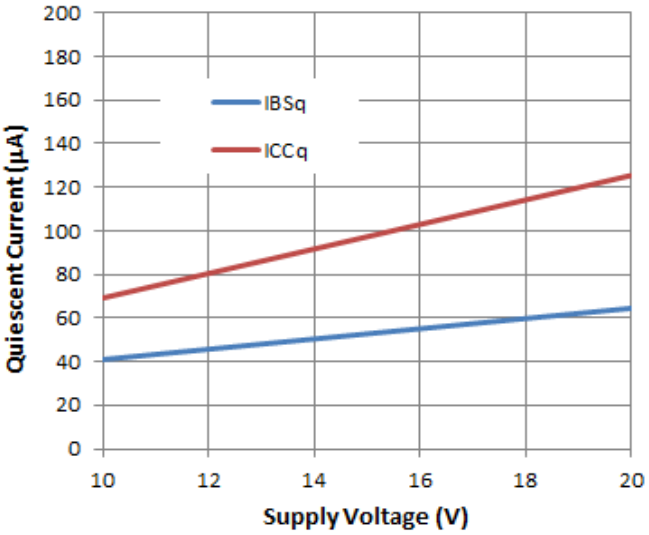


Figure 13. Quiescent current vs. supply voltage

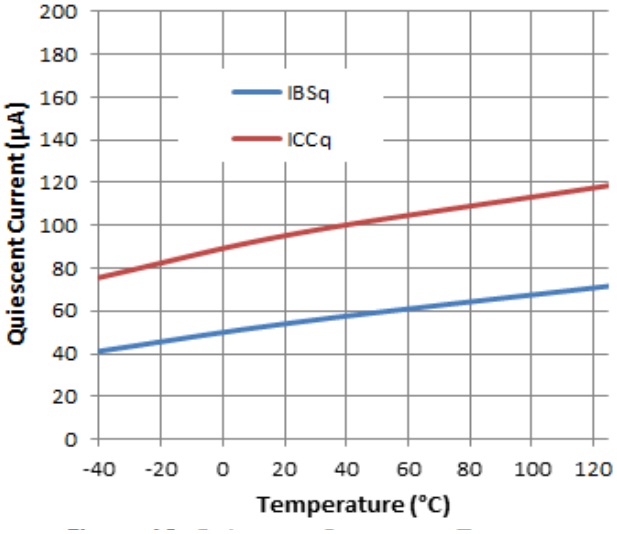


Figure 14. Quiescent current vs. temperature

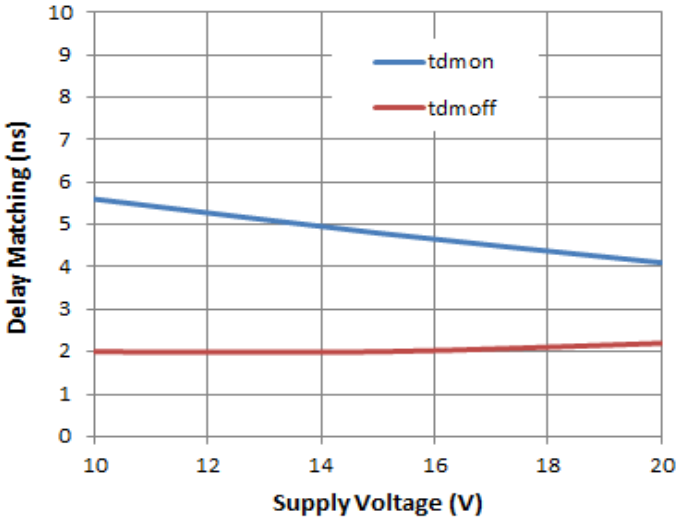


Figure 15. Delay Matching vs. supply voltage

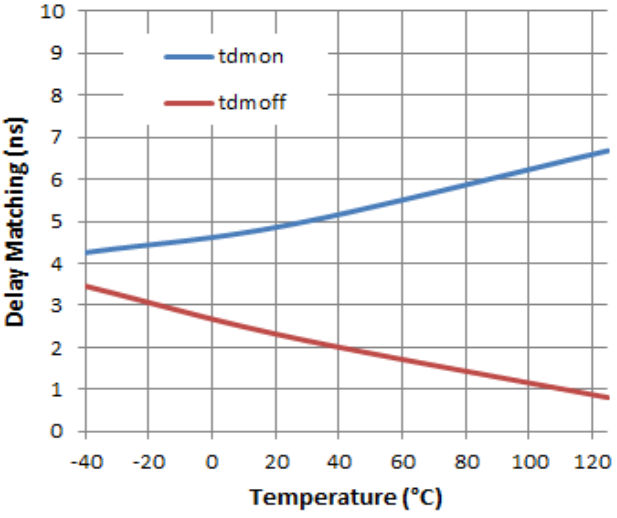


Figure 16. Delay Matching vs. temperture

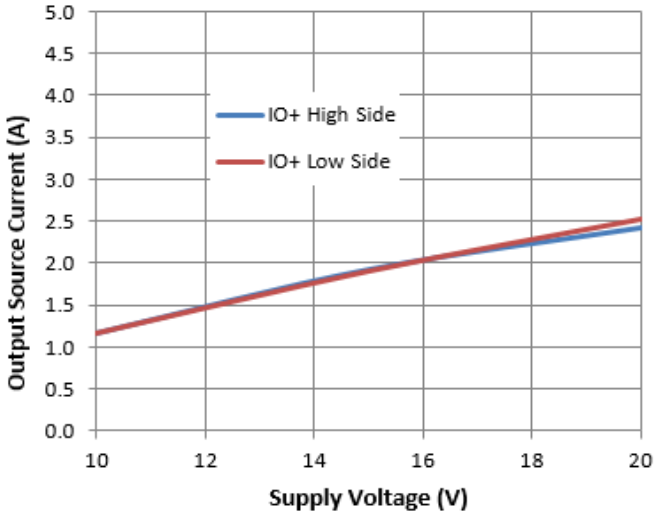


Figure 17. Output source current vs. supply voltage

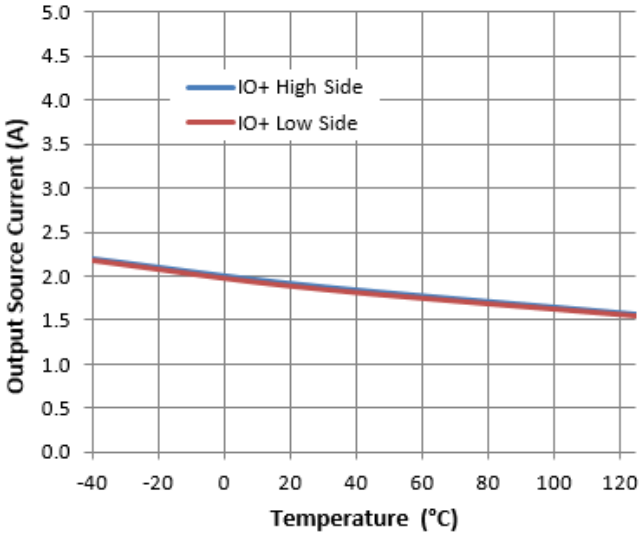


Figure 18. Output source current vs. temperature

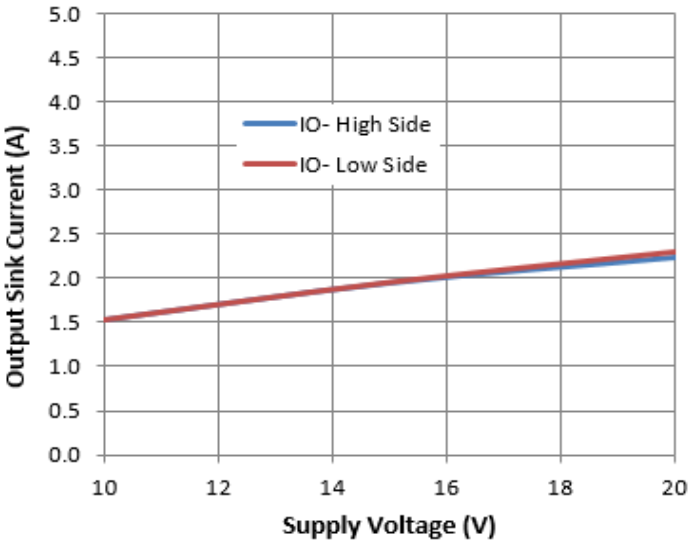


Figure 19. Output sink current vs. temperature

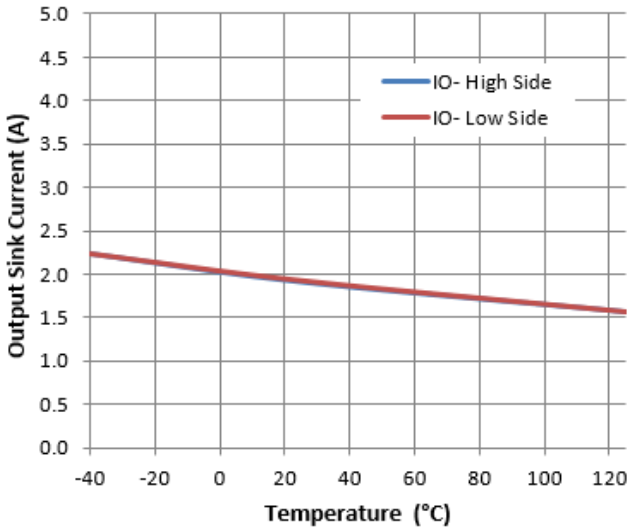


Figure 20. Output sink current vs. temperature

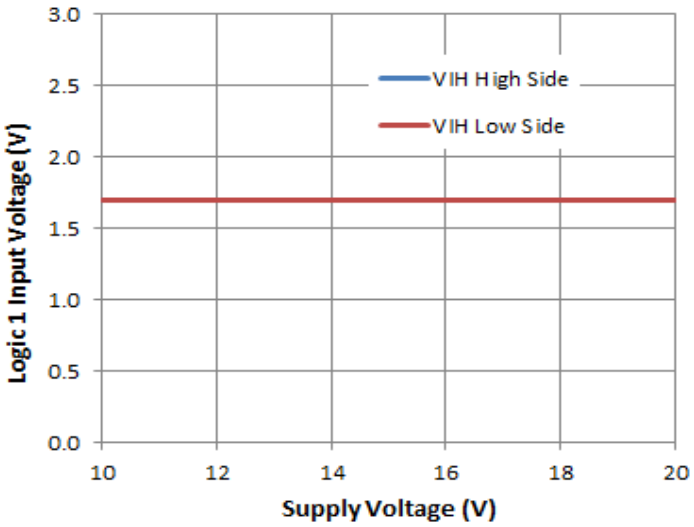


Figure 21. Logic 1 input voltage vs. supply voltage

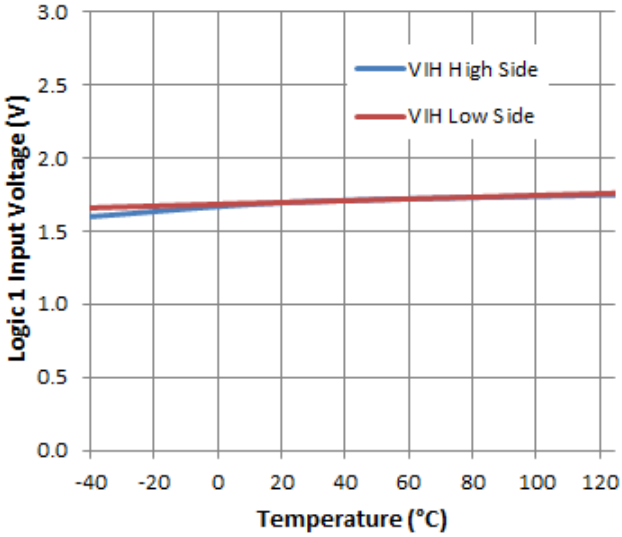


Figure 22. Logic 1 input voltage vs. temperature

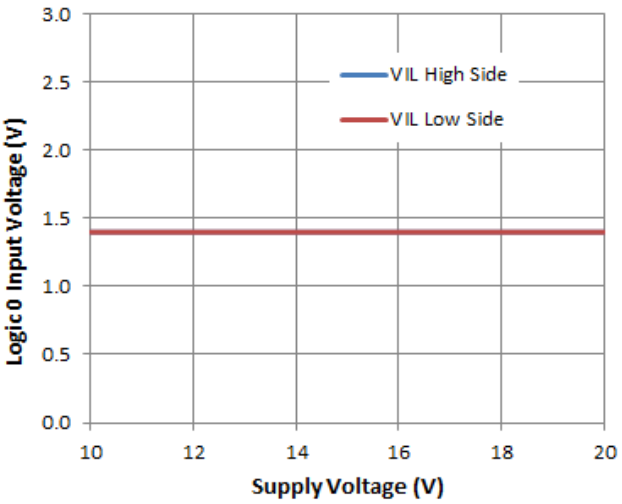


Figure 23. Logic 0 input voltage vs. supply voltage

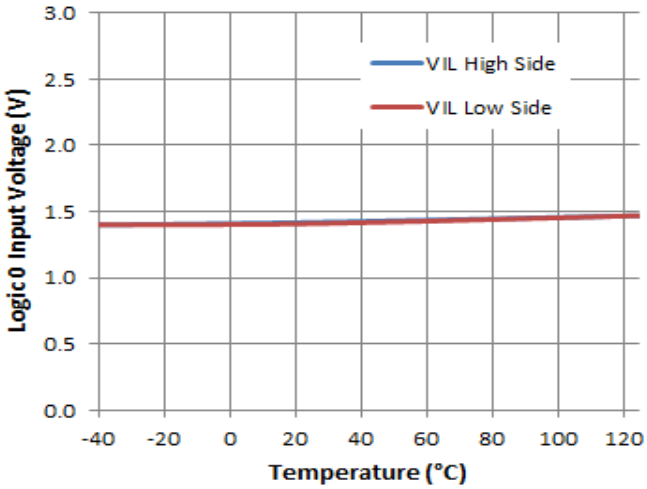


Figure 24. Logic 0 input voltage vs. temperature

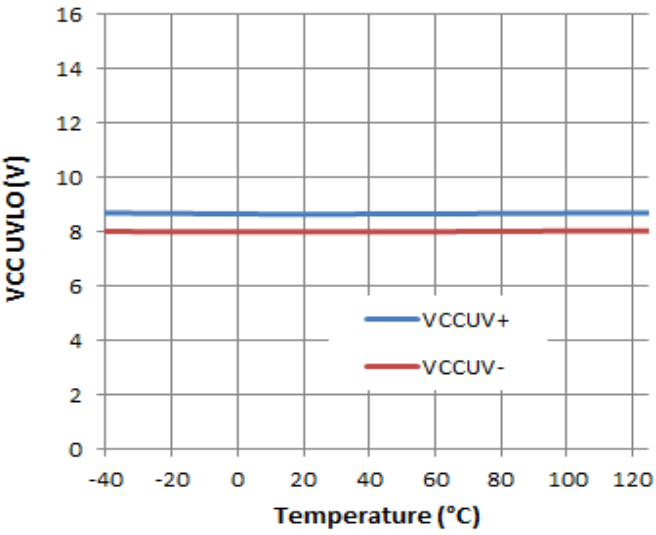


Figure 25. VCC UVLO vs. temperature

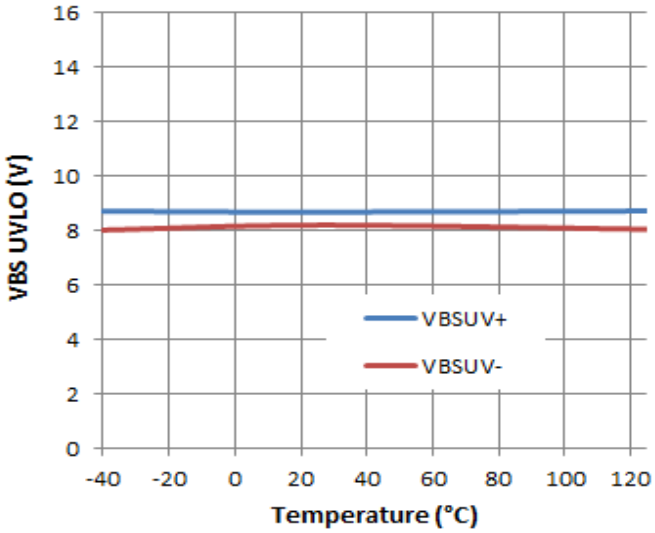


Figure 26. VBS UVLO vs. temperature

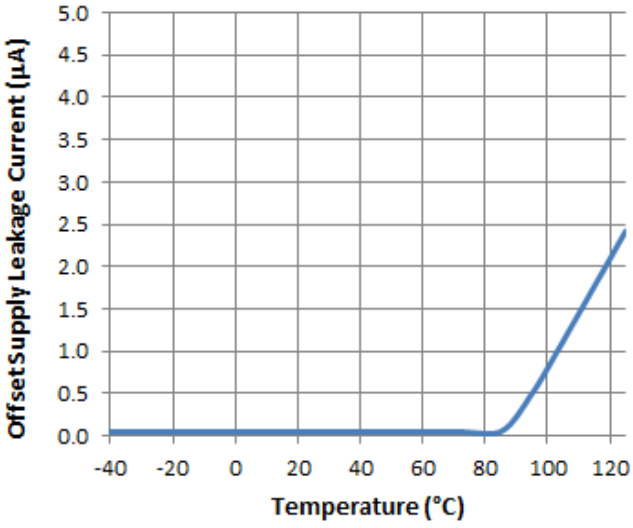
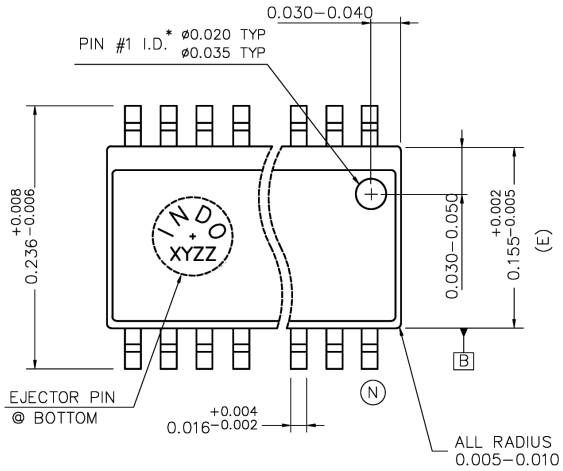


Figure 27. Offset supply leakage current vs. temperature

Package Dimensions (SOIC-14 N)

Please contact support@tfsemi.com for package availability.

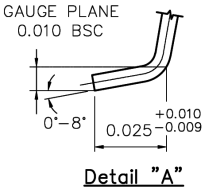
REV	DESCRIPTION	DATE	BY	REV	DESCRIPTION	DATE	
M	UPDATE FOOT LENGTH MEASUREMENT METHOD	04SEPT06	AGUS S/PE	J	CHANGE FR .035/.045 & FR .045/.055 CHANGE PIN 1 DIA FR ø.045 & ADD ø.020 TYP	07FEB01	AI
N	CHANGE COMPANY NAME & LOGO REMOVE "GULL WING " FROM TITLE UPDATE 16L VARIATION	13JUN08	AGUS S/PE	K	UPDATE TABLE, REMOVE CONVENTIONAL MOLD COLUMN	29APR03	HA
				L	UPDATE TABLE, REMOVE MGP MOLD FOR 08N SOIC STANDARD LEAD FRAME	01JUL04	SI



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

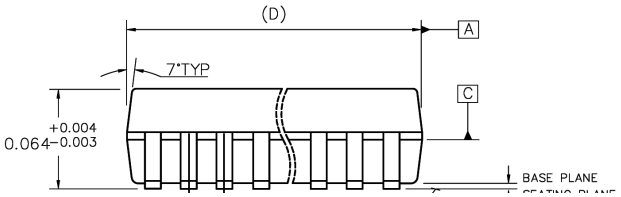
NOTES:

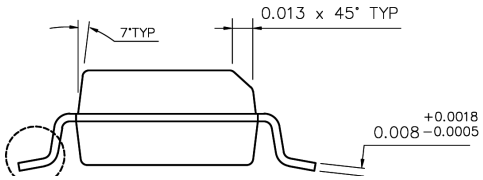
1. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 6 MILS PER SIDE.
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 3 MILS (@ SEATING PLANE) OUTGOING ASSEMBLY & 4 MILS AFTER TEST.
4. THE BOTTOM PACKAGE LEAD SIDE MAY BE BIGGER THAN THE TOP PACKAGE LEAD SIDE BY 4 MILS (2 MILS PER SIDE). BOTTOM PACKAGE DIMENSION SHALL FOLLOW DIMENSION STATED IN THIS DRAWING.
5. THE BOTTOM EJECTOR PIN CONTAINS COUNTRY OF ORIGIN "INDO" AND MOLD ID. (REFER TO TABLE FOR OPTION).
6. THIS DRAWING CONFORMS TO JEDEC REF. MS–012 REV. E



Detail "A"

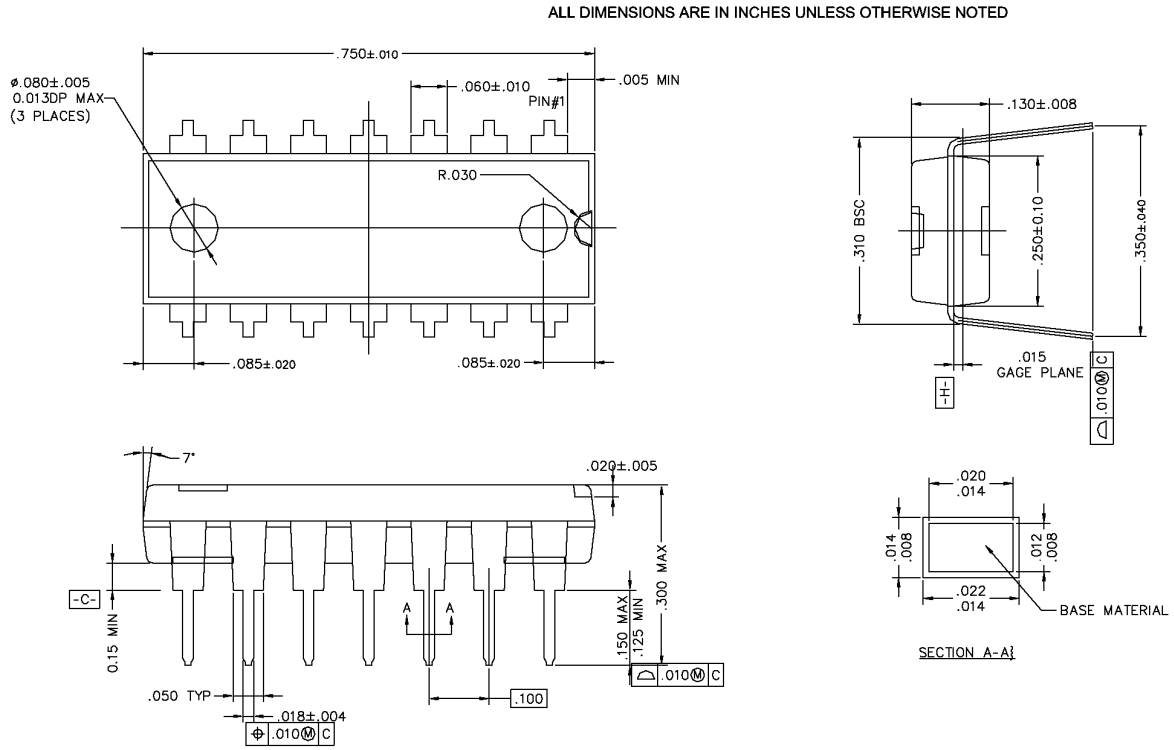
N	D VARIATION			MGP MOLD			
				STANDARD		MATRIX	
	MIN	NOM	MAX	PIN 1 I.D.	EJECT PIN	PIN 1 I.D.	EJECT PIN
08	0.189	0.193	0.196	N/A		YES	YES
14	0.337	0.339	0.344	YES	NO	YES	YES
⚠ 16	0.386	0.390	0.393	N/A		YES	YES





Package Dimensions (PDIP-14)

Please contact support@tfsemi.com for package availability.



Note: Drawing conforms to jedec ref. MS-001 rev D

Revision History

Rev.	Change	Owner	Date
1.0	First release, Final datasheet	Keith Spaulding	8/3/2020
1.1	Add Applications Informations page	Raj Selvarag	9/20/2021
1.2	Add Typical Performance Graphs	Keith Spaulding	9/27/2022

Important Notice

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