

40V N-channel Shielding Gate MOSFET

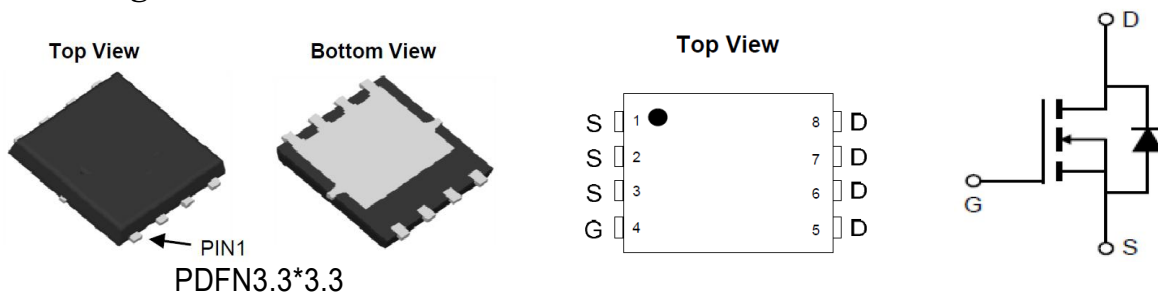
General Description

Features			Applications
VDS (max)	I_D (max)	Typ.RDS(on)	<ul style="list-style-type: none"> □ Battery protection □ Battery Powered Systems □ Portable Power Equipment □ DC-DC conversion □ Hard switching and high speed circuit
40V	45A	5.5mΩ@V _{GS} =10 V	
<ul style="list-style-type: none"> □ N-channel, optimized for high speed smooth switching □ Excellent Gate charge × RDS(on) (FOM) □ Very low on-resistance RDS(on) □ 100% UIS Tested 			

Ordering Information

Device	Package	Pin count	Marking
PAS40N055P	PDFN3*3	8	PAS40N055P

Pin Configurations



Main Parameters

Symbol	Parameter	Value	Units
V _{DS}	Drain-Source Voltage	40	V
I _D	Drain Current - Continuous (TC= 25°C)	45	A
	- Continuous (TC= 100°C)	30*	A
I _{DM}	Drain Current - Pulsed (Note 1)	180*	A
V _{GS}	Gate-Source Voltage	± 20	V



E_{AS}	Single Pulsed Avalanche Energy (Note 2)	115	mJ
P_D	Power Dissipation (TC = 25°C)	20	W
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +175	°C

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	6.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	47	°C/W

Electrical Characteristics TC = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	40			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
On Characteristics						
$V_{GS(TH)}$	Gate Threshold voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.6	2.0	V
$R_{DS(on)}$	Drain-Source on-state resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		5.4	6.8	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		7.5	9.4	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 20\text{ A}$ (Note 3)	30			S
Dynamic Characteristics						
C_{iss}	Input capacitance	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V},$ $F = 1.0\text{ Mhz}$		1031		pF
C_{oss}	Output capacitance			318		pF
C_{rss}	Reverse transfer capacitance			24		pF
Switching Characteristics						
$t_{d(on)}$	Turn On Delay Time	$V_{DD} = 20\text{ V}, I_D = 20\text{ A},$ $V_{GS} = 10\text{ V}, R_g = 1.6\text{ Ohm}$ (Note 3, 4)		6		ns
t_r	Rising Time			2.8		ns
$t_{d(off)}$	Turn Off Delay Time			23		ns

t_f	Fall Time			3		ns
Q_g	Total Gate Charge	$V_{DD}=20V, I_D=20A,$ $V_{GS}=10V$ (Note 3, 4)		36		nC
Q_{gs}	Gate-Source Charge			18.5		nC
Q_{gd}	Gate-Drain Charge			4.5		nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current			45		A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current			180		A
V_{SD}	Diode Forward Voltage	$V_{GS}= 0 V, I_S =20 A$			1.2	V
T_{rr}	Reverse recovery time	$I_F=50A, di/dt=100A/\mu S$		38		ns
Q_{rr}	Reverse recovery charge			28		nC


NOTE:

1. REPETITIVE RATING: PULSE WIDTH LIMITED BY MAXIMUM JUNCTION TEMPERATURE.
2. SURFACE MOUNTED ON FR4 BOARD, $T \leq 10$ SEC.
3. PULSE TEST: PULSE WIDTH ≤ 300 MS, DUTY CYCLE $\leq 2\%$.
4. GUARANTEED BY DESIGN, NOT SUBJECT TO PRODUCTION
5. EAS CONDITION : $T_J=25, V$
 $^{\circ}C$ $DD=20V, VG=10V, L=0.5MH, RG=25\Omega$

Typical Electrical and Thermal Characteristics

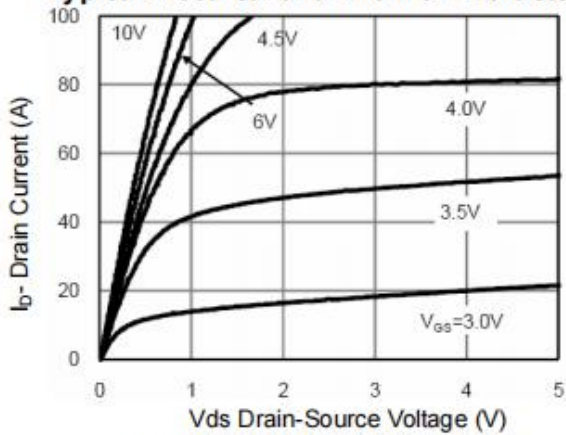


Figure 1 Output Characteristics

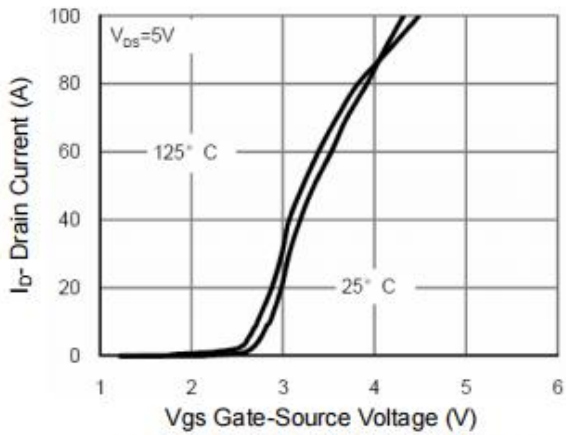


Figure 2 Transfer Characteristics

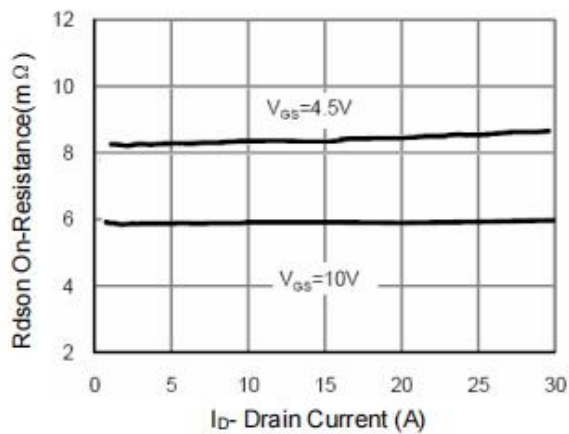


Figure 3 $R_{DS(on)}$ - Drain Current

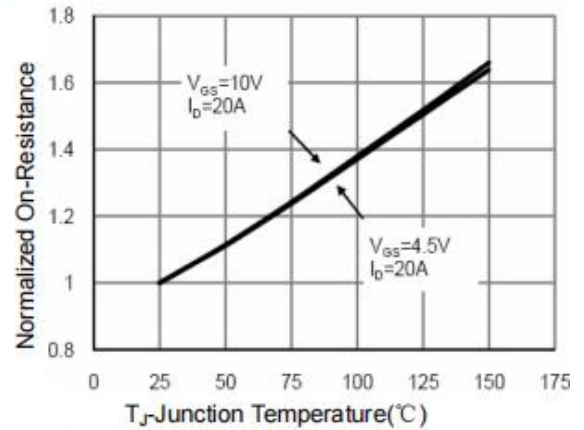


Figure 4 $R_{DS(on)}$ -Junction Temperature

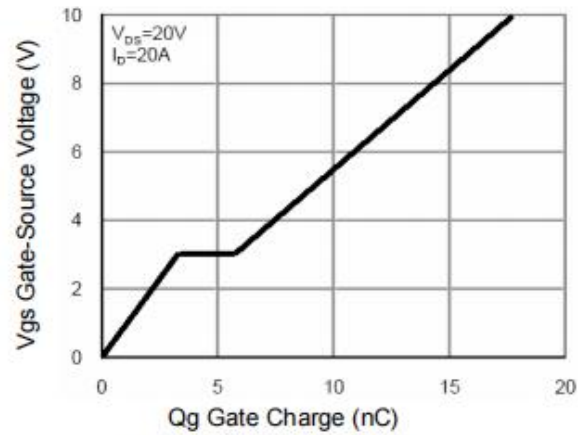


Figure 5 Gate Charge

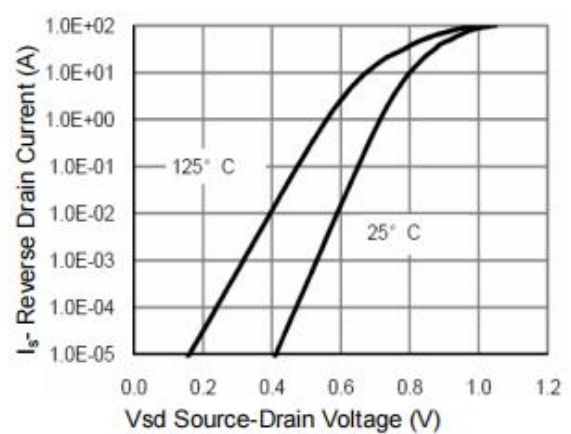


Figure 6 Source- Drain Diode Forward

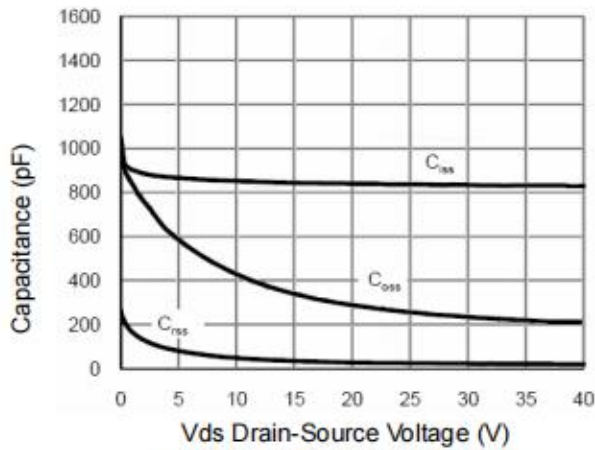


Figure 7 Capacitance vs Vds

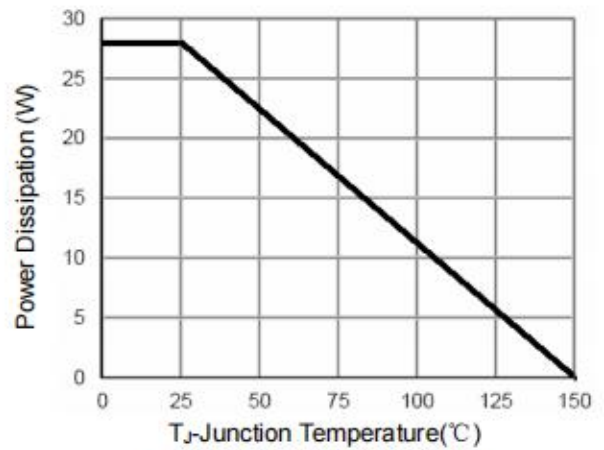


Figure 9 Power De-rating

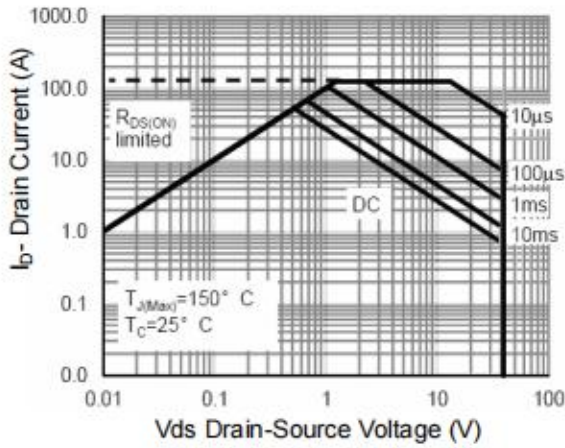


Figure 8 Safe Operation Area

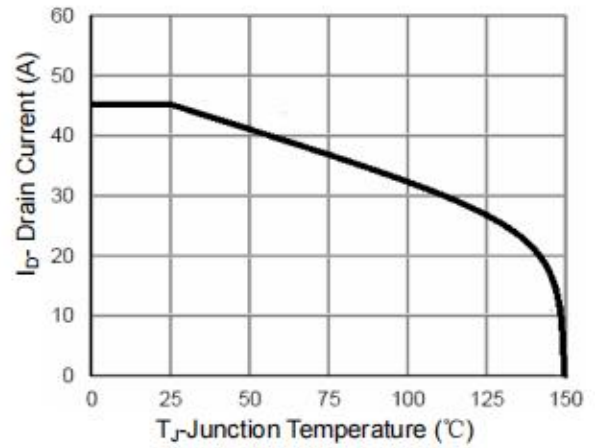


Figure 10 Current De-rating

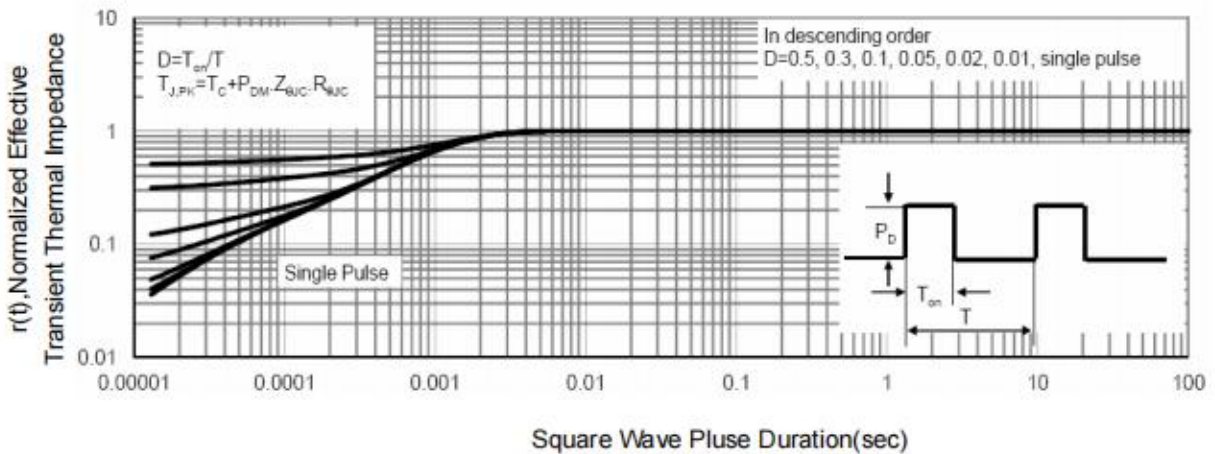
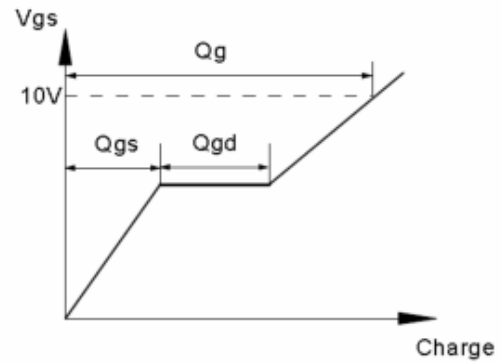
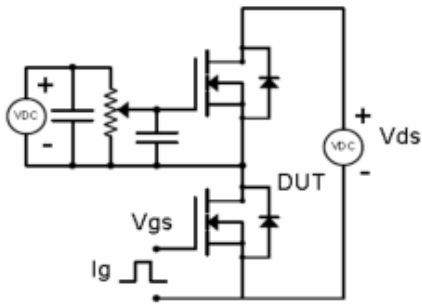


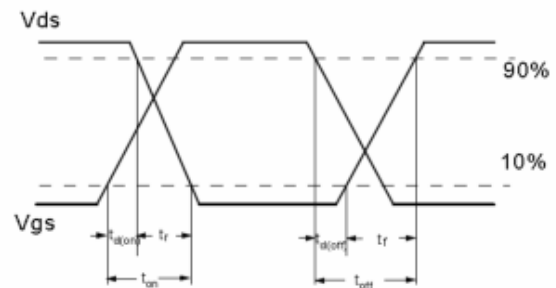
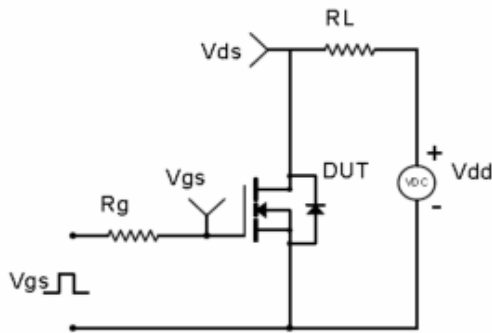
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit & Waveform

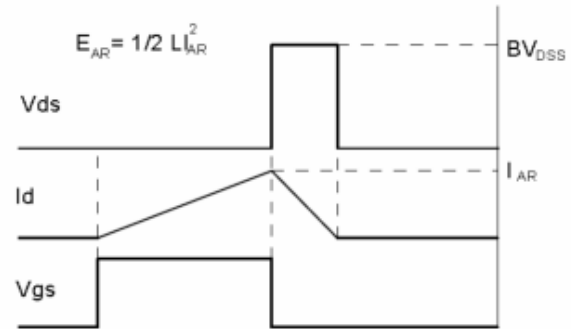
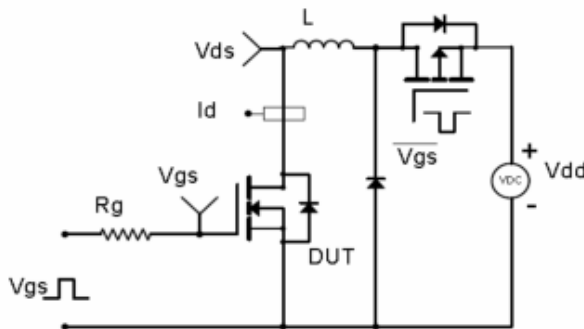
Gate Charge Test Circuit & Waveform



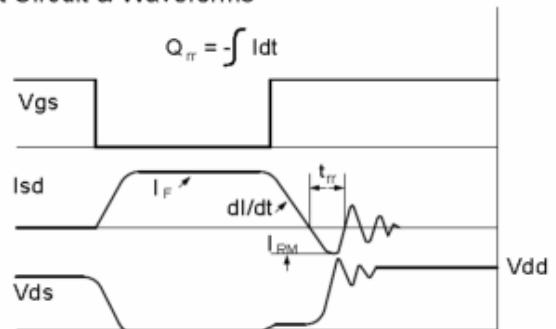
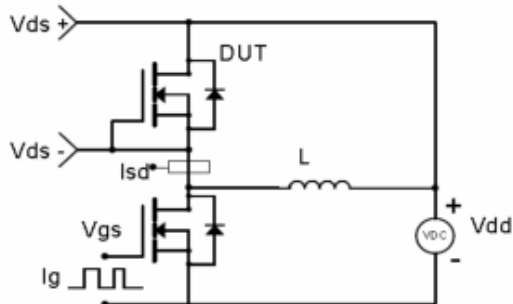
Resistive Switching Test Circuit & Waveforms

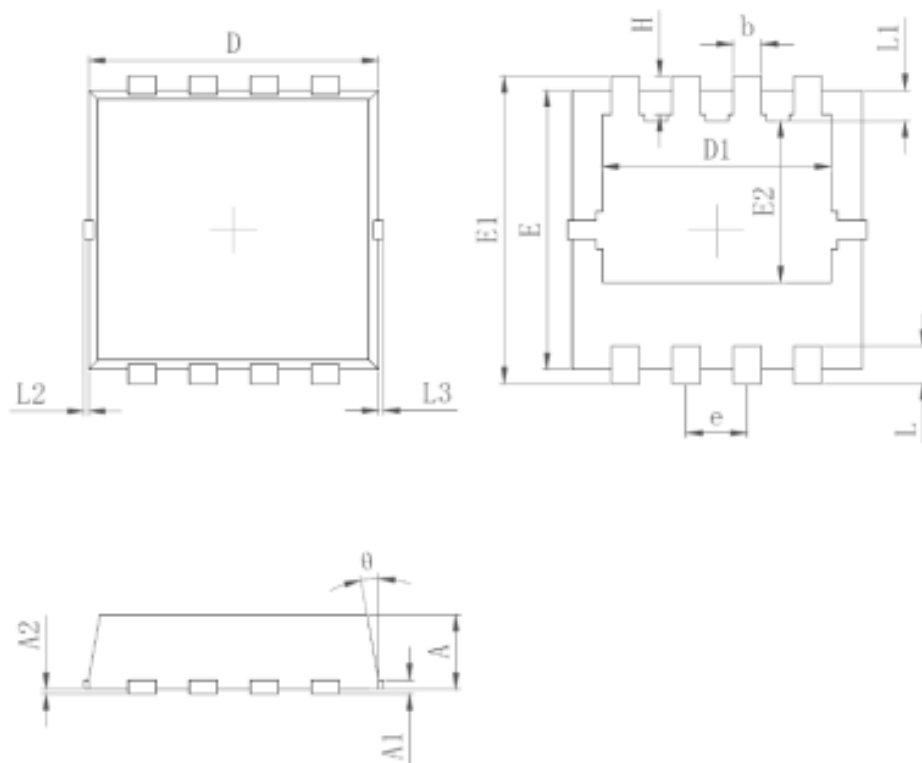


Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Package Dimensions


SYMBOL	MILLIMETER	
	MIN	MAX
A	0.700	0.900
A1	0.152 REF.	
A2	0 [~] 0.05	
D	3.000	3.200
D1	2.300	2.600
E	2.900	3.100
E1	3.150	3.450
E2	1.535	1.935
b	0.200	0.400
e	0.550	0.750
L	0.300	0.500
L1	0.180	0.480
L2	0 [~] 0.100	
L3	0 [~] 0.100	
H	0.315	0.515
θ	8°	12°

PDFN3*3-8L

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Revision History

Date	Version	Content of revision
20211104	V1.0	Initial