

## 2SK2995-VB Datasheet

### Power MOSFET

PRODUCT SUMMARY		
V <sub>DS</sub> (V)	250	
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V	0.040
Q <sub>g</sub> (Max.) (nC)	70	
Q <sub>gs</sub> (nC)	13	
Q <sub>gd</sub> (nC)	39	
Configuration	Single	

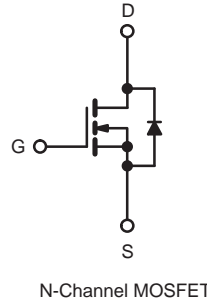
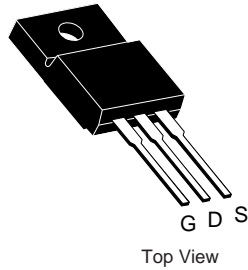
#### FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Surface Mount
- Low-Profile Through-Hole
- Available in Tape and Reel
- Dynamic dV/dt Rating
- 150 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Compliant to RoHS Directive 2002/95/EC



**RoHS\***  
COMPLIANT  
HALOGEN  
**FREE**  
Available

TO-220 FULLPAK



ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL		LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>		250	V
Gate-Source Voltage	V <sub>GS</sub>		± 20	
Continuous Drain Current	V <sub>GS</sub> at 10 V	T <sub>C</sub> = 25 °C	40	A
		T <sub>C</sub> = 100 °C	33	
Pulsed Drain Current <sup>a, e</sup>	I <sub>DM</sub>		150	
Linear Derating Factor			1.0	W/°C
Single Pulse Avalanche Energy <sup>b, e</sup>	E <sub>AS</sub>		580	mJ
Avalanche Current <sup>a</sup>	I <sub>AR</sub>		20	A
Repetitive Avalanche Energy <sup>a</sup>	E <sub>AR</sub>		13	mJ
Maximum Power Dissipation	T <sub>C</sub> = 25 °C		3.1	W
	T <sub>A</sub> = 25 °C		130	
Peak Diode Recovery dV/dt <sup>c, e</sup>	dV/dt		5.0	V/ns
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>		- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s		300 <sup>d</sup>	

**Notes**


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- V<sub>DD</sub> = 50 V, starting T<sub>J</sub> = 25 °C, L = 2.7 mH, R<sub>g</sub> = 25 Ω, I<sub>AS</sub> = 18 A (see fig. 12).
- I<sub>SD</sub> ≤ 20 A, di/dt ≤ 150 A/μs, V<sub>DD</sub> ≤ V<sub>DS</sub>, T<sub>J</sub> ≤ 150 °C.
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mounted, Steady-State) <sup>a</sup>	R <sub>thJA</sub>	-	40	°C/W
Maximum Junction-to-Case (Drain)	R <sub>thJC</sub>	-	1.0	

**Note**

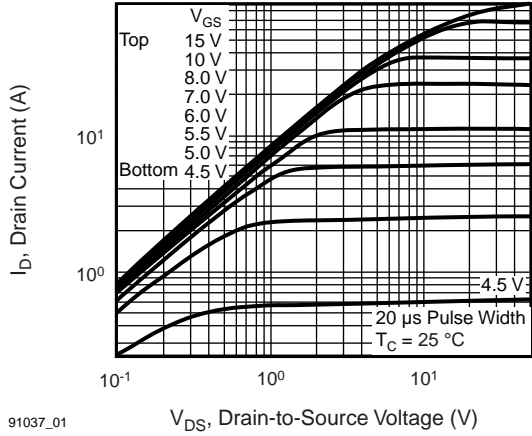
a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	250	-	-	V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	Reference to 25 °C, I <sub>D</sub> = 1 mA <sup>c</sup>	-	0.29	-	V/°C
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 200 V, V <sub>GS</sub> = 0 V	-	-	25	μA
		V <sub>DS</sub> = 160 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C	-	-	250	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V   I <sub>D</sub> = 11 A <sup>b</sup>	-	0.040	-	Ω
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 11 A <sup>d</sup>	6.7	-	-	S
<b>Dynamic</b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1.0 MHz, see fig. 5 <sup>d</sup>	-	1300	-	pF
Output Capacitance	C <sub>oss</sub>		-	430	-	
Reverse Transfer Capacitance	C <sub>rss</sub>		-	130	-	
Total Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = 10 V   I <sub>D</sub> = 20 A, V <sub>DS</sub> = 160 V, see fig. 6 and 13 <sup>b, c</sup>	-	-	70	nC
Gate-Source Charge	Q <sub>gs</sub>		-	-	13	
Gate-Drain Charge	Q <sub>gd</sub>		-	-	39	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 100 V, I <sub>D</sub> = 20 A, R <sub>g</sub> = 9.1 Ω, R <sub>D</sub> = 5.4 Ω, see fig. 10 <sup>b, c</sup>	-	14	-	ns
Rise Time	t <sub>r</sub>		-	51	-	
Turn-Off Delay Time	t <sub>d(off)</sub>		-	45	-	
Fall Time	t <sub>f</sub>		-	36	-	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Source-Drain Diode Current	I <sub>S</sub>	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	20	A
Pulsed Diode Forward Current <sup>a</sup>	I <sub>SM</sub>		-	-	72	
Body Diode Voltage	V <sub>SD</sub>	T <sub>J</sub> = 25 °C, I <sub>S</sub> = 20 A, V <sub>GS</sub> = 0 V <sup>b</sup>	-	-	2.0	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	T <sub>J</sub> = 25 °C, I <sub>F</sub> = 20 A, di/dt = 100 A/μs <sup>b, c</sup>	-	300	610	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>		-	3.4	7.1	μC
Forward Turn-On Time	t <sub>on</sub>	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> and L <sub>D</sub> )				

**Notes**

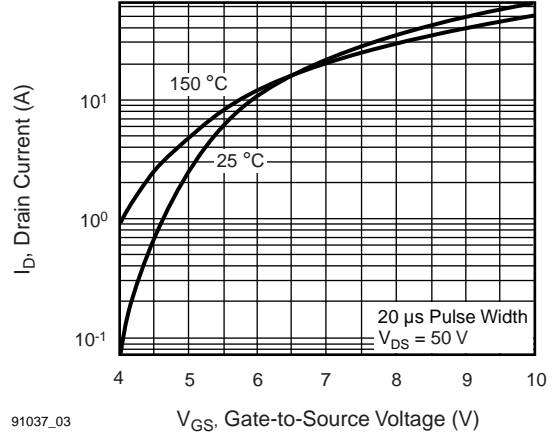
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.
- c. Uses IRF640/SiHF640 data and test conditions.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



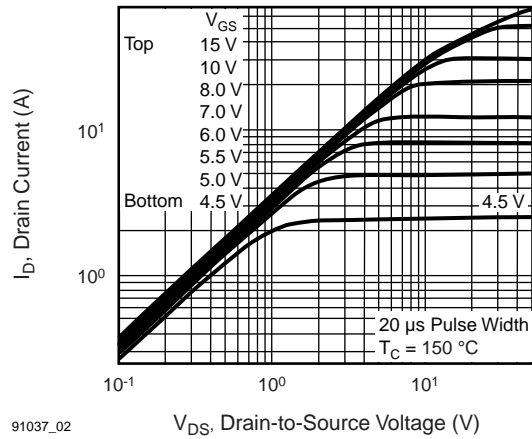
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**Fig. 1 - Typical Output Characteristics,  $T_J = 25\text{ °C}$**



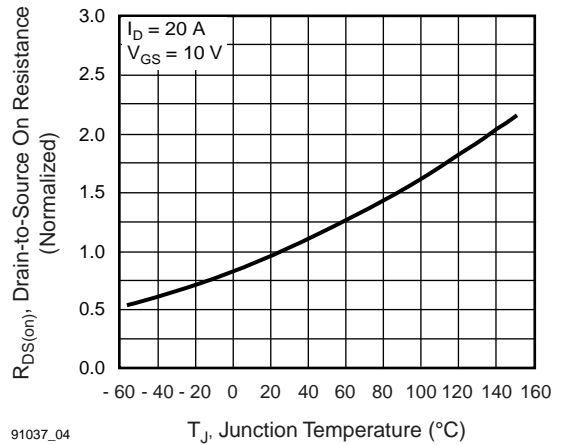
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**Fig. 3 - Typical Transfer Characteristics**



91037\_02

**Fig. 2 - Typical Output Characteristics,  $T_J = 175\text{ °C}$**



91037\_04

**Fig. 4 - Normalized On-Resistance vs. Temperature**

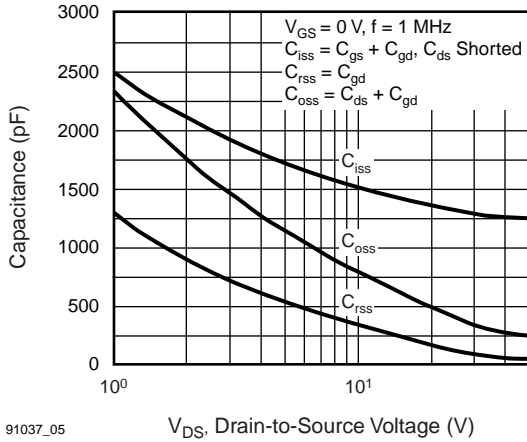


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

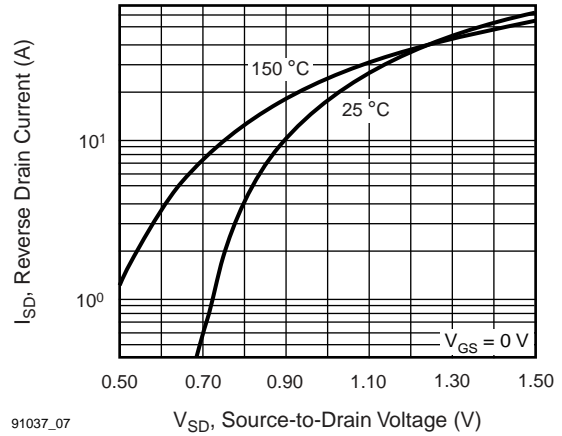


Fig. 7 - Typical Source-Drain Diode Forward Voltage

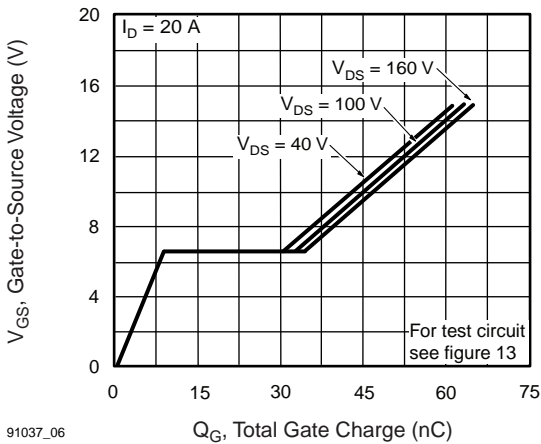


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

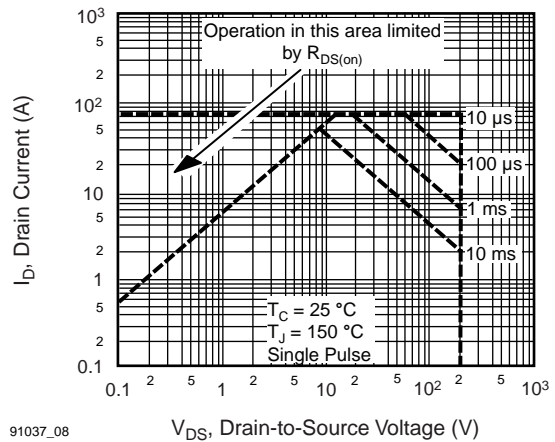
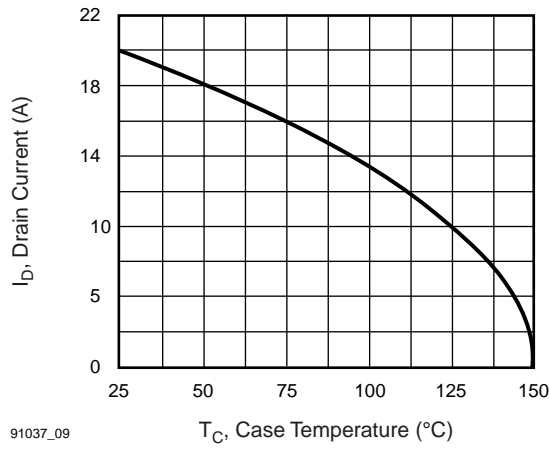
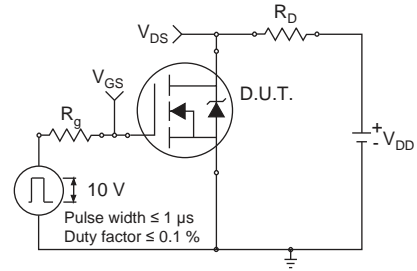


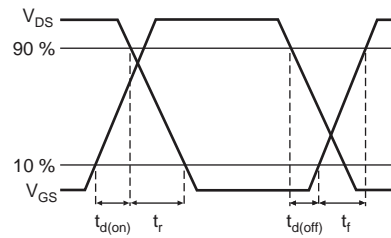
Fig. 8 - Maximum Safe Operating Area



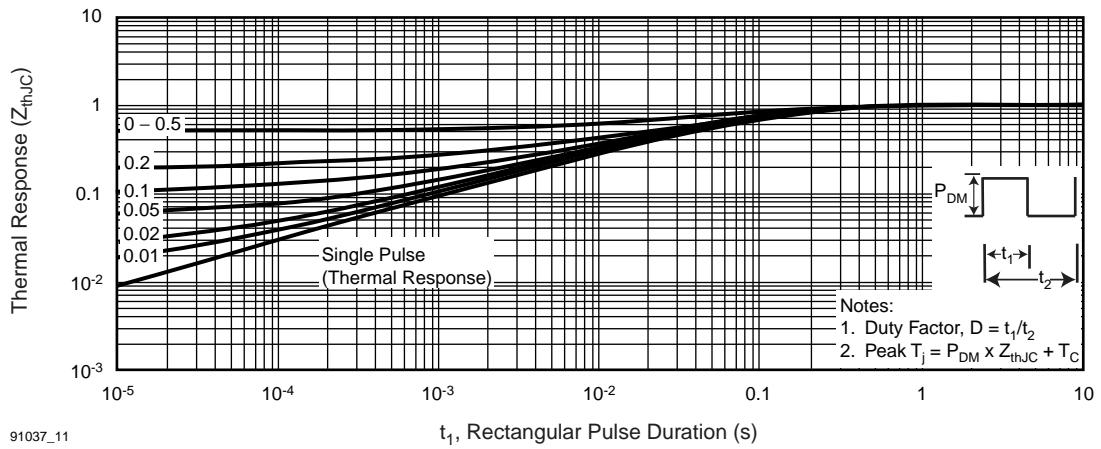
**Fig. 9 - Maximum Drain Current vs. Case Temperature**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**



**Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case**

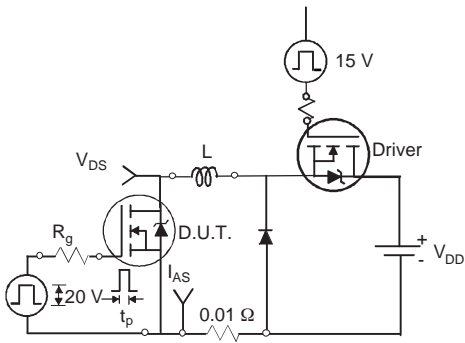


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

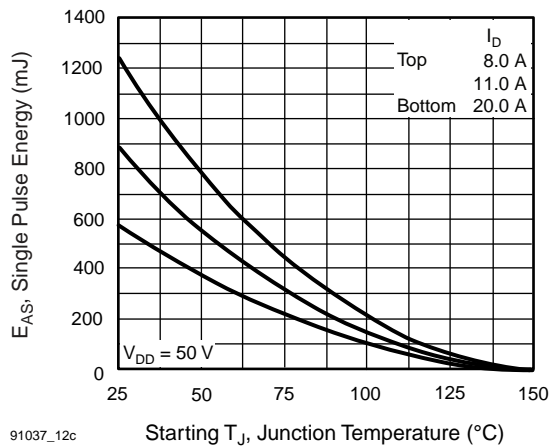


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

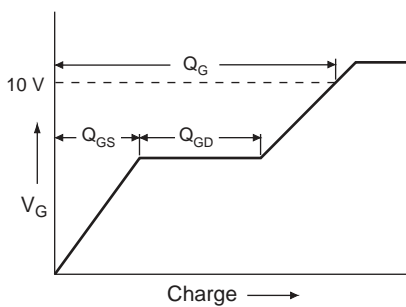


Fig. 13a - Basic Gate Charge Waveform

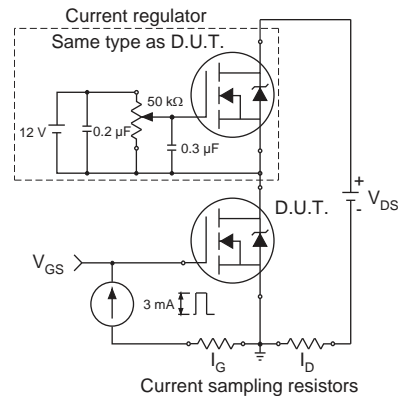
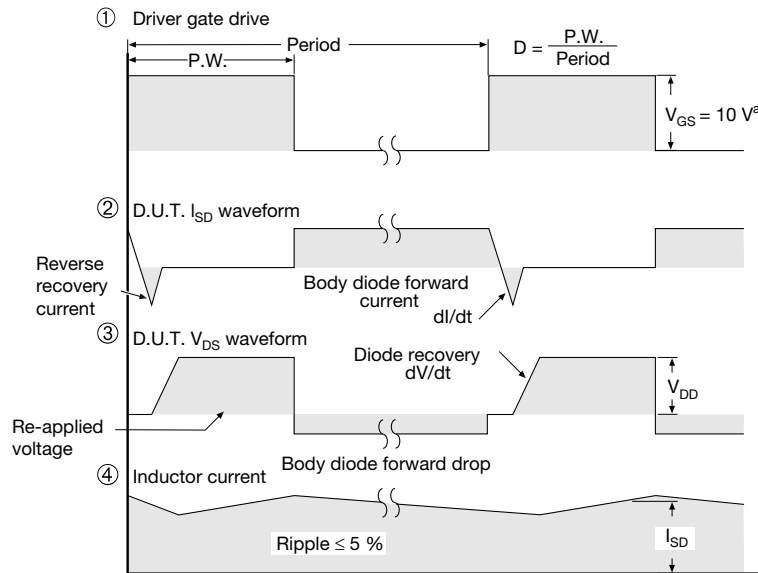
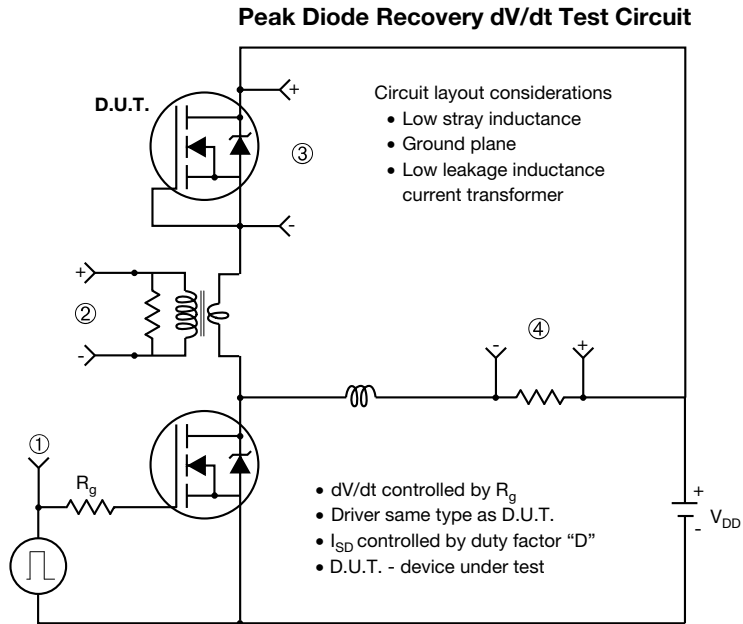


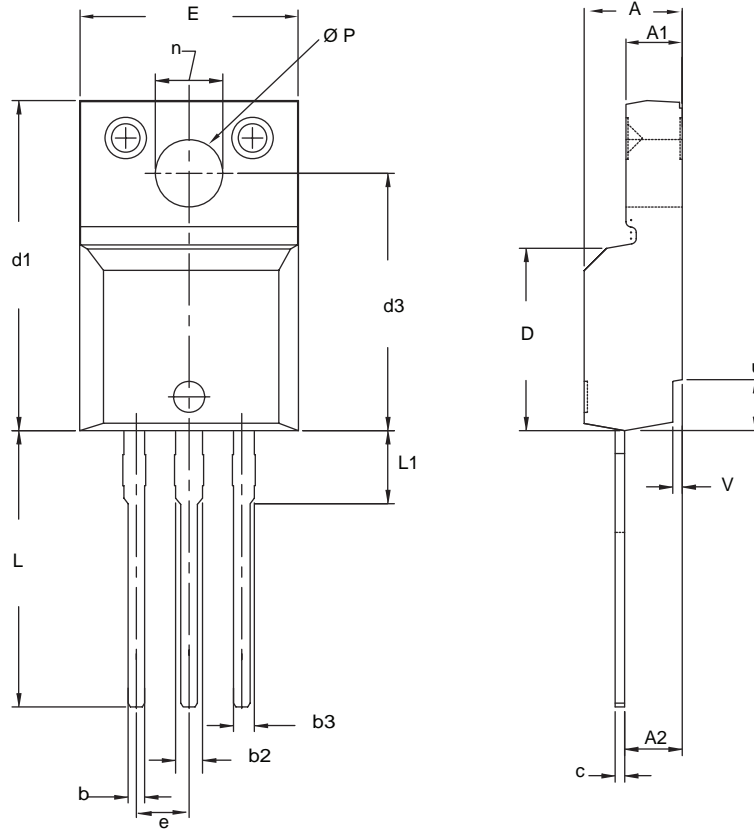
Fig. 13b - Gate Charge Test Circuit



**Note**  
a.  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

**TO-220 FULLPAK (HIGH VOLTAGE)**



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.570	4.830	0.180	0.190
A1	2.570	2.830	0.101	0.111
A2	2.510	2.850	0.099	0.112
b	0.622	0.890	0.024	0.035
b2	1.229	1.400	0.048	0.055
b3	1.229	1.400	0.048	0.055
c	0.440	0.629	0.017	0.025
D	8.650	9.800	0.341	0.386
d1	15.88	16.120	0.622	0.635
d3	12.300	12.920	0.484	0.509
E	10.360	10.630	0.408	0.419
e	2.54 BSC		0.100 BSC	
L	13.200	13.730	0.520	0.541
L1	3.100	3.500	0.122	0.138
n	6.050	6.150	0.238	0.242
Ø P	3.050	3.450	0.120	0.136
u	2.400	2.500	0.094	0.098
v	0.400	0.500	0.016	0.020

ECN: X09-0126-Rev. B, 26-Oct-09  
DWG: 5972

**Notes**

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet  $C_{pk} > 1.33$ .
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.



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