GE
Intelligent Platforms

Hardware Reference

PCIE-5565PIORC*

Ultrahigh Speed Fiber-Optic Reflective Memory with Interrupts

THE PCIE-5565PIORC IS DESIGNED TO MEET THE EUROPEAN UNION (EU) RESTRICTION OF HAZARDOUS SUBSTANCE (ROHS) DIRECTIVE (2002/95/EC) CURRENT REVISION.

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Overview

The PCIE-5565PIORC* is a PCI Express (PCIe) member of GE's family of Reflective Memory real-time fiber-optic network products that supports both low profile and standard height PCIe boards. Two or more PCIE-5565PIORCs, along with other members of this family, can be integrated into a network using standard fiber-optic cables. Each board in the network is referred to as a "node."

Reflective Memory allows computers, workstations, PLCs and other embedded controllers with different architectures and dissimilar operating systems to share data in real time. The 5565 family of Reflective Memory (referred to as RFM-5565 in this manual) is fast, flexible and easy to operate. Data is transferred by writing to memory (SDRAM), which appears to reside globally in all boards on the network. Onboard circuitry automatically performs the data transfer to all other nodes with little or no involvement of any host processor. A block diagram of the PCIE-5565PIORC is shown in Figure 1 on page 9.

Features

Features include:

- High speed, easy to use fiber-optic network (2.12 Gbaud serially)
- x4 lane PCI Express 1
- No host processor involvement in the operation of the network
- Selectable Redundant Mode of Operation
- Up to 256 nodes
- Connectivity with multimode fiber up to 300 m, singlemode fiber up to 10 km
- Dynamic packet size, 4 to 64 bytes of data per packet
- Fiber network transfer rate 43 MByte/s to 170 MByte/s
- 128/256 MBytes SDRAM Reflective Memory with selectable parity
- Independent Direct Memory Access (DMA) channel
- Four general purpose network interrupts; each with 32 bits of data
- Configurable endian conversion for multiple CPU architectures on the same network
- Selectable PCI PIO window size from 2 MByte to 64 MByte to full installed memory size
- Operating System support: Windows® 2000, Windows XP, Linux® and VxWorks®
- RoHS Compliant

PCI Express Compliance

The PCIE-5565PIORC complies with requirements of the PCI Express Specification, Revision 1.1.

Vendor and Device Identification

The PCI Configuration register reserved for the vendor ID has the value of $114A, which designates GE. The PCI Configuration register reserved for the device ID has the value of $5565, which is GE's board type.

Subsystem Vendor ID and Subsystem ID

The PCI Configuration register reserved for the subsystem vendor ID has the value of $1556, which designates PLD Applications. The PCI Configuration register reserved for the subsystem ID has the value of $0080, which is the PLD Applications PCI-X core identification number.

Block Diagram

Figure 1 Block Diagram of PCIE-5565PIORC

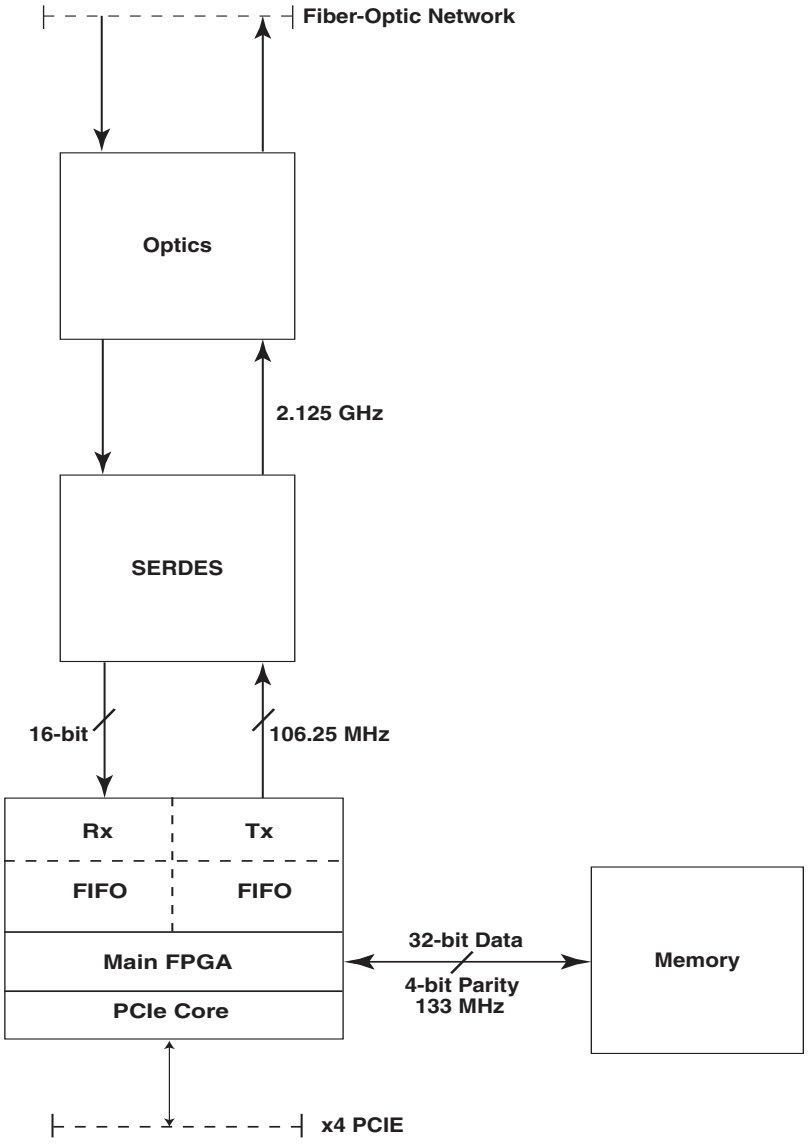
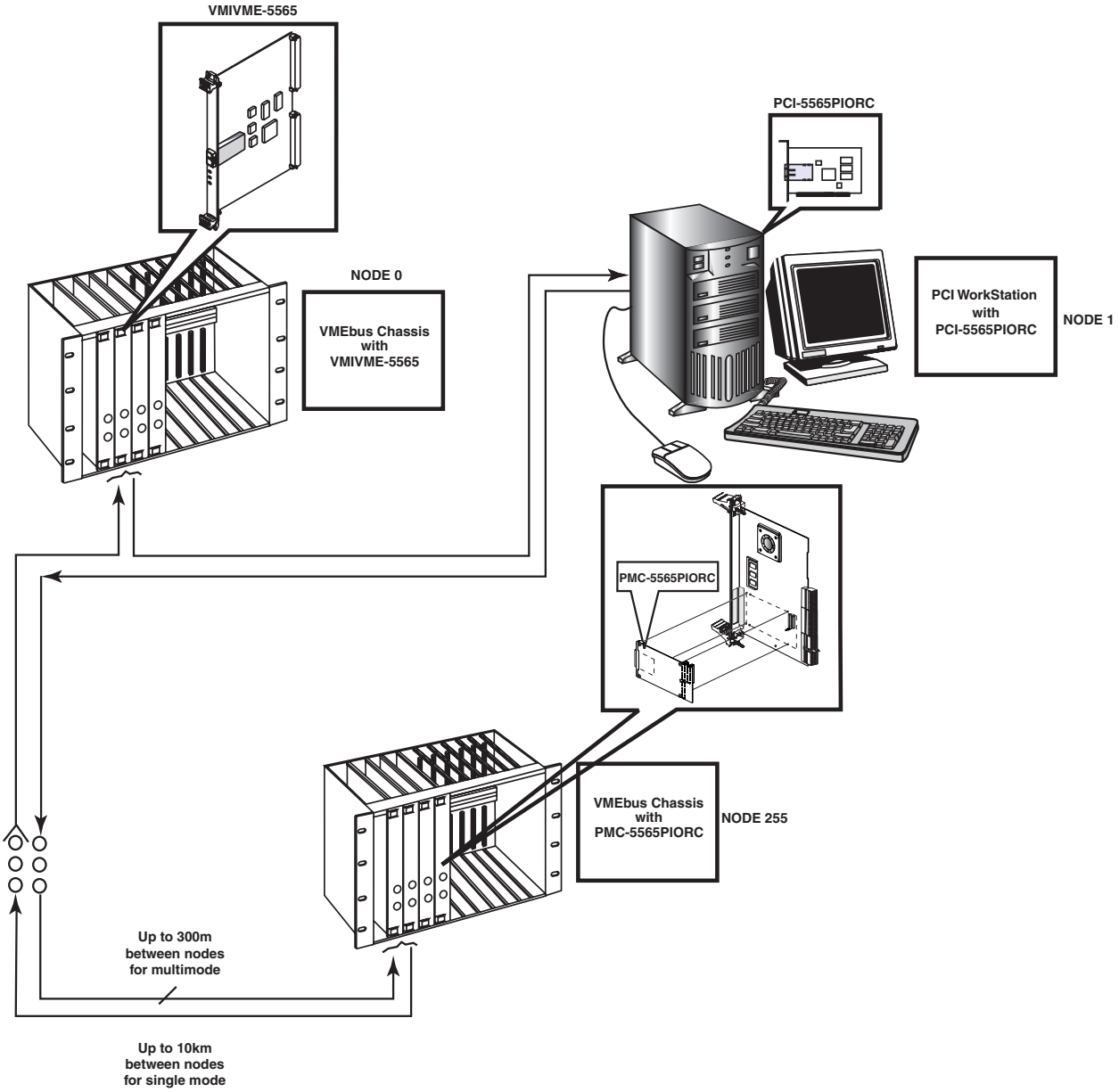


Figure 2 Typical Reflective Memory Network



References

PCI Express™ Card Electromechanical Specification Revision 1.1
March 28, 2005

PCI Express Base Specification, Revision 1.1
March 28, 2005

Organization

This manual is composed of the following chapters:

Overview provides a general description of the PCIE-5565PIORC, and General Safety terms and symbols.

Chapter 1 Handling and Installation describes unpacking and installation of the hardware.

Chapter 2 Theory of Operation describes the product's features and functionality.

Chapter 3 Programming describes PCI Configuration Registers and other registers for programming and installation.

Maintenance provides GE's contact information relative to the care and maintenance of the unit.

Compliance provides the applicable information regarding regulatory compliance.

Safety Summary

The following general safety precautions must be observed during all phases of the operation, service and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of the design, manufacture, and intended use of this product.

GE assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this system.
Use extreme caution when handling, testing and adjusting.

Warnings, Cautions and Notes

WARNING

WARNING denotes a hazard. It calls attention to a procedure, practice, or condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

CAUTION

CAUTION denotes a hazard. It calls attention to an operating procedure, practice, or condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE

NOTE denotes important information. It calls attention to a procedure, practice, or condition which is essential to highlight.

TIP

Tip denotes a bit of expert information.

LINK

This is link text.

1 • Handling and Installation

This chapter describes the installation and configuration of the board. Cable configuration and board layout are illustrated in this chapter.

1.1 Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Technical Support.

1.2 Handling Precaution

Some of the components assembled on GE's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high-energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material should be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

1.3 Switch S1 and S2 Configuration

Prior to installing the RFM-5565 in a host system, the desired node ID must be set using switch S2. Each node in the network must have a unique node ID. See Figure 1-1 on page 18 for the location of switch S2.

Switch S2 corresponds to 8 node ID select signal lines. The 8 node ID select lines permit any binary node ID from 0 to $FF (255 decimal). Switch S2 position 1 corresponds to the least significant node ID line and switch S2 position 8 corresponds to the most significant node ID line. Placing switch S2 in the **OFF** position sets the binary node ID line low (0), while placing switch S2 in the **ON** position sets the binary node ID line high (1). Table 1-1 on page 17 provides examples of possible node IDs.

1.3.1 Before Installation Switch S1 and S2 Configuration

NOTE

ALL nodes on the ring MUST be configured for the SAME transfer mode, either redundant or non-redundant transfer mode. A mismatch of this setting will result in certain packets being removed from the ring, and that data will be lost.

NOTE

No more than one node on the ring should be configured with Rogue Master 0 enabled. Certain packets will be removed from the ring when two or more nodes are configured with Rogue Master 0 enabled, and that data will be lost.

NOTE

No more than one node on the ring should be configured with Rogue Master 1 enabled. Certain packets will be removed from the ring when two or more nodes are configured with Rogue Master 1 enabled, and that data will be lost.

Prior to installing the RFM-5565 in the host system, switch S1 must be configured for the appropriate mode of operation. Switch S1 controls six functions on the board. Settings on Switch S1 should only be changed while power is off.

1. S1 position 1 selects the non-redundant (**OFF** position) or redundant network transfer modes.
2. S1 position 2 selects between the low network usage (**ON** position) of the classic 5565 boards or the higher performance achievable on this board (**OFF** position).
3. S1 positions 3 and 4 select the PCI window size for PIO memory accesses. The default (when both switch positions 3 and 4 are **OFF**) is to use the full installed memory size. The reduced memory window size choices are 64 MByte, 16 MByte or 2 MByte.
4. S1 position 5 enables (**ON** position) or disables the Rogue Master 0 function.
5. S1 position 6 enables (**ON** position) or disables the Rogue Master 1 function.
6. S1 position 8 selects between the factory default control logic (**ON** position) or the most recent control logic flashed to the board (**OFF** position).

S1 position 7 is currently reserved and should not be used (left in the **OFF** position).

NOTE

S1 position 8 should be set in the **ON** position only when a flash update of the control logic has failed. After a successful flash update of the control logic, S1 position 8 should be set in the **OFF** position.

Table 1-1 Example Node ID Switch S2 RFM-5565

S2 Position 8	S2 Position 7	S2 Position 6	S2 Position 5	S2 Position 4	S2 Position 3	S2 Position 2	S2 Position 1	Node ID Hex (Dec.)
ON	ON	ON	ON	ON	ON	ON	ON	$FF (255)
ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$80 (128)
OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	$40 (64)
OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	$20 (32)
OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	$10 (16)
OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	$8 (8)
OFF	OFF	OFF	OFF	OFF	ON	OFF	OFF	$4 (4)
OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF	$2 (2)
OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON	$1 (1)
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	$0 (0)

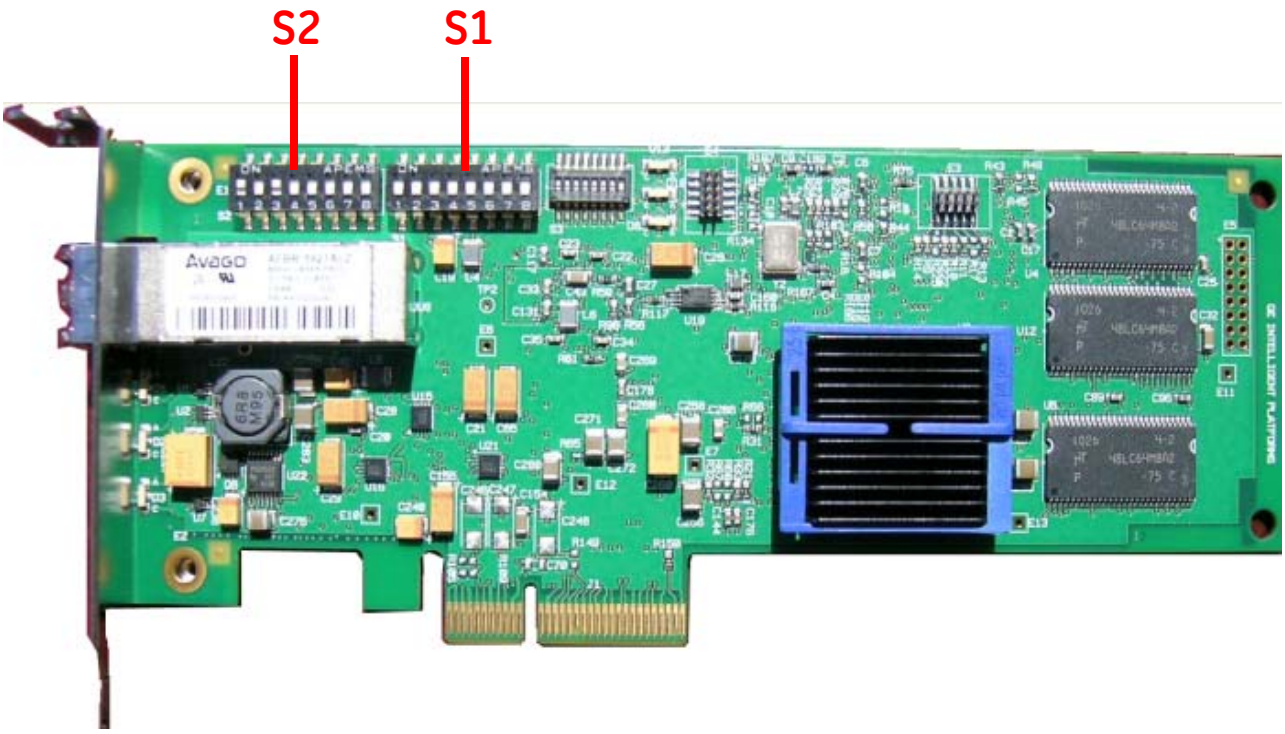
Factory Default: S2 positions 1 through 8 OFF

Table 1-2 Switch S1 Configuration RFM-5565

Position 1 OFF (non-redundant mode) Position 1 ON (redundant mode)	Position 2 OFF (higher performance achievable) Position 2 ON (low network usage)
Position 5 OFF (disables Rogue Master 0) Position 5 ON (enables Rogue Master 0)	Position 6 OFF (disables Rogue Master 1) Position 6 ON (enables Rogue Master 1)
Position 8 OFF (most recent control logic) Position 8 ON (original factory control logic)	**Factory Defaults** Positions 1-8 OFF

PCI Window Size	S1 Position 3	S1 Position 4
Default	Off	Off
64 MByte	On	Off
16 MByte	Off	On
2 MByte	On	On

Figure 1-1 S1 and S2 Location PCIE-5565PIORC



1.4 Physical Installation

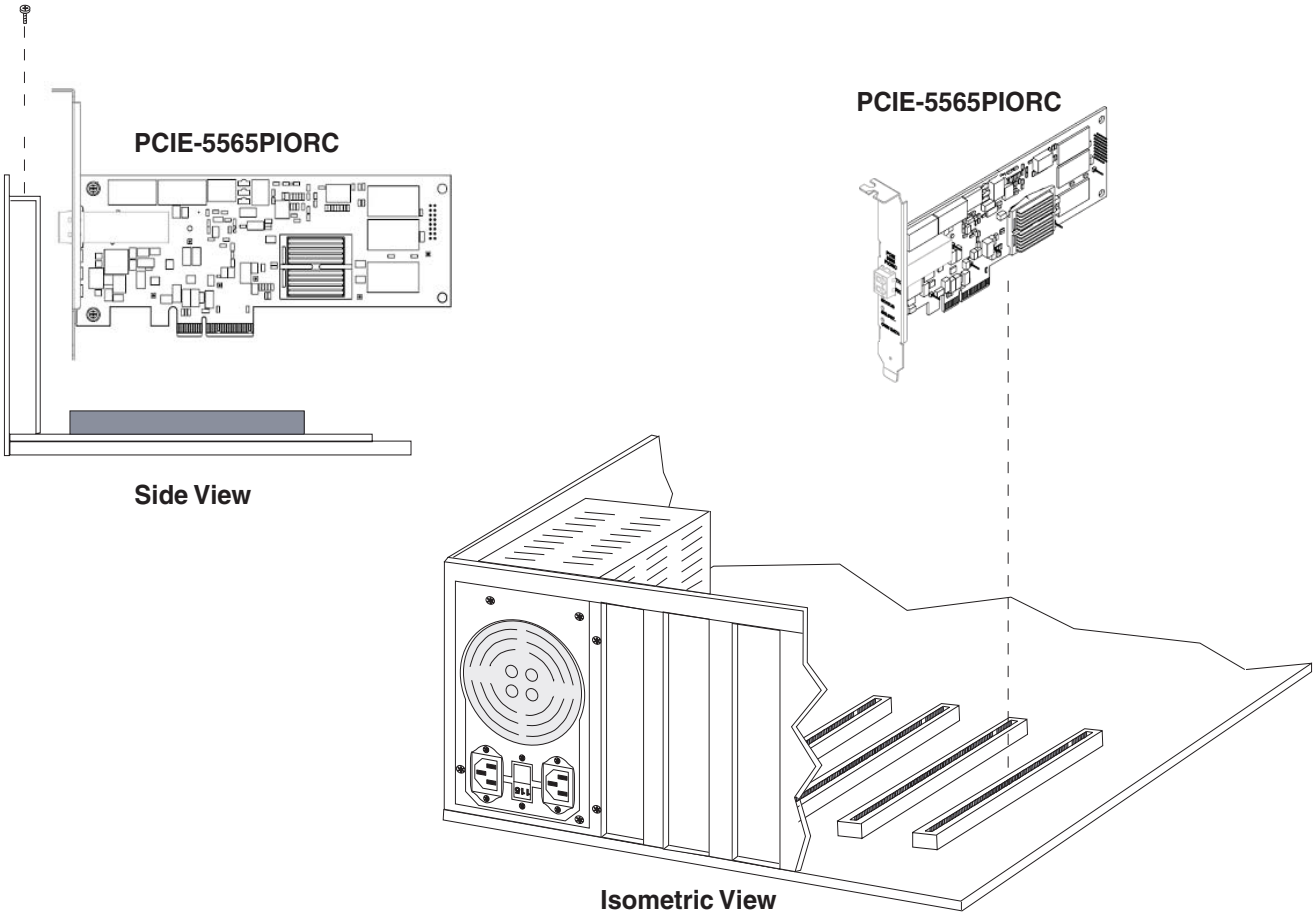
CAUTION

Do not install or remove the board while power is applied.

Host PCI Express compatible sites vary widely in appearance and board installation procedures. GE recommends examining the host system installation procedures prior to installing this board. The following procedure outlines the installation of the PCIE-5565PIORC onto a suitable motherboard with an available PCIe connector (x4, x8, or x16).

1. Open the system chassis. Ensure that the node ID has been set prior to installation. Also, setup the board for the desired mode of operation. See Section *Switch S1 and S2 Configuration* on page 16.
2. Install the PCIE-5565PIORC firmly into the PCIe connector (refer to Figure 1-2 on page 19 for installation of the PCIE-5565PIORC). Install the screw to secure the PCIE-5565PIORC to the chassis.
3. Close the system chassis, apply power.

Figure 1-2 Installing the PCIE-5565PIORC



This PCIE-5565PIORC comes in two physical form factors: low profile and standard height.

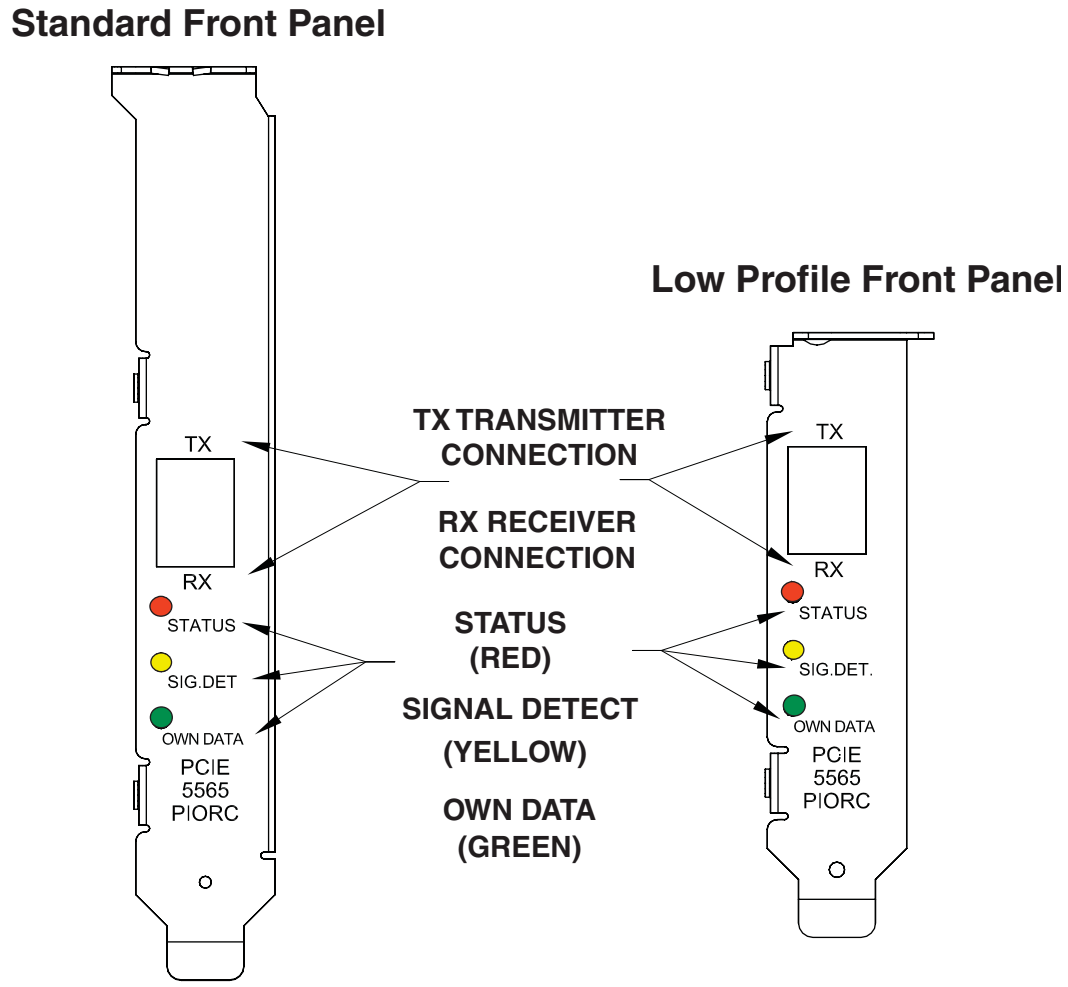
NOTE

The PCIE-5565PIORC is designed to interface with any suitable PCIe compliant motherboard using a direct PCIe x4 lane interface, or larger; compliant with Revision 1.1 of the PCI Express Specification.

1.5 Front Panel Description

The PCIE-5565PIORC has an optical transceiver and three LEDs located on the front panel illustrated in the figure below. Table 1-3 on page 21 outlines the front panel's LEDs. The port labeled "RX" is the receiver and the port labeled "TX" is the transmitter. The PCIE-5565PIORC uses "LC" type fiber-optic cables.

Figure 1-3 Low Profile and Standard Front Panels of the PCIE-5565PIORC



CAUTION

When fiber-optic cables are not connected, the supplied dust caps need to be installed to keep dust and dirt out of the optics. Do not power up the PCIE-5565PIORC without the fiber-optic cables installed. This could cause eye injuries.

1.5.1 LED Description

Table 1-3 LED Descriptions

LED	Color	Description
Status	Red	User defined board status indicator.
SIG. DET.	Yellow	Indicates optical network connection.
Own Data	Green	Indicates when own data is received.

The status LED's power up default state is **ON**. The status LED is a user defined board indicator and can be toggled **ON** or **OFF** by writing to Bit 31 of the Control and Status register. The signal detect LED turns **ON** if the receiver detects light and can be used as a simple method of checking that the optical network is properly connected to the receiver. The Own Data LED is turned **ON** when the board detects its own data returning over the network. The default setting is **OFF**.

1.6 Cable Configuration

The RFM-5565 is available with a multimode or singlemode fiber-optic interface. Figure 1-4 on page 22 is an illustration of the "LC" type multimode or singlemode fiber-optic connector.

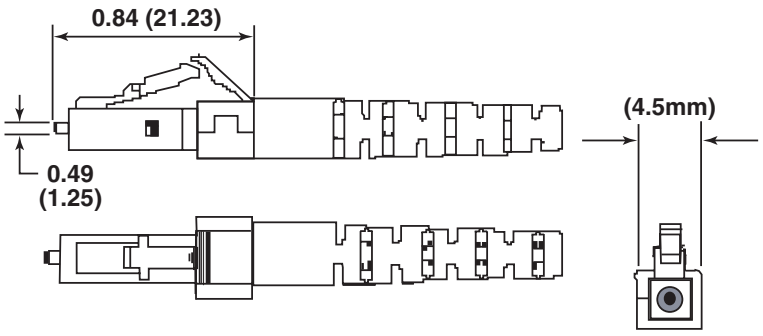
Table 1-4 Cable Specifications for Multimode and Singlemode

Specification	Singlemode	Multimode
Core Diameter	8.3 ± 1.0 µM	50/62.5 ±3 µM
Cladding Diameter	125 ±2 µM	125 ±2 µM
Jacket Outer Diameter	3.0 mm ±.1 mm	3.0 mm ±.1 mm
Attenuation	0.8 dB/Km (max) at 1310 nm	4.0 dB/Km (max) at 850 nm
Bandwidth	N/A	160 to 300 MHz-Km (min) at 850 nm
UL	type OFNR, CSA type OFN FT4	type OFNR, CSA type OFN FT4

1.6.1 Connector Specification (Singlemode and Multimode):

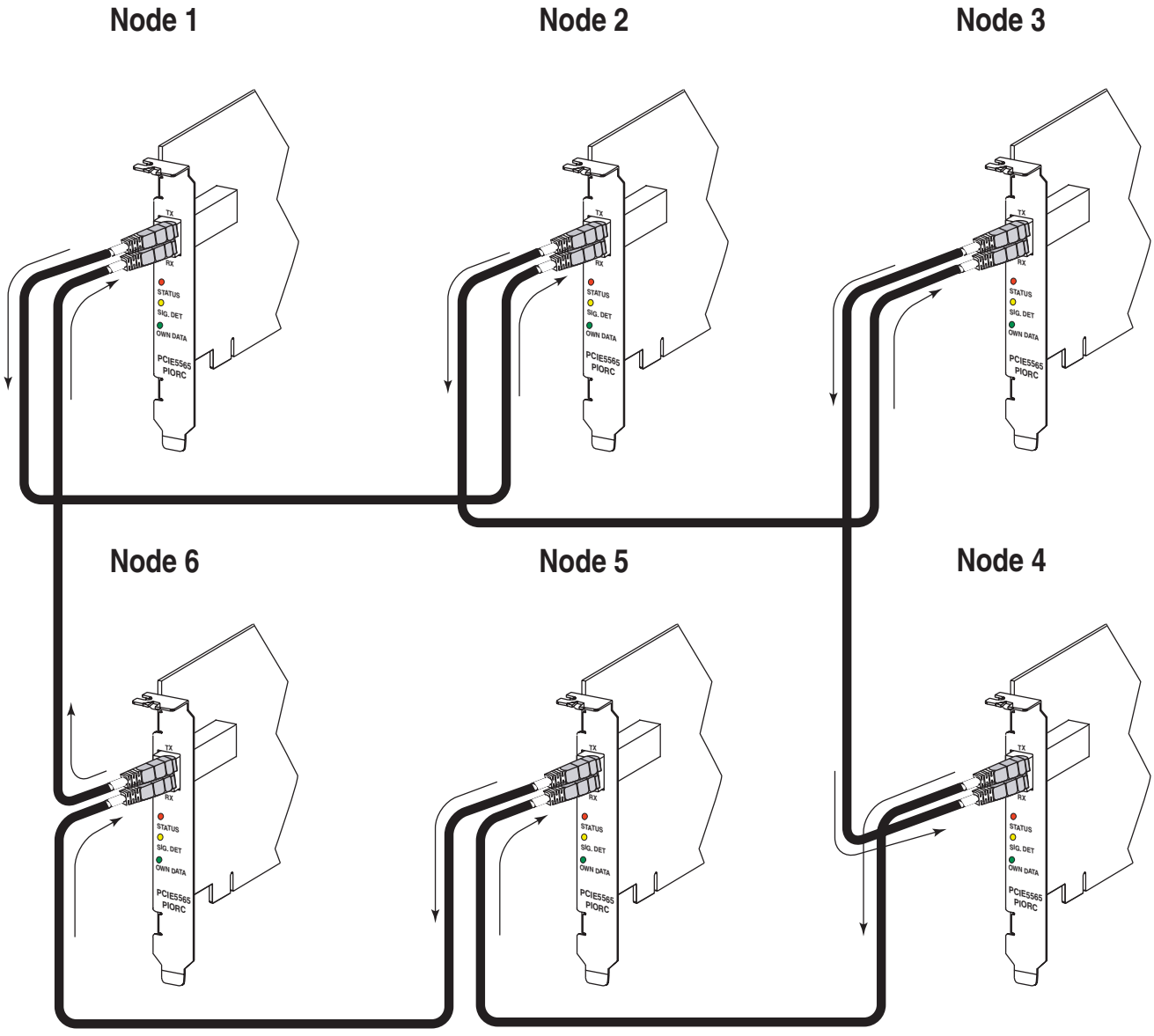
- Compatible with LC standard and JIS C 5973 compliant
- Ceramic ferrule
- Temperature range: -20° C to +85° C

Figure 1-4 LC Type Fiber-Optic Cable Connector



Dimensions: inches (mm)

Figure 1-5 Example: Six Node Ring Connectivity PCIE-5565PIORC



2 • Theory of Operation

The following sections describe the functionality of the RFM-5565 Reflective Memory board. A description of the major sub-circuits and their operation is included. This section will also occasionally mention Control and Status registers related to operations. To see a detailed description of these Control and Status registers please refer to Chapter 3, *Programming,* on page 29 of this manual.

2.1 Basic Operation

Each RFM-5565 node (any 5565 Reflective Memory board) in the network is interconnected using fiber-optic cables in a daisy chain loop. The transmitter of the first board must be connected to the receiver of the second board. The transmitter of the second board is connected to the receiver of the third, and so on, until the loop is completed back at the receiver of the first board. Alternatively, any node can be connected to the ring network using one or more ACC-5595* Reflective Memory Hubs. It is important that the ring network be complete (i.e., every receiver and transmitter must be connected). The RFM-5565 will not transmit packets if the receiver does not detect a signal or it has lost synchronization (e.g., the cable is damaged). Each node must have a unique node ID, which is set using switch S2 (i.e. no two nodes should have the same node ID). The order of the node IDs is unimportant.

A transfer of data over the network is initiated by a write to onboard SDRAM from the host system. The write can be as simple as a PIO target write, or it can be due to a DMA cycle by the resident DMA engine.

While the write to the SDRAM is occurring, circuitry on the RFM-5565 automatically writes the data and other pertinent information into the transmit FIFO. From the transmit FIFO, the transmit circuit retrieves the data and puts it into a variable length packet of 4 to 64 bytes that is transmitted over the fiber-optic interface to the receiver of the next board.

The receiver then checks the packet for errors. When the error free data is received, the receive circuit opens the packet and stores the data in the board's receive FIFO. From the receive FIFO, another circuit writes the data into the local onboard SDRAM at the same relative location in memory as the originating node. This circuit also simultaneously routes the data into the board's own transmit FIFO. From there, the process is repeated until the data returns to the receiver of the originating node. At the originating node, the data packet is removed from the network.

2.2 Front Bezel LED Indicators

The RFM-5565 has three LED indicators located on the bezel. The top red LED is a status indicator; its power up default state is **ON**. The status LED may be toggled **OFF** or **ON** by writing to Bit 31 of the LCSR1 register, which indicates a user defined board status. The middle yellow LED is the signal detect indicator. The signal detect LED turns **ON** if the receiver detects light. It can be used as a simple method of checking that the optical network is properly connected to the receiver. The bottom green LED is the OWN DATA indicator. When a board detects its own data returning on the network, it turns this LED **ON**.

2.3 RFM-5565 Register Sets

To go beyond the simple target read and write operation of the board, the user must understand and manipulate bits within three register sets. The three register sets are referred to as:

- PCI Configuration Registers
- Local Configuration Registers
- RFM Control and Status Registers

PCI Configuration Registers – This set of registers is predefined by the PCI Local Bus Specification and is standard for all PCI and PCI Express devices. This register set contains the Vendor ID, Device ID, Subsystem Vendor ID and Base Address registers. The PCI Configuration Registers are first initialized and then modified as needed by the PCI bus system BIOS. The register set is rarely altered by the user, but the ability to read these registers, particularly the Base Address Registers, will be necessary to locate the other two sets of registers.

Local Configuration Registers – Base Address Register 0 has the starting address for register memory space accesses and Base Address Register 1 has the starting address for register IO space accesses. Some Local Configuration Registers pertinent to the RFM-5565's operation include the Interrupt Control and Status Register (INTCSR) and the DMA Control Registers.

RFM Control and Status Registers – The RFM Control and Status Registers implement the functions unique to the RFM-5565 Reflective Memory board. These functions include RFM operation status, detailed control of the RFM sources for the PCI interrupt, and network interrupt access. These registers are accessed at locations offset from the address contained in Base Address Register 2.

2.4 Reflective Memory RAM

This board is available with 128 or 256 MByte of onboard Reflective Memory SDRAM. The SDRAM starts at the location specified in Base Address Register 3. Unlike the previous versions of Reflective Memory products, the RFM Control and Status Registers do NOT replace the first $40 locations of RAM. The offset address range is $0 to $7FFFFFF for the 128 MByte and $0 to $FFFFFFF for the 256 MByte option.

2.5 Interrupt Circuits

The RFM-5565 has a single interrupt output (INTA#). One or more events on the RFM-5565 board can cause the interrupt. The sources of the interrupt can be individually enabled and monitored through several registers.

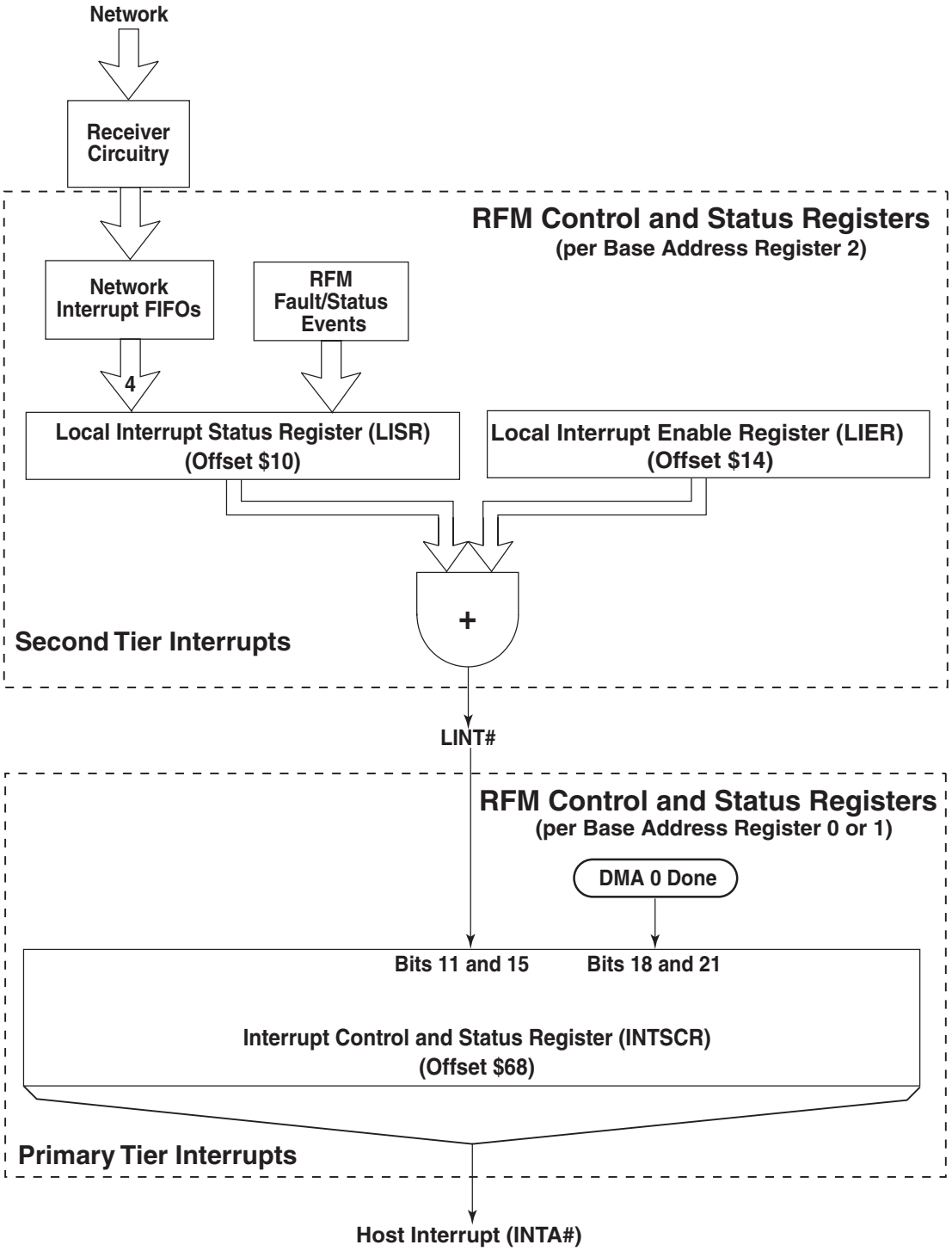
The interrupt circuitry of the RFM-5565 is arranged in two tiers. The primary tier of interrupts is enabled and monitored by the Local Configuration Register's INTCSR at offset $68. The sources for monitoring the primary tier interrupts include:

1. DMA Ch 0 Done
2. Local Interrupt Input (LINTi#)

The primary tier interrupt source (1) is used during DMA cycles and must be configured in the DMA registers.

The other primary tier interrupt source (2) is the Local Interrupt Input (LINTi#). All secondary tier interrupts are funneled through the LINTi#. Second tier interrupts include several operational status bits, faults, and network interrupts. The second tier interrupts are selected and monitored through the two RFM Control and Status Registers referred to as the Local Interrupt Status Register (LISR) and the Local Interrupt Enable Register (LIER). For a detailed description of these two registers refer to Chapter 3, *Programming,* on page 29. A block diagram of the main interrupt circuitry is shown in Figure 2-1 on page 26 .

Figure 2-1 Interrupt Circuitry Block Diagram



2.6 Network Interrupts

The RFM-5565 is capable of passing interrupt packets, as well as data packets, over the network. The network interrupt packets can be directed to a specific node or broadcast globally to all other nodes on the network. Each network interrupt packet contains the sender's node ID, the destination node ID, the interrupt type and 32 bits of user defined data.

The types of network interrupts include four general purpose interrupts and a reset node request interrupt. Node specific interrupts are sent by configuring three RFM Control and Status registers. Each receiving node evaluates the interrupt packets as they pass through. If a general purpose interrupt is directed to that node, then the sender's node ID is stored in the appropriate Sender ID FIFO (one of four). Each Sender ID FIFO is 127 locations deep. The accompanying data will be stored in a companion 127 locations deep data FIFO.

If enabled through the LISR, LIER and INTCSR registers, any of the network interrupts can also generate a host PCI interrupt at each receiving node.

The reset node request interrupt is not stored in a FIFO like the four general purpose interrupts. Furthermore, it does not cause an immediate reset of the board. Instead, it sets a bit in the LISR register, which will result in a PCI interrupt if enabled. The actual board reset should be performed by the host system in an orderly fashion. However, the user application could use this network interrupt for any purpose.

2.7 Redundant Transfer Mode of Operation

The RFM-5565 is capable of operating in a redundant transfer mode. The board is configured for redundant mode when switch S1 position 1 is in the **ON** position. In the redundant transfer mode, each packet transfers twice, regardless of the packet size. The receiving circuitry of each node on the network evaluates each of the redundant transfers. If no errors are detected in the first transfer, it is used to update the onboard memory and the second transfer is discarded. However, if the first transfer contains an error, the second transfer is used to update the onboard memory provided it has no transmission errors. If errors are detected in both transfers, the transfers will not be used and the data is completely removed from the network.

Redundant transfer mode reduces the chance that any data is dropped from the network. However, the redundant transfer mode also reduces the network data transfer rate. The single Dword (Double-word = 4 bytes) transfer rate drops from the non-redundant rate of 43 MByte/s to approximately 20 MByte/s. The 16 Dword (64 byte) transfer rate drops from the non-redundant rate of 170 MByte/s to the redundant rate of 85 MByte/s.

2.8 Rogue Packet Removal Operation

A rogue packet is a packet that does not belong to any node on the network. Recalling the basic operation of Reflective Memory, one node originates a packet on the network in response to a memory write from the host. The packet is transferred around the network to all nodes until it returns to the originating node. It is a requirement that the originating node remove the packet from the network. If, however, the packet is erroneously altered as it passes through another node, or if the originating node begins to malfunction, then the originating node may fail to recognize the packet as its own and will not remove it from the network. In this case, the packet will continue to traverse the network as a "rogue packet."

Rogue packets are extremely rare. A rogue packet could be created when turning a node's power on or off while connected to a 5595 Hub. It could also occur when connecting or disconnecting fiber cables. A rogue packet might be created if any node in the network overflows a network FIFO. Their existence could indicate a malfunctioning board due to true component failure, or due to operation in an overly harsh environment. Normally, the solution is to isolate and replace the malfunctioning board and/or improve the environment. However, some users prefer to tolerate sporadic rogue packets rather than halt the system for maintenance provided the rogue packets are removed from the network.

To provide tolerance for rogue packet faults, the RFM-5565 contains circuitry that allows it to operate as one of two Rogue Masters. A rogue master marks each packet as it passes through from another node. If the same packet returns to the rogue master a second time, the Rogue Master recognizes that it is a rogue packet and removes it from the network (after the rogue packet has affected every node). When a rogue packet is detected, a rogue packet fault flag is set in the LISR. The assertion of the rogue packet fault bit may optionally assert a PCI interrupt to inform the host that the condition exists.

Two rogue masters, Rogue Master 0 and Rogue Master 1, are provided to cross check each other. Rogue Master 0 is enabled by placing switch S1 position 5 in the **ON** position. Rogue Master 1 is enabled by placing switch S1 position 6 in the **ON** position. Just as two boards in a network should not have the same node ID, two boards in the same network should not be set as the same Rogue Master. Otherwise, one of the two will erroneously remove packets marked by the other.

3 • Programming

Basic target write and read operations of the RFM-5565 require little or no software. The board powers up in a functional mode. The user will need to access the PCI Configuration registers (Base Address Register 0, 1, 2 and 3) to learn where the system BIOS has located the other register sets and the Reflective Memory.

The location of the register sets and the Reflective Memory varies from system to system, and can even vary from slot to slot within a system. For operations beyond the basic setup, such as enabling or disabling interrupts or performing DMA cycles, the user must know the specific bit assignments of the registers within the three register sets. That information is provided in this chapter.

The three register sets are:

- PCI Configuration Registers
- Local Configuration Registers
- RFM Control and Status Registers

3.1 PCI Configuration Registers

The PCI Configuration registers are located in 256 bytes of the PCI Configuration Space, which follows a template defined by the PCI Specification v2.2. The first 64 bytes of the PCI Configuration Space are composed of a fully predefined header. Within that header region, each device implements only the necessary and relevant registers. However, all registers and bit functions within the header region, that are present, must comply with the definitions of the PCI Specification. Beyond the first 64 byte boundary, each device can implement additional device unique registers. Although the PCI Configuration registers are accessible at all times, they are rarely altered by the user.

Table 3-1 PCI Configuration Registers

Address (Hex)	31..24	23..16	15..8	7..0
00	Device ID		Vendor ID	
04	Status Register		Command Register	
08	Class Code			Revision ID
0C	BIST	Header Type	Latency Timer	Cache Line Size
10	Base Address Register 0			
14	Base Address Register 1			
18	Base Address Register 2			
1C	Base Address Register 3			
20	Base Address Register 4			
24	Base Address Register 5			
28	Cardbus CIS Pointer			
2C	Subsystem Device ID		Subsystem Vendor ID	
30	Expansion ROM Base Address			
34	**Reserved**			CAP. Pointer
38	**Reserved**			
3C	0x00	0x00	Interrupt Pin	Interrupt Line
50..5C	MSI Capability Structure			
78..7C	Power Management Capability Structure			
80..90	PCIe Capability Structure			

NOTE

All registers can be accessed as either Byte, Word or Double-word request.

Table 3-2 PCI Configuration ID Registers

PCI Configuration ID: Offset $00				
Bit	Description	Read	Write	Value after PCI Reset
15:0	**Vendor ID**. Identifies manufacturer of device.	Yes	No	$114A
31:16	**Device ID.** Identifies particular device.	Yes	No	$5565

Table 3-3 PCI Command Register

PCI Command: Offset $04				
Bit	Description	Read	Write	*Value after PCI Reset
0	**I/O Space.** Writing a one (1) allows the device to respond to I/O Space accesses. Writing a zero (0) disables the device from responding to I/O Space accesses.	Yes	Yes	0
1	**Memory Space**. Writing a one (1) allows device to respond to Memory Space accesses. Writing a zero (0) disables the device from responding to Memory Space accesses.	Yes	Yes	0
2	**Master Enable.** Writing a one (1) allows the device to behave as a bus master. Writing a zero (0) disables the device from generating bus master accesses.	Yes	Yes	0
3	**Special Cycle.** Not Supported	Yes	No	0
4	**Reserved**	N/A	N/A	0
5	**VGA Palette Snoop**. Not Supported	Yes	No	0
6	**Parity Error Response.** Writing a zero (0) indicates parity error is ignored and the operation continues. Writing a one (1) indicates parity checking is enabled.	Yes	Yes	0
7	**Wait Cycle Control.** Controls whether a device does address/data stepping. A zero (0) indicates the device never does stepping. A one (1) indicates the device always does stepping. (NOTE: Hardwired to zero (0).)	Yes	No	0
8	**SERR# Enable.** Writing a one (1) enables SERR# driver. Writing a zero (0) disables SERR# driver.	Yes	Yes	0
9	**Reserved**	N/A	N/A	0
10	**Interrupt Disable:** When set (1), this bit disables the Reflective Memory from asserting its interrupt pin. When not set (0), interrupts are generated normally.	Yes	Yes	0
15:11	**Reserved**	Yes	No	$0

*__NOTE__: This register will be altered by the system BIOS during the system boot process (e.g., $0107).

Table 3-4 PCI Status Register

PCI Status: Offset $06				
Bit	Description	Read	Write	Value after PCI Reset
2:0	**Reserved**	Yes	No	$0
3	**Interrupt Status.** Set by the Reflective Memory when the function would normally assert an interrupt pin, regardless of interrupt disable bit state.	Yes	No	0
4	**New Capabilities Functions Support.** Hardwired to a one (1). The Reflective Memory implements a capabilities list.	Yes	No	1
5	**66 MHz Capable.** Not applicable to PCI Express.	Yes	No	0
6	**User Definable Functions.** If set to one (1), this device supports user definable functions. Read-only from the PCI bus.	Yes	No	0
7	**Fast Back-to-Back Capable.** Not applicable to PCI Express.	Yes	No	0
8	**Master Data Parity Error Detected.** Set by the Reflective Memory acting as a master when it detects a poisoned completion, if parity error response bit is set.	Yes	Yes/Clr	0
10:9	**DEVSEL# Timing.** Not applicable to PCI Express.	Yes	No	0
11	**Target Abort.** When set to one (1), indicates the Reflective Memory has signaled a Completer Abort. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
12	**Received Target Abort.** When set to one (1), indicates the Reflective Memory has received a Completer Abort. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
13	**Received Master Abort.** When set to one (1), indicates the Reflective Memory has received a Unsupported Request Completion Status. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
14	**Signal System Error.** When set to one (1), indicates the Reflective Memory has sent an ERR_FATAL or ERR_NONFATAL message. Writing a one (1) clears this bit to zero (0).	Yes	Yes/Clr	0
15	**Detected Parity Error.** When set to one (1), indicates the Reflective Memory has detected a poisoned completion, even if parity error handling is disabled (the Parity Error Response bit in the Command register is clear). Writing a one (1) clears this bit to zero (0)	Yes	Yes/Clr	0

Table 3-5 PCI Revision ID Register

PCI Revision ID: Offset $08				
Bit	Description	Read	Write	Value after PCI Reset
7:0	**Revision ID.** Revision of board	Yes	No	Current Rev#

Table 3-6 PCI Class Code Register

PCI Class Code: Offset $09				
Bit	Description	Read	Write	Value after PCI Reset
7:0	**Register Level Programming Interface.** None defined.	Yes	No	$0
15:8	**Subclass Code**	Yes	No	$80
23:16	**Base Class Code**	Yes	No	$02
Base Class Code of $02 equals Network Controller. Subclass Code of $80 equals other network controller.				

Table 3-7 PCI Cache Line Size Register

PCI Cache Line Size: Offset $0C				
Bit	Description	Read	Write	*Value after PCI Reset
7:0	**System Cache Line Size.** Not applicable to PCI Express.	Yes	Yes	$0
***NOTE:** This register can be altered by the system BIOS during the system boot process.				

Table 3-8 PCI Latency Timer Register

PCI Latency Timer: Offset $0D				
Bit	Description	Read	Write	*Value after PCI Reset
7:0	**PCI Bus Latency Timer**. Not applicable to PCI Express.	Yes	Yes	$00
***NOTE:** This register can be altered by the system BIOS during the system boot process.				

Table 3-9 PCI Header Type Register

PCI Header Type: Offset $0E				
Bit	Description	Read	Write	Value after PCI Reset
6:0	**Configuration Layout Type.** Specifies layout of bits $10 through $3F in Configuration Space. Only one encoding, $0, is defined. All other encodings are reserved.	Yes	No	$0
7	**Header Type.** Writing a one (1) indicates multiple functions. Writing a zero (0) indicates single function.	Yes	No	0

Table 3-10 PCI Built-in Self Test Register

PCI Built-in Self Test: Offset $0F				
Bit	Description	Read	Write	Value after PCI Reset
3:0	**BIST Pass/Failed**. Writing $0 indicates a device passed its test. Non-$0 values indicate a device failed its test. Device-specific failure codes can be encoded in a non-$0 value.	Yes	No	$0
5:4	**Reserved**.	Yes	No	00
6	**PCI BIST Interrupt Enable**. The PCI bus writes a one (1) to enable BIST, which generates an interrupt to the Local bus. The Local bus resets this bit when BIST is complete. The software should fail device if BIST is not complete after two seconds. Refer to the Runtime registers for interrupt Control and Status.	Yes	Yes	0
7	**BIST Support**. Returns a one (1) if device supports BIST. Returns a zero (0) if device is not BIST-compatible.	Yes	No	0

PCI Base Address Register 0 contains the starting address for memory mapped accesses to the Local Configuration Registers, which include the interrupt Control and Status and the DMA Registers. The value in this register is loaded by the system BIOS.

Table 3-11 PCI Base Address Register 0 for Access to Local Configuration Registers

PCIBAR0: Offset $10				
Bit	Description	Read	Write	*Value after PCI Reset
0	**Memory Space Indicator**. Writing zero (0) indicates the register maps into Memory Space. Writing a one (1) indicates the register maps into I/O Space. (**NOTE**: Hardcoded to zero (0).)	Yes	No	0
2:1	**Register Location.** Values: 00 - Locate anywhere in 32-bit Memory Address Space. 01 - Locate below 1 MByte Memory Address Space. 10 - Locate anywhere in 64-bit Memory Address Space. 11 - Reserved (**NOTE**: Hardcoded to 00.)	Yes	No	00
3	**Prefetchable**. Writing a one (1) indicates there are no side effects on reads. (**NOTE**: Hardcoded to zero (0).)	Yes	No	0
8:4	**Memory Base Address**. Memory Base Address for access to Local Configuration registers (requires 512 bytes). (**NOTE**: Hardcoded to $0.)	Yes	No	$0
31:9	**Memory Base Address**. Memory Base Address for access to Local Configuration registers.	Yes	Yes	$0

***NOTE:** This register will be altered by the system BIOS during the system boot process.

PCI Base Address Register 1 contains the starting address for I/O mapped accesses to Local Configuration Registers. The value in this register is loaded by the system BIOS.

Table 3-12 PCI Base Address Register 1 for Access to Local Configuration Registers

PCIBAR1: Offset $14				
Bit	Description	Read	Write	*Value after PCI Reset
0	**Memory Space Indicator**. A zero (0) indicates the register maps into Memory Space. A one (1) indicates the register maps into I/O Space. (**NOTE**: Hardcoded to one (1).)	Yes	No	1
1	**Reserved**.	Yes	No	0
7:2	**I/O Base Address**. Base Address for I/O access to Local Configuration registers (requires 256 bytes). (**NOTE**: Hardcoded to $0.)	Yes	No	$0
31:8	**I/O Base Address**. I/O Base Address for access to Local Configuration registers.	Yes	Yes	$0

*__NOTE__: This register will be altered by the system BIOS during the system boot process. I/O Accesses not supported.

PCI Base Address Register 2 contains the starting address for memory mapped accesses to the RFM Control and Status Registers. The value in this register is loaded by the system BIOS.

Table 3-13 PCI Base Address Register 2 for Access to RFM Control and Status Registers

PCIBAR2: Offset $18				
Bit	Description	Read	Write	*Value after PCI Reset
0	**Memory Space Indicator**. A zero (0) indicates the register maps into Memory Space. A one (1) indicates the register maps into I/O Space.	Yes	No	0
2:1	**Register Location**. Values: 00 - Locate anywhere in 32-bit Memory Address Space. 01 - Locate below 1 MByte Memory Address Space. 10 - Locate anywhere in 64-bit Memory Address Space. 11 - Reserved If I/O Space, Bit 1 is always 0 and Bit 2 is included in the base address.	Yes	Mem: No I/O: Bit 1 no, Bit 2 yes	00
3	**Prefetchable** (If Memory Space). A one (1) indicates there are no side effects on reads. If I/O Space, Bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
7:4	Memory Base Address bits hardwired to zero for 256 bytes.	Yes	No	0000
31:8	**Memory Base Address**. Memory Base Address for access to RFM registers.	Yes	Yes	$0

*__NOTE__: This register will be altered by the system BIOS during the system boot process.

PCI Base Address Register 3 contains the starting address for PIO memory mapped accesses to the Reflective Memory RAM. The value in this register is loaded by the system BIOS. It depends on both the amount of installed SDRAM and the settings of S1 switch positions 3 and 4. The address offset range is:

$0 to $01FFFFF for the 2 MByte window setting,
$0 to $0FFFFFF for the 16 MByte window setting,
$0 to $3FFFFFF for the 64 MByte window setting,
$0 to $7FFFFFF for the 128 MByte SDRAM option, and
$0 to $FFFFFFF for the 256 MByte option.

Table 3-14 PCI Base Address Register 3 for Access to Reflective Memory

PCIBAR3: Offset $1C				
Bit	Description	Read	Write	*Value after PCI Reset
0	**Memory Space Indicator**. Writing zero (0) indicates the register maps into Memory Space. Writing a one (1) indicates the register maps into I/O Space.	Yes	No	0
2:1	**Register Location**. Values: 00 - Locate anywhere in 32-bit Memory Address Space. 01 - Locate below 1 MByte Memory Address Space. 10 - Locate anywhere in 64-bit Memory Address Space. 11 - Reserved If I/O Space, Bit 1 is always 0 and Bit 2 is included in the base address.	Yes	Mem: No I/O Bit 1 no, Bit 2 yes	00
3	**Prefetchable** (If Memory Space). Writing a one (1) indicates there are no side effects on reads. Does not affect operation of the Reflective Memory. The associated Bus Region Descriptor register controls prefetching functions of this address space. If I/O Space, Bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	**Memory Base Address**. Memory Base Address for access to SDRAM.	Yes	Yes	$0

*__NOTE__: This register will be altered by the system BIOS during the system boot process.

Table 3-15 PCI Base Address Register 4

PCIBAR4: Offset $20				
Bit	Description	Read	Write	Value after PCI Reset
31:0	**Reserved**.	Yes	No	$0

Table 3-16 PCI Base Address Register 5

PCIBAR5: Offset $24				
Bit	Description	Read	Write	Value after PCI Reset
31:0	**Reserved**.	Yes	No	$0

Table 3-17 PCI Cardbus CIS Pointer Register

PCI Cardbus CIS Pointer: Offset $28				
Bit	Description	Read	Write	Value after PCI Reset
31:0	**Cardbus Information Structure Pointer for PCMCIA**. Not Supported.	Yes	No	$0

Table 3-18 PCI Subsystem Vendor ID Register

PCI Subsystem Vendor ID: Offset $2C				
Bit	Description	Read	Write	*Value after PCI Reset
15:0	Subsystem Vendor ID (unique add-in board Vendor ID).	Yes	No	$1556
*__NOTE__: The value $1556 denotes a PLD Application.				

Table 3-19 PCI Subsystem ID Register

PCI Subsystem ID: Offset $2E				
Bit	Description	Read	Write	*Value after PCI Reset
15:0	Subsystem ID (unique add-in board device ID).	Yes	No	$0080
*__NOTE__: The value $0080 denotes a PLD Application PCI-X core.				

Table 3-20 PCI Expansion ROM Base Register

PCI Expansion ROM Base: Offset $30				
Bit	Description	Read	Write	*Value after PCI Reset
0	**Address Decode Enable.** A one (1) indicates a device accepts accesses to the Expansion ROM address. A zero (0) indicates a device does not accept accesses to Expansion ROM space. Should be set to zero (0) if there is no Expansion ROM. Works in conjunction with EROMRR[0].	Yes	No	0
10:1	**Reserved**	Yes	No	$0
31:11	Expansion ROM Base Address (upper 21 bits).	Yes	Yes	$0
*__NOTE__: PCI Expansion ROM and related registers are not applicable to the Reflective Memory.				

Table 3-21 PCI Capability Pointer Register

Capability Pointer: Offset $34				
Bit	Description	Read	Write	Value after PCI Reset
7:0	**New Capability Pointer.** Offset into PCI Configuration Space for the location of the first item in the New Capabilities Linked List.	Yes	No	$78
31:8	**Reserved**	Yes	No	$0

Table 3-22 PCI Interrupt Line

PCI Interrupt Line: PCIILR, Offset $3C				
Bit	Description	Read	Write	*Value after PCI Reset
7:0	**Interrupt Line Routing Value.** Value indicates which input of the system interrupt controller(s) is connected to each interrupt line of the device.	Yes	Yes	$0

***NOTE:** This register will be altered by the system BIOS during the system boot process.

Table 3-23 PCI Interrupt Pin

PCI Interrupt Pin: PCIIPR, Offset $3D				
Bit	Description	Read	Write	Value after PCI Reset
7:0	**Interrupt Pin Register.** Indicates which interrupt pin the device uses. The following values are decoded (the Reflective Memory supports only INTA#). 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD#	Yes	No	$1

Table 3-24 MSI Capability Structure

Offset	31::16	15:8	7:0
0x050	Message Control	0x78 (next cap ptr)	0x05 (capability ID)
0x054	Message Address		
0x058	Message Upper Address		
0x05C	Reserved		Message Data

Table 3-25 Message Control bit definition

Message Control bit definition: Offset 0x050			
Bit(s)	Field	Description	R/W
15:9	Reserved		R/W
8	Mask Capability	Not Supported. Hardwired to 0	R
7	64-bit Address Capability	Not Supported. Hardwired to 0	R
6:4	Multiple Message Enable	Indicates the number of MSI signals allocated by system software. - 000: 1MSI allocated - 001: 2 MSI allocated - 010: 4 MSI allocated - 011: 8 MSI allocated - 100: 16 MSI allocated - 101: 32 MSI allocated - 110: Reserved - 111: Reserved	R/W
3:1	Multiple Message Capable	Indicates the number of requested MSI messages - 010:4 MSI allocated	R
0	MSI Enable	1= MSI Enabled	R/W

Table 3-26 Power Management Capability Structure

Offset	31::24	23::16	15:8	7:0
0x078	Capabilities Register (Hardwire to 0x0003)		0x80 Next Cap Ptr	0x01 Capability ID
0x070	Data (hardwired to 0x00)	PM Control/Status Bridge Extensions (hardwired to 0xx00)	Power Management Status and Control (hardwired to 0x0008)	

Table 3-27 PCIe Capability Structure

Offset	31::24	23::16	15:8	7:0
0x080	PCI Express Capabilities Register		0x00	0x10 Capability ID
0x084	Device Capabilities			
0x088	Device Status		Device Control	
0x08C	Link Capabilities			
0x090	Link Status		Link Control	

Table 3-28 PCIe Capabilities Register Bit Definition

PCIe Capabilities Register Bit Definition: Offset 0x082			
Bit(s)	Field	Description	R/W
15:14	Reserved		R
13:9	Interrupt Message Number	Not Supported. Hardwired to 0	R
8	Slot Implemented	Not Supported. Hardwired to 0	R
7:4	Device/Port type	Indicates the PCIe logical device type. - 0001:Legacy PCI Express Endpoint	R
3:0	Capability Version	- 0x1	R

Table 3-29 Device Capabilities Register Bit Definition

Device Capabilities Register Bit Definition: Offset 0x084			
Bit(s)	Field	Description	R/W
31:28	Reserved		R
27:26	Captured Slot Power Limit Scale	Not Applicable to endpoint. Hardwired to 00	R
25:18	Capture Slot Power Limit Value	Not applicable to endpoint. Hardwired to 00011001	R
17:15	Reserved	- 001	R
14	Power Indicator Present	Not Supported. Hardwired to 0	R
13	Attention Indicator Present	Not Supported. Hardwired to 0	R
12	Attention Indicator Button Present	Not Supported. Hardwired to 0	R
11:9	Endpoint L1 Acceptable Latency	000 (less than 1 micro seconds)	R
8:6	Endpoint L0 Acceptable Latency	000 (less than 64 nano seconds)	R
5	Extended TAG Field Supported	5-bit Tag field supported 0	R

Table 3-29 Device Capabilities Register Bit Definition (Continued)

Device Capabilities Register Bit Definition: Offset 0x084			
4:3	Phantom Functions Supported	Not Supported. Hardwired to 00	R
2:0	Max Payload Size Supported	Max payload is 256 bytes 001	R

Table 3-30 Device Control Register Bit Definition

Device Control Register Bit Definition: Offset 0x088			
Bit(s)	Field	Description	R/W
15	Reserved		R
14:12	Max Read Request	This card will only generate a max read request of 128 bytes, but this register may be written to any of the following. - 000 = 128 Byte - 001 = 256 Byte - 010 = 512 Byte - 011 = 1K Byte -100 = 2K Byte -101 = 4K Byte	R/W
11	Enable No Snoop	1 = Enable 0 = Disable	R/W
10	Aux Power PM Enable	Not Supported. Hardwired to 0	R
9	Phantom Functions Enable	Not Supported. Hardwired to 0	R
8	Extended Tag Field Enable	Not Supported. Hardwired to 0	R
7:5	Max payload Size	000 = 128 Byte 001 = 256 Byte	R/W
4	Enable Relaxed Ordering	1 = Enable 0 = Disable	R/W
3	Unsupported Request Reporting Enable	1 = Enable 0 = Disable	R/W
2	Fatal Error Reporting Enable	1 = Enable 0 = Disable	R/W
1	Non-Fatal Error Reporting Enable	1 = Enable 0 = Disable	R/W
0	Correctable Error Reporting Enable	1 = Enable 0 = Disable	R/W

Table 3-31 Device Status Register Bit Definition

Device Status Register Bit Definition: Offset 0x08A			
Bit(s)	Field	Description	R/W
15:6	Reserved		R
5	Transactions Pending	When set to one, indicates that this function has issued non-posted request packets which have not yet been completed.	R
4	Aux Power Detected	Aux power not required. Hardwired to 0	R
3	Unsupported Request Detected	1 = Error Detected 0 = Error Not Detected	RW1C
2	Fatal Error Detected	1 = Error Detected 0 = Error Not Detected	RW1C
1	Non-Fatal Error Detected	1 = Error Detected 0 = Error Not Detected	RW1C
0	Correctable Error Detected	1 = Error Detected 0 = Error Not Detected	RW1C

Table 3-32 Link Capabilities Register Bit Definition

Link Capabilities Register Bit Definition: Offset 0x08C			
Bit(s)	Field	Description	R/W
31:24	Port Number	Hardwired to 0x01	R
23:18	Reserved	Hardwired to 000000	R
17:15	L1 Exit Latency	More than 64 micro seconds. Hardwired to 111	R
14:12	L0s Exit Latency	More than 4 micro seconds. Hardwired to 111	R
11:10	Active Stake Link PM Support	L0s entry supported. Hardwired to 01	R
9:4	Maximum Link Width	X4. Hardwired to 000100	R
3:0	Maximum Speed	2.5 Gb/s Hardwired to 0001	R

Table 3-33 Link Control Register Bit Definition

Link Control Register Bit Definition: Offset 0x090			
Bit(s)	Field	Description	R/W
15:8	Reserved	Hardwired to 000	R
7	Extended Sync	1 = 4096 FTS Ordered Sets during L0s state and 1024 TS1 Ordered Sets prior to entering the recovery state 0 = Do not use extended FTS and TS1 ordered sets	R/W
6	Common Clock Configuration	1 = Uses common clock on both ends of link 0 = Uses separate clocks on each end of link	R/W
5	Retrain link	1 = Retrain Link 0 = Do not Retrain Link	R/W
4	Link Disable	1 = Disable Link 0 = Do not Disable Link	R/W
3	Read Completion Boundary Control	0 = 64 Byte 1 = 128 Byte	R/W
2	Reserved		
1:0	Active State PM Control	00 = Disabled 01 = L0s Entry Enabled 10 = L1 Entry Enabled 11 = L0s and L1 Entry Enabled	R/W

Table 3-34 Link Status Register Bit Definition

Link Status Register Bit Definition: Offset 0x092			
Bit(s)	Field	Description	R/W
15:13	Reserved	Hardwired to 0x00	R
12	Slot Clock Configuration	1 = The card uses the reference clock provided on the connector	R
11	Link Training	1 = Link Training in process 0 = Link Training done	R
10	Link Training Error	1 = Link Training Error Occurred 0 = Link Successfully Trained	R
9:4	Negotiated Link Width	- 000001 = x1 - 000010 = x2 - 000100 = x4	R
3:0	Link Speed	0001 (2.5 Gb/s)	R

3.2 Local Configuration Registers

The Local Configuration Registers are memory cycle accessible at the offsets from the value stored in Base Address Register 0. The registers at offsets $00 to $FF are also I/O cycle accessible at the offsets from the value stored in Base Address Register 1. The offsets are specified below.

Table 3-35 Local Configuration and DMA Control Registers

PCI (Offset from Base Address)	Register Name	Writable
$00-$07	**Reserved**	N/A
$08	MARBR (same as $AC)	Y
$0C	Big/Little Endian Descriptor	Y
$10-$67	**Reserved**	N/A
$68	INTCSR	Y
$70	**Reserved**	N/A
$74	PCI H Rev	Y
$78	**Reserved**	N/A
$80	DMA Channel 0 Mode	Y
$84	DMA Channel 0 PCI Address	Y
$88	DMA Channel 0 Local Address	Y
$8C	DMA Channel 0 Transfer Byte Count	Y
$90	DMA Channel 0 Descriptor Pointer	Y
$94-$A7	**Reserved**	N/A
$A8	DMA CSR 0	Y
$AC	MARBR (same as $08)	Y
$B0	**Reserved**	N/A
$B4	DMA Channel 0 PCI DAC Upper Address	Y
$B8-$EF	**Reserved**	N/A
$F0	PCI PIO Address Range	N
$F4	PCI PIO Base Address (Remap)	Y
$F8-$1FF	**Reserved**	N/A

NOTE

To ensure software compatibility with other RFM-5565 boards using the PLX 9656 and to ensure compatibility with future enhancements, write zero (0) to all unused bits.

Table 3-36 Mode/DMA Arbitration Register

MARBR: BAR0/1 Offset $08 or $AC				
Bit	Description	Read	Write	Value after PCI Reset
23:0	**Reserved**	Yes	No	$040000
24	**Reserved**	Yes	Yes	0
25	**Reserved**	Yes	No	1
31:26	**Reserved**	Yes	No	$00

Table 3-37 Big/Little Endian Descriptor Register

BIGEND: BAR0/1 Offset $0C				
Bit	Description	Read	Write	Value after PCI Reset
4:0	**Reserved**	Yes	No	$00
5	**PCI PIO RFM Address Space Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for PCI accesses to the RFM Address Space. Writing a zero (0) specifies Little Endian ordering.	Yes	Yes	0
6	**Reserved**	Yes	No	0
7	**DMA Channel 0 Big Endian Mode (Address Invariance)**. Writing a one (1) specifies use of Big Endian data ordering for DMA Channel 0 accesses to the RFM Address Space. Writing a zero (0) specifies Little Endian ordering.	Yes	Yes	0

Table 3-38 Interrupt Control and Status Register

INTCSR: BAR0/1 Offset $68				
Bit	Description	Read	Write	Value after PCI Reset
7:0	**Reserved**	Yes	No	$00
8	**PCI Interrupt Enable**. Writing a one (1) enables PCI interrupts.	Yes	Yes	1
10:9	**Reserved**	Yes	No	0
11	**Local Interrupt Input Enable.** Writing a one (1) enables a local interrupt (i.e., RFM interrupts) to assert a host Interrupt.	Yes	Yes	0
14:12	**Reserved**	Yes	No	0
15	**Local Interrupt Input Active**. When set to a one (1), indicates the Local interrupt input is active.	Yes	No	0
16	**Reserved**	Yes	No	1
17	**Reserved**	Yes	No	0
18	**Local DMA Channel 0 Interrupt Enable.** Writing a one (1) enables DMA Channel 0 interrupts. Clearing the DMA status bit also clears the interrupt.	Yes	Yes	0
20:19	**Reserved**	Yes	No	0
21	**DMA Channel 0 Interrupt Active.** Reading a one (1) indicates the DMA Channel 0 interrupt is active.	Yes	No	0
23:22	**Reserved**	Yes	No	$0
27:24	**Reserved**	Yes	No	$f
31:28	**Reserved**	Yes	No	$0

The PCI Interrupt Enable (Bit 8) functions as a global PCI interrupt enable. It must be set high (1) in addition to other enable bits before any primary or secondary tier interrupt source will result in a PCI interrupt.

Table 3-39 on page 45 summarizes the INTCSR Interrupt Enables that pertain to RFM-5565 operation.

Table 3-39 INTCSR Interrupt Enables

Enable the interrupt source:	Set the following Bit high (1):
Global PCI interrupt enable for all sources	8
Any second tier int. through Local Int. Input (LINTi#)	11
Local DMA Channel 0 interrupt	18

Table 3-40 on page 45 summarizes the INTCSR Interrupt Status bits that pertain to RFM-5565 operation.

Table 3-40 INTCSR Interrupt Status

To check the assertion of the following interrupt source:	Check for a high (1) at Bit:
Any second tier int. through Local Int. Input (LINTi#)	15
Local DMA Channel 0 interrupt	21

Table 3-41 PCI Core/Features Revision ID

PCIHREV: BAR0/1 Offset $74				
Bits	Description	Read	Write	Value after PCI Reset
7:0	**PCI Core/Features Revision ID**. This value is read by the RFM-5565 driver to determine the features of this board.	Yes	No	Current Rev#

Table 3-42 DMA Channel 0 Mode Register

DMAMODE0: BAR0/1 Offset $80				
Bit	Description	Read	Write	Value after PCI Reset
1:0	**Local Bus Width.** An 11 indicates a 32-bit bus width.	Yes	No	11
6:2	**Reserved**	Yes	No	$00
7	**Continuous Burst Enable.** A one (1) enables Continuous Burst mode.	Yes	No	1
8	**Local Burst Enable.** A one (1) indicates Local Bursting.	Yes	No	1
9	**Scatter-Gather Mode.** Writing one (1) indicates DMA Scatter-Gather mode is enabled. For Scatter-Gather mode, the DMA descriptors are loaded from memory in PCI Address space. Writing zero (0) indicates DMA Block mode is enabled.	Yes	Yes	0
10	**Done Interrupt Enable.** A one (1) enables an interrupt when done.	Yes	No	1
16:11	**Reserved**	Yes	No	$00
17	**DMA Channel 0 Interrupt Select**. A one (1) routes the DMA Channel 0 interrupt to the PCI bus interrupt.	Yes	No	1
31:18	**Reserved**	Yes	No	$00

Table 3-43 DMA Channel 0 PCI Address Register

DMAPADR0: BAR0/1 Offset $84				
Bits	Description	Read	Write	Value after PCI Reset
31:0	**PCI Address Register.** Indicates from where in PCI Memory space DMA transfers (read or write) start.	Yes	Yes	$0

Table 3-44 DMA Channel 0 Local Address Register

DMALADR0: BAR0/1 Offset $88				
Bits	Description	Read	Write	Value after PCI Reset
31:0	**Local Address Register.** Indicates from where in Local Memory space DMA transfers (read or write) start.	Yes	Yes	$0

Table 3-45 DMA Channel 0 Transfer Size (Bytes) Register

DMASIZ0: BAR0/1 Offset $8C

Bit	Description	Read	Write	Value after PCI Reset
22:0	**DMA Transfer Size (Bytes).** Indicates the number of bytes to transfer during a DMA operation.	Yes	Yes	$0
31:23	**Reserved**	Yes	No	$0

Table 3-46 DMA Channel 0 Descriptor Pointer Register

DMADPR0: BAR0/1 Offset $90

Bit	Description	Read	Write	Value after PCI Reset
0	**DMA Channel 0 Descriptor Location.** A one (1) indicates PCI Address space.	Yes	No	1
2:1	**Reserved**	N/A	N/A	0
3	**Direction of Transfer.** Writing a one (1) indicates transfer from the RFM to the PCI bus. Writing a zero (0) indicates transfer from the PCI bus to the RFM.	Yes	Yes	0
31:4	**Channel 0 First Descriptor Address.** This field holds bits [31:4] of the first DMA descriptor address. The first descriptor address must be aligned on a 16-byte boundary (i.e., address bits [3:0] are considered to be $0).	Yes	Yes	$0

Table 3-47 DMA Channel 0 Command/Status Register

DMACSR0: BAR0/1 Offset $A8

Bit	Description	Read	Write	Value after PCI Reset
0	**Channel 0 Enable**. Writing a one (1) enables channel to transfer data. Writing a zero (0) disables the channel from starting a DMA transfer.	Yes	Yes	0
1	**Channel 0 Start**. Writing a one (1) causes channel to start transferring data if the channel is enabled.	No	Yes/Set	0
2	**Reserved**	No	No	0
3	**Channel 0 Clear Interrupt**. Writing a one (1) clears Channel 0 interrupts.	No	Yes/Clr	0
4	**Channel 0 Inactive**. Reading a one (1) indicates a channel transfer is complete. Reading a zero (0) indicates a channel transfer is not complete.	Yes	No	1
7:5	**Reserved**	Yes	No	000

Table 3-48 DMA Channel 0 PCI Dual Address Cycles Upper Address

DMADAC0: BAR0/1 Offset $B4				
Bit	Description	Read	Write	Value after PCI Reset
31:0	**Upper 32 Bits for 64-bit addressing during DMA Channel 0 Cycles.** If set to $0, the DMA performs a 32-bit address DMA Channel 0 access.	Yes	Yes	$0

Table 3-49 PCI PIO Direct Slave Local Address Range

LAS1RR: BAR0/1 Offset $F0				
Bit	Description	Read	Write	Value after PCI Reset
0	**Memory Space Indicator.** A zero (0) indicates Local Address Space 1 maps into PCI Memory space.	Yes	No	0
3:1	**Reserved**	Yes	No	$0
31:4	**Range.** Specifies which PCI Address bits to use for decoding a PCI access to Local Address Space 1. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to address bit 31. Write one (1) to all bits that must be included in decode and zero (0) to all others. (Used in conjunction with PCIBAR3).	Yes	No	$FFE0000 (for 2 MB) $FF00000 (for 16 MB) $FC00000 (for 64 MB) $F800000 (for 128 MB) $F000000 (for 256 MB)

NOTE: LAS1RR range must be power of 2. The LAS1RR range value is two's complement of the range.

Table 3-50 PCI PIO Direct Slave Local Base Address (Remap)

LAS1BA: BAR0/1 Offset $F4				
Bit	Description	Read	Write	Value after PCI Reset
0	**Local Address Space 1 Enable.** A one (1) enables decoding of PCI addresses for PIO addresses for PIO Direct Slave access to Local Address Space 1 (PCIBAR3).	Yes	No	1
3:1	**Reserved**	Yes	No	$0
31:4	**Remap PCIBAR3 Base Address to Local Address Space 1 Base Address.** The PCIBAR3 base address translates to the Local Address Space 1 Base Address programmed in this register. A Direct Slave access to an offset from PCIBAR3 maps to the same offset from this Local Base Address.	Yes	Yes	$0

NOTE: Remap Address value must be a multiple of the LAS1RR range.

3.3 RFM Control and Status Registers

The RFM Control and Status Registers for the RFM-5565 are memory cycle accessible at the offsets from the value stored in Base Address Register 2. The offsets are specified below. The space reserved for this group of registers is 64 bytes.

Table 3-51 Memory Map of the Local Control and Status Registers

Offset	Mnemonic	Description	Access	Comments
$0	BRV	Board Revision	read only	Current board revision/model
$1	BID	Board ID Register	read only	BID is $65 for RFM-5565
$3.2	BRB	Board Revision Build	read only	Current board revision build
$4	NID	Node ID Register	read only	Set by 8 switches of S2
$7..5	--	**Reserved**	--	
$B..8	LCSR1	Local Control & Status Reg. 1	read/write	Some bits reserved. Some bits read-only.
$F..C	--	**Reserved**	--	
$13..10	LISR	Local Interrupt Status Reg.	read/write	Some bits reserved. Some bits read-only.
$17..14	LIER	Local Interrupt Enable Reg.	read/write	
$1B..18	NTD	Network Target Data	read/write	32 Data bits for network target
$1C	NTN	Network Target Node	read/write	Target node ID for network Int.
$1D	NIC	Network Interrupt Command	read/write	Select Int type and initiate interrupt
$1F..1E	--	**Reserved**	--	
$23..20	ISD1	Int. 1 Sender Data	read only	127 loc. By 32-bit FIFO for network Int. 1
$24	SID1	Int. 1 Sender ID	read/clear	127 loc. Deep FIFO/ write clears pointers
$27..25	--	**Reserved**	--	
$2B..28	ISD2	Int. 2 Sender Data	read only	127 loc. By 32-bit FIFO for network Int. 2
$2C	SID2	Int. 2 Sender ID	read/clear	127 loc. Deep FIFO/ write clears pointers
$2F..2D	--	**Reserved**	--	
$33..30	ISD3	Int. 3 Sender Data	read only	127 loc. By 32-bit FIFO for network Int. 3
$34	SID3	Int. 3 Sender ID	read/clear	127 loc. Deep FIFO/ write clears pointers
$37..35	--	**Reserved**		
$3B..38	ISD4	Int. 4 Sender Data	read only	127 loc. By 32-bit FIFO for network Int. 4
$3C	SID4	Int. 4 Sender ID	read/clear	127 loc. Deep FIFO/ write clears pointers
$3F..3D	--	**Reserved**	--	

3.3.1 Board Revision Register

Board Revision (BRV) BAR2 (Offset $0): An 8-bit register used to represent revisions or model numbers. This register is read-only.

3.3.2 Board ID Register

Board ID (BID) BAR2 (Offset $1): An 8-bit register which contains an 8-bit code unique to the RFM-5565 type boards. The code is $65. This register is read-only.

3.3.3 Board Revision Build Register

Board Revision Build (BRB) BAR2 (Offset $2): A 16-bit register used to represent the build number for this specific revision. The upper four bits indicate the PCI memory window size corresponding to the FPGA configuration file currently loaded. This register is read-only.

- 1 = 2 MB memory window
- 2 = 16 MB memory window
- 3 = 64 MB memory window
- 4 = 128 MB memory window
- 5 = 256 MB memory window

3.3.4 Node ID Register

Node ID (NID) BAR2 (Offset $4): An 8-bit register containing the node ID of the board. This register reflects the setting of the onboard switch S2 and is read-only. Each board on a network must have a unique node ID.

3.3.5 Local Control and Status Register 1

Local Control and Status Register 1 (LCSR1) BAR2 (Offset $08): A 32-bit register containing Reflective Memory control and status bits is described below.

Table 3-52 Local Control and Status Register 1

LCSR1: BAR2 Offset $08							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Status LED	Transmitter Disable	Dark-on-Dark Enable	Loopback Enable	Local Memory Parity Enable	Redundant Mode Enabled	Rogue Master 1 Enabled	Rogue Master 0 Enabled
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved	S1-4 PCI Window Switch 4	Config 1	Config 0	S1-3 PCI Window Switch 3	S1-2 Delay TX from PCI write	Offset 1	Offset 0
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Reserved							
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
TX FIFO Empty	TX FIFO Almost Full	Latched RX FIFO Full	Latched RX FIFO Almost Full	Latched Sync Loss	RX Signal Detect	Bad Data	Own Data

Local Control and Status Register 1 Bit Definitions

Bit 31: **Status LED** – The board contains a user defined RED status LED. Setting this bit low (0) turns OFF the LED. The default state of this bit after reset is high (1) and the LED will be ON.

Bit 30: **Transmitter Disable** – Setting this bit high (1) will manually turn OFF the board's transmitter. The default state of this bit after reset is low (0) and the transmitter is enabled. When turning the board's transmitter back ON by setting this bit back to low (0), an unspecified amount of time must be allowed to provide for the turn-on time of the optics.

Bit 29: **Dark-on-Dark Enable** – When this bit is set high (1), the board's transmitter will be turned OFF if the board's receiver does not detect a signal or if the receiver detects invalid data patterns. The dark-on-dark feature is useful in hub configurations.

Bit 28: **Loopback Enable** – When this bit is set high (1), the fiber optic transmitter and receiver are disabled and the transmit signal is looped back to the receiver circuit internally. This allows basic functional testing with or without an external cable.

Bit 27: **Local Memory Parity Enable** – When this bit is set high (1), parity checking is enabled when reading from the RFM-5565 SDRAM. Note that parity works only on 32-bit and 64-bit accesses. Byte (8-bit), Word (16-bit), and 24-bit memory write accesses are inhibited while parity is enabled.

Bit 26: **Redundant Mode Enabled** – When this bit is set high (1), redundant mode of network transfers has been enabled. This bit is read-only. Redundant mode is enabled by setting switch S1 position 1 in the ON position.

Bit 25: **Rogue Master 1 Enabled** – When this bit is set high (1), the board is operating as Rogue Master 1. This bit is read-only. Rogue Master 1 operation is enabled by setting switch S1 position 6 in the ON position.

Bit 24: **Rogue Master 0 Enabled** – When this bit is set high (1), the board is operating as Rogue Master 0. This bit is read-only. Rogue Master 0 operation is enabled by setting switch S1 position 5 in the ON position.

Bit 23: **Reserved** – This bit is reserved.

Bits 22 and 19: **Window 1 and Window 0** – The PCI PIO window size is selected by setting S1 switch positions 3 and 4. Bit 19 (Window 0) is connected to S1 switch position 3 ('1' when ON, '0' when OFF). Bit 22 (Window 1) is connected to S1 switch position 4 ('1' when ON, '0' when OFF). These two bits indicate the memory PCI PIO window size as defined in the following table. The two bits are read only.

Window 1	Window 0	PCI PIO Window Size
0	0	default = installed memory size
0	1	64 MByte
1	0	16 MByte
1	1	2 MByte

Bits 21 and 20: **Config 1 and Config 0 –** These two bits indicate the installed memory size as defined in the following table. The two bits are read-only.

Config 1	Config 0	Memory Size
0	0	64 MByte
0	1	128 MByte
1	0	256 MByte
1	1	Reserved

Bit 18: **Delay TX from PCI Write –** When this bit is set high (1), the board is operating with reduced PCI write bandwidth. This bit is read-only. This mode is enabled by setting switch S1 position 2 in the ON position. Data received on the PCI bus will be delayed before it is written to memory or transmitted on the network. This prevents the node from using full network bandwidth. This setting is normally OFF.

Bits 17 and 16: **Offset 1 and Offset 0 –** When the host PCI system writes to the onboard memory and initiates a packet over the network, Offset 1 and Offset 0 will apply an offset to the network address as it is sent or received over the network. The offset does not appear on local access to the memory, and the offset does not alter network packets as they pass through the board. Offset 1 and Offset 0 provide four possible binary increments of 64 MByte each through the 256 MByte network address range. When the address and offset exceeds the 256 MByte network address range, the address bits beyond 256 MByte will be truncated. This causes the write to wrap around into a lower memory location. Offsets 1 and 0's bits correspond to the network address bits A27 and A26 respectively.

Offset 1	Offset 0	Offset Applied
0	0	$0
0	1	$4000000
1	0	$8000000
1	1	$C000000

Bits 15 through 08: **Reserved** – These bits are reserved.

Bit 07: **TX FIFO Empty** – A logic high (1) indicates the TX FIFO is currently empty. This bit provides immediate status only (not latched) and is read-only.

Bit 06: **TX FIFO Almost Full** – A logic high (1) indicates the TX FIFO is currently almost full. This bit provides immediate status only (not latched) and is read-only. Periodic assertion of this bit is normal.

Bit 05: **Latched RX FIFO Full** – A logic high (1) indicates the RX FIFO has experienced a full condition at least once. This bit is read-only within this register. To clear this condition write to the corresponding bit within the Local Interrupt Status Register.

NOTE

The occurrence of the Latched RX FIFO Full signal is a fault condition due to a board malfunction and indicates that the received data may have been lost.

Bit 04: **Latched RX FIFO Almost Full** – A logic high (1) indicates the RX FIFO is operating at the maximum acceptable rate. Under normal operating conditions, this event should not occur. This bit is read-only within this register. To clear this condition, write to the corresponding bit within the Local Interrupt Status Register.

Bit 03: **Latched Sync Loss** – A logic high (1) indicates the receiver circuitry has detected the loss of a valid signal at least once since the last time the flag has been cleared. Under normal operating conditions, this event should not occur and may indicate a loss of data. A logic high may indicate the receiver's link was intentionally or unintentionally disconnected.

Bit 02: **RX Signal Detect** – A logic high (1) indicates the board receiver is currently detecting light. This bit provides immediate status only (not latched) and is read-only.

Bit 01: **Bad Data** – A logic high (1) indicates the board receiver circuit has detected bad (invalid) data at least once since power up or since the flag had previously been cleared. Under normal operating conditions, this event should not occur and may indicate a loss of data. This bit is read-only within this register. To clear this condition, write to the corresponding bit within the Local Interrupt Status Register.

Bit 00: **Own Data** – A logic high (1) indicates the board has detected the return of its own data packet at least once since this bit has previously been cleared. This bit serves as an indicator that the link is intact. The Own Data bit should be set any time a write to the onboard memory occurs or any time network interrupt is initiated. This bit is both read and write accessible.

3.3.6 Local Interrupt Control Registers

The RFM-5565 contains a number of sources for the interrupt. The second tier of interrupts is controlled by two registers called the LISR as shown in Table 3-53 on page 54 and the LIER shown in Table 3-54 on page 57. All Local Interrupts are logically "ORed" together into the single interrupt called the LINTi#. The LINTi# line is, in turn, controlled by Bit 11 of the Local Configuration register (INTCSR at offset $68 to Base address 0). The control and status of local interrupts are implemented in the two local registers (LISR and LIER). The bit functions of these two registers mirror each other.

Local Interrupt Status Register

Local Interrupt Status Register (LISR) BAR2 (Offset $10): This is a 32-bit register containing a group of interrupt status flags. The LIER contains a corresponding group of enables. Before any local interrupt can cause an interrupt on the LINTi# line, the Status Bit, its Enable and the Global Enable must be asserted.

Table 3-53 Local Interrupt Status Register

LISR: BAR2 Offset $10							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Auto Clear Flag	Global Interrupt Enable	Local Memory Parity Error	Memory Write Inhibit	Latched Sync Loss	RX FIFO Full	RX FIFO Almost Full	Bad Data
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Pending Net. Int. 4	Rogue Packet Fault	TX FIFO Full	Reserved	Reset Node Request	Pending Net. Int. 3	Pending Net. Int. 2	Pending Net. Int. 1

Local Interrupt Control Register Bit Definitions

Bits 31 through 16: **Reserved** - These bits are reserved.

Bit 15: **Auto Clear Flag** – This bit is a read-only status indicator of the corresponding bit in the LIER Register. When this bit is high (1), the Global Interrupt Enable (Bit 14) will automatically be cleared as this register (LISR) is being read. Clearing the Global Interrupt Enable de-asserts the LINTi# and, in turn, releases the PCI Interrupt.

Bit 14: **Global Interrupt Enable** – This bit must be set high (1) in addition to any interrupt flag and its associated enable bit in the LIER before the LINTi# line is asserted and a PCI interrupt can result. If the Auto Clear enable bit in the LIER is

set high (1), the Global Interrupt Enable bit will automatically be cleared as this register (LISR) is being read. This bit is read and write accessible with this register and thus allows a single read-modify-write operation to service the local interrupts.

Bit 13: **Local Memory Parity Error** - When this bit is high (1), one or more parity errors have been detected on local memory accesses. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. Note that Bit 27 of the LCSR1 must be set high before parity is active. Also note that parity works only on 32-bit and 64-bit accesses. Word (16-bit) and byte (8-bit) memory write accesses are inhibited.

Bit 12: **Memory Write Inhibited** - When this bit is high (1), an 8-bit byte, a 16-bit word, or a 24-bit write to local memory was attempted and inhibited while the board was in the parity enabled mode. This bit is latched. Once set, it must be cleared by writing a zero to this bit location.

Bit 11: **Latched Sync Loss** – When this bit is high (1), the receiver circuit has lost synchronization with the incoming signal one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. The assertion of the Latched Sync Loss usually indicates the receiver link was or is disconnected, either intentionally or unintentionally, and data may have been lost. This event will also occur if the upstream node tied to the receiver is powered off or is disabled.

Bit 10: **RX FIFO Full** – When this bit is high (1), the RX FIFO has been full one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. This is a fault condition and data may have been lost.


NOTE

This condition should not occur during normal operation. Bit 10 is for diagnostic purposes only.

Bit 09: **RX FIFO Almost Full** – When this bit is high (1), the RX FIFO has been almost full one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location. The assertion of the RX FIFO Almost Full bit indicates the receiver circuit is operating at maximum capacity. If it does occur, the PCI bus master should temporarily suspend all write and read operations to the board.

Bit 08: **Bad Data** – When this bit is high (1), the receiver circuit has detected invalid data one or more times. This bit is latched. Once set, it must be cleared by writing a zero to this bit location.

Bit 07: **Pending Net. Int. 4** – When this bit is high (1), one or more type 4 network interrupts have been received. To see the sender data and sender node ID, read the Interrupt Sender Data 4 (ISD4) FIFO at offset $38 and the Interrupt Sender ID (SID4) at offset $3C respectively.

Bit 06: **Rogue Packet Fault** - When this bit is set high (1), the board is operating as either Rogue Master 1 or 0 and has detected and removed a rogue packet. This bit is latched. Once set, it must be cleared by writing a zero (0) to this bit location.

Bit 05: **TX FIFO Full** - When this bit is high (1), the TX FIFO has been full one or more times. This bit is latched. Once set, it must be cleared by writing a zero (0) to this bit location. This is a fault condition and data may have been lost.


NOTE

This condition should not occur during normal operation. Bit 05 is for diagnostic purposes only.

Bit 04: **Reserved** - This bit is reserved.

Bit 03: **Reset Node Request** – When this bit is high (1), another node on the network has requested that the local PCI bus master reset this board. The RFM-5565 does not reset itself automatically.

Bit 02: **Pending Net. Int. 3** – When this bit is high (1), one or more type 3 network interrupts have been received. To see the sender data and sender node ID(s), read the Interrupt Sender Data 3 (ISD3) FIFO at offset $30 and the Interrupt Sender ID (SID3) FIFO at offset $34 respectively.

Bit 01: **Pending Net. Int. 2** – When this bit is high (1), one or more type 2 network interrupts have been received. To see the sender data and sender node ID(s), read the Interrupt Sender Data 2 (ISD2) FIFO at offset $28 and the Interrupt Sender ID (SID2) FIFO at offset $2C respectively.

Bit 00: **Pending Net. Int. 1** – When this bit is high (1), one or more type 1 network interrupts have been received. To see the sender data and sender node ID(s), read the Interrupt Sender Data 1 (ISD1) FIFO at offset $20 and the Interrupt Sender ID (SID1) FIFO at offset $24 respectively.

Local Interrupt Enable Register

Local Interrupt Enable Register (LIER) BAR2 (Offset $14): A 32-bit register containing a group of interrupt enables corresponding to the status bits in LISR.

Table 3-54 Local Interrupt Enable Register

LIER: BAR2 Offset $14							
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	Bit 26	Bit 25	Bit 24
Reserved							
Bit 23	Bit 22	Bit 21	Bit 20	Bit 19	Bit 18	Bit 17	Bit 16
Reserved							
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 09	Bit 08
Auto Clear Enable	Reserved	Enable Int on Local Memory Parity Error	Enable Int on Memory Write Inhibit	Enable Int on Latched Sync Loss	Enable Int on RX FIFO Full	Enable Int on RX FIFO Almost Full	Enable Int on Bad Data
Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
Enable Int on Pending Net. Int. 4	Enable Int on Rogue Packet Fault	Enable Int on TX FIFO Full	Reserved	Enable Int on Reset Node Request	Enable Int on Pending Net. Int. 3	Enable Int on Pending Net. Int. 2	Enable Int on Pending Net. Int. 1

3.3.7 Network Target Data Register

Network Target Data (NTD) BAR2 (Offset $18): A 32-bit register containing the data associated with one of the four network interrupts that will be sent to the target (destination) node. Writing data to this register does not initiate the actual interrupt; only writing to the Network Interrupt Command (NIC) register will do so. The NTD register is both read and write accessible.

3.3.8 Network Target Node Register

Network Target Node (NTN) BAR2 (Offset $1C): An 8-bit register containing the node ID of the target (destination) node. Writing to the NTN register does not initiate the actual network interrupt. This register is both read and write accessible. The NTN register can be written or read with the Network Interrupt Command Register as a single 16-bit word.

3.3.9 Network Interrupt Command Register

Network Interrupt Command (NIC) BAR2 (Offset $1D): An 8-bit register containing a four-bit code that defines the type of network interrupt issued. See Table 3-55 on page 58 for a definition of the possible codes. The NIC is both read and write accessible. Only writing to the NIC register will initiate the network interrupt. The network interrupt is transmitted in order following after all previously written data.

Table 3-55 Network Interrupt Command Register

NIC: BAR2 Offset $1D	
NIC[3,2,1,0]	Function
X000	Reset Node Request (sets LISR Bit 03 only, the user application must perform the actual reset)
X001	Network Interrupt 1 (stored in a 127 deep FIFO at the receiving node)
X010	Network Interrupt 2 (stored in a 127 deep FIFO at the receiving node)
X011	Network Interrupt 3 (stored in a 127 deep FIFO at the receiving node)
X100	Reserved (Setting to this type will only set the OWN DATA bit in the LCSR1)
X101	Reserved (Setting to this type will only set the OWN DATA bit in the LCSR1)
X110	Reserved (Setting to this type will only set the OWN DATA bit in the LCSR1)
X111	Network Interrupt 4 (stored in a 127 deep FIFO at the receiving node)
1XXX	Global enable. Send to all nodes regardless of NTN Register

The NTD, NTN and the NIC registers described above are used to generate network interrupts. Four pairs of registers described below are involved with receiving those network interrupts.

3.3.10 Interrupt 1 Sender Data FIFO

Interrupt 1 Sender Data FIFO (ISD1) BAR2 (Offset $20): A 32-bit FIFO containing up to 127 Dwords of data, which has been sent to this node in type 1 network interrupt packets. The function of the 32 bits of data is user defined. The ISD1 is a 127 location deep FIFO, but it is coupled and slaved to the companion FIFO SID1. Essentially, there is only one address pointer for both FIFOs and that pointer is only affected by access to the SID1 FIFO. For this reason, each location within the data (ISD1) FIFO can be read multiple times without incrementing the address pointer, while reading the companion SID1 FIFO increments the pointer for both FIFOs. For this same reason, the user must read the data (ISD1) before the Sender ID (SID1) or the corresponding data will be lost.

3.3.11 Interrupt 1 Sender ID FIFO

Interrupt 1 Sender ID FIFO (SID1) BAR2 (Offset $24): An 8-bit FIFO containing the Node ID corresponding to the data in ISD1. Each time one node issues a network interrupt, it includes its own node ID as part of the packet. At each other network node, the interrupt packet is evaluated. If the network interrupt is directed to that node, and if the network interrupt is of type 1, then the sender's node ID is stored in a 127 location deep FIFO called the Interrupt 1 Sender ID FIFO or SID1. Like any normal FIFO, each time the SID1 is read, the FIFO address pointer automatically increments to the next location in the FIFO. Therefore, each sender ID can only be read once from the SID1 FIFO. Writing any data to the SID1 FIFO causes the SID1 FIFO to be set to empty. Note that the value of zero is NOT a true indicator that the FIFO is empty since zero is also a valid node ID. To see if

network interrupts are pending, examine bits 07, 02, 01 and 00 in the LISR register.

3.3.12 Interrupt 2 Sender Data FIFO

Interrupt 2 Sender Data FIFO (ISD2) BAR2 (Offset $28): A 32-bit FIFO functioning just like ISD1, except it responds only to type 2 network interrupts.

3.3.13 Interrupt 2 Sender ID FIFO

Interrupt 2 Sender ID FIFO (SID2) BAR2 (Offset $2C): An 8-bit FIFO functioning just like SID1, except it responds only to type 2 network interrupts.

3.3.14 Interrupt 3 Sender Data FIFO

Interrupt 3 Sender Data FIFO (ISD3) BAR2 (Offset $30): A 32-bit FIFO functioning just like ISD1, except it responds only to type 3 network interrupts.

3.3.15 Interrupt 3 Sender ID FIFO

Interrupt 3 Sender ID FIFO (SID3) BAR2 (Offset $34): An 8-bit FIFO functioning just like SID1, except it responds only to type 3 network interrupts.

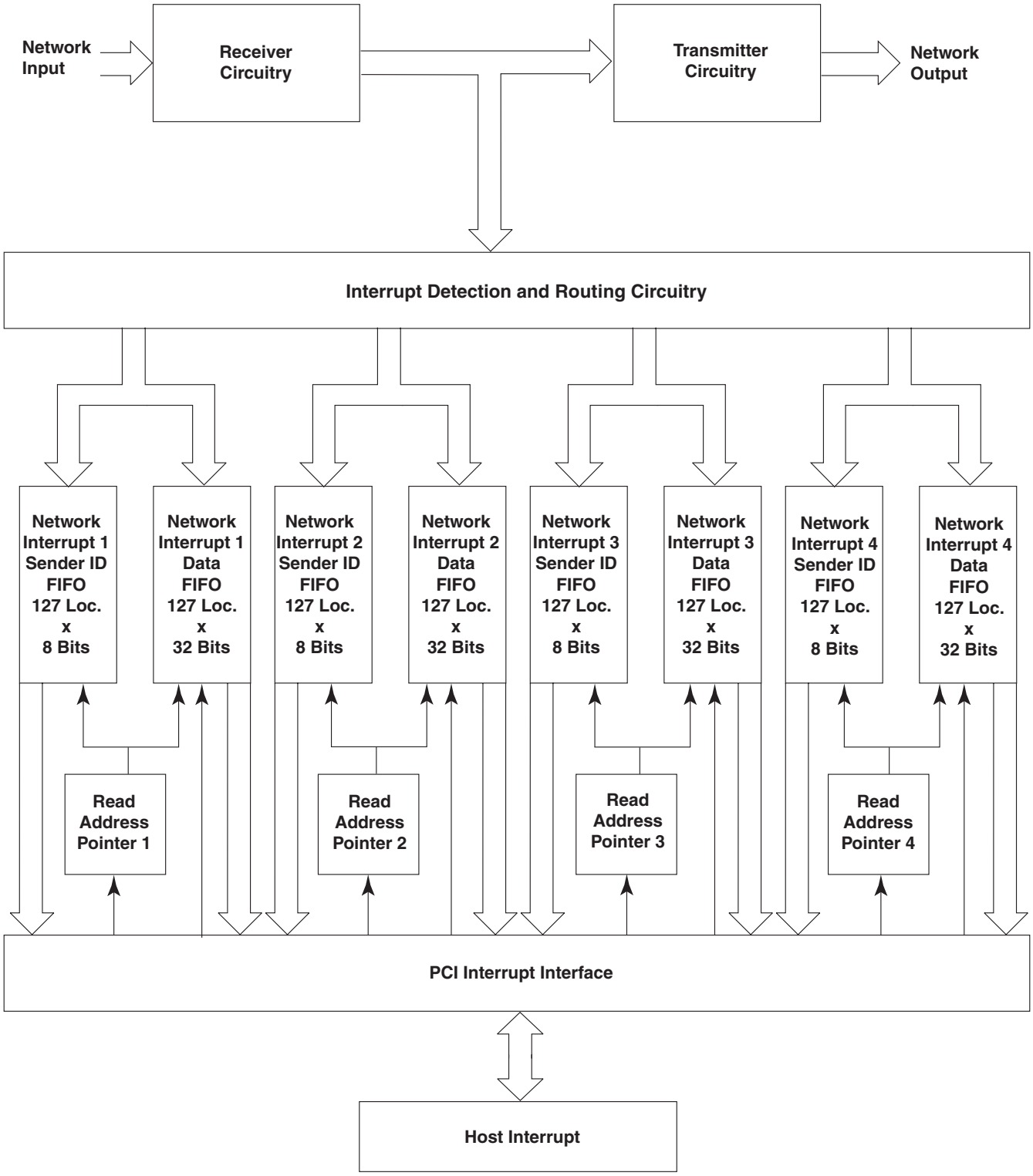
3.3.16 Interrupt 4 Sender Data FIFO

Interrupt 4 Sender Data FIFO (ISD4) BAR2 (Offset $38): A 32-bit FIFO functioning just like ISD1, except it responds only to type 4 network interrupts.

3.3.17 Interrupt 4 Sender ID FIFO

Interrupt 4 Sender ID FIFO (SID4) BAR2 (Offset $3C): An 8-bit FIFO functioning just like SID1, except it responds only to type 4 network interrupts.

Figure 3-1 Block Diagram of the Network Interrupt Reception Circuitry



3.4 Example of a Block DMA Operation for RFM-5565

1. Base Address Register 0 stores the starting address of the Local Control and Configuration registers, which include the DMA Control registers. The value in this register is PCIBAR0.
2. There are six DMA registers that must be configured to set up the DMA cycle. These DMA registers will remain unchanged after the DMA cycle.

DMA channel 0 mode setting: Bit 9 set to 0 indicates the use of normal Block DMA (not Scatter/Gather mode).	**DMAMODE0 at PCIBAR0 + offset $80**
DMA channel 0 PCI starting address: Set to the starting address of the PC memory (for either source or destination transfer).	**DMAPADR0 at PCIBAR0 + offset $84**
DMA channel 0 local starting address: Set to the starting address of the local (RFM) memory (for either source or destination transfers). **NOTE**: The first local (RFM) memory location is at $0.	**DMALADR0 at PCIBAR0 + offset $88**
DMA channel 0 transfer size: Set to the number of bytes to be transferred (maximum $7FFFFF).	**DMASIZ0 at PCIBAR0 + offset $8C**
DMA channel 0 Descriptor Pointer: Set to $0 for PCI-to-Local or set to $8 for Local-to-PCI.	**DMADPR0 at PCIBAR0 + offset $90**
DMA channel 0 PCI DAC upper address: This register is set to $0 when using 32-bit addresses.	**DMADAC0 at PCIBAR0 + offset $B4**

3. To initiate and monitor the transfer, access DMACSR0 as follows:

   DMA channel 0 Command/Status register:

   DMACSR0 at PCIBAR0 + offset $A8.

   Write $0003 to start the transfer, then poll the same register. When Bit 4 is high (1), the DMA cycle is complete.

NOTE

Polling read cycles take priority over the DMA cycles. Overly aggressive polling will slow the DMA transfer. Rather than polling for the DMA done condition, the user can choose to enable the PCI interrupt on DMA done by setting Bit 18 of the INTCSR at offset $68 to high (1). Once the interrupt is enabled, the user software routine waits for the interrupt to occur.

4. After the DMA is finished, clear the DMA completion bit with a write to DMACSR0 as follows. This is necessary when using DMA interrupts.

   DMA channel 0 Command/Status register:

   DMACSR0 at PCIBAR0 + offset $A8.

   Write $8 to clear the DMA completion bit before attempting another DMA.

3.5 Example of a Scatter-Gather DMA Operation for RFM-5565

Scatter-Gather DMA transfer is a mode usually used to perform large data transfers separated into multiple smaller pages or blocks. Note that a data page must not cross a 4 GByte address boundary. The DMA descriptor pointer is the address for a chained list of page descriptors.

Each page descriptor defines the address and size of a data block plus a pointer to the next descriptor block. The descriptors are automatically fetched when needed and then data is read/written to the corresponding page. The descriptor chain is processed until the data transfer is finished or the end of the descriptor chain is reached, whichever comes first.

Page descriptor blocks cannot be mapped in 64-bit addressing space. The first descriptor must be on a 16-byte boundary. For best performance, each descriptor block should be aligned on a 16-byte or 8-byte boundary.

A descriptor chain must be created in PCI 32-bit memory space before starting a Scatter-Gather DMA. Each descriptor in the chain has this format:

1st Dword: Lower 32-bit PCI Address for Data (each page must be aligned on an 8-byte boundary),

2nd Dword: Upper 32-bit PCI Address for Data ($0 for 32-bit addressing),

3rd Dword: Number of bytes to transfer to/from PCI Address (each page size must be a multiple of 8 bytes),

4th Dword: PCI Address of Next Descriptor (write $1 in this field to denote end of chain)

Also, keep a total for the size of all data blocks pointed to by the chain. This total length value must be written to the DMA transfer size register.

1. Base Address Register 0 stores the starting address of the Local Control and Configuration registers, which include the DMA Control registers. The value in this register is PCIBAR0.
2. There are six DMA registers that must be configured to set up the DMA cycle. These registers will remain unchanged after the DMA cycle.

DMA channel 0 mode setting: Bit 9 set to 1 indicates the use of Scatter-Gather DMA (not normal Block mode).	**DMAMODE0 at PCIBAR0 + offset $80**
DMA channel 0 PCI starting address: This register is unused during Scatter-Gather DMA.	**DMAPADR0 at PCIBAR0 + offset $84**
DMA channel 0 local starting address: Set to the starting address of the local (RFM) memory (for either source or destination transfers). **NOTE**: The first local (RFM) memory location is at $0.	**DMALADR0 at PCIBAR0 + offset $88**
DMA channel 0 transfer size: Set to the total number of bytes to be transferred in all blocks (maximum $7FFFFF).	**DMASIZ0 at PCIBAR0 + offset $8C**
DMA channel 0 Descriptor Pointer: Set bits 31:4 to the PCI Address of the first DMA Scatter-Gather descriptor location. Set bit-3 to 0 for PCI-to-Local or set bit-3 to 1 for Local-to-PCI.	**DMADPR0 at PCIBAR0 + offset $90**
DMA channel 0 PCI DAC upper address: This register is unused during Scatter-Gather DMA.	**DMADAC0 at PCIBAR0 + offset $B4**

3. To initiate and monitor the transfer, access DMACSR0 as follows:

   DMA channel 0 Command/Status register:

   DMACSR0 at PCIBAR0 + offset $A8.

   Write $0003 to start the transfer, then poll the same register. When Bit 4 is high (1), the DMA cycle is complete.

NOTE

Polling read cycles take priority over the DMA cycles. Overly aggressive polling will slow the DMA transfer. Rather than polling for the DMA done condition, the user can choose to enable the PCI interrupt on DMA done by setting Bit 18 of the INTCSR at offset $68 to high (1). Once the interrupt is enabled, the user software routine waits for the interrupt to occur.

4. After the DMA is finished, clear the DMA completion bit with a write to DMACSR0 as follows. This is necessary when using DMA interrupts.

   DMA channel 0 Command/Status register:

   DMACSR0 at PCIBAR0 + offset $A8.

   Write $8 to clear the DMA completion bit before attempting another DMA.

3.6 Example of a PCI PIO Sliding Window Operation for RFM-5565

RFM-5565 cards are currently available with 128 or 256 MByte of installed memory. Under some circumstances, it is useful to reduce the PCI memory address space window size. For example, a BIOS may have difficulty dividing the address space into enough windows with appropriate granularity for all of the installed devices. In another example, the operating system may not be able to assign resources for all of the drivers loaded. Reducing the PCI window size allows the RFM-5565 to use a smaller footprint on the PCI bus address space.

However, changing the PCI PIO window size does not affect other functions of the card. All of the installed memory on the card can be updated by data packets on the Reflective Memory network. For example, a 256 MByte card will reflect every value written in the 256 MByte Reflective Memory network address space. Also, the RFM-5565 DMA engine can be used to access every byte of the memory installed on the card. It is also possible to move (remap) the PCI PIO window to access every byte of the memory installed on the card using PIO accesses.

Here is a brief description of selecting the PCI memory window size. There are four possible choices: 2 MByte, 16 MByte, 64 MByte or use the default full memory size. Two switches on S1 are used to configure the PCI memory window size. The switch settings should only be changed while the power is off. Use S1 switch positions 3 and 4 to select one of the four window sizes. Bits 20 and 21 of RFM register LCSR1 (PCIBAR2 Offset $08) indicate the full installed memory size. Bit 19 of LCSR1 is connected to S1 switch position 3 and bit 22 of LCSR1 is connected to S1 switch position 4. Both bits 19 and 22 can be read by software (‘1’ when on, ‘0’ when off). The table below lists the number of PCI PIO window selections available with various RFM-5565 memory options.

PCI PIO Window Size	Switch S1 Position 4	Switch S1 Position 3	LCSR1 bit-22	LCSR1 bit-19	Number of PIO Windows with 64 MByte	Number of PCI Windows with 128 MByte	Number of PIO Windows with 256 MByte
Default	Off	Off	0	0	1	1	1
64 MByte	Off	On	0	1	1	2	4
16 MByte	On	Off	1	0	4	8	16
2 MByte	On	On	1	1	32	64	128

Two registers in PCIBAR0 are used to implement the PCI PIO Sliding Windows. The LAS1BA register (Direct Slave Local Address Space 1 Range, PCIBAR0 Offset $F0) is read-only. It is determined by switch settings and the installed memory option. The LAS1RR (Remap) register (Direct Slave Local Address Space 1 Local Base Address, PCIBAR0 Offset $F4) is writeable in bits 27:21. The 32-bit register masks off invalid upper and lower bits based on switch and installed memory settings (defaults to $00000001).

Consider this example with a PCI PIO window set to 2 MByte. First, the firmware will set the range register to $FFE00000 to indicate a 2 MByte PCI PIO window. Next, the system (BIOS) will set the PCI Base Address (PCIBAR3) on a 2 MByte boundary. For example, the BIOS could set the PCIBAR3 to $F7600000 (allowing a PCI window up to $F77FFFFF). This serves as the PCI Base Address for PIO access to the local Reflective Memory address space. The firmware also defaults setting the Remap Value to 0 at the beginning of the installed memory address

space. This gives the user application PIO access to the Reflective Memory locations $00000000 up to $001FFFFF. The user application can set the Local Base Address (Remap) register pointing to any valid window in the installed memory. For example, the user application can write $00200000 to the Remap register to access the second 2 MByte PCI PIO window. The register value will be $00200001 since bit-0 is hardwired to 1. This gives the user application PIO access to the Reflective Memory locations $00200000 up to $003FFFFF. The user application uses the same PCIBAR3 window ranging from $F7600000 up to $F77FFFFF.

NOTE

After writing a new value to the LAS1BA remap register, the user application should read the LAS1BA remap register before accessing the new window. This ensures the new window mapping has taken effect and subsequent memory accesses will be to the new memory window.

In summary, register LAS1RR is the range register corresponding to the size of the PCI window and is read-only. Register LAS1BA is the writeable base address register. It is used to remap or offset the PCI PIO window to access other sections of the installed memory. The RFM-5565 firmware prevents the user from entering an invalid Remap Value. The value written must be a multiple of the PCI window size. For example, using a PCI window size of 2 MByte with 64 MByte of installed memory means there are 32 valid base address settings from $00000000 to $03E00000, incrementing by $00200000 (all other bits are masked off when written). Also, a 64 MByte card with a 64 MByte window has no valid base address settings other than the default 0.

Since the PCI window size and the Remap register only affect PCI PIO accesses, DMA (Local-to-PCI and PCI-to-Local) can be used normally to transfer up to $7FFFFF bytes with another location on the PCI bus regardless of the Remap value.

3.7 Example of Network Interrupt Handling

The following is an example of the steps necessary to set up the RFM-5565 to generate a PCI interrupt in response to one of the four basic network interrupts. This example also lists the steps necessary to service that interrupt. When using this example, it is advisable to examine Figure 2-1 on page 26 and Figure 3-1 on page 60 to obtain a visual sense of the circuitry involved.

3.7.1 Setup

1. Clear any prior unscheduled interrupts in the SID1 FIFO by writing zero (0) to the SID1 at PCIBAR2 + offset $24.
2. Clear any prior unscheduled interrupts in the SID2 FIFO by writing zero (0) to the SID2 at PCIBAR2 + offset $2C.
3. Clear any prior unscheduled interrupts in the SID3 FIFO by writing zero (0) to the SID3 at PCIBAR2 + offset $34.
4. Clear any prior unscheduled interrupts in the SID4 FIFO by writing zero (0) to the SID4 at PCIBAR2 + offset $3C.
5. Using a read-modify-write operation, set Bit 07, Bit 02, Bit 01 and Bit 00 high (1) in the LIER register at PCIBAR2 + offset $14. This allows any one of the four basic network interrupts to assert the onboard signal LINTi#, provided the global enable in the LISR is also high (1).
6. Write the value $4000 to the LISR register at PCIBAR2 + offset $10. The value $4000 sets the Global Interrupt Enable (Bit 14) high (1) and clears any unrelated sources. You may prefer to use a read-modify-write operation if other sources in the LISR are to remain unchanged.
7. Using a read-modify-write operation, set Bit 8 and Bit 11 high (1) in the INTCSR register at PCIBAR0 + offset $68. Bit 8 is the PCI Interrupt Enable and Bit 11 is the Local Interrupt Input (LINTi#) Enable.

3.7.2 Servicing Network Interrupts

Read the INTCSR register at PCIBAR0 + offset $68. Verify that the Local Interrupt Input Active (Bit 15) is high (1). If Bit 15 is not high, or if another interrupt source within the INTCSR has priority, then the user's interrupt service routine would take different steps from this point on.

Read the LISR register at PCIBAR2 + offset $10. Determine if the Pending Network Interrupt 4 (Bit 07), the Pending Network Interrupt 3 (Bit 02), the Pending Network Interrupt 2 (Bit 01), or the Pending Network Interrupt 1 (Bit 00) is high (1).

Assuming, for example, the previous step indicates Network Interrupt 2 is pending, read the Interrupt 2 Sender Data FIFO at PCIBAR2 + offset $28 and place the value in the desired user location. If the user is not passing data with the interrupt, then this step is unnecessary and may be skipped.

Read the Interrupt 2 Sender ID FIFO at PCIBAR2 + offset $2C and place the value in the desired user location. This value is the node ID of the source of the network interrupt. Provided that there are no additional network interrupts stored in the Sender ID FIFO, the act of reading this value will de-assert the Pending Network Interrupt 2 bit (Bit 01) in the LISR, which in turn de-asserts the LINTi# line. De-asserting the LINTi# line will de-assert the PCI interrupt.

Maintenance

If a GE product malfunctions, please verify the following:

1. Software version resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact GE for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.** RMA request forms can be obtained from: www.ge-ip.com/rma

GE Technical Support is available at: 1-800-433-2682 in North America, or +1-780-401-7700 for international calls. Requests for Technical Support can be sent to: support.huntsville.ip@ge.com

Or, visit our website:www.ge-ip.com

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

Compliance Information

This chapter provides the applicable information regarding regulatory compliance for the PCIE-5565PIORC. The PCIE-5565PIORC has met the requirements for compliance to the following standards:

CE

GE has evaluated the PCIE-5565PIORC has met the requirements for compliance to the following standards:

- EN55024
- EN55022, Class A
- EN60950-1:2006

International Compliance

It has also met the following international levels.

European Union

- EN 55024:1998/A1:2001/A2:2003 ITE
- EN 55022:2006/A1:2007 (Class A)
- EN 60950-1:2006

United States

- FCC 47 CFR Part 15 Class A
- UL 60950-1 (2nd Edition)

Australia/New Zealand

- AS/NZS CISPR 22:2006 Class A ITE
- EN55022 :2006/A1:2007 (Class A)

Japan

- VCCI (April 2005) Class A using:

Canada

- ICES-003 Issue 4 Class A
- CSA 22.2 No. 60950-1-07

FCC Part 15

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

FCC Class A

NOTE

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

CAUTION

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canadian Regulations

The PCIE-5565PIORC Class A digital apparatus complies with Canadian ICES-003.

NOTE

Any equipment tested and found compliant with FCC Part 15 for unintentional radiators or EN55022 (previously CISPR 22) satisfy ICES-003.

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Additional Resources

For more information, please visit the GE Intelligent Platforms Embedded Systems web site at:

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