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YT8522C/YT8522H/YT8522E/

YT8522A

Datasheet

10/100 FAST ETHERNET TRANSCEIVER

VERSION DRAFT 0.4
DATE 2023-05-15

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Revision History

Revision	Release Date	Summary
Draft 0.1	2022/12/04	draft version
Draft 0.2	2023/03/11	Modify strappin setting and some description errors
Draft 0.3	2023/05/05	Add register overview
Draft 0.4	2023/05/15	Add block diagram and modify pin map

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1. General Description

YT8522 is a low power single-port 10/100 Mbps Ethernet PHY. It provides all physical layer functions needed to transmit and receive data over both standard twisted pair cables transceiver or Fiber PECL interface to an external 100Base-FX optical transceiver module. Additionally, YT8522 provides flexibility to connect to a MAC through a standard MII and RMII interface.

YT8522 uses mixed-signal processing to perform equalization, data recovery, and error correction to achieve robust operation over CAT5 twisted-pair cable or 100Base-FX optical transceiver module.

YT8522 offers integrated built-in self-test and loopback capabilities for ease of use.

YT8522 offers innovative and robust approach for reducing power consumption through EEE, WoL and other programmable energy savings modes.

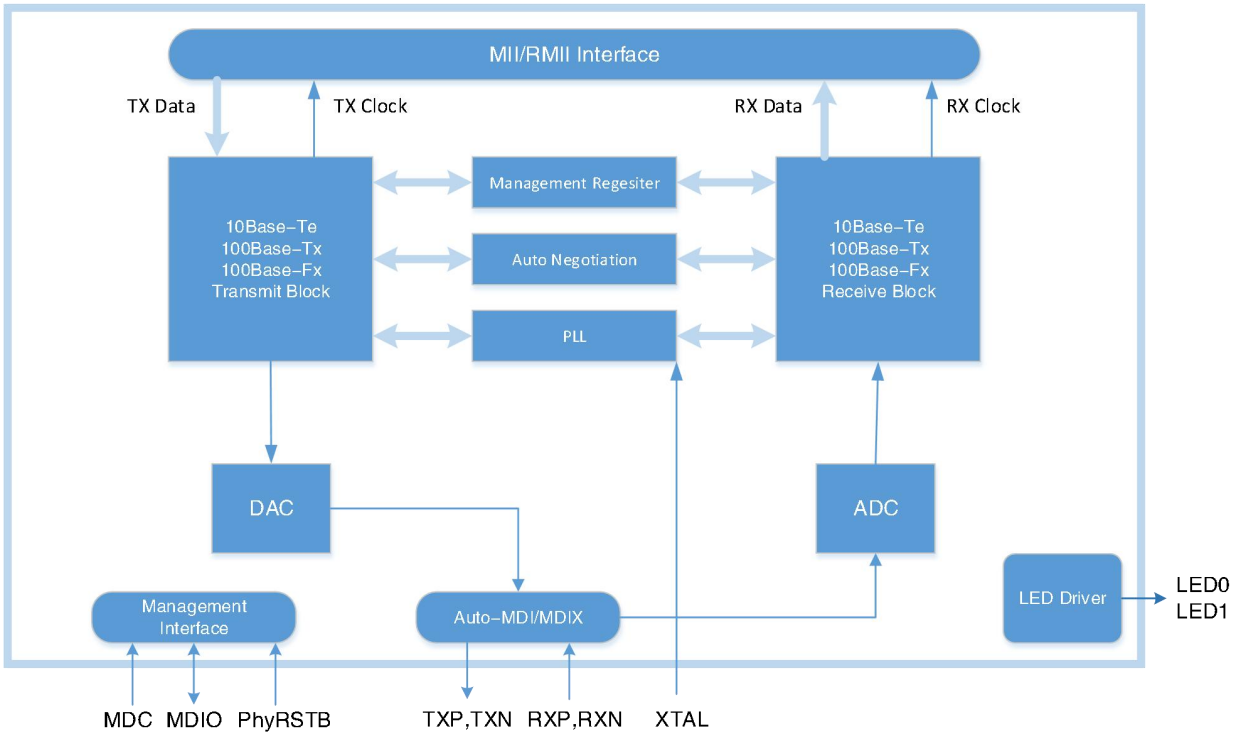
1.1. Features

- Supports IEEE 802.3az (Energy Efficient Ethernet)
- 100Base-TX IEEE 802.3u Compliant
- 10Base-Te IEEE 802.3 Compliant
- Supports MII mode
- Supports RMII mode
- Supports I/O 1.5V/1.8V/2.5V/3.3V (except for Crystal and LED pins)
- Full/Half duplex operation
- 100BASE-FX support (share with MDI pins)
- Twisted pair or fiber mode output
- Supports Auto-negotiation
- Supports Power down mode
- Supports Base Line Wander (BLW) compensation
- Supports Auto MDIX
- Supports Interrupt function
- Supports WOL, Wake on Lan
- Automatic Polarity correction
- 2 sets LED indicator
- 25MHz crystal or external OSC
- 50MHz external OSC input
- Provide 50Mhz clock source for MAC
- Single Power supply, internal LDO
- Package QFN 32, 5x5mm

1.2. Target Applications

- Ethernet Switch
- DTV (Digital TV)
- Communication and Network Riser
- Routers, PON Equipment
- Printer and Office Machine
- MAU(Media Access Unit)

1.3. Block Diagram



2. Pin Assignment

2.1. Pin Map

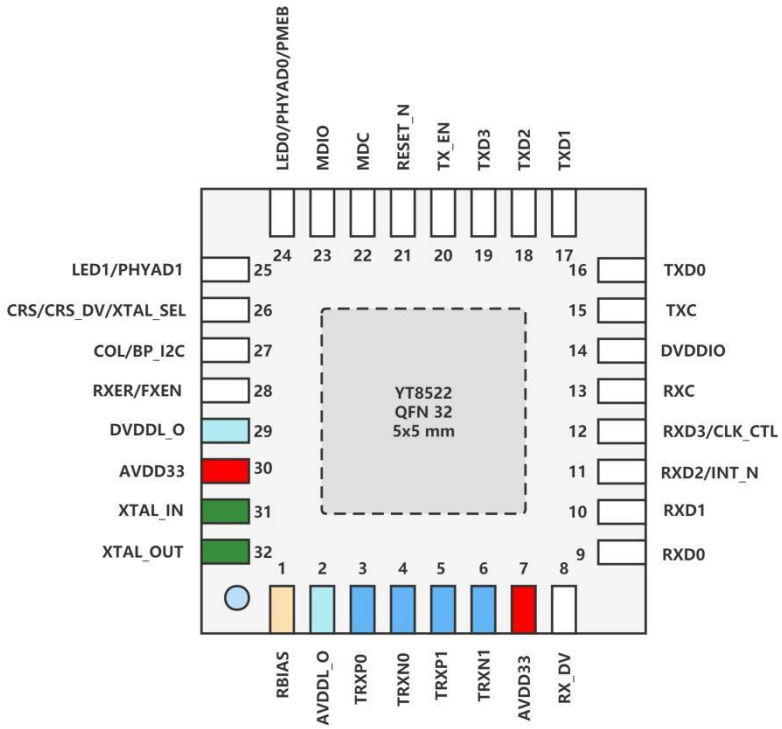


Figure 1.PIN MAP

2.2. Pin Descriptions

- I = Input
- O = Output
- I/O = Bidirectional
- OD = Open–drain output
- PU = Internal pull–up
- PD = Internal pull–down
- HZ = High Impendence during power on reset
- PWR = Power related
- XT = Crystal related

Table 1.Pin Assignment

No.	Name	Type	Description
1	RBIAS	I	Bias Resistor. An external 2.49 kΩ ± 1% resistor must be connected between the RBIAS pin and GND
2	AVDDL_O	PWR/O	Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
3	TRXP0	IO	Transmit/Receive Pairs for channel 0. Differential data from copper media is transmitted and received on the single TRD ± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center–tap power supply.
4	TRXN0	IO	
5	TRXP1	IO	Transmit/Receive Pairs for channel 1. Differential data from copper media is transmitted and received on the single TRD ± signal pair. There are 50Ω internal terminations on each pin. Since this device incorporates voltage driven DAC, it does not require a center–tap power supply.
6	TRXN1	IO	
7	AVDD33	PWR	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
8	RX_DV	O/PD	Receive Data Valid. This pin’s signal is asserted high when received data is present on the RXD[3:0] lines. The signal is de–asserted at the end of the packet. The signal is valid on the rising edge of the RXC. This pin should be pulled low when operating in MII mode. Power On Strapping for MII/RMII selection. 0: MII mode 1: RMII mode An internal weakly pulled low resistor sets this to the default of MII mode. It is possible to use an external 4.7KΩ pulled high resistor to enable RMII mode.After power on, the pin operates as the Receive Data Valid pin.
9	RXD[0]	O/PD	Receive Data [0]
10	RXD[1]	O/PD	Receive Data [1] An internal weakly pulled low resistor sets RXD[1] to the LED function (default). Use an external 4.7KΩ pulled high resistor to enable the WOL function.
11	RXD[2]/INT_N	O/OD/PD	Receive Data [2] When in RMII mode, this pin is used for the interrupt function.
12	RXD[3]/CLK_CTL	O/PD	Receive Data [3] RXD[3]/CLK_CTL pin is the Power On Strapping in RMII Mode. 1: REF_CLK input mode, RMII1 mode 0: REF_CLK output mode, RMII2 mode Note: An internal weakly pulled low resistor sets RXD[3]/CLK_CTL to REF_CLK output mode (default).

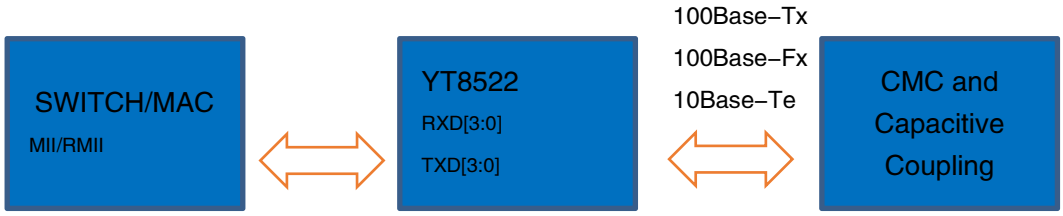
13	RXC	O/PD	Receive Clock. This pin provides a continuous clock reference for RX_DV and RXD [0:3] signals. RXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode.
14	DVDDIO	PWR	Supports 3.3V/2.5V/1.8V/1.5V Digital Power Input. 3.3V/2.5V/1.8V/1.5V power supply for digital circuit. Note:IO level register should be connfigured
15	TXC	IO/PD	MII Mode Transmit Clock. This pin provides a continuous clock as a timing reference for TXD [3:0] and TXEN signals. TXC is 25MHz in 100Mbps mode and 2.5MHz in 10Mbps mode RMII Mode Synchronous 50MHz Clock Reference for Receive, Transmit, and Control Interface. The default direction is reference clock output mode if RXD[3]/CLK_CTL pin floating.
16	TXD[0]	I/PD	Transmit Data [0]
17	TXD[1]	I/PD	Transmit Data [1]
18	TXD[2]	I/PD	Transmit Data [2]
19	TXD[3]	I/PD	Transmit Data [3]
20	TX_EN	I/PD	MII/RMII Mode Transmit Enable. The input signal indicates the presence of valid nibble data on TXD [3:0]. An internal weakly pulled low resistor prevents the bus floating.
21	RESET_N	I,HZ	RESET. Active–low, reset pin for chip.
22	MDC	I/PU	Management Data Clock. This pin provides a clock synchronous to MDIO, which may be asynchronous to the transmit TXC and receive RXC clocks. The clock rate can be up to 12.5MHz. Use an internal weakly pulled high resistor to prevent the bus floating.
23	MDIO	IO/PU	Management Data Input/Output. This pin provides the bi–directional signal used to transfer management information
24	LED0/PHYAD[0]/ PMEB	O/OD/PD	LED 0, Link On/Off. PHY address 0 selection
25	LED1/PHYAD[1]	O/PD	LED 1, Link On/Off,Active blink. PHY address 1 selection
26	CRS/CRS_DV/ XTAL_SEL	O/PD	MII mode: Carrier Sense. This pin’s signal is asserted high if the media is not in Idle state. RMII mode: Carrier Sense/Receive Data Valid. CRS_DV shall be asserted by the PHY when the receive medium is non–idle. This pin status is latched at power on reset to determine Reference Clock

			Input Selection . 1:Reference Clock from TXC 0:Reference Clock from XTAL An internal weakly pulled low resistor sets this to select Reference Clock from XTAL.It is possible to use an external 4.7KΩ pulled high resistor to select Reference Clock from TXC.After power on,the pin operates as the CRS/CRS_DV pin.
27	COL/BP_I2C	O/PD	Collision Detect. COL is asserted high when a collision is detected on the media. It is possible to use an external 4.7KΩ pulled high resistor to bypass I2C load.After power on,the pin operates as the collision detect pin.
28	RXER/FXEN	O/PD	Receive Error. 100FX/UTP Enable. This pin status is latched at power on reset to determine the media mode to operate in. 1:Fiber mode 0:UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode.It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode.After power on,the pin operates as the receive error pin.
29	DVDDL_O	PWR/O	DVDDL Power Output. Be sure to connect a 1uF +0.1uF ceramic capacitor for decoupling purposes.
30	AVDD33	PWR	3.3V Analog Power Input. 3.3V power supply for analog circuit; should be well decoupled.
31	XTAL_IN	XT	25 MHz Crystal Input Pin. If use external oscillator or clock from another device. 1. When an external 25Hhz oscillator or clock from another device drivers XTAL_OUT. XTAL_IN must be shorted to GND 2. When an external 25Hhz oscillator or clock from another device drivers XTAL_IN; keep the XTAL_OUT floating.
32	XTAL_OUT	XT	25 MHz Crystal Output Pin. If use external oscillator or clock from another device. 1. When an external 25Hhz oscillator or clock from another device drivers XTAL_OUT. XTAL_IN must be shorted to GND 2. When an external 25Hhz oscillator or clock from another device drivers XTAL_IN; keep the XTAL_OUT floating.
33	EPAD	GND	Exposed ground pad on back of the chip, tie to ground

3. Function Description

3.1. Application Diagram

3.1.1. 100Base-Tx/100Base-Fx/10Base-Te application



3.2. MII Interface

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 10BASE-Te, 100BASE-TX/FX,. The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin-count limitations, the YT8522 supports a subset of MII signals. This subset includes all MII signals except TX_ER.

3.3. RMII Interface

Reduced media-independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock frequency.

3.4. Management Interface

The Status and Control registers of the device are accessible through the MDIO and MDC serial interface. The functional and electrical properties of this management interface comply with IEEE 802.3, Section 22 and also support MDC clock rates up to 12.5 MHz

3.5. DAC

The digital-to-analog converter (DAC) transmits MLT3, and Manchester coded symbols. The transmit DAC performs signal wave shaping that reduces electromagnetic interference (EMI). The transmit DAC uses voltage driven output with internal terminations and hence does not require external components or magnetic supply for operation.

3.6. ADC

Receive channel has its own analog-to-digital converter (ADC) that samples the incoming data on the receive channel and feeds the output to the digital data path.

3.7. Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference (ISI) created by the channel. The equalizer accepts sampled data from the analog-to-digital converter (ADC) on channel and produces equalized data. The coefficients of the equalizer are adaptive to accommodate varying conditions of cable quality and cable length.

3.8. Auto-Negotiation

The YT8522 negotiates its operation mode using the auto negotiation mechanism according to IEEE 802.3 clause 28 over the copper media. Auto negotiation supports choosing the mode of operation automatically by comparing its own abilities and received abilities from link partner. The advertised abilities include:

a) Speed: 10/100Mbps

b) Duplex mode: full duplex and/or half duplex

c) Pause

Auto negotiation is initialized when the following scenarios happen:

a) Power-up/Hardware/Software reset

b) Auto negotiation restart

c) Transition from power-down to power up

d) Link down

Auto negotiation is enabled for YT8522 by default, and can be disable by software control.

3.9. Polarity Detection and Auto Correction

YT8522 can detect and correct two types of cable errors: swapping of pairs within the UTP cable and swapping of wires within a pair.

For 10BASE-Te/100BASE-TX, YT8522 can handle both cable errors at the same time.

3.10. EEE

EEE is IEEE 802.3az, an extension of the IEEE 802.3 standard. EEE defines support for the PHY to operate in Low Power Idle (LPI) mode which, when enabled, supports QUIET times during low link utilization allowing both link partners to disable portions of each PHY's circuitry and save power.

4. Operational Description

4.1. Reset

YT8522 have a hardware reset pin(RESET_N) which is low active. RESET_N should be active for at least 10ms to make sure all internal logic is reset to a known state. Hardware reset should be applied after power up.

RESET_N is also used as enable for power on strapping. After RESET_N is released , YT8522 latches input value on POS related pins are used as configuration information which provides flexibility in application without mdio access.

YT8522 also provides a software reset control registers which are used to reset all internal logic except some mdio configuration registers. For detailed information about what register will be reset by software reset, please refer to register table.

4.2. Strapping pins Setting

4.2.1. POS

Table 2.Power on strapping

No.	Name	POS	Internal Pull/Down	Description
24	LED0/PHYAD[0]	phy_address[0]	Pull Down	The PHY address is 00~11 config by phy_address[1:0].Wol_led_sel=1, this PAD works as PMEB, it shall be external pull–up, then phy_address[0] always =1.
25	LED1/PHYAD[1]	phy_address[1]	Pull Down	The PHY address is 00~11 config by phy_address[1:0]
10	RXD[1]	Wake on LAN selection	Pull Down	The power on strapping value of PAD RXD1, Wol_led_sel, determines the PAD LED0 working as LED0 or PMEB. 1, LED0 works as PMEB (WOL interrupt) 0, LED0 works as LED0.
12	RXD[3]/ CLK_CTL	Clock control	Pull Down	The power–on strapping value of {RX_DV, RXD3} determines the xMII mode:

8	RX_DV	MII/RMII mode selection	Pull Down	{RX_DV, RXD3}=2’b00 means MII mode; {RX_DV, RXD3}=2’b01 means ReMII mode; {RX_DV, RXD3}=2’b10 means RMII2 mode, TXC 50Mhz reference clock is output. {RX_DV, RXD3}=2’b11 means RMII1 mode, TXC 50Mhz reference clock is input.
26	CRS/CRS_DV/ XTAL_SEL	Reference Clock selection	Pull Down	This pin status is latched at power on reset to determine Reference Clock Input Selection . 1:Reference Clock from TXC 0:Reference Clock from XTAL An internal weakly pulled low resistor sets this to select Reference Clock from XTAL.It is possible to use an external 4.7KΩ pulled high resistor to select Reference Clock from TXC.After power on,the pin operates as the CRS/CRS_DV pin.
27	COL/BP_I2C	Bypass I2C load	Pull Down	It is possible to use an external 4.7KΩ pulled high resistor to bypass I2C load.After power on,the pin operates as the collision detect pin.
28	RX_ER/FXEN	FX_EN	Pull Down	This pin status is latched at power on reset to determine the media mode to operate in. 1:Fiber mode 0:UTP mode An internal weakly pulled low resistor sets this to the default of UTP mode.It is possible to use an external 4.7KΩ pulled high resistor to enable fiber mode.After power on,the pin operates as the receive error pin.

4.2.2. Phy address

Table 3.Power on strapping-Phy address

Pin 25 LED1/ PHYAD[1] (PD)	Pin 24 LED0/ PHYAD[0] (PD)	PHY address
0	0	00
0	1	01
1	0	10
1	1	11

4.2.3. Mode config

Table 4.Power on strapping-Mode config

Pin 8 RX_DV (PD)	Pin 12 RXD3 (PD)	Mode
0	0	MII
0	1	ReMII, Reverse MII Mode
1	0	RMII2, TXC 50Mhz reference clock is output by default
1	1	RMII1, TXC 50Mhz reference clock is input

4.2.4. Wake on lan selection

Table 5.Power on strapping-Wake on lan

Pin 10 RXD1 (PD)	Function	Mote
0	LED Mode	Pin 24 is LED0
1	WOL Mode	Pin 24 is PMEB, Must external pull up

4.3. XMII Interface

YT8522 support 4 kinds of MII related interfaces: MII, RMII1, RMII2 and REMII.

4.3.1. MII

The Media Independent Interface (MII) is the digital data interface between the MAC and the physical layer that can be enabled when the device is functioning in 10BASE–Te, 100BASE–TX, The original MII transmit signals include TX_EN, TXC, TXD[3:0], and TX_ER. The receive signals include RX_DV, RXC, RXD[3:0], and RX_ER. The media status signals include CRS and COL. Due to pin–count limitations, the YT8522 supports a subset of MII signals. This subset includes all MII signals except TX_ER. For 100M application, TXC and RXC are 25MHz; for 10M application, TXC and RXC are 2.5MHz. TXC and RXC are output in this case.

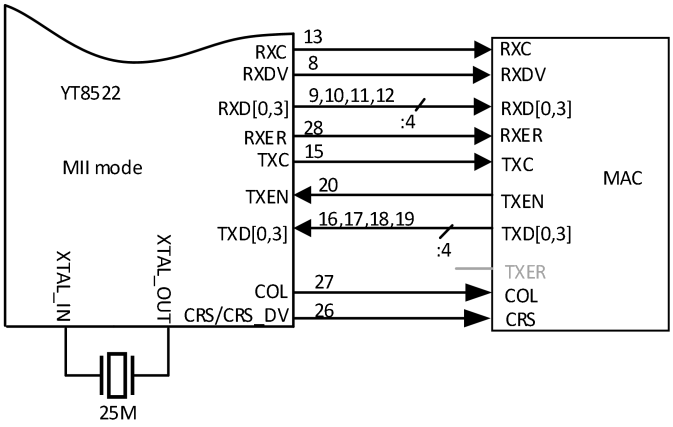


Figure 2. Connection diagram of MII

4.3.2. RMII

Reduced media–independent interface (RMII) is a standard which was developed to reduce the number of signals required to connect a PHY to a MAC. If this interface is active, the number of data signal pins required to and from the MAC is reduced to half by doubling clock speed compared to MII. It has 7 signals: REF_CLK, TX_EN, TXD[1:0], RX_DV and RXD[1:0]. YT8522 uses TXC or Cystal as REF_CLK. For 100M application, REF_CLK is 50MHz; for 10M application, REF_CLK is still 50MHz, data will be duplicated for 10 times in 20ns cycles. YT8522 supports two types of connection method;

1. RMII1 mode: This is fully conforming to RMII standard.For RMII1, YT8522 supports Cystal 25M/50M ,TXC 50M without Cystal.

2. RMII2 mode: TXC will be 50MHz output to MAC.

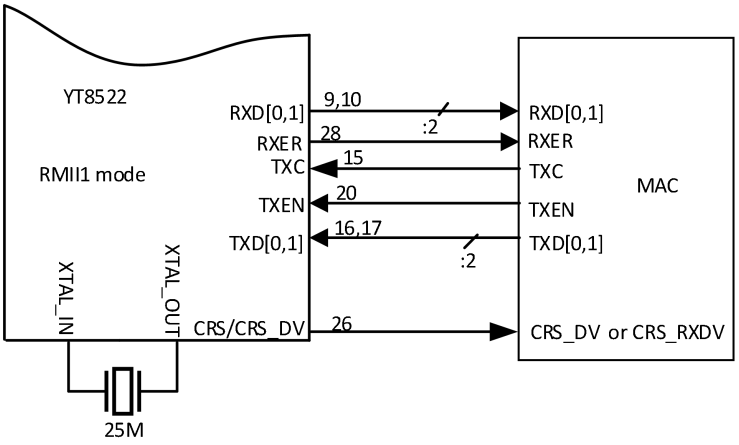


Figure 3. Connection diagram of RMII1(with 25MHz and 50MHz clock)

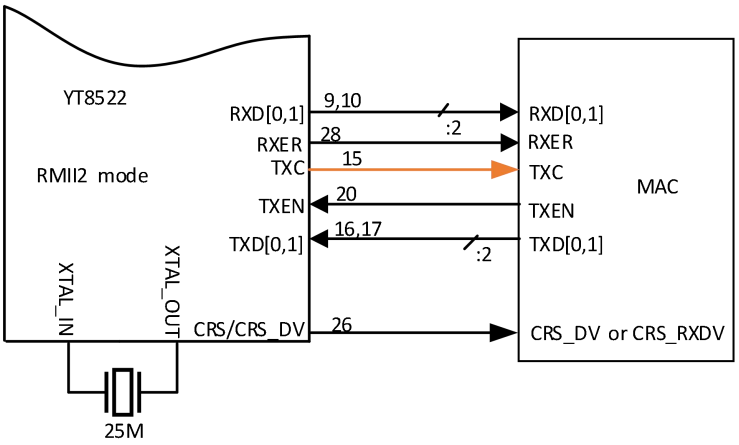


Figure 4. Connection diagram of RMII2

4.3.3. REMII interface

Reverse media independent interface is the opposite of MII interface. The only difference is the direction of tx clock and rx clock. For MII, tx clock and rx clock are output; for REMII, tx clock and rx clock are input. REMII interface are used for back to back connection of two phys.

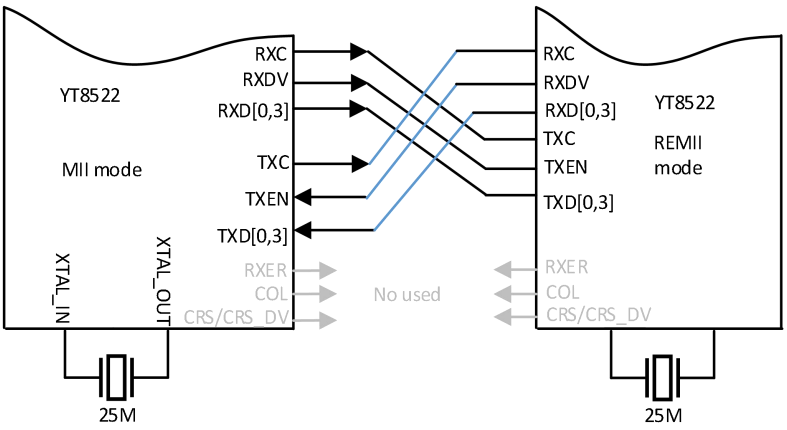


Figure 5. Connection diagram of REMII

4.4. Loopback Mode

There are three loopback modes in YT8522.

4.4.1. Internal loopback:

In Internal loopback mode, YT8522 feed transmit data to receive path in chip.

Configure bit 14 of mii register(address 0h0) to enable internal loopback mode. For 10Base–Te and 100Base–Tx, YT8522 feeds digital DAC data to ADC directly.

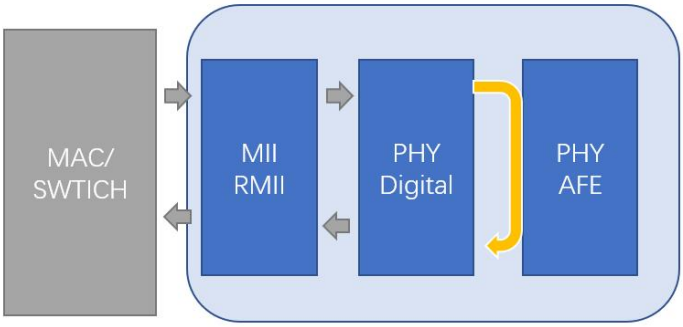


Figure 6. Internal loopback

4.4.2. External loopback

In external loopback mode, YT8522 feed transmit data to receive path out of chip. For 10Base–Te and 100Base–Tx, just connect TRX_P0/N0 to TRX_P1/N1.

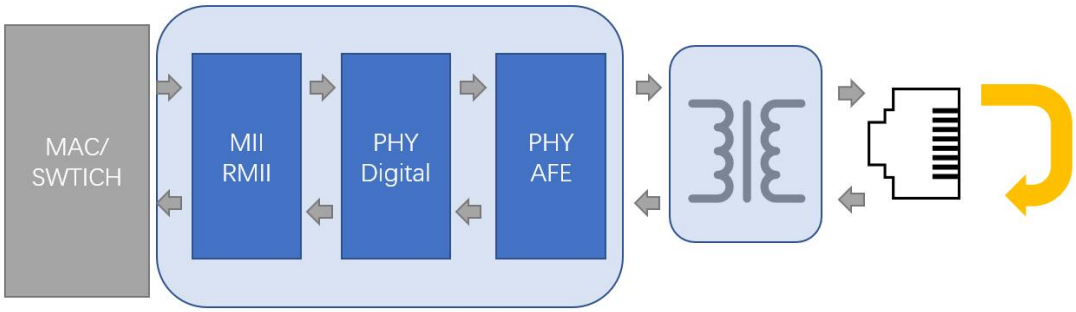


Figure 7. External loopback

4.4.3. Remote loopback

In remote loopback mode, YT8522 feed MII receive data to transmit path in chip. Configure bit 11 of extended register(address 0h4000) and for TRX interface, just connect to link partner normally.

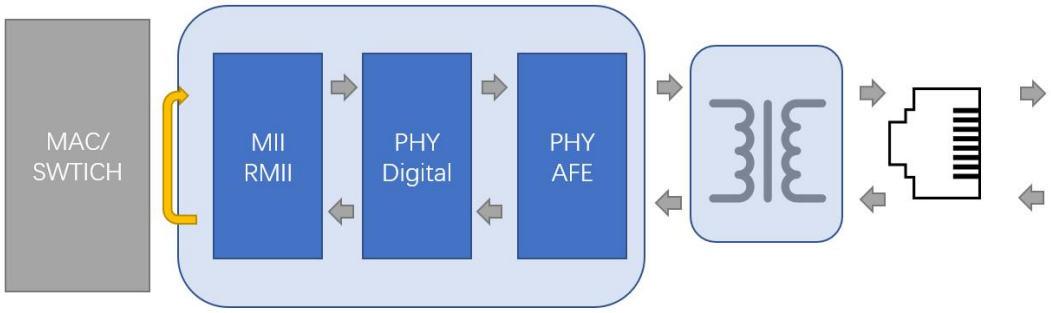


Figure 8. Remote loopback

4.5. Wake on Lan

4.5.1. WOL

Wake-on-LAN (WOL) is a mechanism to manage and regulate the total network power consumption.YT8522 supports automatic detection of a specific frame and notification via dedicated hardware interrupt pin or general PHY interrupt pin. The specific frame contains a specific data sequence located anywhere inside the packet. The data sequence consists of 6 bytes of consecutive 1 (0xFFFFFFFFFFFF), followed by 16 repetitions of the MAC address of the computer to be waked up. The 48-bit MAC address is written in EXT 0x4004, 0x4005, 0x4006 registers.

For example, to write a specific MAC address (0xAAAABBBBCCCC) to PHY, write EXT 0x4004 = 0xAAAA, 0x4005 = 0xBBBB, and 0x4006 = 0xCCCC. The PHY internal MAC address can be set to any value.

NOTE: The MAC address is not a real MAC address and is only a symbol to indicate the content of the frame.The WOL mechanism is enabled via EXT 0x4000 bit2. POS RXD[1] can't control enable or disable the WOL mechanism but only control pad LED0 working as WOL interrupt.

4.5.2. WOL Interrupt

YT8522 support dedicated WOL interrupt pin. When the pad RXD[1] is externally PULL UP, pad LED0 will work as WOL interrupt.

If EXT 0x4003 bit7 is 0, the dedicated WOL interrupt is programmed to a level, otherwise, it's programed to a pulse; either is active low. When it's programmed to a pulse, the pulse width can be programmed via EXT 0x4003 bit9:8.

WOL interrupt is also wire–and to general PHY interrupt RXD[2]_INTN when the bit6 INT_WOL in Interrupt enable register (MII Register 0x12) is set to 1. If the general PHY interrupt is triggered by WOL, it can be cleared by reading MII register 0x13 bit6.

NOTE:

When general PHY interrupt is used to monitor WOL interrupt, EXT 0x4003 bit7 should be 1, otherwise, the general PHY interrupt can't be read cleared.

Because PHY requires to receive packets from the line side, PHY cannot be powered down. If the link partner supports Energy Efficient Ethernet function, both ends can use EEE mode to save more power.

MII register 0x0 bit10 ISOLATE: When this bit is set to 1, the xMII output pins are HighZ. The xMII inputs are ignored.

5. Register Overview

5.1. MII Management Interface Clause 22 Register Programming

The YT8522 transceiver is designed to be fully compliant with the MII clause of the IEEE 802.3u Ethernet specification.

The MII management interface registers are written and read serially, using the MDIO and MDC pins.

A clock of up to 12.5 MHz must drive the MDC pin of the YT8512. Data transferred to and from the MDIO pin is synchronized with the MDC clock. The following sections describe what each MII read or write instruction contains.

Notation	Description
RW	Read and write
SC	Self–clear
RO	Read only
LH	Latch high
LL	Latch Low
RC	Read clear
SWC	Software reset clear

5.2. MII Registers

5.2.1. Mii register 00H: Basic control register

Bit	Symbol	Access	Default	Description
15	Reset	RW SC	1’b0	PHY Software Reset. Writing 1 to this bit causes immediate PHY reset. Once the operation is done, this bit is cleared automatically. 0: Normal operation 1: PHY reset
14	Loopback	RW SWC	1’b0	Internal loopback control 1’b0: disable loopback 1’b1: enable loopback

<table>
<tr><td>13</td><td>Speed Selection(LSB)</td><td>RW</td><td>1’b0</td><td>LSB of speed_selection[1:0]. Link speed can be selected via either the Auto–Negotiation process, or manual speed selection speed_selection[1:0]. Speed_selection[1:0] is valid when Auto–Negotiation is disabled by clearing bit 0.12 to zero.
<table>
<tr><th>Bit 6</th><th>Bit 13</th><th></th></tr>
<tr><td>1</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>1000Mb/s</td></tr>
<tr><td>0</td><td>1</td><td>100Mb/s</td></tr>
<tr><td>0</td><td>0</td><td>10Mb/s</td></tr>
</table></td></tr>
<tr><td>12</td><td>Autoneg_En</td><td>RW</td><td>1’b1</td><td>1: to enable auto–negotiation;
0: auto–negotiation is disabled.</td></tr>
<tr><td>11</td><td>Power_down</td><td>RW
SWC</td><td>1’b0</td><td>=1: Power down
=0: Normal operation
When the port is switched from power down to normal operation, software reset and Auto–Negotiation are performed even bit[15] RESET and bit[9] RESTART_AUTO_NEGOTIATION are not set by the user.</td></tr>
<tr><td>10</td><td>Isolate</td><td>RW
SWC</td><td>1’b0</td><td>Isolate phy from MII/RMII: PHY will not respond to xMII TXD/TX_EN, and present high impedance on RXD/RX_DV.
1’b0: Normal mode
1’b1: Isolate mode</td></tr>
<tr><td>9</td><td>Re_Autoneg</td><td>RW
SWS
SC</td><td>1’b0</td><td>Auto–Negotiation automatically restarts after hardware or software reset regardelss of bit[9] RESTART.
=1: Restart Auto–Negotiation Process
=0: Normal operation</td></tr>
<tr><td>8</td><td>Duplex_Mode</td><td>RW</td><td>1’b1</td><td>The duplex mode can be selected via either the Auto–Negotiation process or manual duplex selection. Manual duplex selection is allowed when Auto–Negotiation is disabled by setting bit[12] AUTO_NEGOTIATION to 0.
=1: Full Duplex
=0: Half Duplex</td></tr>
</table>

7	Collision_Test	RW SWC	1’b0	Setting this bit to 1 makes the COL signal asserted whenever the TX_EN signal is asserted. =1: Enable COL signal test =0: Disable COL signal test
6	Speed_ Selection(MSB)	RW	1’b1	See bit13.
5:0	Reserved	RO	5’b0	Reserved. Write as 0, ignore on read

5.2.2. Mii register 01H: Basic status register

Bit	Symbol	Access	Default	Description
15	100Base-T4	RO	1’b0	PHY doesn’t support 100BASE-T4
14	100Base-X_Fd	RO	1’b1	PHY supports 100BASE-X_FD
13	100Base-X_Hd	RO	1’b1	PHY supports 100BASE-X_HD
12	10Mbps_Fd	RO	1’b1	PHY supports 10Mbps_Fd
11	10Mbps_Hd	RO	1’b1	PHY supports 10Mbps_Hd
10	100Base-T2_Fd	RO	1’b0	PHY doesn’t support 100Base-T2_Fd
9	100Base-T2_Hd	RO	1’b0	PHY doesn’t support 100Base-T2_Hd
8	Extended_Status	RO	1’b1	Whether support extended status register in 0Fh 0: Not supported 1: Supported
7	Unidirect_Ability	RO	1’b0	1’b0: PHY able to transmit from MII only when the PHY has determined that a valid link has been established 1’b1: PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	Mf_Preamble_Suppression	RO	1’b1	1’b0: PHY will not accept management frames with preamble suppressed 1’b1: PHY will accept management frames with preamble suppressed
5	Autoneg_Complete	RO SWC	1’b0	1’b0: Auto-negotiation process not completed 1’b1: Auto-negotiation process completed
4	Remote_Fault	RO RC SWC LH	1’b0	1’b0: no remote fault condition detected 1’b1: remote fault condition detected
3	Autoneg_Ability	RO	1’b1	1’b0: PHY not able to perform Auto-negotiation 1’b1: PHY able to perform Auto-negotiation

2	Link_Status	RO LL SWC	1’b0	Link status 1’b0: Link is down 1’b1: Link is up
1	Jabber_Detect	RO RC LH SWC	1’b0	10BaseTe jabber detected 1’b0: no jabber condition detected 1’b1: Jabber condition detected
0	Extended_Capability	RO	1’b1	To indicate whether support EXTs, to access from address register 1Eh and data register 1Fh 1’b0: Not supported 1’b1: Supported

5.2.3. Mii register 02H: PHY identification register1

Bit	Symbol	Access	Default	Description
15:0	Phy_Id	RO	16’b0	Bits 3 to 18 of the Organizationally Unique Identifier

5.2.4. Mii register 03H: PHY identification register2

Bit	Symbol	Access	Default	Description
15:10	Phy_Id	RO	6’b0	Bits 19 to 24 of the Organizationally Unique Identifier
9:4	Type_No	RO	6’h12	
3:0	Revision_No	RO	4’h8	4 bits manufacturer’s revision number

5.2.5. MII register 04H: Auto-Negotiation advertisement

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	1’b0	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down If 1000BASE-T is advertised, the required next pages are automatically transmitted.

				This bit must be set to 0 if no additional next page is needed. =1: Advertise =0: Not advertised
14	Reserved	RO	1’b0	Reserved
13	Remote_Fault	RW	1’b0	=1: Set Remote Fault bit =0: Do not set Remote Fault bit
12	Extended_Next_Page	RW	1’b1	Extended next page enable control bit =1: Local device supports transmission of extended next pages =0: Local device does not support transmission of extended next pages.
11	Asymmetric_Pause	RW	1’b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto−Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Asymmetric Pause =0: No asymmetric Pause
10	Pause	RW	1’b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto−Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down

				=1: MAC PAUSE implemented =0: MAC PAUSE not implemented
9	100BASE–T4	RO	1’b0	=1: Able to perform 100BASE–T4 =0: Not able to perform 100BASE–T4 Always 0
8	100BASE–TX_Full_Duplex	RW	1’b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto–Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
7	100BASE–TX_Half_Duplex	RW	1’b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto–Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
6	10BASE–Te_Full_Duplex	RW	1’b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto–Negotiation is triggered by

				writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
5	10BASE-Te_Half_Duplex	RW	1’b1	This bit is updated immediately after the writing operation; however the configuration does not take effect until any of the following occurs: • Software reset is asserted by writing register 0x0 bit[15] • Restart Auto-Negotiation is triggered by writing register 0x0 bit[9] • The port is switched from power down to normal operation by writing register 0x0 bit[11] • Link goes down =1: Advertise =0: Not advertised
4:0	Selector_Field	RW	5’b00001	Selector Field mode. 00001 = IEEE 802.3

5.2.6. MII register 05H: Auto-Negotiation link partner ability

Bit	Symbol	Access	Default	Description
15	1000Base-X_Fd	RO SWC	1’b0	Received Code Word Bit 15 =1: Link partner is capable of next page =0: Link partner is not capable of next page
14	ACK	RO SWC	1’b0	Acknowledge. Received Code Word Bit 14 =1: Link partner has received link code word =0: Link partner has not received link code word
13	REMOTE_FAULT	RO SWC	1’b0	Remote Fault. Received Code Word Bit 13 =1: Link partner has detected remote fault =0: Link partner has not detected remote fault
12	RESERVED	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 12

11	ASYMMETRIC_PAUSE	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 11 =1: Link partner requests asymmetric pause =0: Link partner does not request asymmetric pause
10	PAUSE	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 10 =1: Link partner supports pause operation =0: Link partner does not support pause operation
9	100BASE–T4	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 9 =1: Link partner supports 100BASE–T4 =0: Link partner does not support100BASE–T4
8	100BASE–TX_FULL_DUPLEX	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 8 =1: Link partner supports 100BASE–TX full–duplex =0: Link partner does not support 100BASE–TX full–duplex
7	100BASE–TX_HALF_DUPLEX	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 7 =1: Link partner supports 100BASE–TX half–duplex =0: Link partner does not support 100BASE–TX half–duplex
6	10BASE–Te_FULL_DUPLEX	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 6 =1: Link partner supports 10BASE–Te full–duplex =0: Link partner does not support 10BASE–Te full–duplex
5	10BASE–Te_HALF_DUPLEX	RO SWC	1’b0	Technology Ability Field. Received Code Word Bit 5 =1: Link partner supports 10BASE–Te half–duplex =0: Link partner does not support 10BASE–Te half–duplex
4:0	SELECTOR_FIELD	RO SWC	5’h0	Selector Field Received Code Word Bit 4:0

5.2.7. MII register 06H: Auto-Negotiation expansion register

Bit	Symbol	Access	Default	Description
15:5	Reserved	RO	11’h0	Always 0
4	Parallel_Detection_fault	RO RC LH SWC	1’b0	=1: Fault is detected =0: No fault is detected
3	Link_partner_next_page able	RO LH SWC	1’b0	=1: Link partner supports Next page =0: Link partner does not support next page
2	Local_Next_Page_able	RO	1’b1	=1: Local Device supports Next Page =0: Local Device does not Next Page
1	Page_received	RO RC LH	1’b0	=1: A new page is received =0: No new page is received
0	Link_Partner_Auto_negotiation_able	RO	1’b0	=1: Link partner supports auto-negotiation =0: Link partner does not support auto-negotiation

5.2.8. MII register 07H: Auto-Negotiation Next Page register

Bit	Symbol	Access	Default	Description
15	Next_Page	RW	1’b0	Transmit Code Word Bit 15 =1: The page is not the last page =0: The page is the last page
14	Reserved	RO	1’b0	Transmit Code Word Bit 14
13	Message_page_mode	RW	1’b1	Transmit Code Word Bit 13 =1: Message Page =0: Unformatted Page
12	Ack2	RW	1’b0	Transmit Code Word Bit 12 =1: Comply with message =0: Cannot comply with message
11	Toggle	RO	1’b0	Transmit Code Word Bit 11 =1: This bit in the previously exchanged Code Word is logic 0 =0: The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message_Unformatte	RW	11’h1	Transmit Code Word Bits [10:0].

	D_Field			These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

5.2.9. MII register 08H: Auto-Negotiation link partner Received Next Page register

Bit	Symbol	Access	Default	Description
15	Next_Page	RO	1’b0	Received Code Word Bit 15 =1: This page is not the last page =0: This page is the last page
14	Reserved	RO	1’b0	Received Code Word Bit 14
13	Message_page_mode	RO	1’b0	Received Code Word Bit 13 =1: Message Page =0: Unformatted Page
12	Ack2	RO	1’b0	Received Code Word Bit 12 =1: Comply with message =0: Cannot comply with message
11	Toggle	RO	1’b0	Received Code Word Bit 11 =1: This bit in the previously exchanged Code Word is logic 0 =0: The Toggle bit in the previously exchanged Code Word is logic 1
10:0	Message_Unformatte D_Field	RO	11’b0	Received Code Word Bit 10:0 These bits are encoded as Message Code Field when bit[13] is set to 1, or as Unformatted Code Field when bit[13] is set to 0.

5.2.10. MII register 0AH: MASTER-SLAVE status register

Bit	Symbol	Access	Default	Description
15	Master_Slave_Configuration_Fault	RO RC SWC LH	1’b0	This register bit will clear on read, rising of MII 0.12 and rising of AN complete. =1: Master/Slave configuration fault detected =0: No fault detected
14	Master_Slave_Configuration_Resolution	RO	1’b0	This bit is not valid

				unless register 0x1 bit5 is 1. =1: Local PHY configuration resolved to Master =0: Local PHY configuration resolved to Slave
13	Local_Receiver_Status	RO	1’b0	=1: Local Receiver OK =0: Local Receiver not OK Always 0.
12	Remote_Receiver_Status	RO	1’b0	=1: Remote Receiver OK =0: Remote Receiver not OK Always 0.
11	Link Partner_ 1000Base−T_Full_Duplex_Capability	RO	1’b0	This bit is not valid unless register 0x1 bit5 is 1. =1: Link Partner supports 1000BASE−T half duplex =0: Link Partner does not support 1000BASE−T half duplex
10	Link_Partner_1000Base−T_Half_Duplex_Capability	RO	1’b0	This bit is not valid unless register 0x1 bit5 is 1. =1: Link Partner supports 1000Base−T full duplex =0: Link Partner does not support 1000Base−T full duplex
9:8	Reserved	RO	2’b0	Always 0
7:0	Idle_Error_Count	RO SC	8’b0	Counter for Idle errors

5.2.11. MII register 0DH: MMD access control register

Bit	Symbol	Access	Default	Description
15:14	Function	RW	2’b0	00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only

13:5	Reserved	RO	9’b0	Always 0
4:0	DEVAD	RW	5’b0	MMD register device address. 00001 = MMD1 00011 = MMD3 00111 = MMD7

5.2.12. MII register 0EH: MMD access data register

Bit	Symbol	Access	Default	Description
15:0	Address_data	RW	16’b0	If register 0xD bits [15:14] are 00, this register is used as MMD DEVAD address register. Otherwise, this register is used as MMD DEVAD data register as indicated by its address register.

5.2.13. Mii register 0FH: Extended status register

Bit	Symbol	Access	Default	Description
15	1000Base–X_Fd	RO	1’b0	PHY not able to support 1000Base–X_Fd
14	1000Base–X_Hd	RO	1’b0	PHY not able to support 1000Base–X_Hd
13	1000Base–T_Fd	RO	1’b0	PHY not able to support 1000Base–T_Fd
12	1000Base–T_Hd	RO	1’b0	PHY not able to support 1000Base–T_Hd
11:8	Reserved	RO	1’b0	Reserved
7	100Base–T1	RO	1’b1	Reserved
6	1000Base–T1	RO	1’b0	Reserved
5:0	Reserved	RO	6’b0	Reserved

5.2.14. MII register 10H: PHY specific function control register

Bit	Symbol	Access	Default	Description
15:7	Reserved	RO	9’b0	Always 0.
6:5	Cross_md	RW	2’b11	Changes made to these bits disrupt normal operation, thus a software reset is mandatory after the change. And the configuration does not take effect until software reset. 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Int_polar_sel	RW	1’b0	No use.

3	Crs_on_tx	RW	1’b0	This bit is effective in 10BASE-Te half-duplex mode and 100BASE-TX mode: =1: Assert CRS on transmitting or receiving =0: Never assert CRS on transmitting, only assert it on receiving.
2	En_sqe_test	RW	1’b0	=1: SQE test enabled =0: SQE test disabled Note: SQE Test is automatically disabled in full-duplex mode regardless the setting in this bit.
1	En_pol_inv	RW	1’b1	If polarity reversal is disabled, the polarity is forced to be normal in 10BASE-Te. =1: Polarity Reversal Enabled =0: Polarity Reversal Disabled
0	Dis_jab	RW	1’b0	Jabber takes effect only in 10BASE-Te =1: Disable jabber function =0: Enable jabber function

5.2.15. MII register 11H: PHY specific status register

Bit	Symbol	Access	Default	Description
15:14	Speed_mode	RO	2’b00	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	1’b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. =1: Full-duplex =0: Half-duplex
12	Page_Received_real-time	RO	1’b0	=1: Page received =0: Page not received
11	Speed_and_Duplex_Resolved	RO	1’b0	This bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled =1: Resolved =0: Not resolved
10	Link_status_real-time	RO	1’b0	=1: Link up

				=0: Link down
9:7	Reserved	RO	3’b111	Always 3’b111.
6	MDI_Crossover_Status	RO	1’b0	This status bit is valid only when bit11 is 1. Bit11 is set when Auto–Negotiation is completed or Auto–Negotiation is disabled. The bit value depends on register 0x10 “ PHY specific function control register ” bits6~bit5 configurations. Register 0x10 configurations take effect after software reset. =1: MDIX =0: MDI
5	Wirespeed_downgrade	RO	1’b0	=1: Downgrade =0: No Downgrade
4:2	Reserved	RO	3’b0	Always 0.
1	Polarity_Real_Time	RO	1’b0	=1: Reverted polarity =0: Normal polarity
0	Jabber_Real_Time	RO	1’b0	=1: Jabber is asserted. =0: No jabber

5.2.16. MII register 12H: Interrupt Mask Register

Bit	Symbol	Access	Default	Description
15	Auto–Negotiation_Error_int _mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
14	Speed_Changed_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
13	Duplex_changed_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
12	Page_Received_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
11	Link_Failed_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
10	Link_Succeed_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
9	Reserved	RW	1’b0	Reserved
8	Reserved	RW	1’b0	Reserved
7	Reserved	RW	1’b0	Reserved
6	WOL_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable

5	Wirespeed_downgraded_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
4:2	Reserved	RW	3’b0	No used.
1	Polarity_changed_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable
0	Jabber_Happened_int_mask	RW	1’b0	=1: Interrupt enable =0: Interrupt disable

5.2.17. MII register 13H: Interrupt Status Register

Bit	Symbol	Access	Default	Description
15	Auto–Negotiation_Error_INT	RO RC	1’b0	Error can take place when any of the following happens: • MASTER/SLAVE does not resolve correctly • Parallel detect fault • No common HCD • Link does not come up after negotiation is complete • Selector Field is not equal • flp_receive_idle=true while Autoneg Arbitration FSM is in NEXT PAGE WAIT state =1: Auto–Negotiation Error takes place =0: No Auto–Negotiation Error takes place
14	Speed_Changed_INT	RO RC	1’b0	=1: Speed changed =0: Speed not changed
13	Duplex_changed_INT	RO RC	1’b0	=1: duplex changed =0: duplex not changed
12	Page_Received_INT	RO RC	1’b0	=1: Page received =0: Page not received
11	Link_Failed_INT	RO RC	1’b0	=1: Link down takes place =0: No link down takes place
10	Link_Succeed_INT	RO RC	1’b0	=1: Link up takes place =0: No link up takes place
9	Reserved	RO	1’b0	Always 0.
8	Reserved	RO	1’b0	Always 0.
7	Reserved	RO	1’b0	Always 0.

6	WOL_INT	RO RC	1’b0	=1: PHY received WOL magic frame. =0: PHY didn’t receive WOL magic frame.
5	Wirespeed_downgraded_INT	RO RC	1’b0	=1: speed downgraded. =0: Speed didn’t downgrade.
4:2	Reserved	RO	3’b0	Always 0.
1	Polarity_changed_INT	RO RC	1’b0	=1: PHY revered MDI polarity =0: PHY didn’t revert MDI polarity
0	Jabber_Happened_INT	RO RC	1’b0	=1:10BaseTe TX jabber happened =0: 10BaseTe TX jabber didn’t happen

5.2.18. MII register 14H: Speed Auto Downgrade Control Register

Bit	Symbol	Access	Default	Description
15:12	Reserved	RO	4’b0	Always 0.
11	En_mdio_latch	RW	1’b1	=1: To latch MII/MMD register’s read out value during MDIO read =0: Do not latch MII/MMD register’s read out value during MDIO read
10:6	Reserved	RW SC	5’b0	Reserved
5	En_speed_downgrade	RW	1’b1	When this bit is set to 1, the PHY enables smart–speed function. Writing this bit requires a software reset to update.
4:2	Autoneg retry limit pre–downgrade	RW	3’b011	If these bits are set to 3, the PHY attempts five times (set value 3 + additional 2) before downgrading. The number of attempts can be changed by these bits.
1	Bp_autospd_timer	RW	1’b0	=1: the wirespeed downgrade FSM will bypass the timer used for link stability check; =0: not bypass the timer, then links that established but hold for less than 2.5s would still be taken as failure, autoneg retry counter will increase by 1.
0	Reserved	RO	1’b0	Always 0.

5.2.19. MII register 15H: Rx Error Counter Register

Bit	Symbol	Access	Default	Description
15:0	Rx_err_counter	RO	16’b0	This counter increase by 1 at the 1st rising of RX_ER when RX_DV is 1. The counter will hold at maximum 16’hFFFF and not roll over. If speed mode is 2’b01, it counts for fe_100 RX_ER; Else, it’s 0.

5.2.20. MII register 1AH:Reference Clock Register

Bit	Symbol	Access	Default	Description
15:2	Reserved	RW	14’b0	Reserved
1	Txc_xtal_sel	RW	1’b0	=1: Use Txc as ext reference clock =0: Use Xtal as ext reference clock
0	Xtal_freq_sel	RW	1’b0	=1: Xtal = 50Mhz =0: Xtal = 25Mhz

5.2.21. MII register 1EH: Debug Register’s Address Offset Register

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Address_Offset	RW	16’b0	It’s the address offset of the EXT that will be Write or Read

5.2.22. MII register 1FH: Debug Register’s Data Register

Bit	Symbol	Access	Default	Description
15:0	Extended_Register_Datas	RW	16’b0	It’s the data to be written to the EXT indicated by the address offset in register 0x1E, or the data read out from that debug register.

5.3. Extended register

5.3.1. EXT 0000h PHY Broadcast addr

Bit	Symbol	Access	default	Description
15:7	reserved	RO	0	reserved
6	En_phyaddr0	RW	1’b1	Enable mdio phy address 0 access

5	En_bdcst_addr	RW	1’b1	Enable mdio broadcast address access
4:0	Bdcst_addr	RW	5’b11111	MDIO Broadcast address

5.3.2. EXT 0001h Interpolator Filter

Bit	Symbol	Access	default	Description
15:10	Reserved	RO	6’b100	reserved
9	Step_sw_en	RW	1’b0	Use manual step for interp filter
8:0	Reserved	RO	9’b1000000	reserved

5.3.3. EXT 0010H: Interpolator Filter Coef.0

Bit	Symbol	Access	default	Description
15:0	Reserved	RO	16’b0	Reserved

5.3.4. EXT 0011H: Interpolator Filter Coef.1

Bit	Symbol	Access	default	Description
15:11	Reserved	RO	8’b0	Reserved
10:8	Step_sw_1[10:8]	RO	3’b0	Interp filter coefficient 1
7:1	Step_sw_1[7:1]	RW	7’b1001_101	Interp filter coefficient 1
0	Step_sw_1[0]	RO	1’b0	Interp filter coefficient 1

5.3.5. EXT 0012H: Interpolator Filter Coef.2

Bit	Symbol	Access	default	Description
15:11	Reserved	RO	5’b0	Reserved
10:9	Step_sw_2[10:9]	RO	2’b0	Interp filter coefficient 2
8:1	Step_sw_2[8:1]	RW	8’b1_0001_101	Interp filter coefficient 2
0	Step_sw_2[0]	RO	1’b0	Interp filter coefficient 2

5.3.6. EXT 0013H: Interpolator Filter Coef.3

Bit	Symbol	Access	default	Description
15:11	Reserved	RO	5’b0	Reserved
10:8	Step_sw_3[10:8]	RO	3’b001	Interp filter coefficient 3
7:1	Step_sw_3[7:1]	RW	7’b1000_000	Interp filter coefficient 3
0	Step_sw_3[0]	RO	1’b0	Interp filter coefficient 3

5.3.7. EXT 0014H: Interpolator Filter Coef.4

Bit	Symbol	Access	default	Description
15:11	Reserved	RO	5’b0	Reserved
10:8	Step_sw_4[10:8]	RO	3’b001	Interp filter coefficient 4
7:1	Step_sw_4[7:1]	RW	7’b1100_110	Interp filter coefficient 4
0	Step_sw_4[0]	RO	1’b0	Interp filter coefficient 4

5.3.8. EXT 0015H: Interpolator Filter Coef.5

Bit	Symbol	Access	default	Description
15:11	Reserved	RO	5’b0	Reserved
10:8	Step_sw_5[10:8]	RO	3’b001	Interp filter coefficient 5
7:1	Step_sw_5[7:1]	RW	7’b1110_011	Interp filter coefficient 5
0	Step_sw_5[0]	RO	1’b0	Interp filter coefficient 5

5.3.9. EXT 0016H: Interpolator Filter Coef.6

Bit	Symbol	Access	default	Description
15:11	Reserved	RO	5’b0	Reserved
10:0	Step_sw_6	RO	11’d512	Interp filter coefficient 6

5.3.10. EXT 0017H: Interpolator Filter Coef.7

Bit	Symbol	Access	default	Description
15:11	Reserved	RO	5’b0	Reserved
10:0	Step_sw_7	RO	11’d512	Interp filter coefficient 7

5.3.11. EXT 0050H: AFE PLL Config

Bit	Symbol	Access	default	Description
15:7	Reserved	RO	9’b0	Reserved
6	Pll_refclk_sel	RW	1’b0	Sel clk source in rmii2 mode
5	Reserved	RW	6’b111111	Reserved

5.3.12. EXT 0061H: AFE Switches

Bit	Symbol	Access	default	Description
15:7	Reserved	RO	9’b110	Reserved

6	en_vco_check	RW	1’b1	enable or disable VCO_fast or VCO_slow check circuit
5:0	reserved	RO	6’b11110	reserved

5.3.13. EXT 00A0H: PLL Lock Detect Status

Bit	Symbol	Access	default	Description
15:2	Reserved	RO	13’b0	reserved
1	Pll_vco_h	RO	1’b0	Analog Pll vco fast flag
0	Pll_vco_l	RO	1’b0	Analog pll vco slow flag

5.3.14. EXT 200AH: 10BT Debug, LPBKs Register

Bit	Symbol	Access	Default	Description
15	En_gate_bt10	RW	1’b1	=1: Control to gate the baset10 module’s clock when link up at 100Mbps.
				=0: disable the clock gating.
14:11	reserved	RO	4'b1001	reserved
10	En_10bt_idl	RW	1’b1	=1: In 10BT mode , if there’s no data or NLP to transmit, shut off DAC; otherwise turn on the DAC;
				=0: In 10BT, DAC will not be turn off.
9:0	Reserved	RO	10'h208	reserved

5.3.15. EXT 2012H: AFE Control Register3

Bit	Symbol	Access	Default	Description
15	Reserved	RW	1’b0	reserved
14	En_clkadc_aon	RW	1’b0	when speed mode is 100Mb/s or 10Mb/s,
				=1: keep channel 0 and 1 clkadc both on;
				=0: open one channel’s clkadc based on mdi status.
13:0	Reserved	RO	12'h2f0	reserved

5.3.16. EXT 2027H: Sleep Control1

Bit	Symbol	Access	default	Description
15	En_sleep_sw	RW	1’b1	=1: enable sleep mode: PHY will enter sleep mode and close AFE after unplug cable for a timer;
14:0	reserved	RO	15’h200	reserved

5.3.17. EXT 2056H: 10BT RX Comparator Threshold

Bit	Symbol	Access	default	Description
15:14	Tenbt_vth_cfg_10M	RW	2’b00	10BT RX comparator threshold. It’s valid only when speed mode is 10Mbps.
13:0	Reserved	RO	14’b0	Always 0.

5.3.18. EXT 2057H: DAC Ctrl for 10BT and 100BT

Bit	Symbol	Access	default	Description
15	Reserved	RO	1’b0	Always 0.
14:12	DAC_amp_100M	RW	3’b010	
11:8	DAC_amp_cfg_100M	RW	4’b0110	
7	Reserved	RO	1’b0	Always 0.
6:4	DAC_amp_10M	RW	3’b010	
3:0	DAC_amp_cfg_10M	RW	4’b0110	

5.3.19. EXT 2058H: PHY DEBUG CONFIGURE1

Bit	Symbol	Access	default	Description
15	reserved	RO	1’b0	reserved
14	En_snap_shot	RW	1’b0	1 = enable to snap shot 1000BT and 100BT PMA FSM and related intermediate status.
13:0	reserved	RO	14'hc00	reserved

5.3.20. EXT 2059H:PHY DEBUG CONFIGURE2

Bit	Symbol	Access	default	Description
15	Prob_auto	RW	1’b0	1 = probe the PMA status immediately, not at certain condition.

14	Cnt_err_auto	RW	1’b0	1 = monitor big slicer error after 1000BT training done;
				0 = monitor big slicer error after 1000BT training done and during RX_DV;
13	Cnt_clp_auto	RW	1’b0	1 = monitor big ADC output after 1000BT training done;
				0 = monitor big ADC output after 1000BT training done and during RX_DV;
12:8	Target_eee_st	RW	5’b0	The target PMA EEE state to be snap shot.
7:0	Err_big_th	RW	8’d64	The amplitude threshold determining the errors after slicer are big.

5.3.21. EXT 205AH:PHY DEBUG, MSE1

Bit	Symbol	Access	default	Description
15	Hold_snap_shot	RO	1’b0	Valid when EXT 2058h bit14 en_snap_shot is set.
				1 = the snap shot condition is met and triggerd
14:0	Mse0	RO	15’b0	Valid when EXT 2058h bit14 en_snap_shot is set, or EXT 2059h bit15 prob_auto is set. Corresponding to these two setting, it is the:
				MSE0 at the time snap shot condition is met, or
				MSE0 at the time this EXT register is being read.

5.3.22. EXT 205BH:PHY DEBUG, MSE2

Bit	Symbol	Access	default	Description
15	Hold_snap_shot_az	RO	1’b0	Valid when EXT 2058h bit15 en_snap_shot_az is set.
				1 = the EEE snap shot condition is met and triggerd
14:0	Reserved	RO	15’b0	Always 0.

5.3.23. EXT 2068H: PHY Debug, Integrator

Bit	Symbol	Access	default	Description
15:0	Integrator	RO	16’h0	Channel 0’s integrator. Frquence different between lp and dut. PPM = 0.95 * integrator; integrator is 2's complement value
				Valid when EXT 2058h bit14 en_snap_shot is set, or EXT 2059h bit15 prob_auto is set. Corresponding to these two setting, it is the:
				Integrator at the time snap shot condition is met, or
				Integrator at the time this EXT register is being read.

5.3.24. EXT 4000H: extended combo control1

Bit	Symbol	Access	default	Description
15	Led0_wk_mode	RW	1’b0	0 = LED,1 = WOL
14	Led0_polarity	RW	1’b0	0 = active high 1 = active low
13	Led1_polarity	RW	1’b0	0 = active high,1 = active low
12	External_Loopback	RW	1’b0	0 = disable 1 = enable
11:7	Reserved	RW	5’b0	Reserved
6	Rmii1_clk_sel	RW	1’b0	1 = rmii tx clk use xtal 0 = txc
5	Jumbo_Enable	RW	1’b0	1 = Enable Jumbo frame, reception up to 18KB frame; 0 = disabled, only up to 4.5KB frame supported
4	Rmii_rxdv_sel	RW	1’b0	Drive PAD CRS_DV of RMII by (0= CRS_DV, 1 = RX_DV).
3	Fx_en	RW	1’b0	1 = enable fx100 mode, 0 = disable
2	Wol_en	RW	1’b0	1 = enable WOL mechanism. 0 = disable.
1	Rmii_en	RW	1’b0	1 = enable RMII mode; 0 = disable RMII mode(default by power on strapping)
0	Clk_sel	RW	1’b0	1 = input TXC/RXC 0 = output TXC/RXC(default by power on strapping)

5.3.25. EXT 4001H: extended pad control

Bit	Symbol	Access	default	Description
15:6	reserved	RO	10'h203	reserved

5:4	Xmii_Dr	RW	2’b10	Xmii interface driver strength control in non-scan mode.
3:0	reserved	RO	4'b1111	reserved

5.3.26. EXT 4003H: extended combo control2

Bit	Symbol	Access	default	Description
15	Reserved	RW	1’b0	Reserved
14	Slave_jitter_test	RW	1’b0	Mux clk_dac to rxc in slave jitter test mode 1: enable 0: disable
13:10	Reserved	RW	4’b0	Reserved
9:7	Wol_lth_sel	RW	3’b100	Wol_lth_sel[0] control WOL INTn to be a level or a pulse. 1’b1: a pulse; 1’b0: a level. Wol_lth_sel[2:1] control WOL INTn pulse width when Wol_lth_sel[0] is 1. 2’b00: 10us; 2’b01: 100us; 2’b10: 1ms; 2’b11: 10ms.

6	En_isolate_txc	RW	1’b1	When isolate (mii.0.10) is 1, control to make TXC input or not. 1’b1: input; 1’b0: keep TXC previous direction.
5	En_isolate_rxc	RW	1’b1	When isolate (mii.0.10) is 1, control to make RXC input or not. 1’b1: input; 1’b0: keep RXC previous direction.
4:0	Reserved	RW	5’b01111	Reserved

5.3.27. EXT 4004H: WOL MAC Address

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[47:32]	RW	16’b0	mac address for WOL

5.3.28. EXT 4005H: WOL MAC Address

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[31:16]	RW	16’b0	mac address for WOL

5.3.29. EXT 4006H: WOL MAC Address

Bit	Symbol	Access	default	Description
15:0	Mac_addr_loc[15:0]	RW	16’b0	mac address for WOL

5.3.30. EXT 40A0H: pkg_selftest control

Bit	Symbol	Access	default	Description
15	Pkg_chk_en	RW	1’b0	1: to enable RX/TX package checker. RX checker checks the MII data at transceiver’s PCS RX; TX checker checks the MII data at mii_bridge’s TX.
14	Pkg_en_gate	RW	1’b1	1: to enable gate all the clocks to package self-test module when bit15 pkg_chk_en is 0, bit13 bp_pkg_gen is 1 and bit12 pkg_gen_en is 0;
				0: not gate the clocks.
13	Bp_pkg_gen	RW	1’b1	1: normal mode, to send xMII TX data from PAD;
				0: test mode, to send out the MII data generated by pkg_gen module.
12	Pkg_gen_en	RW SC	1’b0	1: to enable pkg_gen generating MII packages. But, the data will only be sent to transceiver when Bit13 bp_pkg_gen is 1’b0.
				If pkg_burst_size is 0, continuous packages will be generated and will be stopped only when pkg_gen_en is set to 0;
				Otherwise, after the expected packages are generated, pkg_gen will stop, pkg_gen_en will be self-cleared.
11:8	Pkg_prm_lth	RW	4’d8	The preamble length of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.

7:4	Pkg_ipg_lth	RW	4’d12	The IPG of the generated packages, in Byte unit. Pkg_gen function only support >=2 Byte preamble length. Values smaller than 2 will be ignored by the pkg_gen module.
3	Xmit_mac_force_gen	RW	1’b0	1: To enable pkg_gen to send out the generated data even when the link is not established.
2	Pkg_corrupt_crc	RW	1’b0	1: to make pkg_gen to send out CRC error packages. 0: pkg_gen sends out CRC good packages.
1:0	Pkg_payload	RW	2’b0	Control the payload of the generated packages. 00: increased Byte payload; 01: random payload; 10: fix pattern 0x5AA55AA5… 11: reserved.

5.3.31. EXT 40A1H: pkg_selftest control

Bit	Symbol	Access	default	Description
15:0	Pkg_length	RW	16’d64	To set the length of the generated packages.

5.3.32. EXT 40A2H: pkg_selftest control

Bit	Symbol	Access	default	Description
15:0	Pkg_burst_size	RW	16’b0	To set the number of packages in a burst of package generation. 0: continuous packages will be generated.

5.3.33. EXT 40A3H: pkg_selftest status

Bit	Symbol	Access	default	Description

15:0	Pkg_ib_valid_high	RO	16’b0	Pkg_ib_valid[31:16], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.34. EXT 40A4H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_valid_low	RO	16’b0	Pkg_ib_valid[15:0], pkg_ib_valid is the number of RX packages from wire whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.35. EXT 40A5H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_high	RO	16’b0	Pkg_ib_os_good[31:16], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

5.3.36. EXT 40A6H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_good_low	RO	16’b0	Pkg_ib_os_good[15:0], pkg_ib_os_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

5.3.37. EXT 40A7H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_high	RO	16’b0	Pkg_ib_us_good[31:16], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are <64Byte.

5.3.38. EXT 40A8H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_us_good_low	RO	16’b0	Pkg_ib_us_good[15:0], pkg_ib_us_good is the number of RX packages from wire whose CRC are good and length are >1518Byte.

5.3.39. EXT 40A9H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_err	RO	16’b0	pkg_ib_err is the number of RX packages from wire whose CRC are wrong and length are >=64Byte, <=1518Byte.

5.3.40. EXT 40AaH: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_os_bad	RO	16’b0	pkg_ib_os_bad is the number of RX packages from wire whose CRC are wrong and length are >=1518Byte.

5.3.41. EXT 40AbH: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_frag	RO	16’b0	pkg_ib_frag is the number of RX packages from wire whose length are <64Byte.

5.3.42. EXT 40AcH: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ib_nosfd	RO	16’b0	pkg_ib_nosfd is the number of RX packages from wire whose SFD is missed.

5.3.43. EXT 40AdH: pkg_selftest status

Bit	Symbol	Access	default	Description

15:0	Pkg_ob_valid_high	RO	16’b0	Pkg_ob_valid[31:16], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.44. EXT 40AeH: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_valid_low	RO	16’b0	Pkg_ob_valid[15:0], pkg_ob_valid is the number of TX packages from MII whose CRC are good and length are >=64Byte and <=1518Byte.

5.3.45. EXT 40AfH: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_high	RO	16’b0	Pkg_ob_os_good[31:16], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

5.3.46. EXT 40B0H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_good_low	RO	16’b0	Pkg_ob_os_good[15:0], pkg_ob_os_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

5.3.47. EXT 40B1H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_high	RO	16’b0	Pkg_ob_us_good[31:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are <64Byte.

5.3.48. EXT 40B2H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_us_good_low	RO	16’b0	Pkg_ob_us_good[15:0], pkg_ob_us_good is the number of TX packages from MII whose CRC are good and length are >1518Byte.

5.3.49. EXT 40B3H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_err	RO	16’b0	pkg_ob_err is the number of TX packages from MII whose CRC are wrong and length are >=64Byte, <=1518Byte.

5.3.50. EXT 40B4H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_os_bad	RO	16’b0	pkg_ob_os_bad is the number of TX packages from MII whose CRC are wrong and length are >=1518Byte.

5.3.51. EXT 40B5H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_frag	RO	16’b0	pkg_ob_frag is the number of TX packages from MII whose length are <64Byte.

5.3.52. EXT 40B6H: pkg_selftest status

Bit	Symbol	Access	default	Description
15:0	Pkg_ob_nosfd	RO	16’b0	pkg_ob_nosfd is the number of TX packages from MII whose SFD is missed.

5.3.53. EXT 40B7H: pkg_selftest control

Bit	Symbol	Access	default	Description
15:1	Reserved	RO	15’b0	

1	Pkgchk_txsrc_sel	RW	1’b0	Control the source of packages for pkg checker in TX direction to check. 1’b1: from pkg_gen; 1’b0: from xMII TX interface.
0	Pkgen_en_az	RW	1’b0	To send AZ LPI pattern during IPG of the packages sent by pkg_gen.

5.3.54. EXT 40B8H: pkg_selftest control

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5’b0	No use.
10:0	Pkgen_pre_az_t	RW	11’b0	Control the IDLE time after traffic and before sending LPI_IDLE, in unit us.

5.3.55. EXT 40B9H: pkg_selftest control

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5’b0	No use.
10:0	Pkgen_in_az_t	RW	11’b0	Control the time sending LPI_IDLE, in unit us. For Giga mode, only Pkgen_in_az_t[8:0] is valid.

5.3.56. EXT 40BAH: pkg_selftest control

Bit	Symbol	Access	default	Description
15:11	Reserved	RW	5’b0	No use.
10:0	Pkgen_aft_az_t	RW	11’b0	Control the IDLE time from end of LPI_IDLE to the beginning of next package.

5.3.57. EXT 40C0H: LED0 control

Bit	Symbol	Access	default	Description
15	Led_force_en	RW	1’b0	To enable LED force mode.
14:13	Led_force_mode	RW	2’b0	Valid when bit15 led_force_en is set. 00 = force LED OFF; 01 = force LED ON; 10 = force LED to blink at Blink Mode1; 11 = force LED to blink at Blink Mode0. There are 4 Blink Mode, which are different at

				blink frequency. Refer to EXT 40C2 for detail of Blink Mode0~3.
12	Led_act_blk_ind	RW	1’b0	When traffic is present, make LED BLINK no matter the previous LED status is ON or OFF, or make LED blink only when the previous LED is ON. when any *_blk_en in bit9~8 and bit3~1 is set and chip do work at corresponding status, =1: LED will blink, no matter bit11~10 (duplex control) and bit5~4 (speed control) are 1 or 0; =0: LED will not blink, unless one (more) of bit11~10 (duplex control) and bit5~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);.
11	Led_fdx_on_en	RW	1’b0	If BLINK status is not activated, when PHY link up and duplex mode is full duplex, =1: make LED ON; =0: don’t make LED ON;
10	Led_hdx_on_en	RW	1’b0	If BLINK status is not activated, when PHY link up and duplex mode is half duplex, =1: make LED ON; =0: don’t make LED ON;
9	Led_txact_blk_en	RW	1’b0	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don’t make LED BLINK.
8	Led_rxact_blk_en	RW	1’b0	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don’t make LED BLINK.
7	Led_txact_on_en	RW	1’b0	=1: if BLINK status is not activated, when PHY link up and TX is active, make LED ON at least 2 second
6	Led_rxact_on_en	RW	1’b0	=1: if BLINK status is not activated, when PHY link up and RX is active, make LED ON at least 2

				second
5	Led_ht_on_en	RW	1’b1	=1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED ON;
4	Led_bt_on_en	RW	1’b1	=1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED ON;
3	Led_col_blk_en	RW	1’b0	=1: if PHY link up and collision happen, make LED BLINK at Blink mode 0 or 1 based on 40C1h bit6 col_blk_sel;
2	Led_ht_blk_en	RW	1’b0	=1: if PHY link up and speed mode is 100Mbps, make LED BLINK at Blink mode 2;
1	Led_bt_blk_en	RW	1’b0	=1: if PHY link up and speed mode is 10Mbps, make LED BLINK at Blink mode 3;
0	Dis_led_an_try	RW	1’b1	when PHY is active and auto-negotiation is at LINK_GOOD_CHECK status, =1: LED will be on; =0: LED will be off.

5.3.58. EXT 40C1H: LED0/1 control

Bit	Symbol	Access	default	Description
15:10	Reserved	RO	6’b0	Always 0.
9	Invert_led_duty	RW	1’b0	=1: to invert the duty cycle of ON and OFF, namely make LED ON time short and OFF time long.
8	Lpbk_led_dis	RW	1’b0	=1: In internal loopback mode, LED will not blink; =0: In internal loopback mode, LED will still blink if it’s configured to blink on activity.
7	Jabber_led_dis	RW	1’b0	=1: when 10Mbps Jabber happens, LED will not blink; =0: when 10Mbps Jabber happens, LED will still blink if it’s configured to blink on TX.
6	Col_blk_sel	RW	1’b0	=1: when collision happens, LED blink at Blink Mode0; =0: when collision happens, LED blink at Blink Mode1;

5	En_led_act_level	RW	1’b0	=1: to make LED blink at different frequency (Blink mode 0) when traffic weight is high. =0: to make LED blink always at Blink mode 1 no matter what the traffic weight is.
4:0	Led_act_level_th	RW	5’d12	Traffic is heavy or not’s threshold. RX/TX traffic is monitored separately. In 1s interval, if RX or TX traffic active time > Led_act_level_th*42ms, then the traffic is heavy; otherwise, traffic is not heavy.

5.3.59. EXT 40C2H: LED0/1 control

Bit	Symbol	Access	default	Description
15:12	Freq_sel_c0	RW	4’d14	Control the LED blink frequency in Blink mode 0. ON/OFF duty cycle could be reverted by 40C1h bit9 invert_led_duty. Below description is the default ON/OFF cycle, that is invert_led_duty=0. 4’d0=LED blink once every 10s, 6% OFF; 4’d1=LED blink once every 9.4s, 7% OFF; 4’d2=LED blink once every 8s, 8% OFF; 4’d3=LED blink once every 7.4s, 9% OFF; 4’d4=LED blink once every 6s, 11% OFF; 4’d5=LED blink once every 5s, 6% OFF; 4’d6=LED blink once every 4s, 8% OFF; 4’d7=LED blink once every 3s, 11% OFF; 4’d8=LED blink once every 2s, 16% OFF; 4’d9=LED blink once every 1s, 16% OFF; 4’d10=LED blink at 2Hz, 50% OFF; 4’d11=LED blink at 3Hz, 50% OFF; 4’d12=LED blink at 4Hz, 50% OFF; 4’d13=LED blink at 6Hz, 50% OFF; 4’d14=LED blink at 8Hz, 50% OFF; 4’d15=LED blink at 10Hz, 50% OFF;
11:8	Freq_sel_c1	RW	4’d12	Control the LED blink frequency in Blink mode 1. See description in bit15~12 Freq_sel_c0 for detail.

7:4	Freq_sel_c2	RW	4’d7	Control the LED blink frequency in Blink mode 2. See description in bit15~12 Freq_sel_c0 for detail.
3:0	Freq_sel_c3	RW	4’d5	Control the LED blink frequency in Blink mode 3. See description in bit15~12 Freq_sel_c0 for detail.

5.3.60. EXT 40C3H: LED1 control

Bit	Symbol	Access	default	Description
15	Led_force_en	RW	1’b0	To enable LED force mode.
14:13	Led_force_mode	RW	2’b0	Valid when bit15 led_force_en is set. 00 = force LED OFF; 01 = force LED ON; 10 = force LED to blink at Blink Mode1; 11 = force LED to blink at Blink Mode0. There are 4 Blink Mode, which are different at blink frequency. Refer to EXT 40C2 for detail of Blink Mode0~3.
12	Led_act_blk_ind	RW	1’b0	When traffic is present, make LED BLINK no matter the previous LED status is ON or OFF, or make LED blink only when the previous LED is ON. when any *_blk_en in bit9~8 and bit3~1 is set and chip do work at corresponding status, =1: LED will blink, no matter bit11~10 (duplex control) and bit5~4 (speed control) are 1 or 0; =0: LED will not blink, unless one (more) of bit11~10 (duplex control) and bit5~4 (speed control) is (are) 1 and related status is (are) matched (ON at certain speed or duplex mode is/are activated);.
11	Led_fdx_on_en	RW	1’b0	If BLINK status is not activated, when PHY link up and duplex mode is full duplex, =1: make LED ON; =0: don’t make LED ON;
10	Led_hdx_on_en	RW	1’b0	If BLINK status is not activated, when PHY link up and duplex mode is half duplex, =1: make LED ON; =0: don’t make LED ON;

9	Led_txact_blk_en	RW	1’b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and TX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don’t make LED BLINK.
8	Led_rxact_blk_en	RW	1’b1	If bit12 Led_act_blk_ind is 1, or it is 0 and LED ON at certain speed or duplex more is/are activated, when PHY link up and RX is active, =1: make LED BLINK at Blink mode 0 or 1 based on traffic weight; =0: don’t make LED BLINK.
7	Led_txact_on_en	RW	1’b0	=1: if BLINK status is not activated, when PHY link up and TX is active, make LED ON at least 10ms;
6	Led_rxact_on_en	RW	1’b0	=1: if BLINK status is not activated, when PHY link up and RX is active, make LED ON at least 10ms;
5	Led_ht_on_en	RW	1’b1	=1: if BLINK status is not activated, when PHY link up and speed mode is 100Mbps, make LED ON;
4	Led_bt_on_en	RW	1’b0	=1: if BLINK status is not activated, when PHY link up and speed mode is 10Mbps, make LED ON;
3	Led_col_blk_en	RW	1’b0	=1: if PHY link up at FE and collision happen, make LED BLINK at Blink mode 0 or 1 based on 40C1h bit6 col_blk_sel;
2	Led_ht_blk_en	RW	1’b0	=1: if PHY link up and speed mode is 100Mbps, make LED BLINK at Blink mode 2;
1	Led_bt_blk_en	RW	1’b0	=1: if PHY link up and speed mode is 10Mbps, make LED BLINK at Blink mode 3;
0	Reserved	RO	1’b0	Always 0.

5.3.61. EXT 4201H: Txclk_delay

Bit	Symbol	Access	default	Description
15:3	Reserved	RW	5’b0	No use.
2:0	txclk_delay_sel_100bt	RW	3’d4	1: use 8ns delayed tx mii clock 2: use 16ns delayed tx mii clock 3: use 24ns delayed tx mii clock 4: use 32ns delayed tx mii clock others: use no delayed tx mii clock

5.3.62. EXT 4216H: IO Level

Bit	Symbol	Access	default	Description
15:4	Reserved	RW	12’b0	No use.
3	en_led_ren_ctrl	RW	1’b1	0: LED PAD ren will be 0 after strap done 1: LED PAD ren will be 1 after strap done
2	en_ren_ctrl	RW	1’b1	0: output PAD ren will be 0 after strap done 1: output PAD ren will be 1 after strap done
1:0	io_level_ctrl	RW	1’d3	0: 1.5V IO level 1: 1.8V IO level 2: 2.5V IO level 3: 3.3V IO level

6. Timing and electrical characteristics

6.1. Crystal Requirement

Table 6. Crystal Requirement

Symbol	Description	Min	Typ	Max	Unit
Fref	Crystal Reference Frequency	–	25	–	MHz
Fref Tolerance	Crystal Reference Frequency tolerance	–50	–	50	ppm
Duty Cycle	Reference clock input duty cycle	40	–	60	%
ESR	Equivalent Series Resistance	–		50	ohm
DL	Drive Level	–	–	0.5	mW
Vih	Crystal output high level	1.4	–	–	V
Vil	Crystal output low level	–	–	0.4	V

6.2. Oscillator/External Clock Requirement

Table 7. Oscillator/External Clock Requirement

Parameter	Condition	Min	Typ	Max	Unit
Frequency			25/50		MHz
Frequency tolerance	Ta= –40~85 C	–50		50	PPM
Duty Cycle		40	–	60	%
Peak to Peak Jitter				200	ps
Vih		1.4		AVDD33+0.3	V
Vil				0.4	V
Rise Time	10%~90%			10	ns
Fall Time	10%~90%			10	ns
Temperature Range	YT8522C	0		70	° C
Temperature Range	YT8522H	–40		85	° C
Temperature Range	YT8522E	–40		125	° C
Temperature Range	YT8522A	–40		125	° C

6.3. DC Characteristics

Table 8. DC Characteristics

Symbol	Description	Min	Typ	Max	Unit
Voh (3.3V)	Minimum High Level Output Voltage	2.4	–	3.63	V
Vol (3.3V)	Maximum Low Level Output Voltage	–0.3	–	0.4	V
Voh (2.5V)	Minimum High Level Output Voltage	2	–	2.8	V
Vol (2.5V)	Maximum Low Level Output Voltage	–0.3	–	0.4	V

Voh (1.8V)	Minimum High Level Output Voltage	1.62	–	2.1	V
Vol (1.8V)	Maximum Low Level Output Voltage	–0.3	–	0.4	V
Voh (1.5V)	Minimum High Level Output Voltage	1.4	–	1.8	V
Vol (1.5V)	Maximum Low Level Output Voltage	–0.3	–	0.4	V
Vih (3.3V)	Minimum High Level Input Voltage	2	–	–	V
Vil (3.3V)	Maximum Low Level Input Voltage	–	–	0.8	V
Vih (2.5V)	Minimum High Level Input Voltage	1.7	–	–	V
Vil (2.5V)	Maximum Low Level Input Voltage	–	–	0.7	V
Vih (1.8V)	Minimum High Level Input Voltage	1.3	–	–	V
Vil (1.8V)	Maximum Low Level Input Voltage	–	–	0.5	V
Vih (1.5V)	Minimum High Level Input Voltage	1.1	–	–	V
Vil (1.5V)	Maximum Low Level Input Voltage	–	–	0.4	V

6.4. MDC/MDIO Timing

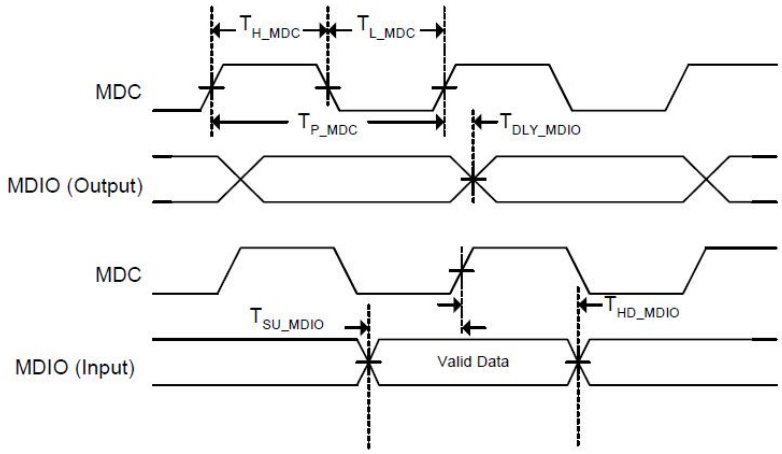


Figure 9. MDC/MDIO Timing

Table 9. MDC/MDIO Timing

Symbol	Description	Min	Typ	Max	Unit
T_{DLY_MDIO}	MDC to MDIO Output Delay Time			20	ns
T_{SU_MDIO}	MDIO Input to MDC Setup Time	10			ns
T_{HD_MDIO}	MDIO Input to MDC Hold Time	10			ns
T_{P_MDC}	MDC Period	80			ns
T_{H_MDC}	MDC High	30			ns
T_{L_MDC}	MDC Low	30			ns
Maximum Frequency = 12.5M Hz					

6.5. MII Transmission Cycle Timing

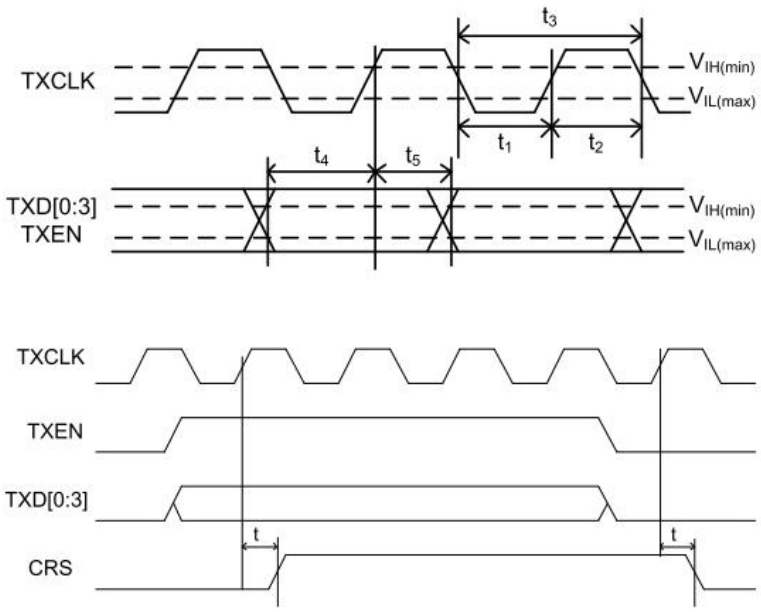


Figure 10. MII Transmission Cycle Timing

Table 10. MII Transmission Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t1	TXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	TXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	TXCLK Period	100Mbps	–	40	–	ns
		10Mbps	–	400	–	ns
t4	TXEN, TXD[0:3] Setup to TXCLK Rising Edge	100Mbps	10	–	–	ns
		10Mbps	5	–	–	ns
t5	TXEN, TXD[0:3] Hold After TXCLK Rising Edge	100Mbps	0	–	–	ns
		10Mbps	0	–	–	ns
t6	TXEN Sampled to CRS High	100Mbps	–	–	40	ns
		10Mbps	–	–	400	ns
t7	TXEN Sampled to CRS Low	100Mbps	–	–	160	ns
		10Mbps	–	–	2000	ns

6.6. MII Reception Cycle Timing

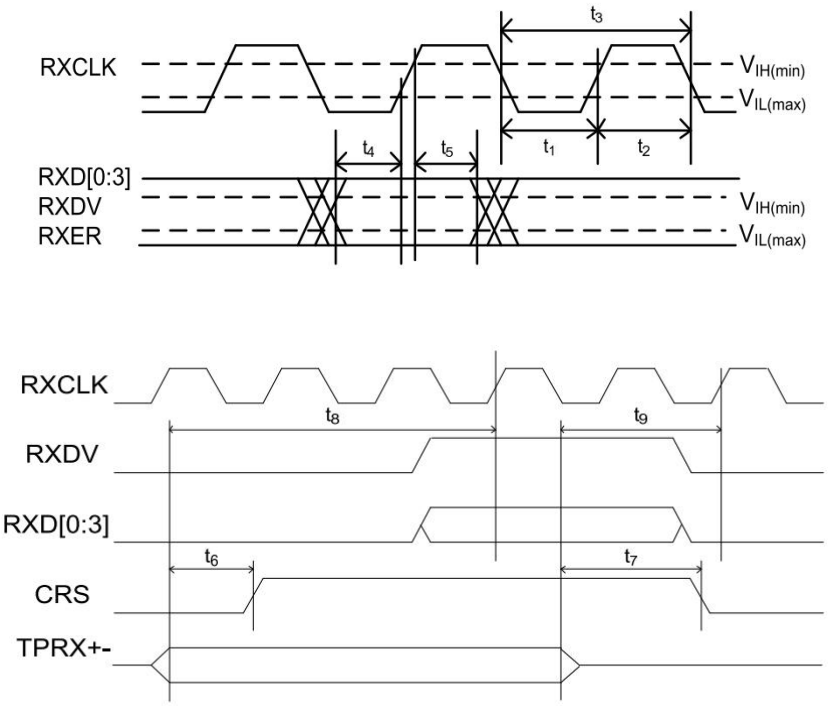


Figure 11. MII Reception Cycle Timing

Table 11. MII Reception Cycle Timing

Symbol	Description		Minimum	Typical	Maximum	Unit
t1	RXCLK Low Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t2	RXCLK High Pulse Width	100Mbps	14	20	26	ns
		10Mbps	140	200	260	ns
t3	RXCLK Period	100Mbps	–	40	–	ns
		10Mbps	–	400	–	ns
t4	RXER, RX_DV,RXD[0:3] Setup to RXCLK Rising Edge	100Mbps	10	–	–	ns
		10Mbps	10	–	–	ns
t5	RXER, RX_DV, RXD[0:3] Hold After RXCLK Rising Edge	100Mbps	10	–	–	ns
		10Mbps	10	–	–	ns
t6	Receive Frame to CRS High	100Mbps	–	–	130	ns
		10Mbps	–	–	2000	ns
t7	End of Receive Frame to CRS Low	100Mbps	–	–	240	ns
		10Mbps	–	–	1000	ns
t8	Receive Frame to Sampled Edge of RX_DV	100Mbps	–	–	150	ns
		10Mbps	–	–	3200	ns
t9	End of Receive Frame to Sampled Edge of RX_DV	100Mbps	–	–	120	ns
		10Mbps	–	–	1000	ns

6.7. RMII1 Transmission and Reception Cycle Timing

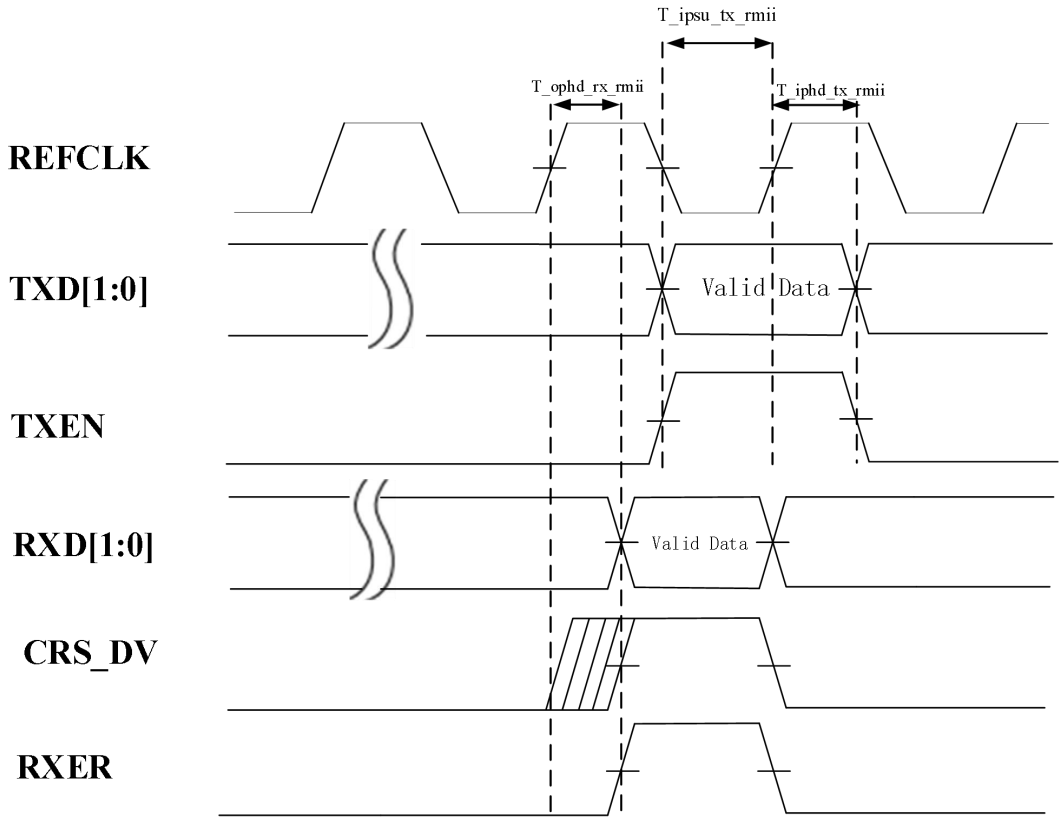


Figure 12. RMII1 Transmission and Reception Cycle Timing

Table 12. RMII1 Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	–	50	–	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	–	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	–	–	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	–	–	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	6	–	12	ns

6.8. RMII2 Transmission and Reception Cycle Timing

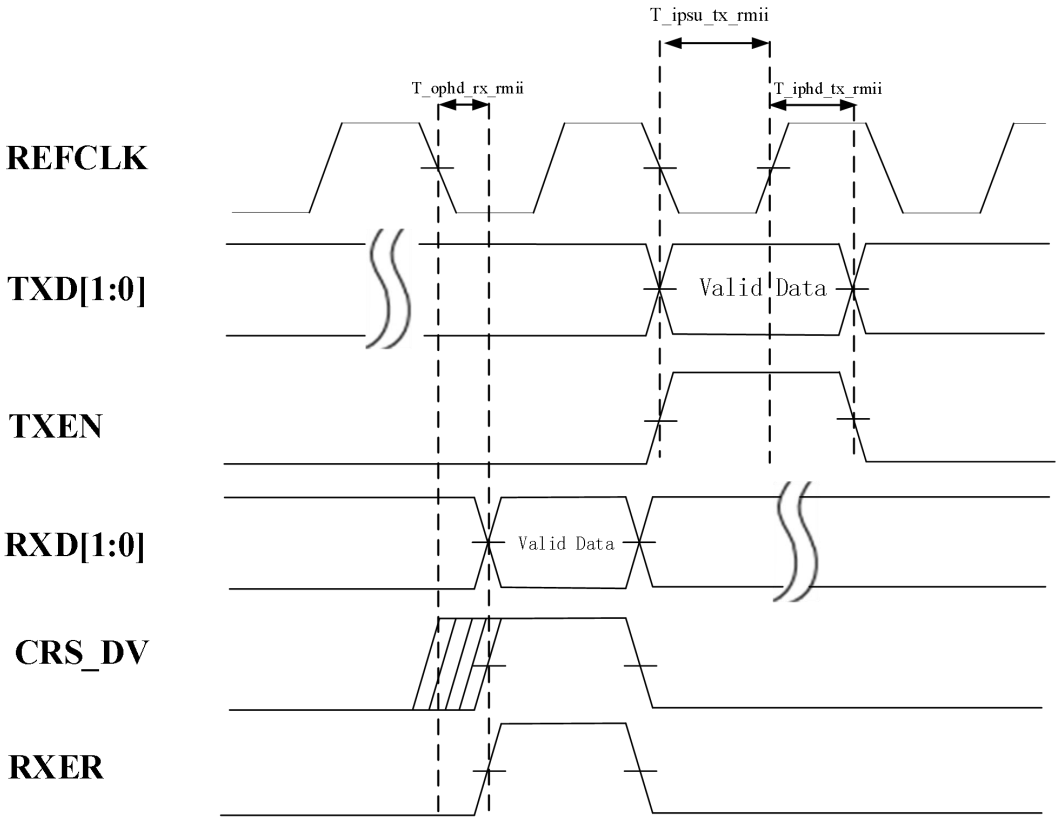


Figure 13. RMII2 Transmission and Reception Cycle Timing

Table 13. RMII2 Transmission and Reception Cycle Timing

Symbol	Description	Minimum	Typical	Maximum	Unit
REFCLK Frequency	Frequency of Reference Clock	–	50	–	MHz
REFCLK Duty Cycle	Duty Cycle of Reference Clock	35	–	65	%
T_ipsu_tx_rmii	TXD[1:0]/TXEN Setup Time to REFCLK	4	–	–	ns
T_iphd_tx_rmii	TXD[1:0]/TXEN Hold Time from REFCLK	2	–	–	ns
T_ophd_rx_rmii	RXD[1:0]/CRS_DV/RXER Output Delay Time from REFCLK	0	–	3	ns

6.9. 100Base-FX Characteristics

6.9.1. 100Base-FX Differential Transmitter Characteristics

Table 14.100Base-FX Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	7.9976	8	8.0024	ns	8ns ± 300ppm
T_X1	Eye Mask	–	–	0.15	UI	–
T_X2	Eye Mask	–	–	0.4	UI	–
T_Y1	Eye Mask	250	–	–	mV	–
T_Y2	Eye Mask	–	–	600	mV	–
$V_{TX-DIFFp-p}$	Output Differential Voltage	500	700	1200	mV	–
T_{TX-EYE}	Minimum TX Eye Width	0.7	–	–	UI	–
$T_{TX-JITTER}$	Output Jitter	–	–	0.3	UI	$T_{TX-JITTER-MAX} = 1 - T_{TX-EYE-MIN}$ = 0.35UI
R_{TX}	Differential Resistance	80	100	120	ohm	–
C_{TX}	AC Coupling Capacitor	80	100	200	nF	–
L_{TX}	Transmit Length in PCB	–	–	10	Inch	–

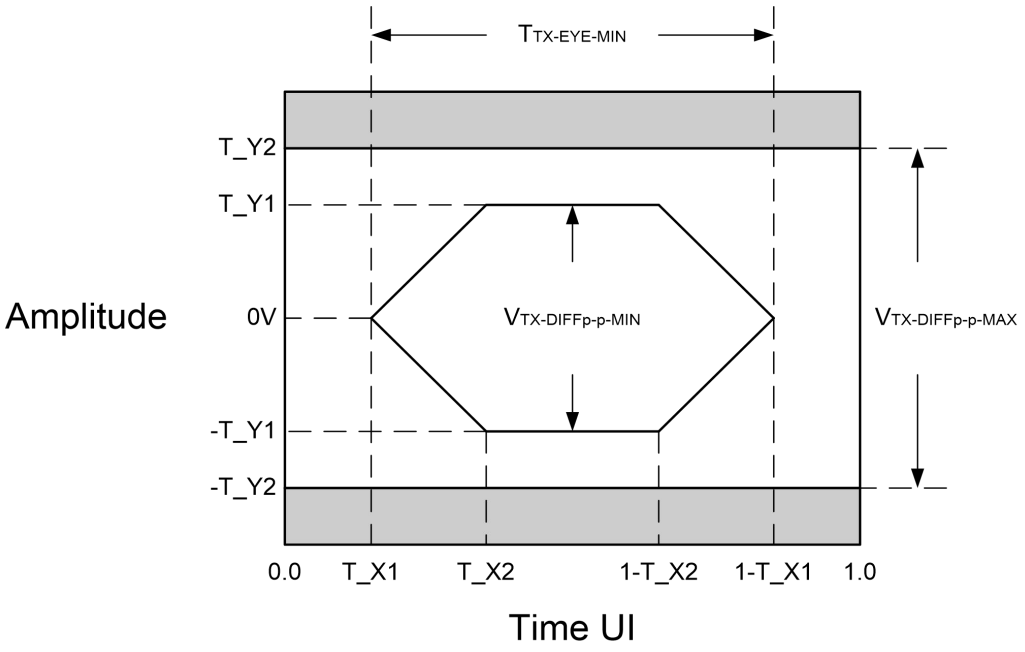


Figure 14. 100Base-FX Differential Transmitter Eye Diagram

6.9.2. 100Base–FX Differential Receiver Characteristics

Table 15.100Base–FX Differential Transmitter Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Notes
UI	Unit Interval	7.9976	8	8.0024	ns	8ns ± 300ppm
R_X1	Eye Mask	–	–	0.3	UI	–
R_Y1	Eye Mask	100	–	–	mV	–
R_Y2	Eye Mask	–	–	1000	mV	–
VRX–DIFFp–p	Input Differential Voltage	200	–	2000	mV	–
T_{RX-EYE}	Minimum RX Eye Width	0.4	–	–	UI	–
$T_{RX-JITTER}$	Input Jitter Tolerance	–	–	0.6	UI	$T_{RX-JITTER-MAX} = 1 - T_{RX-EYE-MIN}$ = 0.6UI
R_{RX}	Differential Resistance	80	100	120	ohm	–

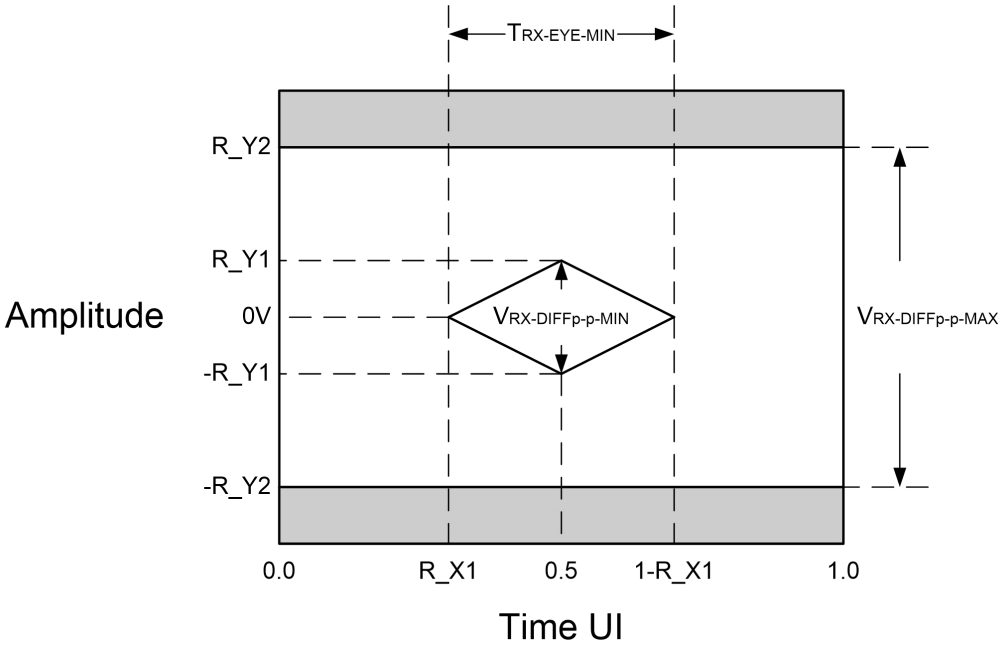


Figure 15.100Base–FX Differential Receiver Eye Diagram

7. Power Requirements

7.1. Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
AVDD33	3.3 V power supply	–0.3	3.70	V
AVDDL	1.2 V power supply	–0.2	1.50	V
DVDDL	1.2 V power supply	–0.2	1.50	V
DVDDIO 3.3V	3.3V power supply	–0.3	3.70	V
DVDDIO 2.5V	2.5V power supply	–0.3	2.8	V
DVDDIO 1.8V	1.8V power supply	–0.3	2.3	V
DVDDIO 1.5V	1.5V power supply	–0.3	1.7	V

7.2. Recommended Operating Condition

Table 17. Recommended Operating Condition

Description	Pins	Min	Typ	Max	Unit
Power Supply	AVDD33	2.97	3.30	3.63	V
	AVDDL	1.08	1.20*	1.32	V
	DVDDL	1.08	1.20*	1.32	V
	DVDDIO 3.3V	2.97	3.30	3.63	V
	DVDDIO 2.5V	2.25	2.50	2.75	V
	DVDDIO 1.8V	1.71	1.8	1.89	V
	DVDDIO 1.5V	1.43	1.5	1.57	V
YT8522C Ambient Operation Temperature Ta		0	–	70	° C
YT8522H Ambient Operation Temperature Ta		–40	–	85	° C
YT8522E Ambient Operation Temperature Ta		–40	–	125	° C
YT8522A Ambient Operation Temperature Ta		–40	–	125	° C
Maximum Junction Temperature				135	° C

Note:AVDDL/DVDDL is from internal LDO.Actual voltage is about 1.15V.

7.3. Power On Sequence

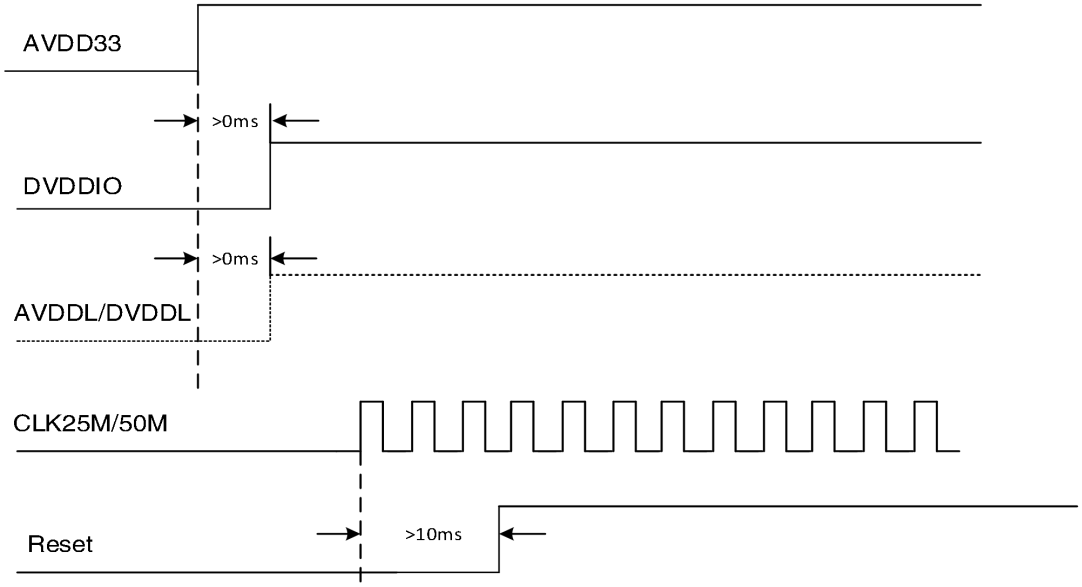


Figure 16.Power On Sequence

When using crystal, the clock generated internally.1.2V power from internal LDO, the sequence between clock and 3.3V, or 1.2V and 3.3V is determined by YT8522 inside and can be ignored. When using external clock CLK 25/50MHz or TXC, CLK 25/50MHz or TXC should be a stable clk after AVDDH/AVDDL reaches 3.3V/1.2V.For a reliable power on reset, suggest to keep asserting the reset low long enough (10ms) to ensure the clock is stable and clock–to–reset 10ms requirement is satisfied.

7.4. Power Consumption

7.4.1. MII mode

Table 19.MII Mode Power Consumption

Condition		DVDDIO=3.3V(mA)	AVDD33(mA)	3.3V total(mA)	Power Consumption(mW)
Reset		1.4	5.8	7.2	23.8
Power down		1.6	6.0	7.6	25.1
Sleep		1.9	6.6	8.5	28.1
Active		1.8	44.2	46.0	151.8
Traffic 100FX		7.0	47.7	54.7	180.5
Link	10M	3.1	29.1	32.2	106.3
	100M	4.6	56.7	61.3	202.3
Traffic	10M	7.9	39.6	47.5	156.8
	100M	10.8	57.1	67.9	224.1

7.4.2. RMII mode

Table 20.RMII Mode Power Consumption

Condition		DVDDIO=3.3V(mA)	AVDD33(mA)	3.3V total(mA)	Power Consumption(mW)
Reset		1.4	5.8	7.2	23.8
Power down		0.9	6.1	7.0	23.1
Sleep		1.0	6.6	7.6	25.1
Active		3.1	46.9	50.0	165.0
Traffic 100FX		5.7	48.1	53.8	177.5
Link	10M	3.8	31.4	35.2	116.2
	100M	3.8	57.4	61.2	202.0
Traffic	10M	5.2	40.5	45.7	150.8
	100M	5.7	57.7	63.4	209.2

Note: The power consumption is measured under room temperature with typical process DUT.When dvddio=2.5/1.8/1.5V,power consumption is close to 3.3v.

7.5. Maximum Power Consumption

Table 21.Maximum Power Consumption

Condition		DVDDIO=3.3V(mA)	AVDD33(mA)	3.3V total(mA)	Power Consumption(mW)
Traffic	100M	15.0	65.0	80.0	264.0

Note: Test by FF corner IC in MII mode with DVDDIO= 3.3V at 125℃ ambient temperature.

8. Package information

8.1. RoHS–Compliant Packaging

Motor–comm offers a RoHS package that is compliant with RoHS

Table 22. RoHS-Compliant Packaging

Part Number	Status	Package	Op temp (℃)	Note
YT8522C	Active	QFN 32 5x5mm	0 to 70	
YT8522H	Active	QFN 32 5x5mm	–40 to 85	
YT8522E	Active	QFN 32 5x5mm	–40 to 125	
YT8522A	Active	QFN 32 5x5mm	–40 to 125	

8.2. Thermal resistance

Table 23. Thermal resistance

Symbol	Parameter	Conditon	Typ	Units
θ_{JA}	Thermal resistance – junction to ambient $\theta_{JA} = (T_J - T_A)/ P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4–layer PCB with no air flow T_A=25° C	37.8	° C/W
		JEDEC 3 in. x 4.5 in. 4–layer PCB with no air flow T_A=125° C	33.3	° C/W
θ_{JC}	Thermal resistance – junction to case $\theta_{JC} = (T_J - T_C)/ Ptop$ Ptop = Power dissipation from the top of the package	JEDEC with no air flow	35	° C/W
θ_{JB}	Thermal resistance – junction to board $\theta_{JB} = (T_J - T_B)/ Pbottom$ Pbottom = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow	16.3	° C/W

9. Mechanical Information

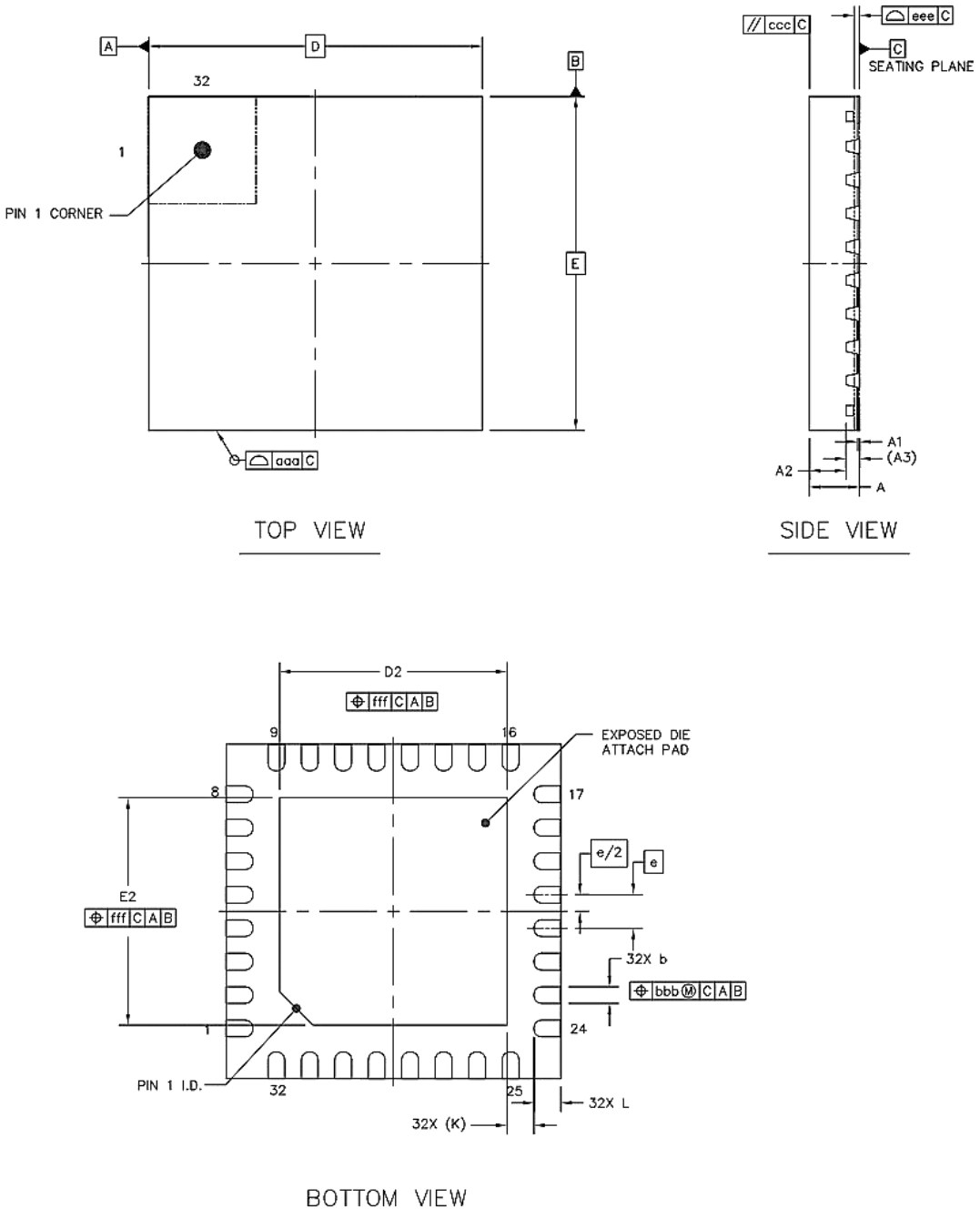


Figure 17. Mechanical Information

		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	3.3	3.4	3.5
	Y	E2	3.3	3.4	3.5
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.4 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

10. Ordering Information

Table 24. Ordering Information

Part Number	Grade	Package	Packaging	Status	Operation temp(℃)
YT8522C	Consumer	QFN 32 5x5mm	Tape Reel 3000ea	Mass production	0 to 70 ℃
YT8522H	Industrial	QFN 32 5x5mm	Tape Reel 3000ea	Mass production	–40 to 85 ℃
YT8522E	Extreme	QFN 32 5x5mm	Tape Reel 3000ea	Sampling	–40 to 125 ℃
YT8522A	Automotive application AECQ–100 Grade 2	QFN 32 5x5mm	Tape Reel 3000ea	Sampling	–40 to 125 ℃