

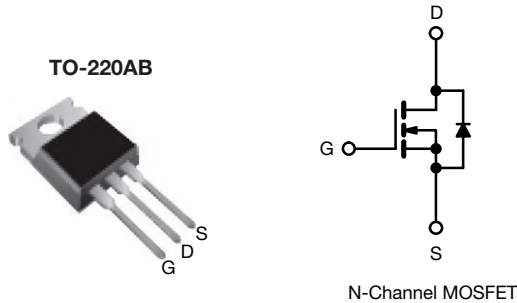
7N60KL-TA3-T-VB Datasheet

N-Channel 600V (D-S) Power MOSFET

| PRODUCT SUMMARY | |
|---------------------------|------------------------------|
| V_{DS} (V) | 600 |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ 0.780 |
| Q_g max. (nC) | 49 |
| Q_{gs} (nC) | 13 |
| Q_{gd} (nC) | 20 |
| Configuration | Single |

FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current



APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

APPLICABLE OFF LINE SMPS TOPOLOGIES


- Active clamped forward
- Main switch

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | |
|---|----------------------------------|----------------|-----------------------------------|--------------------|---|
| PARAMETER | | SYMBOL | LIMIT | UNIT | |
| Drain-Source Voltage | | V_{DS} | 600 | V | |
| Gate-Source Voltage | | V_{GS} | ± 30 | | |
| Continuous Drain Current | V_{GS} at 10 V | I_D | $T_C = 25\text{ }^\circ\text{C}$ | 8.0 | A |
| | | | $T_C = 100\text{ }^\circ\text{C}$ | 5.8 | |
| Pulsed Drain Current ^a | | I_{DM} | 37 | | |
| Linear Derating Factor | | | 1.3 | $W/^\circ\text{C}$ | |
| Single Pulse Avalanche Energy ^b | | E_{AS} | 290 | mJ | |
| Repetitive Avalanche Current ^a | | I_{AR} | 8.0 | A | |
| Repetitive Avalanche Energy ^a | | E_{AR} | 17 | mJ | |
| Maximum Power Dissipation | $T_C = 25\text{ }^\circ\text{C}$ | P_D | 170 | W | |
| Peak Diode Recovery dV/dt ^c | | dV/dt | 5.0 | V/ns | |
| Operating Junction and Storage Temperature Range | | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ | |
| Soldering Recommendations (Peak temperature) ^d | for 10 s | | 300 | | |
| Mounting Torque | 6-32 or M3 screw | | 10 | lbf · in | |
| | | | 1.1 | N · m | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 6.8\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 9.2\text{ A}$ (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$, $dI/dt \leq 50\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

| THERMAL RESISTANCE RATINGS | | | | |
|-------------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 62 | °C/W |
| Case-to-Sink, Flat, Greased Surface | R_{thCS} | 0.50 | - | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 0.75 | |

| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|-----------------------|--|---|-------|-----------|---------------|-----|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT | |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 600 | - | - | V | |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$ | - | 660 | - | mV/°C | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2.0 | - | 4.0 | V | |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 30\text{ V}$ | - | - | ± 100 | nA | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$ | - | - | 25 | μA | |
| | | $V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | - | - | 250 | | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 5.5\text{ A}^b$ | - | 0.780 | - | Ω | |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 5.5\text{ A}$ | 5.5 | - | - | S | |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V},$ $V_{DS} = 25\text{ V},$ $f = 1.0\text{ MHz},$ see fig. 5 | - | 1400 | - | pF | |
| Output Capacitance | C_{oss} | | - | 180 | - | | |
| Reverse Transfer Capacitance | C_{rss} | | - | 7.1 | - | | |
| Output Capacitance | C_{oss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$ | - | 1957 | - | |
| Effective Output Capacitance | $C_{oss\text{ eff.}}$ | | $V_{DS} = 480\text{ V}, f = 1.0\text{ MHz}$ | - | 49 | - | |
| | | | $V_{DS} = 0\text{ V to } 480\text{ V}$ | - | 96 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 8.0\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b | - | - | 49 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 13 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 20 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 300\text{ V}, I_D = 8.0\text{ A}$ $R_g = 9.1\text{ }\Omega, R_D = 35.5\text{ }\Omega,$ see fig. 10 ^b | - | 13 | - | ns | |
| Rise Time | t_r | | - | 25 | - | | |
| Turn-Off Delay Time | $t_{d(off)}$ | | - | 30 | - | | |
| Fall Time | t_f | | - | 22 | - | | |
| Gate Input Resistance | R_g | | $f = 1\text{ MHz},$ open drain | 0.5 | - | | 3.2 |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 9.2 | A | |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | 37 | | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 8.0\text{ A}, V_{GS} = 0\text{ V}^b$ | - | - | 1.5 | V | |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 8.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$ | - | 530 | 800 | ns | |
| Body Diode Reverse Recovery Charge | Q_{rr} | | - | 3.0 | 4.4 | μC | |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- $C_{oss\text{ effective}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

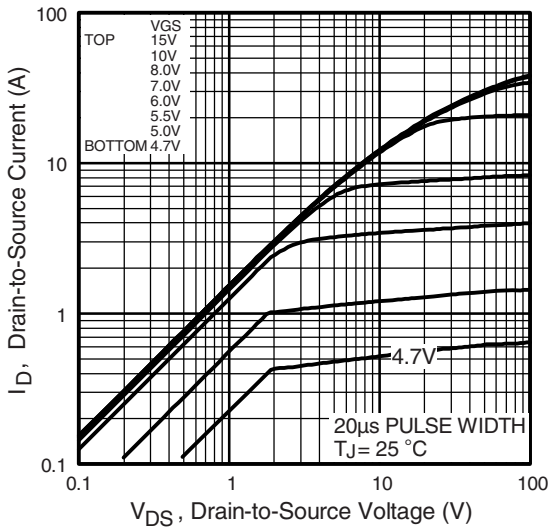


Fig. 1 - Typical Output Characteristics

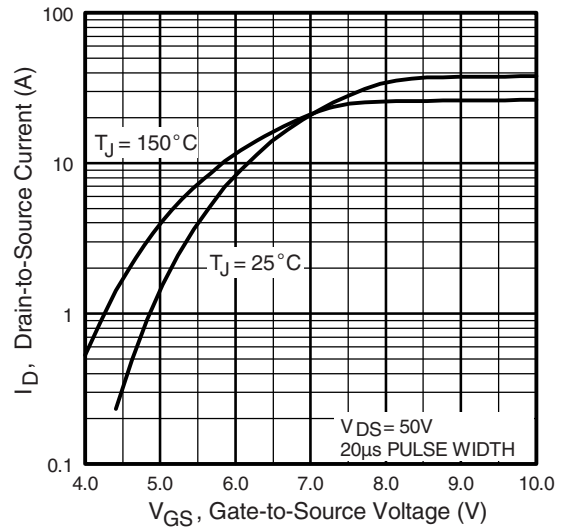


Fig. 3 - Typical Transfer Characteristics

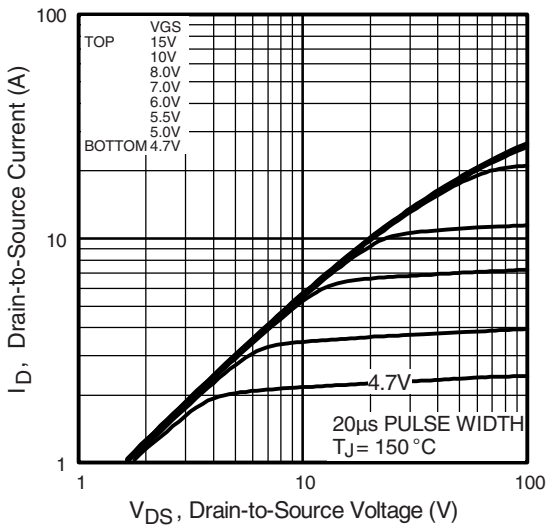


Fig. 2 - Typical Output Characteristics

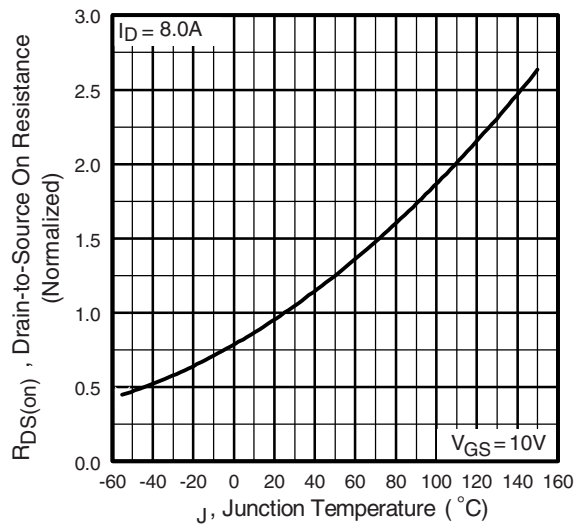


Fig. 4 - Normalized On-Resistance vs. Temperature



Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage



Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

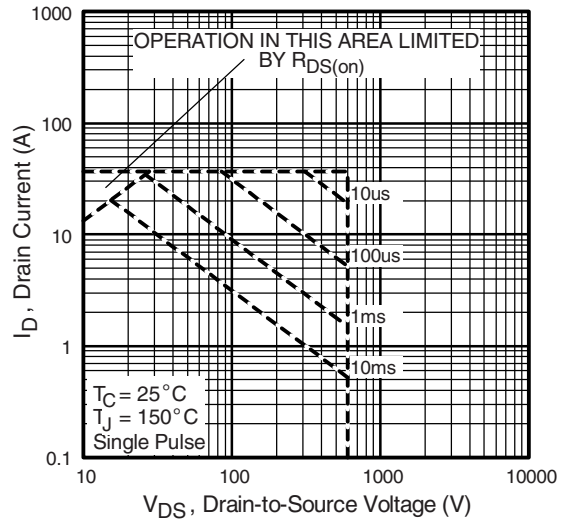


Fig. 8 - Maximum Safe Operating Area



Fig. 9 - Maximum Drain Current vs. Case Temperature

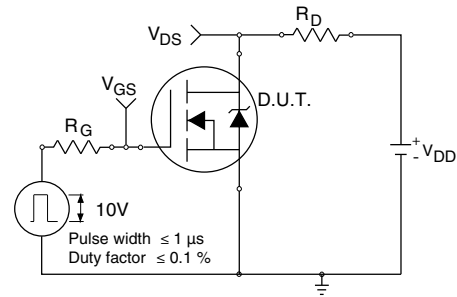


Fig. 10a - Switching Time Test Circuit

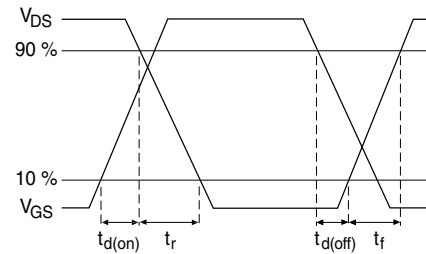


Fig. 10b - Switching Time Waveforms



Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

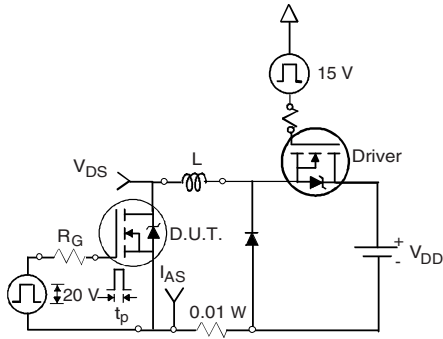


Fig. 12a - Unclamped Inductive Test Circuit



Fig. 12b - Unclamped Inductive Waveforms

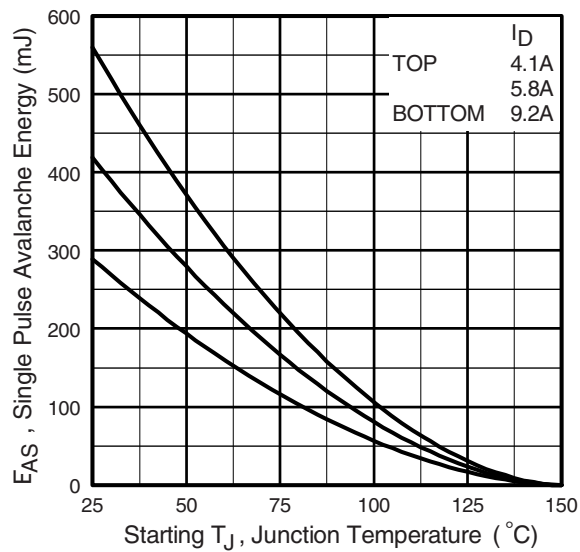


Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform

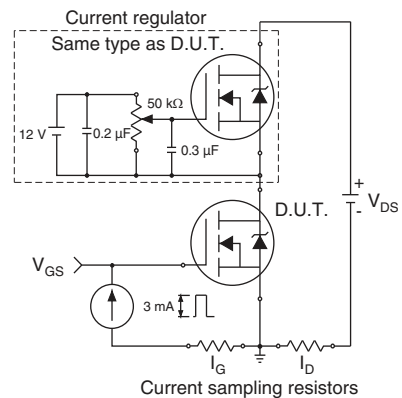
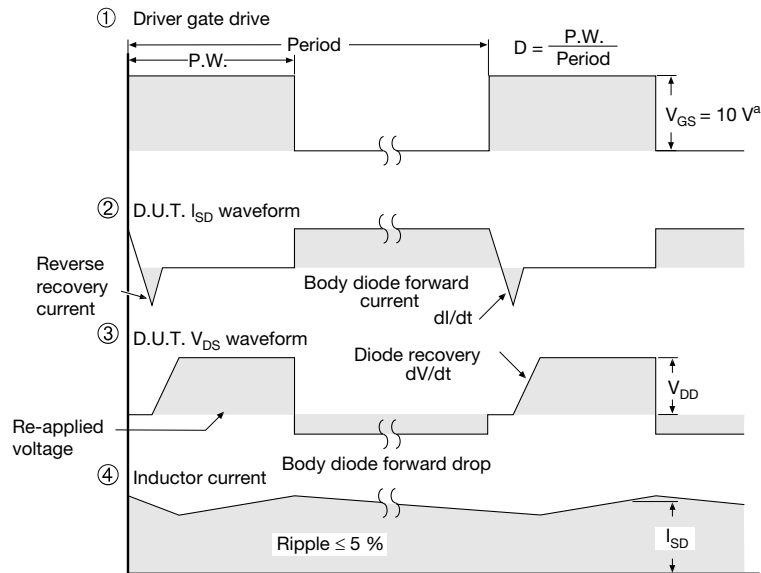
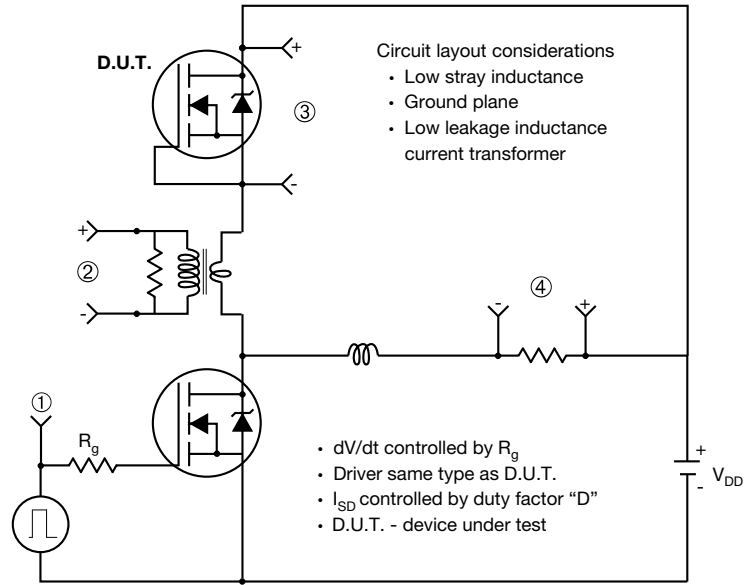


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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